Hindawi
International Transactions on Electrical Energy Systems
Volume 2022, Article ID 4175292, 18 pages
https://doi.org/10.1155/2022/4175292

Research Article

A Single Switch High Step-Up DC-DC Converter Based on Tri-Winding Coupled Inductor for Renewable Energy Applications

Mana Hosseinzadehlish,[1] **Seyed Majid Hashemzadeh**,[2] **Saeed Pourjafar**,[3] **and Ebrahim Babaei**[2,4]

[1]*Faculty of Engineering, University of Bristol, Bristol, UK*
[2]*Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran*
[3]*Electrical Engineering Department, University of Mohaghegh Ardabili, Ardabil, Iran*
[4]*Engineering Faculty, Near East University, North Cyprus, Mersin 10, Nicosia, Turkey*

Correspondence should be addressed to Seyed Majid Hashemzadeh; ma_hashemzadeh@tabrizu.ac.ir

Received 23 July 2022; Accepted 10 October 2022; Published 28 October 2022

Academic Editor: Jesus Valdez-Resendiz

This article introduces a novel nonisolated single-switch high step-up DC-DC converter using a tri-winding coupled inductor (TWCL) for renewable energy applications such as PV systems. Also, the voltage multiplier cell (VMC) is used to attain a high voltage gain. The used VMC acts as a passive clamp circuit and reduces the voltage stress across the power switch. So, a low voltage-rated power switch can be used in the presented converter. The suggested topology uses only one power switch with low on-state resistance ($R_{DS\text{-}ON}$), which leads to a simple control circuit and decreases the conduction losses. Highefficiency, operating with low duty cycle, low peak voltage over semiconductor elements, low turns ratio, the number of the coupled inductor, and high voltage conversion ratio are the significant benefits of the recommended DC-DC converter. To show the achievement of the presented structure, operational mode principles, steady-state, efficiency calculations, and comparison results are provided. Finally, a 120 W experimental prototype with 200 V output voltage and 50 kHz switching frequency is built to prove the usefulness of the suggested high step-up converter. The efficiency is measured 92.11% at rated power.

1. Introduction

In recent years, fossil fuel energy diminution leads to an increase of the serious economic problems [1]. To solve these significant concerns, renewable energy resources such as photovoltaic (PV) power systems are proposed by researchers [2]. Unfortunately, these sources cannot generate high voltage levels [3]. A method for voltage enhancement is the series connection of the PV panels. However, this method increases the system's cost. Another suitable method is the high voltage gain DC-DC converters utilization. These converters can be used to obtain the required high voltage levels [4, 5].

A classical boost DC-DC converter can obtain high voltage by a high duty cycle near to 1. But, this high duty cycle results in high conduction loss and low efficiency [6, 7]. Another drawback of the classical high step-up converter appears in high voltage utilization, where the power switch suffers from high voltage stress [8, 9]. As a result, the classical boost converter is not proper for high voltage applications. There are various voltage lifting methods that have been proposed by researchers, including switched inductor, voltage multiplier (VMC), switched capacitor (charge pump), and magnetic coupling [10]. The converters that use the abovementioned voltage boosting methods are able to accommodate higher voltage gain than the classical high

step-up structure. However, the large number of these presented converters needs a high component count. Therefore, a high cost and complexity and also low efficiency are resulted. The magnetic coupling technique for voltage lifting can be implemented by transformers or coupled inductors [11, 12]. Transformer-based DC-DC converters use isolated or built-in transformers for achieving electrical isolation. However, these types of transformers enhance the cost and volume of the system. Coupled inductors are the precious elements of the nonisolated converters. Using coupled inductors, two or more windings can be implemented by only one core. So, the core losses and cost of the converter are literally decreased. In Reference [13], using coupled inductor and VMC, a high step-up structure with soft-switched ability is suggested. However, in this structure, two power switches are used. Meanwhile, a high voltage gain is obtained in higher numbers of turns ratio. The proposed converter in Reference [14] has used a TWCL and VMCs for voltage boosting. To recycle the leakage inductance's energy, a passive clamp circuit is utilized to the converter. The main drawback of this structure is the higher number of elements than the other similar structures. In References [15, 16] using magnetic coupling, interleaved high step-up DC-DC converters are presented, which are proper for renewable energy uses. However, these converters suffer from low efficiency due to the high component count. In Reference [17], a fully soft-switched single-switch converter is presented. In this converter, an isolated transformer is used. It has a low cost and volume compared with other isolated converters. However, the maximum voltage on diodes is almost equal to the output voltage. In Reference [18], using coupled inductor, a nonisolated SEPIC-integrated high-voltage conversion ratio boost converter is presented. There is only one power switch in this topology, which decreases the total conduction loss. However, the maximum voltage across diodes is high, and the voltage gain of this structure is low compared to other similar structures. The presented converter in Reference [19] has used the coupled inductor technique for integrating the standard boost converter with VMC to achieve a high step-up hybrid topology for PV uses. However, the number of used diodes is high, which can reduce efficiency by increasing the conduction and forward losses. The converters in References [20, 21] have used coupled inductor in their structures for voltage increasing. However, these converters suffer from low efficiency, a high number of components, and higher maximum voltage stress on switches and diodes. Reference [22] suggested converters based on the coupled inductor, and clamp circuits are used in their structure in order to reduce the voltage stress of the main switch, However, the main downside of the converters proposed in Reference [23, 24] is that high boost factor can be obtained in higher duty cycle and higher number of turns ratio. In References [25–28], TWCL is used for enhancing the voltage gain. This type of coupled inductor has two secondary windings, which give two freedom degrees to regulate voltage gain and semiconductor element voltage stresses.

In this paper, a new single-switch nonisolated high step-up DC-DC converter based on TWCL and VMC with high voltage gain is suggested. The used VMC operates as a passive clamp and decreases the voltage stress on the power switch. So, a low voltage-rated power switch can be used in the presented converter. The suggested topology uses only one low on-state resistance ($R_{DS\text{-}ON}$) power switch, which leads to a simple control circuit and decreases the conduction losses. (1) high efficiency, (2) operating with low duty cycle, (3) low turns ratio of the coupled inductor, (4) low voltage stress across semiconductor components, and (5) high voltage conversion ratio are the significant benefits of the presented DC-DC converter. In the rest of the paper, to illustrate the performance of the suggested structure, operational principles, steady-state and efficiency analysis, design considerations, comparison study, and experimental results are provided.

2. Suggested Converter and Operational Principle

The configuration of the presented converter is shown in Figure 1. This structure includes a TWCL, one power switch (S), four diodes (D_1, D_2, D_3, and D_o), and four capacitors (C_1, C_2, C_3, and C_o). N_1, N_2, and N_3 are the primary, secondary, and tertiary windings turn number of the TWCL, respectively. Capacitor C_1 operates as a voltage-boosting capacitor. D_1 and C_2 operate as a voltage clamp, which reduces the peak voltage across S. D_2 and D_3 and C_3 operate as a VMC. Diode D_o and capacitor C_o are the output diode and output filter, respectively. To simplify the operation principles and steady-state analysis, the following suppositions are counted:

(1) All semiconductor elements are ideal.

(2) TWCL is modelled as an ideal tree-winding transformer with magnetizing (L_m) and leakage (L_k) inductances. The secondary and tertiary turn ratios of this transformer are obtained as follows:

$$\frac{V_{N_2}}{V_{N_1}} = \frac{N_2}{N_1} = n_2, \tag{1}$$

$$\frac{V_{N_3}}{V_{N_1}} = \frac{N_3}{N_1} = n_3, \tag{2}$$

$$k = \frac{L_m}{L_m + L_k}. \tag{3}$$

(3) The used capacitors are large adequately. Hence, the voltages across capacitors are invariable during the switching period (T_s). The operation principles of the recommended topology are analysed in a continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Figures 2(a) and 2(b) show the main waveforms of the suggested structure in CCM and DCM, respectively.

2.1. Mode Analysis in CCM. CCM operation includes four modes. Modes 1 and 3 are transient modes with small-time durations and modes 2 and 4 are the main modes of CCM.

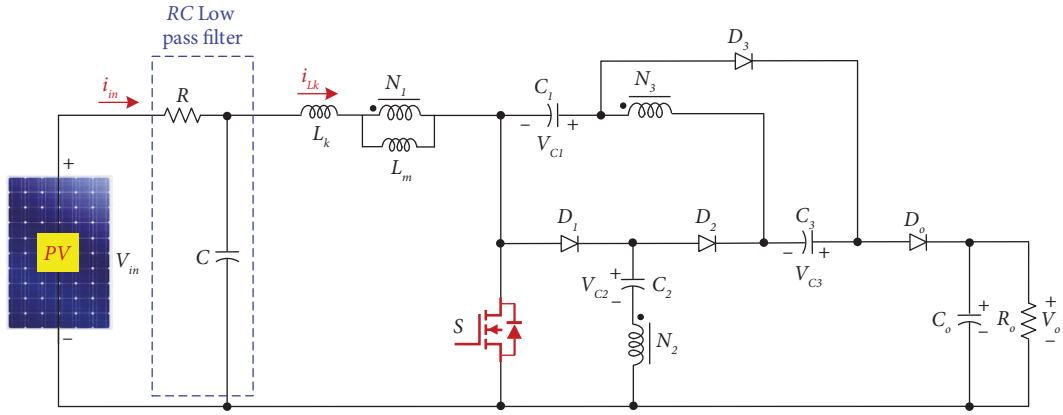


Figure 1: Presented converter.

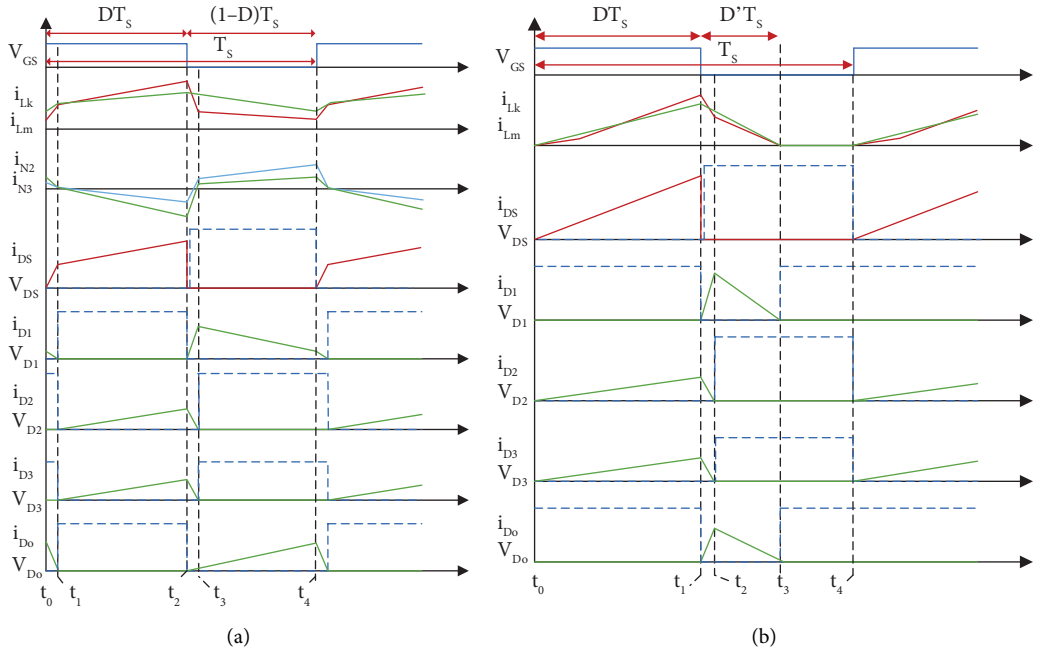


Figure 2: Main waveforms of the presented topology: (a) CCM and (b) DCM.

Mode 1. **[$t_0 < t < t_1$]:** At $t = t_0$, power switch S is turned ON. So, the magnetizing L_m and leakage L_k inductances of the TWCL receive energy from input sources, and their currents enhance linearly. D_1 and D_o are conducting and diodes D_2 and D_3 are reverse-biased. The current pass of mode 1 is shown in Figure 3(a). As can be seen in this figure, capacitors C_1 and C_3 are discharged through the output diode D_o, and the energy of these capacitors along with the tertiary side of the TWCL is transferred to the load. Moreover, C_2 is charged through diode D_1. This mode finishes at $t = t_1$, when D_1 and D_o are turned OFF.

Mode 2. **[$t_1 < t < t_2$]:** At the beginning of this mode, D_2 and D_3 are forward-biased, and power switch S is still turned ON. Same as mode 1, L_m and L_k are still charged by V_{in} and their currents are increased. Also, the currents of the secondary and tertiary sides of the TWCL reduce linearly. The equivalent power circuit of this mode is demonstrated in Figure 4(a). According to this figure, capacitors C_1, C_3, and C_o are charged and C_2 is discharged through diode D_2.

Mode 3. **[$t_2 < t < t_3$]:** In mode 3, power switch S is turned OFF and all of the diodes are forward-biased. Due to the demagnetizing of L_m and L_k, their currents start to decrease. The energy of L_k is transferred to C_1 by D_1 and D_2. So, the leakage energy is recycled. It should be noticed that during this mode C_3 is charged and C_2 is discharged. This mode ends at $t = t_3$ when diodes D_2 and D_3 are turned OFF. The equivalent power circuit of this mode is depicted in Figure 3(b).

Mode 4. **[$t_3 < t < t_4$]:** During this mode, power switch S and D_2 and D_3 are turned OFF and D_1 and D_o are conducting. The magnetizing L_m and leakage L_k inductances release their energy. Thus, i_{lm} and i_{lk} are decreased. Also, the currents of the secondary and tertiary sides of the TWCL increased

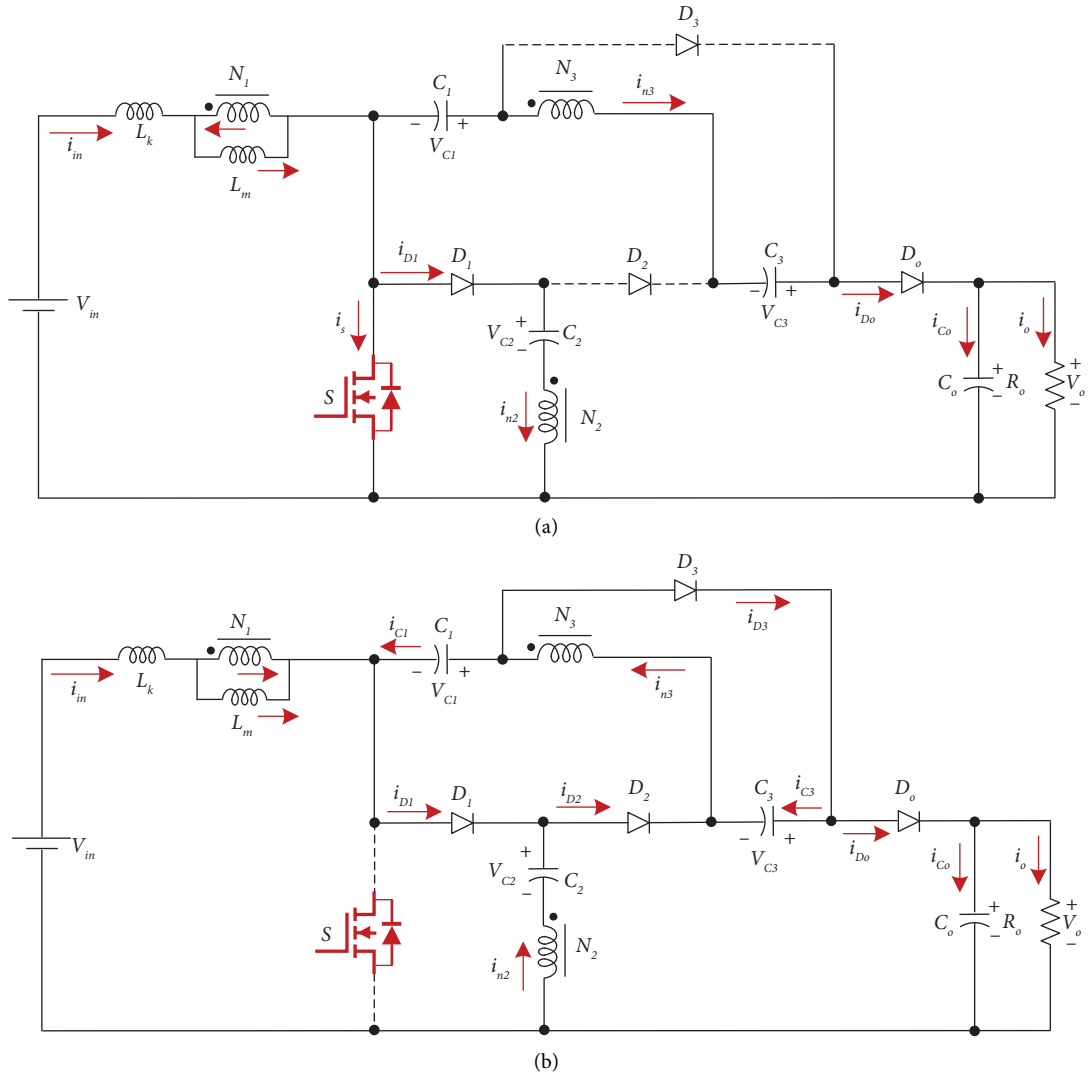


FIGURE 3: Equivalent power circuits of the suggested structure in transient modes: (a) mode 1 in CCM, (b) mode 3 in CCM, and mode 2 in DCM.

linearly. The energy of L_k is recycled by D_1 and C_2. The current of diode D_1 is decreased, and the current decrease rate of this diode is controlled by L_k. Furthermore, the energy of the capacitors C_1 and C_3 and the tertiary side of the TWCL is transferred to the load by diode D_o. It can be mentioned that during this mode, diode D_1 and capacitor C_2 act as a passive clamp and suppresses the voltage spikes across the power switch. The equivalent circuit of this mode is presented in Figure 4(b).

2.2. Mode Analysis in DCM. The DCM operation of the recommended topology is separated into four modes. Modes 1, 2, and 4 are the main modes and mode 3 is the transient mode with a small-time duration. As can be seen in Figure 3, modes 1, 2, and 3 are like to CCM operation. In the fourth mode, the magnetizing and leakage currents (i_{Lm} and i_{Lk}) of the TWCL fall to zero. All of the semiconductors are turned OFF, and the stored energy in the output capacitor C_o is transferred to the load. The equivalent circuit of this mode is presented in Figure 4(c).

3. Steady-State Analysis

3.1. Analysis of CCM Operation. To streamline the steady-state analysis of the proposed topology, only modes 2 and 4 are taken into account, owing to the fact that the time intervals of other modes are extremely short. When S is turned ON in mode 2, equations (4)–(7) are derived for V_{N1}, V_{N2}, V_{N3}, and V_{Lk}:

$$V_{N_1}^{II} = \frac{L_m}{L_m + L_k} V_{in} = kV_{in}, \tag{4}$$

$$V_{N_2}^{II} = n_2 V_{N_1}^{II} = n_2 k V_{in}, \tag{5}$$

$$V_{N_3}^{II} = n_3 V_{N_1}^{II} = n_3 k V_{in}, \tag{6}$$

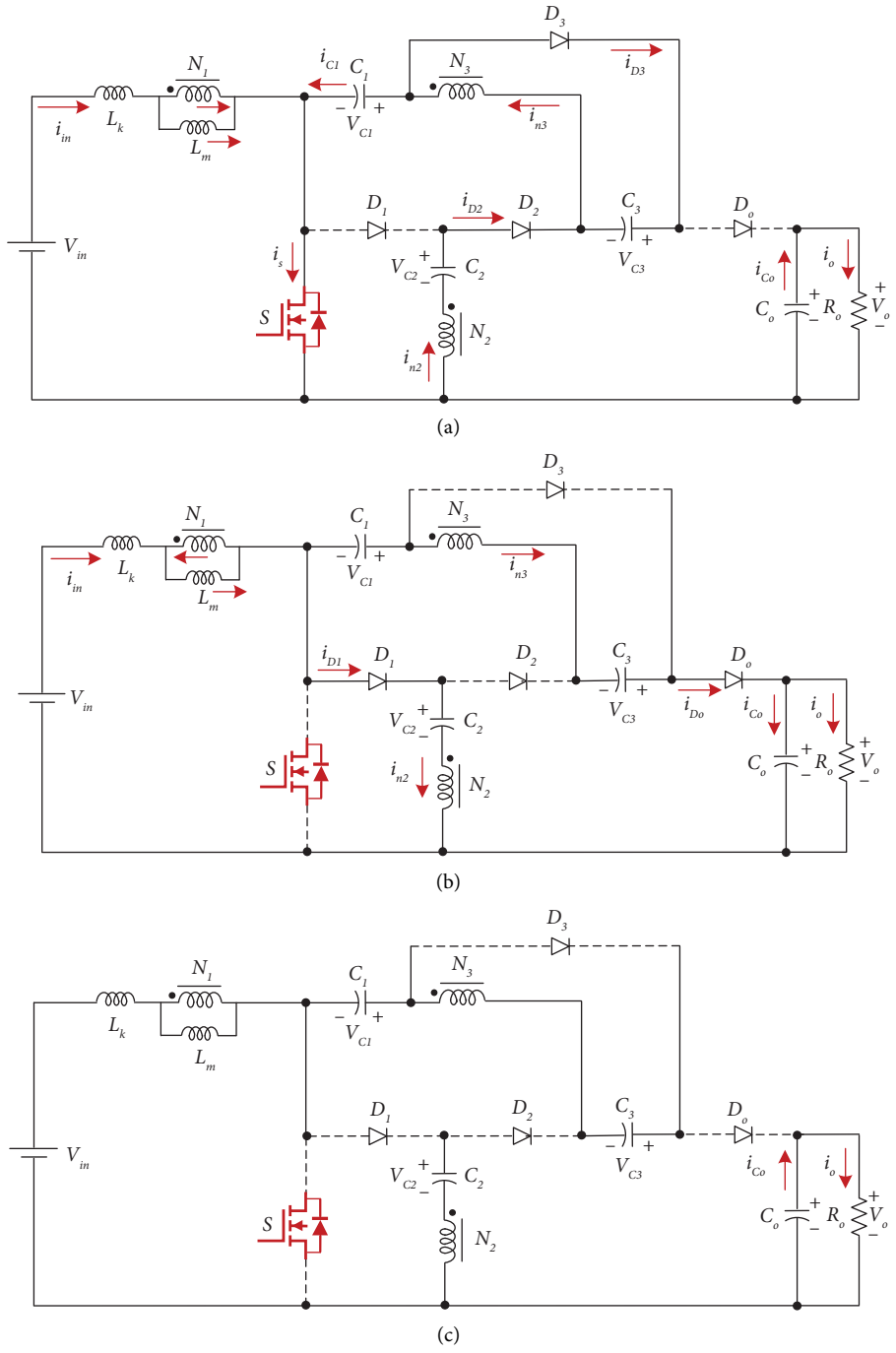


FIGURE 4: Equivalent power circuits of the suggested structure in main modes: (a) mode 2 in CCM and mode 1 in DCM, (b) mode 4 in CCM and mode 3 in DCM, and (c) mode 4 in DCM.

$$V_{L_k}^{II} = \frac{L_k}{L_m + L_k} V_{in} = (1-k)V_{in}. \quad (7)$$

By using voltage-second balance law to N_1, N_2, N_3, and L_k, equations (8)–(11) are achieved in mode 4

$$V_{N_1}^{IV} = -\frac{kD}{1-D} V_{in}, \quad (8)$$

$$V_{N_2}^{IV} = -\frac{n_2 kD}{1-D} V_{in}, \quad (9)$$

$$V_{N_3}^{IV} = -\frac{n_3 kD}{1-D} V_{in}, \quad (10)$$

$$V_{L_k}^{IV} = -\frac{(1-k)D}{1-D} V_{in}. \quad (11)$$

The voltages of capacitors C_1, C_2, and C_3 are achieved as follows:

$$V_{C_2} = V_{in} - V_{L_k}^{IV} - V_{n_1}^{IV} - V_{n_2}^{IV} = \frac{1 + n_2 kD}{1-D} V_{in}, \quad (12)$$

$$V_{C_1} = V_{C_2} + V_{N_2}^{II} + V_{N_3}^{II} = \frac{1 + n_2 k + n_3 k - n_3 kD}{1-D} V_{in}, \quad (13)$$

$$V_{C_3} = V_{N_3}^{II} = n_3 k V_{in}. \quad (14)$$

Based on (8), (10), (11), (13), and (14), the output voltage and voltage gain of the recommended structure in CCM are obtained as follows:

$$V_o = V_{c_o} = V_{in} - V_{L_K}{}^{IV} - V_{N_1}{}^{IV} + V_{C_1} - V_{N_3}{}^{IV} + V_{C_3} = \frac{2 + n_2 k + 2n_3 k - n_3 kD}{1-D} V_{in}, \quad (15)$$

$$M_{\mathrm{CCM}} = \frac{V_o}{V_{in}} = \frac{2 + n_2 k + n_3 k(2-D)}{1-D}. \quad (16)$$

The voltage conversion ratio of the presented topology versus duty cycle in terms of the diverse value of the coupling coefficient is depicted in Figure 5(a), where the turns ratio is considered to be $n_2 = n_3 = 2$. As can be seen in this figure, it is clear that the voltage conversion ratio is enhanced with increasing the leakage inductance; so, to decrease the skin effects and leakage inductance to attain a higher voltage conversion ratio, sandwich winding construction is applied in the used high-frequency TWCL.

By considering the value of the coupling coefficient k equal to 1 and the secondary and tertiary turns ratio equal to N ($n_2 = n_3 = N$), the suggested structure's ideal voltage conversion ratio is derived as follows:

$$M_{\mathrm{CCM}} = \frac{V_o}{V_{in}} = \frac{2 + N(3-D)}{1-D}. \quad (17)$$

Figure 5(b) indicates the presented DC-DC converter's ideal voltage conversion ratio (M_{CCM}) versus duty cycle under diverse turns ratio. It is evident that a higher voltage conversion ratio is attained by enhancement of the coupled inductor's turns ratio either without operating at an extremely large duty cycle.

3.2. DCM Operation Analysis. DCM operation consists of four modes in which modes 1, 2, and 3 are the same as modes in CCM operation; so, the voltage and current relations of these modes are similar too. In mode 4, the voltages V_{N1}, V_{N2}, and V_{N3} are derived as follows:

$$V_{N_1}^{IV} = V_{N_2}^{IV} = V_{N_3}^{IV} = 0. \quad (18)$$

The voltage-second balance law is utilized on the primary winding of the TWCL as follows:

$$\int_0^{DT_s} V_{N_1}^{I} dt + \int_{DT_s}^{(D+D')T_s} V_{N_1}^{III} dt + \int_{(D+D')T_s}^{T_s} V_{N_1}^{IV} dt = 0. \quad (19)$$

Based on (19), the voltage V_{n1} in mode 2 is attained as follows:

$$V_{N_1}^{III} = \frac{-D}{D'} V_{in}. \quad (20)$$

The capacitor voltage can be expressed as follows:

$$V_{C_1} = \frac{D(N+1) + D'}{D'} V_{in}, \quad (21)$$

$$V_{C_2} = \frac{D(N+1) + D'(2N+1)}{D'} V_{in}, \quad (22)$$

$$V_{C_3} = N V_{in}. \quad (23)$$

Considering the above equations, the converter's voltage conversion ratio in DCM operation is obtained as follows:

$$M_{\mathrm{DCM}} = \frac{V_o}{V_{in}} = \frac{D(2N+2) + D'(3N+2)}{D'}. \quad (24)$$

By considering (24), D' is calculated as follows (25):

$$D' = \frac{D(2N+2)}{M_{DC\,M} - (3N+2)}. \quad (25)$$

The peak current of the magnetizing inductance is obtained as follows:

$$I_{L_m}^{\mathrm{peak}} = \frac{DT_s}{L_m} V_{in}. \quad (26)$$

Also, the average current of C_o is written as follows:

$$I_{C_o}^{\mathrm{avg}} = I_{D_o}^{\mathrm{avg}} - I_o = \frac{1}{2} D' \frac{I_{L_m}^{\mathrm{peak}}}{N} - I_o. \quad (27)$$

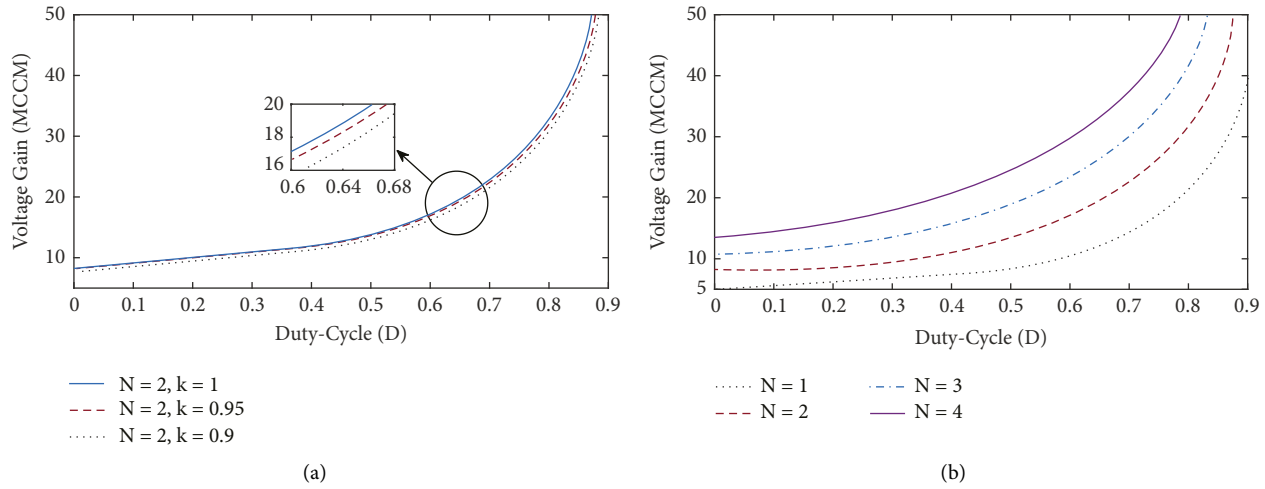


FIGURE 5: (a) Voltage conversion ratio of the converter versus duty cycle under various values of the coupling coefficient (for $n_2 = n_3 = N = 2$) and (b) voltage gain of the presented structure (M_{CCM}).

At steady-state operation, the average current of output capacitor I_{Co} is zero and $I_o = V_o/R_o$. So, by substituting (25) and (26) in (27), equation (28) is obtained:

$$\frac{D^2(2N+2)V_{in}}{2NV_o[V_o/V_{in}-(3N+2)]} = \frac{L_m}{R_oT_s}. \tag{28}$$

The magnetizing inductance time constant is equal to:

$$\tau_{L_m} = \frac{L_m}{R_oT_s}. \tag{29}$$

By replacing (29) into (28), the DCM operation voltage gain of the suggested topology is calculated as follows:

$$M_{\mathrm{DCM}} = \frac{(3N+2)+\sqrt{(3N+2)^2+2\left((2N+2)/N\tau_{L_m}D^2\right)}}{2}. \tag{30}$$

The voltage gain of the recommended topology at CCM operation and at DCM operation under various τ_{Lm} and $N=2$ is shown in Figure 6. It is clear that M_{CCM} is higher than M_{DCM}, particularly at higher duty cycles.

3.3. Analysis of BCM Operation. To operate the presented structure in boundary conduction mode, the voltage gain M_{CCM} and M_{DCM} should be considered to be equal. Considering equations (17) and (30), the boundary normalized magnetizing inductance time constant can be obtained as follows:

$$\tau_{L_{mB}} = \frac{D(1-D)^2}{2N(2+N(3-D))}. \tag{31}$$

The curve of τ_{LmB} versus duty cycle under different turn ratio is depicted in Figure 7. For τ_{Lm} higher than τ_{LmB}, the recommended topology will operate at the CCM condition.

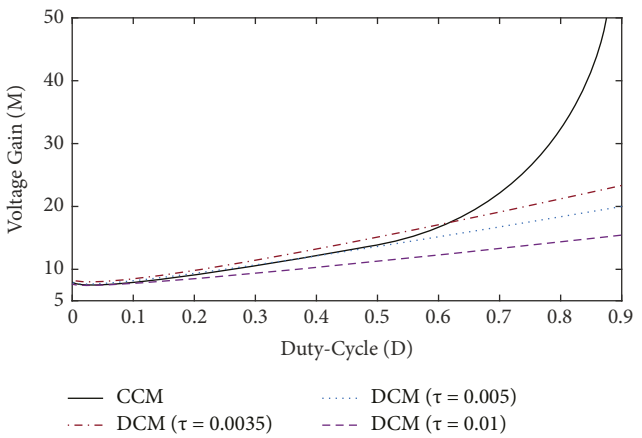


FIGURE 6: Voltage conversion ratio of the presented structure versus duty cycle at CCM operation under $N=2$ and at DCM operation under various τ_{Lm}.

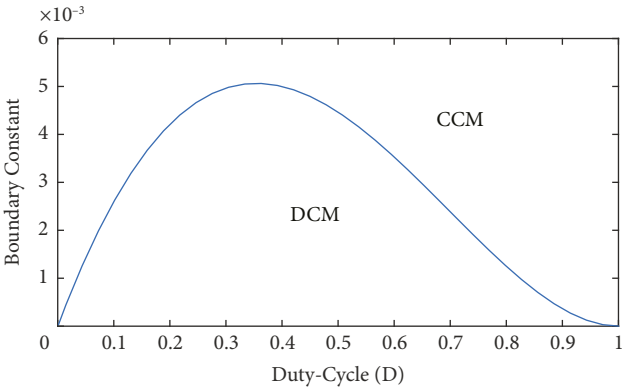


FIGURE 7: Suggested structure's boundary condition versus duty cycle under $N=2$.

4. Design Guidance

4.1. Voltage Stress Analysis. The voltage stress across the semiconductor components in CCM operation is achieved as follows:

$$V_{D_1} = V_{D_o} = \frac{N+1}{1-D}V_{in} = \frac{1+N}{(3-D)N+2}V_o, \tag{32}$$

$$V_{D_2} = \frac{2N+1}{1-D}V_{in} = \frac{1+2N}{(3-D)N+2}V_o, \tag{33}$$

$$V_{D_3} = \frac{N}{1-D}V_{in} = \frac{N}{(3-D)N+2}V_o, \tag{34}$$

$$V_{ds} = \frac{1}{1-D}V_{in} = \frac{1}{(3-D)N+2}V_o. \tag{35}$$

4.2. Current Stress Analysis. When switch S is in on/off state in CCM operation, the input current's average value is calculated as follows:

$$\begin{aligned} I_{\text{in}}(on) &= I_{Lm} - Ni_{C_2\,(on)} + N\left(i_{C_3\,(\text{on})} - i_{C_2\,(\text{on})}\right) \\ &= I_{Lm} + 3Ni_{C_3\,(\text{on})}, \end{aligned} \tag{36}$$

$$I_{\text{in}}(\text{off}) = I_o + i_{C_o\,(\text{off})} + i_{C_2\,(\text{off})}. \tag{37}$$

The average current of capacitors in on/off state is obtained as equations (38) and (39):

$$i_{C_1(\text{on})} = -i_{C_2(\text{on})} = i_{C_3(\text{on})} = -Di_{C_o(\text{on})} = \frac{1}{D}I_o, \tag{38}$$

$$i_{C_1\,(\text{off})} = -i_{C_2\,(\text{off})} = i_{C_3\,(\text{off})} = -Di_{C_o\,(\text{off})} = \frac{-1}{1-D}I_o. \tag{39}$$

Based on the conversion of the power and equations (36), (37), (38), and (39), the magnetizing inductance average value is calculated as follows:

$$I_{L_m}^{\text{avg}} = \frac{M_{\text{CCM}} - 3N - 2}{1-D}I_o = \frac{2(N+1)}{1-D}I_o. \tag{40}$$

Also, the magnetizing inductance current ripple is obtained as follows:

$$\Delta I_{Lm} = \frac{DT_S V_{in}}{L_m}. \tag{41}$$

According to equations (40) and (41), the peak current of the magnetizing inductance is calculated as follows:

$$I_{L_m}^{\text{peak}} = \frac{2(N+1)}{1-D}I_o + \frac{DT_S V_{in}}{2L_m}. \tag{42}$$

By considering the amp-sec balance on capacitors, the average currents of the used diodes will be equal to I_o, so the peak currents of power switch and diodes are derived:

$$I_{D_1}^{\text{peak}} = I_{D_o}^{\text{peak}} = \frac{2I_o}{1-D}, \tag{43}$$

$$I_{D_2}^{\text{peak}} = I_{D_3}^{\text{peak}} = \frac{2I_o}{D}, \tag{44}$$

$$I_{ds}^{\text{Peak}} \approx \frac{2N - D(N-1) + 2}{D(1-D)}I_o. \tag{45}$$

4.3. Design of Magnetizing Inductance. In order to CCM operation of the presented structure, equations (29) and (31) are used to calculate the minimum value of magnetizing inductance which is attained as follows:

$$L_m \geq \frac{D(1-D)^2 R_o}{2N(2+N(3-D))f_s}. \tag{46}$$

4.4. Design of Capacitors. According to $i_C = CdV_{Ci}/dt$, $dt = DT_S = D/f_S$ and $dV_C\text{i} = \Delta V_{Ci}$, where ΔV_{Ci} is the voltage ripple of capacitors that is considered 2% of the voltage on capacitors. Based on equations (12)–(15), the values of capacitors are derived as follows:

$$C_i \geq \frac{DV_o}{\Delta V_{Ci} R_o f_s}, \tag{47}$$

$$C_o \geq \frac{DV_o}{\Delta V_{Co} R_o f_s}, \tag{48}$$

where $i = 1$, 2, 3, and 4.

5. Efficiency Analysis

In order to obtain the efficiency of the suggested topology, the parasitic resistances of elements are assumed as follows:

R_{ds-on}: on-state resistance of power switch.
$R_{F(D_1 \sim D_o)}$: the forward resistance of diodes.
$R_{(C_1 \sim C_o)}$: ESR of capacitors.
$R_{(LN_1 \sim LN_3)}$: ESR of the coupled inductor's windings.
$V_{F(D_1 \sim D_o)}$: the forward voltage of diodes.

Efficiency of the presented topology (η) is calculated as follows [29]:

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}}, \tag{49}$$

$$\begin{aligned} P_{\text{loss}} &= P_{\text{switch}} + P_{RF(D_1 \sim D_o)} + P_{VF(D_1 \sim D_o)} + P_{R(C_1 \sim C_o)} \\ &\quad + P_{R(LN_1 \sim LN_3)}. \end{aligned} \tag{50}$$

The power switch total loss is equal to:

$$P_{\text{Switch}} = P_{R_{ds-on}} + P_{SW}. \tag{51}$$

Also, the power switch conduction loss is obtained as follows:

$$P_{R_{ds-\text{on}}} = R_{ds-\text{on}} \times \left(I_{s(\text{rms})}\right)^2 = R_{ds-\text{on}} \times \left(\frac{2N - D(N-1) + 2}{\sqrt{D}\,(1-D)}\right)^2. \tag{52}$$

The switching loss of the power switch is obtained as follows:

$$P_{SW} = f_s c_s v_s^2 = f_s c_s \left(\frac{1}{2 + N(3-D)}\right)^2. \tag{53}$$

The following equation expresses diode forward resistance losses:

$$\begin{aligned} P_{RF(D_1 \sim D_o)} &= R_{F(D_1 \sim D_o)} \times \left(I_{(D_1 \sim D_o)(\text{rms})}\right)^2 \\ &= \left[\left(R_{FD_1} + R_{FD_o}\right) \times \left(\frac{I_o}{\sqrt{1-D}}\right)^2\right] + \left[\left(R_{FD_2} + R_{FD_3}\right) \times \left(\frac{I_o}{\sqrt{D}}\right)^2\right]. \end{aligned} \tag{54}$$

Forward voltage losses of the used diodes are achieved as follows:

$$\begin{aligned} P_{VF(D_1 \sim D_o)} &= V_{F(D_1 \sim D_o)} \times I_{(D_1 \sim D_o)(\text{ave})} \\ &= \left(V_{FD_1} + V_{FD_2} + V_{FD_3} + V_{FD_o}\right) \times I_o. \end{aligned} \tag{55}$$

Moreover, capacitor power losses are expressed as follows:

$$\begin{aligned} P_{R(C)} &= R_{(C_1 \sim C_o)} \times \left(I_{(C_1 \sim C_o)(\text{rms})}\right)^2 + R_{(C_{in})} \times \left(I_{(C_{in})(\text{rms})}\right)^2 \\ &= \left[\left(R_{C_1} + R_{C_2} + R_{C_3}\right) \times \left(\frac{I_o}{\sqrt{D(1-D)}}\right)^2\right] + \left[\left(R_{C_o}\right) \times \left(\frac{I_o}{\sqrt{D}}\right)^2\right] \\ &\quad + R_{\text{Cin}} \times \left(I_{(L_{in})(\text{rms})} - I_{(LN_1)(\text{rms})}\right)^2. \end{aligned} \tag{56}$$

The primary, secondary, and tertiary sides of coupled inductor and input filter's inductor conduction loss can be obtained as follows:

$$\begin{aligned} P_{R(L)} &= R_{(L_{in})} \times \left(I_{(L_{in})(\text{rms})}\right)^2 + R_{(LN_1 \sim LN_3)} \times \left(I_{(LN_1 \sim LN_3)(\text{rms})}\right)^2 \\ &= \left[R_{L_{in}} \times \left(\sqrt{\frac{[(2D(N+1)) + 3N(1-D)]^2}{D(1-D)^2} + \frac{(3-D)^2}{1-D}}\, I_o\right)^2\right] + \\ &\quad \left[R_{LN_1} \times \left(\frac{N\sqrt{9-5D}}{\sqrt{D(1-D)}} I_o\right)^2\right] + \left[R_{LN_2} \times \left(\frac{1}{\sqrt{D(1-D)}} I_o\right)^2\right] \\ &\quad + \left[R_{LN_2} \times \left(\sqrt{\frac{4-3D}{D(1-D)}}\, I_o\right)^2\right]. \end{aligned} \tag{57}$$

Table 1: Comparison of the suggested DC-DC structure with other comparable converters.

Converter	Number of				Voltage gain	Voltage stress on switch	Voltage stress on output diode	Current stress on switch	Max current stress on diode	Continuous input current
	S	D	C	L+CL						
[4]	1	4	5	$1+1^{2w}$	$(1+D+N(2-D))/(1-D)$	$V_o/(1+D+N(2-D))$	$(N+1)\ Vo/(1+D+N(2-D))$	$(2D+N(3.14-2.14D))\ I_o/D(1-D)$	$(2+N)I_o/(1-D)$	Yes
[5]	1	6	5	$0+1^{2w}$	$(2+N+ND)/(1-D)$	$V_o/(2+N+ND)$	$NV_o/(2+N+ND)$	—	—	No
[6]	1	4	5	$1+1^{2w}$	$((N+1)\ (1+D))/(1-D)$	$V_o/((N+1)\ (1+D))$	$V_o/(1+D)$	$2\ (N+1)I_o/D(1-D)$	$2\ (N+1)I_o/D\ (1-D)$	Yes
[7]	1	5	5	$0+1^{2w}$	$(1+D+N(2-D))/(1-D)$	$V_o/(1+D+N(2-D))$	$NV_o/(1+D+N(2-D))$	$2\ (N+1)I_o/D$	$2I_o/(1-D)$	No
[11]	1	5	5	$0+1^{2w}$	$(2+N(2-D))/(1-D)$	$V_o/(2+N(2-D))$	$V_o/(2+N(2-D))$	$(2+ND\ (2-D))I_o/D(1-D)$	$2\ (N+1)I_o/(1-D)$	Yes
[19]	1	7	8	$1+1^{2w}$	$(4\text{-}D+N(2-D))/(1-D)$	$V_o/(4-D+N(2-D))$	$(N\ (-\text{-}D)-D)\ V_o/(4-D+N\ (2-D))$	—	—	No
[20]	1	4	5	$1+1^{2w}$	$((N+1)\ D+N+2)/(1-D)$	$V_o/((N+1+N+2)\ D)$	$(N+1)\ V_o/(N+1)\ D+N+2)$	$(2+2N\ D)I_o/D(1-D)$	$(2+2N\ D)I_o/D(1-D)$	Yes
[21]	1	4	5	$1+1^{2w}$	$(2+N+D)/(1-D)$	$V_o/(2+N+D)$	$(N+1)\ V_o/(2+N+D)$	$(2+D+N(2-D))I_o/D(1-D)$	$2\ (2D+N(2-D))\ I_o/D(1-D)$	Yes
[22]	1	4	4	$0+1^{2w}$	$(1+N+ND)/(1-D)$	$V_o/(1+N+ND)$	$NV_o/(1+N+ND)$	$(1+ND)I_o/D(1-D)$	$I_o/(1-D)$	Yes
[23]	1	5	5	$0+1^{2w}$	$(2+2N)/(1-D)$	$V_o/(2+2N)$	$(N+1)\ V_o/(2+2N)$	$2\ (N+D)I_o/D(1-D)$	$2NI_o/D(1-D)$	Yes
[24]	1	5	4	$0+1^{2w}$	$(1+D+ND(1+D))/2(1-D)$	$V_o/(2<+N+ND)$	$2NDV_o/(1+D+ND(1+D))$	$(2N+(1-N)D)I_o/D(1-D)$	$2I_o/(1-D)$	No
[25]	2	3	4	$0+1^{3w}$	$(2+N(1+D))/(1-D)$	$V_o/(2+N(1+D))$	$(ND)Vo/(2+N(1+D))$	$(2+N(1+D))I_o/(1-D)$	$2I_o/(1-D)$	Yes
[26]	1	6	6	$0+1^{3w}$	$((3-D)N+2)/(1-D)$	$V_o/((3-D)N+2)$	$(N+1)\ V_o/((3-D)\ N+2)$	$((6-4D)N+2)I_o/D(1-D)$	$2I_o/(1-D)$	Yes
[27]	2	4	4	$0+1^{3w}$	$(1+N+D)/(1-D)$	$V_o/(1+N+D)$	$NV_o/(1+N+D)$	$(0.5\,N\,D)I_o/D(1-D)$	$(N+2)I_o/2(1-D)$	Yes
[28]	1	4	4	$1+1^{3w}$	$(2-D+N(2-D))/(1-D)$	$V_o/(2-D+N(2-D))$	$NV_o/(2-D+N(2-D))$	—	—	No
[30]	2	2	2	$2+0$	$2/(1-D)$	$V_o/2$	V_o	—	—	Yes
[31]	2	2	2	$2+0$	$(1-D^2))/(1-2D+D^2)$	$V_o/(1-D^2)$	$V_o/(1-D^2)$	—	—	Yes
[32]	1	3	3	$1+1^{2w}$	$(N+2)/(1-D)$	$V_o/(N+2)$	$(N+1)\ V_o/(N+2)$	$(2N\,D+1)\ I_o/(D)$	$(2N+2-ND)\ I_o/(D(1-D))$	Yes
[33]	1	4	4	$0+1^{3w}$	$(2+2N\,ND)/(1-D)$	$V_o/(2+2N\,ND)$	$(1+N\ V_o)/(2+2N\,ND)$	$(1+2N\,ND+D)\ I_o/(D(1-D))$	$2I_o/(1-D)$	Yes
[34]	1	6	6	$0+1^{3w}$	$(3+4N\,ND)/(1-D)$	$V_o/(3+4N\,ND)$	$(2N+1)\ V_o/(3+4N\,ND)$	$(3+4N\,ND)\ I_o/(1-D)+(4\ (N+1)I_o/D)$	$2I_o/(1-D)$	No
Proposed	1	4	5	$0+1^{3w}$	$((3-D)N+2)/(1-D)$	$V_o/((3-D)N+2)$	$(N+1)\ V_o/((3-D)\ N+2)$	$(1+D+N(3-D))I_o/D(1-D)$	$2I_o/(1-D)$	Yes

6. Comparison Assessment

Table 1 shows a comparison between the recommended DC-DC topology and other similar converters in terms of voltage gain, component number, voltage and current stress of the switch, voltage stress of output diode, maximum current stress of diodes, and input current. To prove the performance of the presented structure, five competitive diagrams have been indicated in Figures 8–11.

According to Figure 8 that illustrates the voltage gain comparison versus duty cycle, it is clear that the suggested structure has a higher voltage conversion ratio than all other converters for all ranges of duty cycle (except converters in References [33, 34]). However, the converter in Reference [34] has more components and high current peak of power switch (based on Figure 11(a)). The voltage gain of the suggested converter is higher than the structure in Reference [33] for duty cycle $0 < D < 0.5$, but for higher duty cycles, the gain of the mentioned topology in Reference [33] is greater; that it depicts the superiority of the recommended structure. Operation with high duty cycle leads to high power loss in switches.

Figure 9 shows the voltage stress comparison of power switches versus D. It is clear that the voltage stress of the power switch in the suggested structure is lower than the one in all introduced converters in Table 1 (except [34]). It means that a low on-state resistance switch can be selected in these converters.

Figure 10 illustrates the voltage stress comparison of output diode versus duty cycle. It is evident that the voltage stress of the output diode in the presented structure is lower than the other converters for all ranges of duty cycle (except converters in References [5, 11, 19, 25, 28]). The voltage stress of the output diode in converters [5, 19, 28] are lower than the suggested structure for $D > 0.4$ and $D < 0.4$, respectively. The voltage stress of the output diode in the structures [11, 25] is lower than the suggested structure for all ranges of D. But, these structures have a higher voltage stress across power switch and lower voltage conversion ratio than the suggested structure.

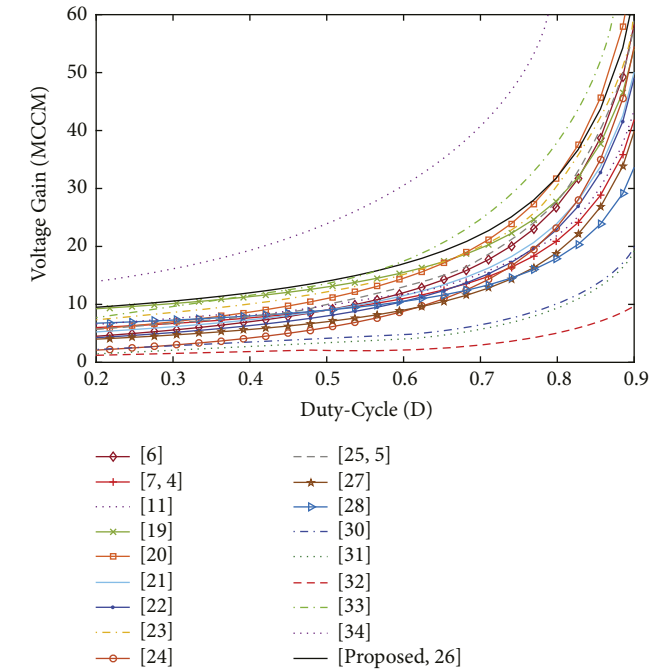


Figure 8: Voltage gain comparison of suggested structure with other converters, $N = 2$.

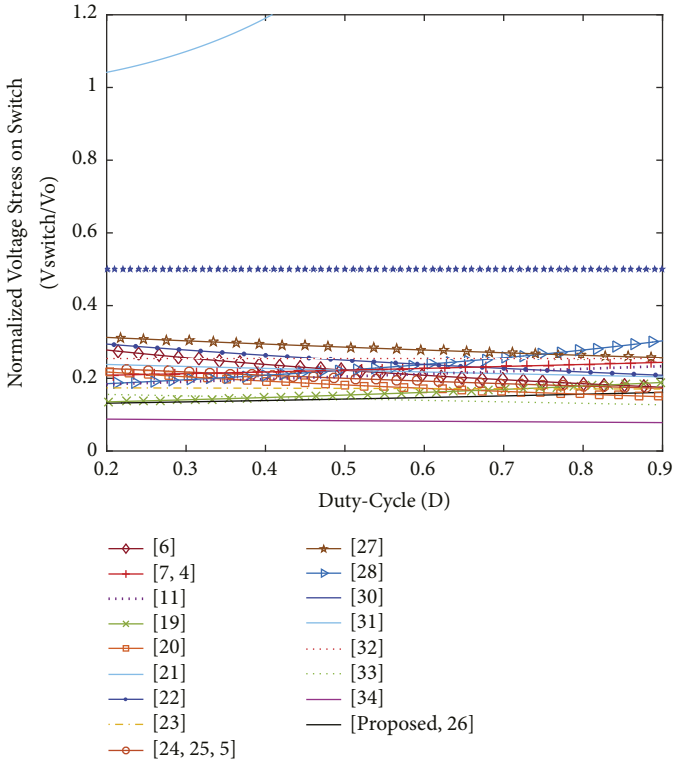


Figure 9: Comparison of the normalized voltage stress of power switch, $N = 2$.

Figure 11(a) depicts the current stress comparison of power switches versus D. It is seen that the current stress in the suggested structure is lower than converters [26, 33] and [34] for $D > 0.4$ and all ranges of duty cycle, respectively. Therefore, the efficiency of the converter in Reference [34] is lower than the proposed converter. Moreover, the minimum rate of current stress of the power switch in the proposed converter happens at duty cycle between $0.3 < D < 0.7$. Figure 11(b) displays the maximum current stress comparison of diodes versus duty cycle. As it can

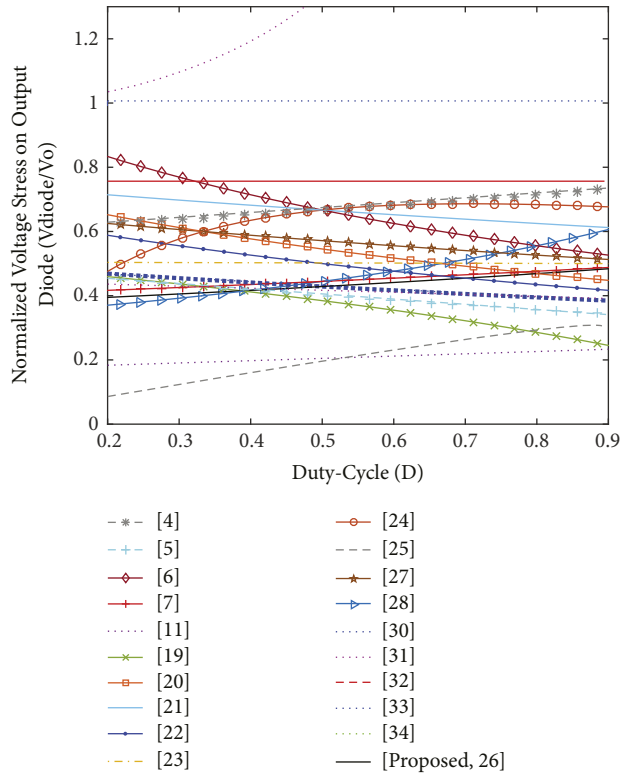


Figure 10: Comparison of the normalized voltage stress of output diode versus, $N = 2$.

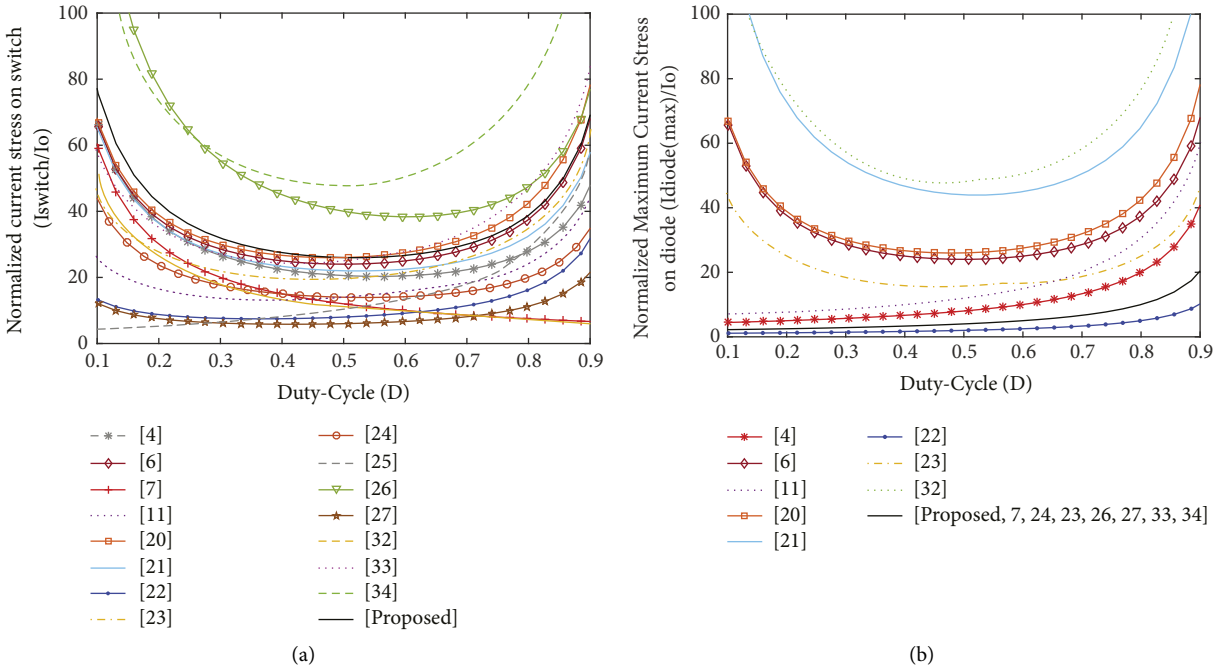


Figure 11: (a) Comparison of the normalized current stress of switch, $N = 2$. (b) Comparison of the normalized maximum current stress of diode, $N = 2$.

Table 2: List of the circuit components of the prototype.

Element	Specification
Power switch S	IRF260 N (200 V/50 A), $R_{DS(ON)} = 0.04\,\Omega$
Diodes	MUR2060 (600 V/20 μA)
C_1, C_2, and C_3	200 V/220 μF
C_o	450 V/470 μF
Coupled inductor	Ferrite EE core with $L_m = 200\,\mu$H
LC input filter	L_{in}: 50 μH
	C_{in}: 220 μF/50 V

Table 3: Specification of the experimental prototype of the presented topology.

Parameter	Value
Rated output power	120 W
V_{in}	12 V
V_{out}	200 V
$(n_1/n_2/n_3)$	1/2/2
Switching frequency (f_s)	50 kHz
Duty cycle	0.6

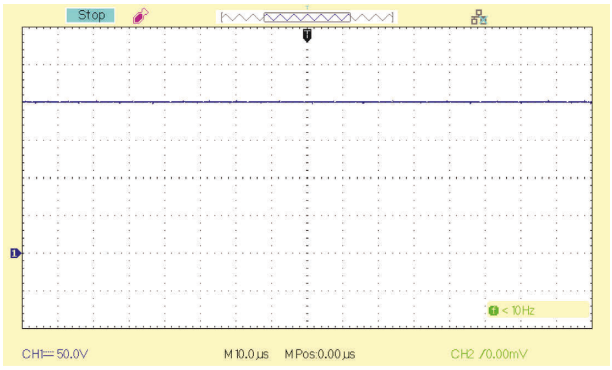


Figure 12: Measured waveform of output voltage V_o.

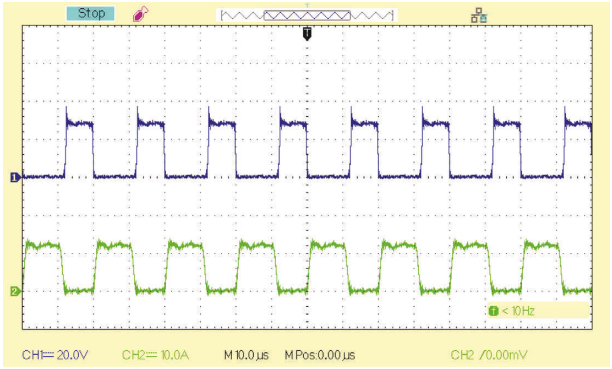


Figure 13: Measured voltage waveform of power switch V_{DS}.

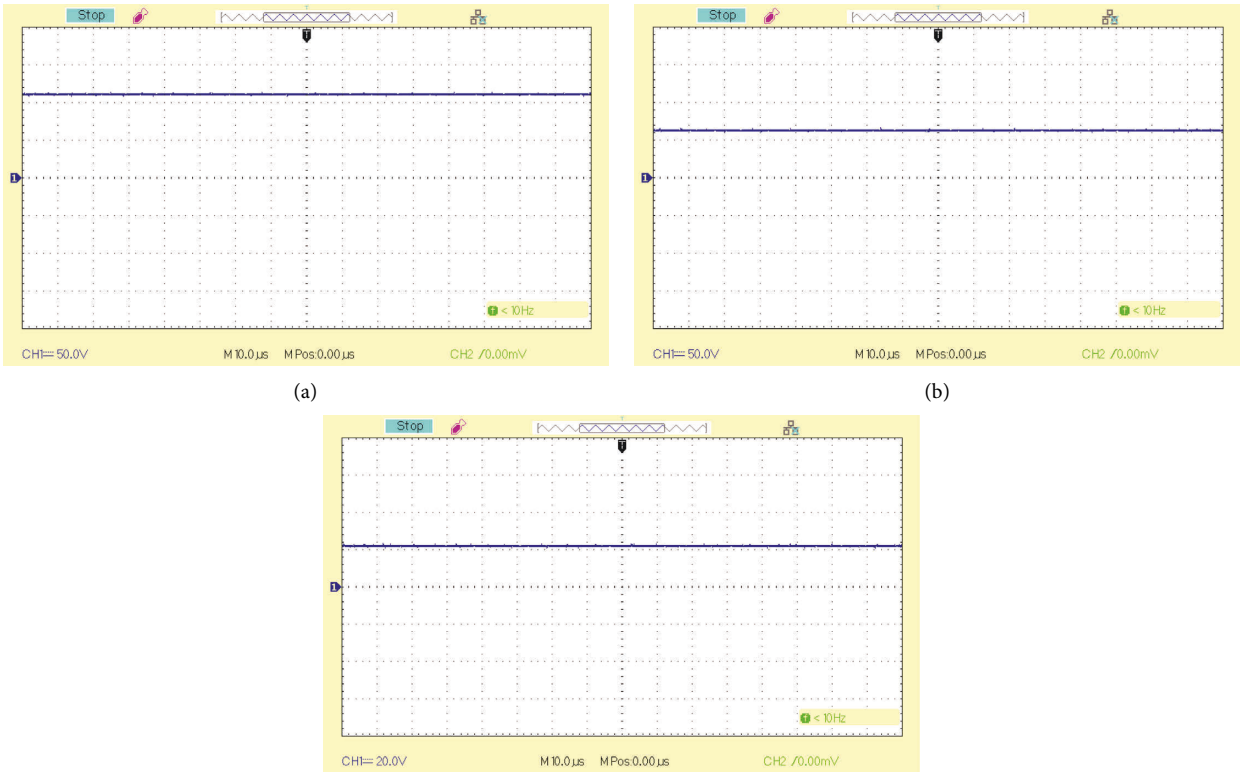


Figure 14: Voltage waveforms of capacitors, (a) V_{C1}, (b) V_{C2}, and (c) V_{C3}.

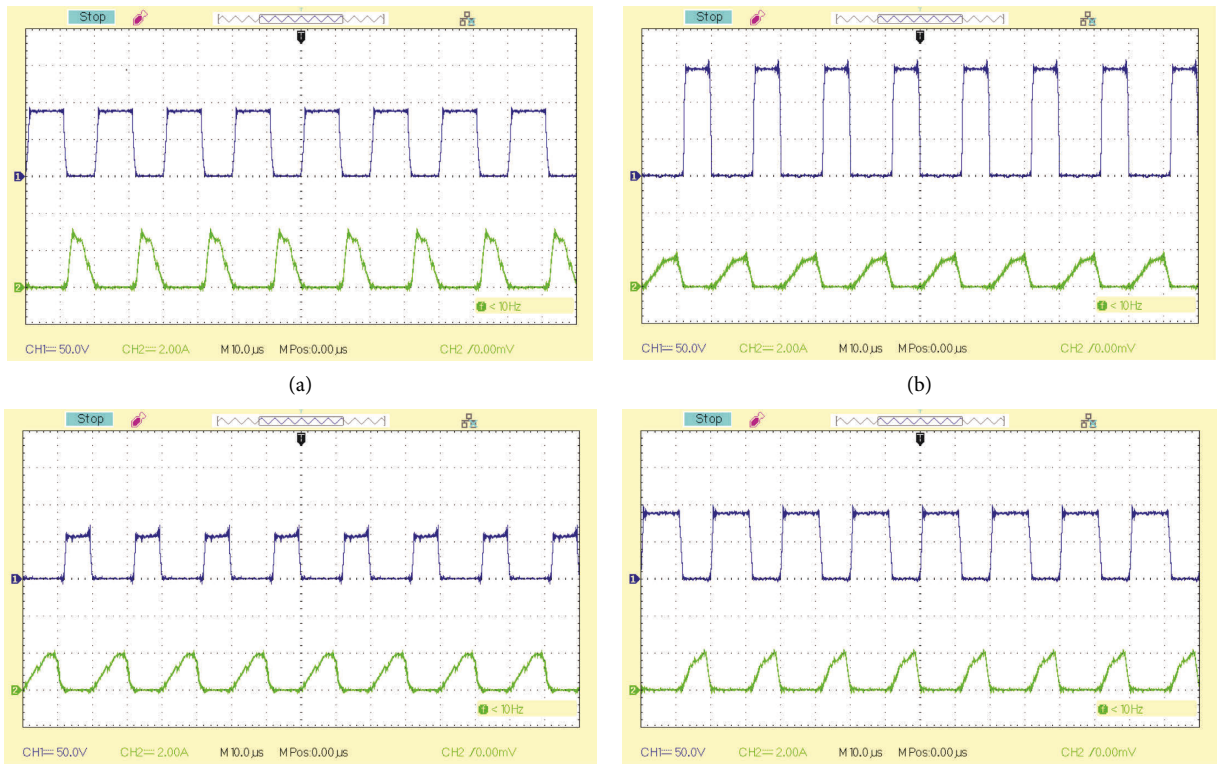
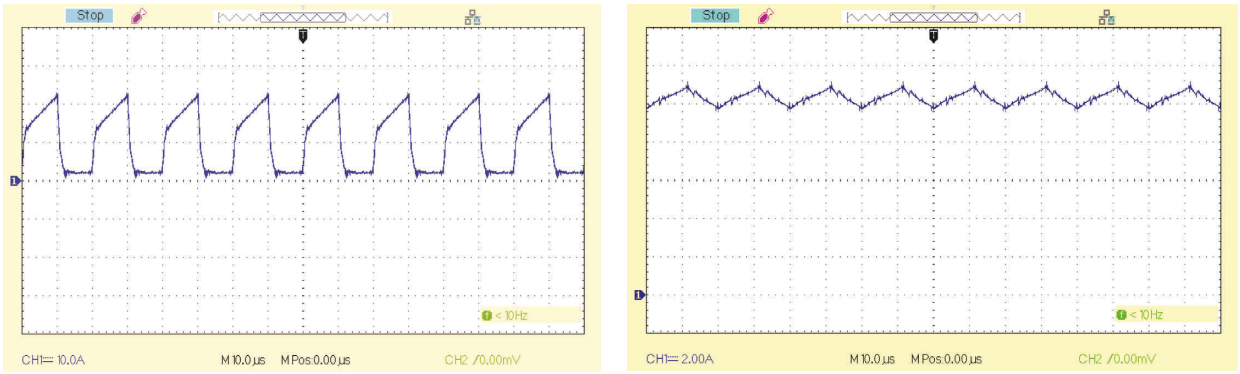


Figure 15: Voltage and current waveforms of diodes, (a) V_{D1} and i_{D1}, (b) V_{D2} and i_{D2}, (c) V_{D3} and i_{D3}, and (d) V_{Do} and and i_{Do}.



(a) (b)

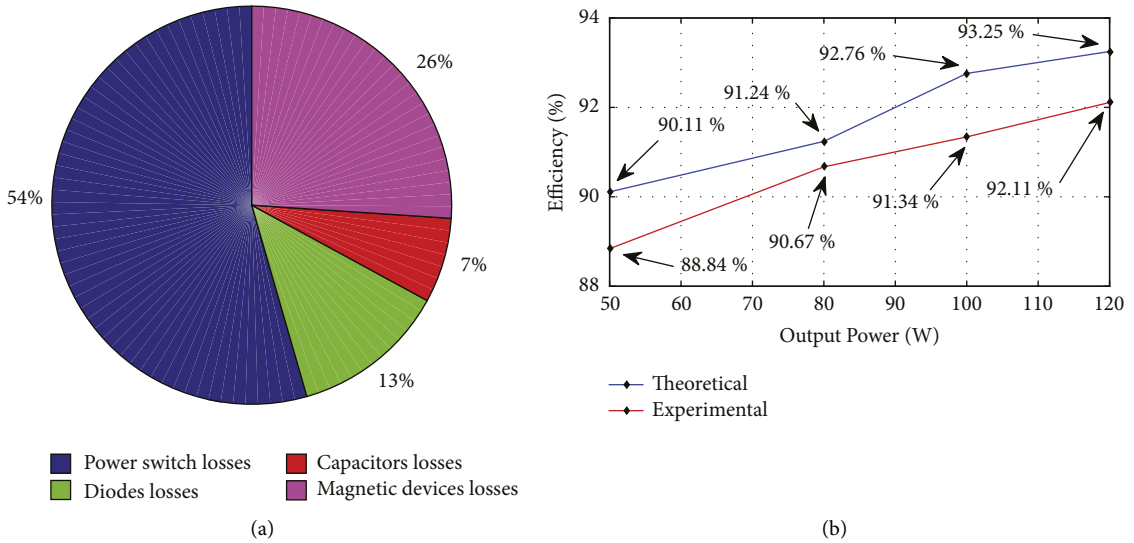
Figure 16: Measured waveform of input source current I_{in}. (a) Without low pass filter and (b) with low pass filter.

Table 4: Comparison between experimental and theoretical voltage values.

Parameter	Experimental value (V)	Theoretical value (V)
V_{C1}	112	114
V_{C2}	64	66
V_{C3}	22	24
V_{Co}	200	204
V_{D1}	88	90
V_{D2}	147	150
V_{D3}	58	60
V_{Do}	88	90
V_{DS}	29	30

Table 5: Power loss specification at $P_o = 120$ W.

Parameter	Value (W)
Total losses of power switch	4.41
Total losses of diodes	1.02
Coupled inductor losses	2.11
Total losses of capacitors and other	0.559
Rated output power	120



(a) (b)

Figure 17: (a) Proportion of component loss breakdown at 120 W. (b) Theoretical and experimental efficiencies of the suggested structure under various output power.

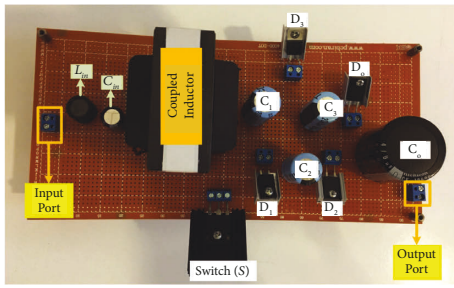


FIGURE 18: Experimental prototype of the proposed converter.

be seen, the maximum current stress on diode in the proposed converter is lower than the one in other structures (except the one in converter [22]).

7. Experimental Results

In order to certify the suggested converter's operation and prove the theoretical results, a 120 W sample has been made in the laboratory. In the proposed converter, the input voltage is boosted from 12 V to 200 V for the duty cycle of 0.6. The circuit components and specifications of the experimental prototype are presented in Tables 2 and 3, respectively.

The experimental results are shown in Figures 12–16. Time per division in the experimental figures is equal to 10μs. Output voltage of the suggested converter is illustrated in Figure 12, which is equal to 200 V for the $D = 0.6$, which confirms equation (17). It is evident that the voltage ripple of the output voltage is very low.

Figure 13 displays the voltage and current of the power switch. Its voltage is equal to 30 V and is much lower than the output voltage, so, it can be noted that a switch with low $R_{DS}(on)$ can be employed in the proposed topology.

Also, this experimental result confirms equation (35). Figures 14(a)-14(c) represent the voltage waveforms of capacitors ($C1 \sim C3$). The experimental value of V_{C1} is equal to 112 V and verifies equation (13). Additionally, V_{C2} and V_{C3} are equal to 64 V and 22 V, which verify equations (12) and (14), respectively.

The voltage and current waveforms of diodes ($D1 \sim Do$) are indicated in Figures 15(a)-15(d). The value of the voltage across diodes D_1 and D_o are equal to 88 V. According to equation (32), the theoretical values of the voltages of these diodes are equal to 90. Also, the voltages across diode D_2 and D_3 are equal to 147 V and 58 V, which confirm equations (33)-(34), respectively. It is plain to see that voltages of diodes are much lower than the output voltage.

The input source current with and without low pass filter is depicted in Figure 16. An LC low pass filter is applied to the converter's input port to reduce the input source current ripple. The proposed converter with an LC low pass filter is shown in Figure 1. Theoretical and experimental voltage values of the semiconductor and capacitors are compared and summarized in Table 4. Experimental values are lower, and this difference is because of the parasitic component effect. Table 5 gives power losses of the elements of the proposed converter at $P_o = 120$ W. It is clear that the main part of the proposed converter total losses is attributed to the switch and diode losses.

Figure 17 shows the proportion of component loss breakdown at $P_o = 120$ W, and the measured theoretical and experimental efficiencies of the recommended topology based on equation (49) under various output powers are ranged from 50 W to 120 W. The maximum value of the efficiency is equal to 92.11% which is derived at $P_o = 120$ W and under $V_{in} = 12$ V, $f_S = 50$ kHz, $n_2 = n_3 = 2$, and duty cycle of 0.6. Also, for output power higher than 80 W, the efficiency is obtained more than 90%. Finally, the experimental prototype of the suggested topology is depicted in Figure 18.

8. Conclusion

In this article, a new single-switch nonisolated high gain DC-DC converter is introduced. To attain a high voltage conversion ratio, a three-winding coupled inductor (TWCL) and a voltage multiplier are used in this topology. VMC also operates as a clamp circuit and recycles the energy of the leakage inductance of the coupled inductor, so voltage stress on the power switch and other semiconductors is reduced and the efficiency will be improved. Steady-state and efficiency analysis of the recommended structure is also provided. Lastly, to prove the operation of the presented structure and the validity of the theoretical results, a 120 W experimental sample with 200 V output voltage is built. According to the theoretical and experimental analyses, it can be expressed that the suggested topology has the following superiorities: (1) high voltage conversion ratio in low duty cycle, (2) low number of elements, (3) input and output sides have common ground, and (4) voltage stress across the power switch and diodes is low, so, a power switch with low $R_{DS\text{-}ON}$ and low-rated diodes can be used that brings about lower power loss, lower cost, and higher efficiency.

Data Availability

The data supporting this study's findings are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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