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Research Article

Advanced Vector Controller for a Four-Switch Three-Phase Rectifier under Unbalanced Grid Voltage

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One of the main challenges of a four-switch three-phase rectifier (FSTPR) is a DC imbalance in capacitor voltages. On the other hand, under unbalanced grid voltage conditions, unbalanced three-phase input current and the DC-link voltage affect the performance of the FSTPR. Although many papers focus on designing a controller to balance DC-link capacitor voltage, a few papers are available to cope with the imbalance of DC-link capacitor voltages and input current simultaneously under unbalanced grid voltage. In this paper, first, the operation of the FSTPR under unbalanced grid voltage conditions is investigated. It can be seen that under these conditions, the oscillatory parts of the active and reactive input power, i.e., sin and cos components, are the leading cause of the problems that can severely degrade the FSTPR performance of the controller. Therefore, this paper presents a promising control technique to eliminate the mentioned oscillation components. Aiming at this purpose, the current control loops in the *dq* axis are divided into two positive and negative sequences, i.e., i_{dq}^{+} and i_{dq}^{-}. Simulation results in MATLAB/SimPowerSystem™ show that the proposed controller can reduce the output voltage ripple, the total harmonic distortion, and the unbalancing of input current compared to a conventional controller. Under these conditions, the DC-link capacitor voltages are more balanced, significantly reducing the voltage limiter of the FSTPR.

1. Introduction

1.1. Motivation. With the daily increase in power grid and flexible alternating current transmission systems (FACTS) and high-voltage direct current (HVDC) transmission, the necessity of using power electronic converters (PEC) has been raised. On the other hand, PEC is an essential and expensive device for power systems. Thus, many tries have been conducted to reduce the expenses of PEC, in which the mentioned converters are introduced with different names such as semiconductor switches reduction, switch-reduced converter, low-cost converter, and element-reduced converters with other usages as well [1]. In a four-switch three-phase converter (FSTPC) with two legs, there are two switches less than six switches with three legs [2]. Therefore, a FSTPC is in the reduced switches group.

1.2. Literature Review. A FSTPC is able to be used as a rectifier and inverter because of having a reverse diode paralleled to switch. In other words, four switch converters are used to reduce expenses, increase robustness performance, and tolerate against faults [3–5]. A FSTPC as an inverter can be used for machine speed controlling, in which many articles have been published in this field, such as induction machines [6, 7], double fed induction machines (DFIM) [8, 9], single-ended primary-inductor converter (SEPIC) [10], permanent magnet synchronous motor (PMSM) [11], brushless PMSM [12], a connection of microgrid to the power grid [13], and active filters [14]. For instance, Wang et al. in [14] proposed a space vector modulation (SVM) and DC-side control algorithm of the FSTPC for application in a parallel active filter. Zhou et al. in [7] designed a model predictive control scheme to control

induction machine speed. Besides, Zaky and Metwaly in [6] investigated the application of FSTPC to drive induction machines at low speeds using fuzzy logic.

Moreover, the four-switch converters are able to be used as a rectifier considered in some articles. For example, space vector modulation to derive switching time [15], distributing vector zero switch [16], modeling, and control at balanced conditions [17]. Designing predictable controller with the observer for load current [18], designing predictable controller at balanced grid [19], designing robust sliding mode [20], designing an auxiliary signal control for omitting the DC amount and current input power factor correction at a balanced voltage [21], and designing controller at an unbalanced grid voltage [22] are articles that have been published in FSTPR subject matter.

1.3. Contribution. The important point regarding the articles considered above is that only Ouni et al [22] have studied designing the proper controller under unbalanced voltage conditions. However, in this article, the operation of a FSTPR under unbalanced voltage with a typical controller and the impact of unbalanced voltage on the rectifier have not been studied. Thus, at first, the operation of a FSTPR with a traditional controller under an unbalanced grid voltage is explored in the current paper. The results show that not only input currents of the rectifier are unbalanced, but also capacitor voltages are imbalanced. The controller needs to separate the positive and negative components of input current and voltage for unbalanced voltage conditions of the grid; therefore, the reference value of the current in the *dq* axis for the positive and negative components is determined separately to eliminate the oscillating components of the real and unreal power. Finally, an auxiliary signal in four-switch rectifiers for operation in the proposed method under unbalanced voltage is designed and developed to eliminate the imbalance in capacitor voltages.

1.4. Organization. The structure of the remainder of the paper is arranged as follows: in Section 2, a mathematical model of FSTPR with a space vector modulation method is presented. In Section 3, a conventional FSTPR controller is introduced. Then, the rectifier under unbalanced conditions is considered, and the oscillating variables, either with real power or an unreal one, are derived. Furthermore, a current reference signal for i_{dq}^{+} and i_{dq}^{-} is determined by introducing a suitable method for separating positive and negative variables. In Section 4, simulation results and analysis are presented, and finally, the conclusion and future research are shown in Section 5.

2. Four-Switch Three-Phase Rectifier (FSTPR)

2.1. Mathematical Model. According to Figure 1, a FSTPR has two parts, i.e., AC and DC. For describing the *dq* frame model, synchronously rotating frame with direct and quadrature components, transformation matrix called

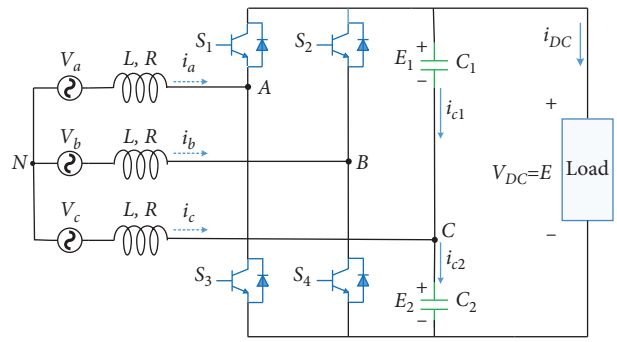

Figure 1: Topology of a FSTPR.

reduced Park Transformation, and T matrix shown in the following equation is used to convert parameters of FSTPR into the synchronous frame [23].

$$T_u = \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\pi\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\pi\right) \end{bmatrix}, \tag{1}$$

where ωt is the angle determined by the source supply voltage with angular frequency ω. Also, considering AC currents in *dq* frame and DC-link voltage as state variables, the state equations of the FSTPR in the rotating *dq* frame are obtained as the equations that are mentioned below [23]. It should be noted that DC-link voltages are equally supposed in the following equations.

$$\frac{di_d}{dt} = -\frac{R}{L}i_d - \omega i_q - \frac{1}{3L}Ev_d - \frac{1}{3L}v_{cd} + \frac{V_m}{L}, \tag{2}$$

$$\frac{di_q}{dt} = \omega i_d - \frac{R}{L}i_q - \frac{1}{3L}Ev_q - \frac{1}{3L}v_{cq}, \tag{3}$$

$$\frac{dE}{dt} = \frac{1}{C}\left(v_d i_d + v_q i_q\right) - \frac{2}{R_L C}E, \tag{4}$$

where v_d and v_q and i_d and i_q are converter's input voltages and currents in *dq* axis, respectively; R and L are line resistance and inductance, respectively; R_L and C are load resistance and capacitance value, respectively. Additionally, ω is the angle speed; u_d and u_q are fundamental voltage in *dq* reference frame; V_m and E are the amplitude of the phase and output voltage, respectively; v_{cd} and v_{cq} are also the capacitor voltage difference terms [23].

2.2. Simplified Space Vector Modulation (SSVM) for FSTPR. As shown in Figure 1, in a FSTPR, the number of switching states and the output voltage vectors lead to four voltage vectors in the vector space modulation (SVM) method. According to Table 1, the four vectors shown in Figure 2 can be drawn. In this method, the time and size of the vector are calculated according to which quarter of the vector space is located [5]. Note that the vector E is located in the first quarter as Figure 2.

Table 1: The four possible voltage vector values for the FSTPR in the stationary reference frame.

Vector	v_A	v_B	v_C	v_α	v_β
V_{00}	$2E_2/3$	$-E_2/3$	$-E_2/3$	$2E_1/3$	0
V_{10}	$E_2 - E_1/3$	$2E_2 + E_1/3$	$-E_1 + 2E_2/3$	$E_2 - E_1/3$	$E_1 + E_2/\sqrt{3}$
V_{11}	$-2E_1/3$	$E_1/3$	$E_1/3$	$-2E_1/3$	0
V_{01}	$E_2 - E_1/3$	$-E_2 - 2E_1/3$	$2E_1 + E_2/3$	$E_2 - E_1/3$	$E_1 + E_2/\sqrt{3}$

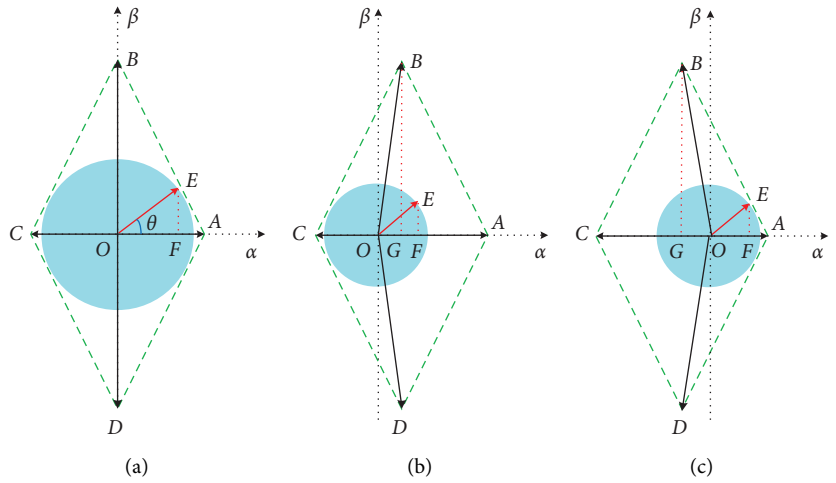

Figure 2: SSVM allocation for FSTPR topology; (a) $E_1 = E_2$, (b) $E_1 < E_2$, and (c) $E_2 < E_1$.

3. FSTPR Controllers under Balanced and Unbalanced Grid Voltages

As mentioned in the first section, controllers of FSTPR are usually designed and provided for balanced conditions. Since three-phase rectifiers have sensitive applications in industry, they must at least be able to work with the unbalanced permissible grid voltage. In the other hand, grid faults can cause voltage imbalance in the power grid, such as three-phase and two-phase. In this section, at first, the conventional controller method is introduced. Then, the traditional controller is modified so as to the rectifier has the desired performance under various grid voltages.

3.1. Conventional Controller of FSTPR. A conventional controller for FSTPR (CCFSTPR) is designed for a balanced condition showing all loops in Figure 3. According to this figure, the CCFSTPR is made of two loops on axes d and q. Loop of d axis is designed to control DC-link capacitor voltages in phase C and loop of q axis handles the input power factor. In this study, the input power factor is considered as the unity, that is to say, $i_q^* = 0$. Note that the voltage loop should be much slower than the current loop for designing the voltage loop's proportional and integral controller gains. In other words, the voltage loop's bandwidth should be less than the current loop one.

In the proposed strategy in [17], as shown in Figure 3, the balancer signal of capacitor voltages is added to the reference current of both d and q loops as an auxiliary signal. These signals, $i_{d\text{-}aux}$ and $i_{q\text{-}aux}$, are used to suppress deviation of capacitor voltages, i.e., E_1 and E_2.

3.2. PI Controller Tuning of Conventional Controller. This section aims to design the converter controller to meet the desired modifications. The control objectives can be summarized as follows: (1) Set the output voltage to the specified reference values, (2) unit input power factor for different loads, and (3) desired response for variations of output load and voltage in the rectifier. It should be noted that the converter controller includes a current and voltage loop, which is discussed in the following.

3.2.1. Design of Current Loop Controller. For the unity input power factor, the input current has only a d-axis component. Therefore, the reference value of the q-axis component of the input current is considered to be zero.

Regarding the transfer function from the output current to the d and q axis input voltage [21], the open loop bandwidth of the rotor current control is R/L. Therefore, considering the rotor controllers to be PI, $k_{pi\_idq} = k_{p\_idq} + k_{i\_idq}/s$, the current open loop transfer function is as follows:

$$G_{ol} = \left(k_{pi} + \frac{k_{ii}}{s}\right)\frac{1}{Ls + R} = \frac{k_{pi}}{s}\left(s + \frac{k_{ii}}{k_{pi}}\right)\frac{1}{L(s + \alpha_{ol})}. \quad (5)$$

By canceling the plant pole with the zero of the controller, i.e., $k_{ii}/k_{pi} = R/L$, the current closed-loop transfer function can be written as follows:

$$G_{cl} = \frac{k_{pi}/L}{s + k_{pi}/L}. \quad (6)$$

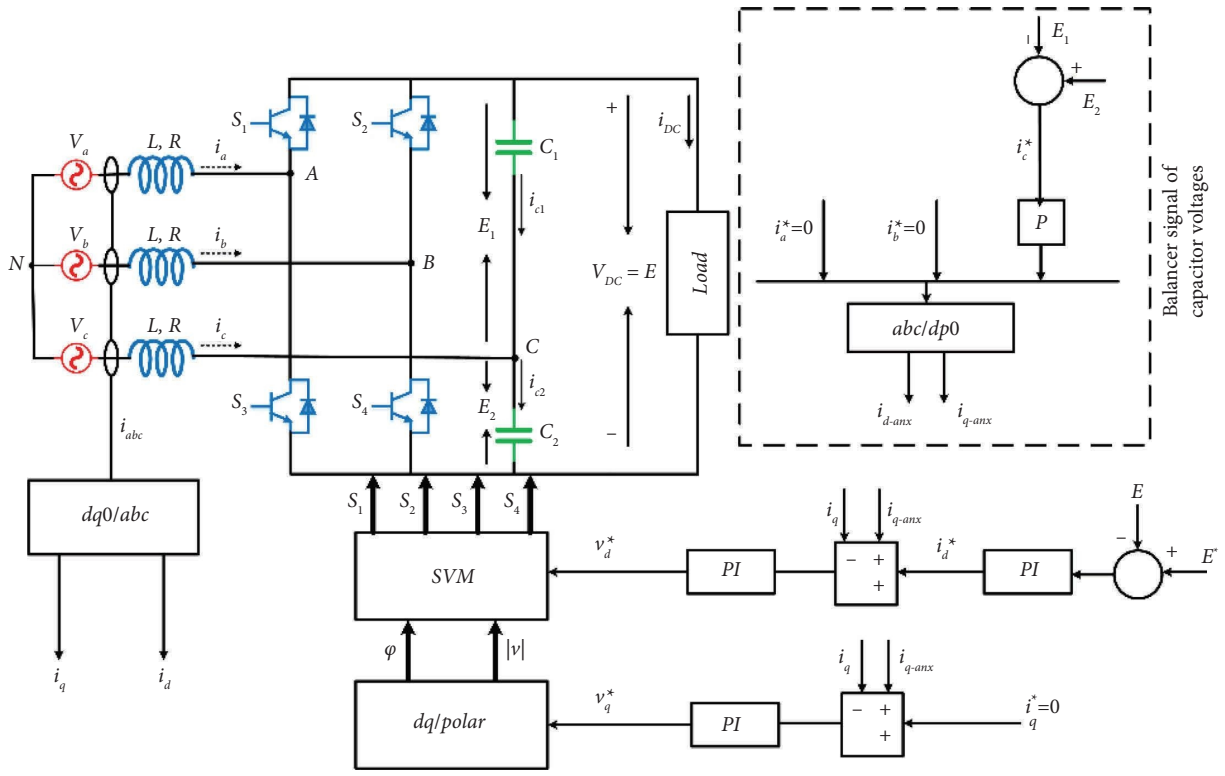

Figure 3: Block diagram of the conventional controller for FSTPR.

Since the current loop is fast, its closed-loop bandwidth (α_I=k_{pi}/L) is selected to be 1000π, and therefore, k_{pi} is computed to be $L\alpha_I$.

3.2.2. Design of Voltage Loop Controller. The inner loop is considered a first-order transfer function. The block diagram of the control system for the voltage loop is shown in Figure 3. Similar to the current loop, a PI controller is also used for the voltage loop. However, it should be noted that the voltage loop must be much slower than the current loop. In other words, the bandwidth of the voltage loop is less than the bandwidth of the current loop. With a fair approximation, since the rotor current control loop is fast enough, it is possible to neglect the closed-loop pole, i.e., we can neglect the dynamic of the current loop. Therefore, the open loop transfer function of the voltage control loop is as follows [21]:

$$H_{ol} = \left(K_{pv} + \frac{K_{iv}}{s}\right)\frac{3/4\,R_L U_d/E}{1/2C_{eq}R_L s + 1}. \tag{7}$$

The closed-loop bandwidth of the voltage controller and damping coefficient is assumed to be $\omega_B = 30\pi$ and $\xi = 0.85$, respectively [21]. On the other hand, in the second order system, for the specified damping coefficient, the phase margin is equal to $\varphi_M \approx 100\xi$, i.e., 85 degrees here. Moreover, with a phase margin, the following equation can be written [24]:

$$\angle H_{ol}(j\omega_c) = -180 + \varphi_M = -95\,\text{deg}, \tag{8}$$

where ω_c is the cutoff angular frequency of the voltage loop. Eventually, considering equations (7) and (8), PI controller coefficients are computed as $K_{pv} = 0.0526$ and $K_{iv} = 2.297$.

3.3. Proposed Controller of FSTPR for Unbalanced Condition

3.3.1. Analysis of FSTPR Behavior under the Unbalanced Condition. Given the instantaneous power theory, real and unreal powers in the stationary $\alpha\beta$ reference frame are as follows [25]:

$$p = v_\alpha i_\alpha + v_\beta i_\beta, \tag{9}$$

$$q = v_\beta i_\alpha - v_\alpha i_\beta, \tag{10}$$

where $i_{\alpha\beta}$ and $v_{\alpha\beta}$ are $\alpha\beta$ components of voltage and current, respectively.

Also, these can be obtained from summing the positive and negative sequences according to equations (7)–(10).

$$v_\alpha = v_\alpha^+ + v_\alpha^-, \tag{11}$$

$$v_\beta = v_\beta^+ + v_\beta^-, \tag{12}$$

$$i_\alpha = i_\alpha^+ + i_\alpha^-, \tag{13}$$

$$i_\beta = i_\beta^+ + i_\beta^-. \tag{14}$$

Using equations (5)–(10) and Park's transformation, the instantaneous real and unreal power considering positive and negative dq sequences can be written as follows:

$$p = v_d^+ i_d^+ + v_q^+ i_q^+ + v_d^- i_d^- + v_q^- i_q^- + \sin(2\theta)\left(v_d^+ i_q^- - v_q^+ i_d^- + v_q^- i_d^+ - v_d^- i_q^+\right) + \cos(2\theta)\left(v_d^+ i_d^- + v_q^+ i_q^- + v_d^- i_d^+ + v_q^- i_q^+\right), \quad (15)$$

$$q = v_q^+ i_d^+ - v_d^+ i_q^+ + v_q^- i_d^- - v_q^- i_q^- + \sin(2\theta)\left(v_d^+ i_d^- + v_q^+ i_q^- - v_d^- i_d^+ - v_q^- i_q^+\right) + \cos(2\theta)\left(v_q^+ i_d^- - v_d^+ i_q^- + v_q^- i_d^+ - v_d^- i_q^+\right). \quad (16)$$

Regarding equations (11) and (12), i.e., p and q relationships, either of the powers consists of three parts; the first part shows average power, and both second and third parts are oscillations parts. Note that the real power oscillation part causes oscillation directly in DC-link voltage [25]. In the next part, this approach is used to design a novel balancer signal at unbalanced conditions.

According to the instantaneous real and unreal powers shown in equations (11) and (12), it is obvious that the values of $v_{\mathrm{dq}}^{\pm}$ and $i_{dq}^{\pm}$ are required to extract the oscillating components. Therefore, a suitable method for separating the $dq^{\pm}$ components are provided in the next part.

3.3.2. Separating Positive and Negative Components. According to equations (11) and (12), in the case of unbalanced input voltage, the values of the positive and negative sequence components of voltage and current must be available to correct the controller. Several methods are used for this purpose, including the use of a low-pass filter, short-pass filter, and delay signal removal methods proposed in [25, 26]. The low-pass filter method used to separate sequence components reduces the stability margin due to the negative phase, and may even cause system instability in some cases. Therefore, the effect of this filter should be considered in the design of the controller. In the method of using a transient filter, the second harmonic component is separated from the converted signal by the positive sequence reference, and the positive dq component is obtained, and the same is performed to convert the negative dq components. In this method, as mentioned earlier in the previous form, the problem of applying a negative phase by the filter and the possibility of instability of the control system is one of the disadvantages of this method. Whereas in another technique called deletion of the delay signal in [25], unlike the previous two ways, the sequences are separated without the use of filters and only rely on mathematical calculations. For this purpose, the $\alpha\beta$ voltage component is first calculated by Clark transformation, and mathematical relations separate the positive and negative elements.

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \begin{bmatrix} v_\alpha^+(t) + v_\alpha^-(t) \\ v_\beta^+(t) + v_\beta^-(t) \end{bmatrix} = \begin{bmatrix} v^+\cos(\omega_s t + \varphi^+) + v^-\cos(\omega_s t + \phi^-) \\ v^+\sin(\omega_s t + \varphi^+) + v^-\sin(\omega_s t + \varphi^-) \end{bmatrix}. \quad (17)$$

By shifting up to T/4 for $\alpha\beta$ elements, it can be written as follows:

$$\begin{bmatrix} v_\alpha\left(t - \frac{T}{4}\right) \\ v_\beta\left(t - \frac{T}{4}\right) \end{bmatrix} = \begin{bmatrix} v^+\sin(\omega_s t + \phi^+) - v^-\sin(\omega_s t + \phi^-) \\ -v^+\cos(\omega_s t + \phi^+) + v^-\cos(-\omega_s t + \phi^-) \end{bmatrix}. \quad (18)$$

As shown in equation (15), the positive sequence and the negative sequence part of $\alpha\beta$ components are calculated using equations (13) and (14).

$$\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \\ v_\alpha^- \\ v_\beta^- \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 \end{bmatrix}\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_\alpha\left(t - \frac{T}{4}\right) \\ v_\beta\left(t - \frac{T}{4}\right) \end{bmatrix}. \quad (19)$$

Finally, using the previous equations, the positive and negative sequences of the dq components can be obtained as follows:

$$\begin{bmatrix} v_d^+ \\ v_q^+ \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}.\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = T_{dq}(\theta).\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix}, \quad (20)$$

$$\begin{bmatrix} v_d^- \\ v_q^- \end{bmatrix} = \begin{bmatrix} \cos(-\theta) & \sin(-\theta) \\ -\sin(-\theta) & \cos(-\theta) \end{bmatrix}.\begin{bmatrix} v_\alpha^- \\ v_\beta^- \end{bmatrix} = T_{dq}(-\theta).\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix}. \quad (21)$$

3.3.3. Proposed Controller under Unbalanced Voltage. As shown in part A, DC link voltage oscillations are caused by $\sin(2\theta)$ and $\cos(2\theta)$ components and instantaneous real power in unbalanced conditions. On the other hand, in a FSTPR, it is desirable that the input power factor of the converter is set to zero ($Q_{\mathrm{ref}} = 0$); that is, the oscillating components in unreal power can be ignored. Therefore, in this case, the goal is that the reference value of unreal power and oscillating components should not be produced and

considered equal to zero. Thus, the relations (11) and (12) can be written as follows (18):

$$\begin{bmatrix} P_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_d^+ & u_q^+ & u_d^- & u_q^- \\ u_q^+ & -u_d^+ & u_q^- & -u_d^- \\ u_q^- & -u_d^- & -u_q^+ & u_d^+ \\ u_d^- & u_q^- & u_d^+ & u_q^+ \end{bmatrix} \cdot \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}. \tag{22}$$

It should be noted that the value of the real power reference signal is extracted from the voltage difference of the capacitor voltages and applied to equation (18). Therefore, the values of the current's positive and negative sequence components can be defined as follows:

$$\begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}_{ref} = \frac{2}{3} \begin{bmatrix} u_d^+ & u_q^+ & u_d^- & u_q^- \\ u_q^+ & -u_d^+ & u_q^- & -u_d^- \\ u_q^- & -u_d^- & -u_q^+ & u_d^+ \\ u_d^- & u_q^- & u_d^+ & u_q^+ \end{bmatrix}^{-1} \cdot \begin{bmatrix} P_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{23}$$

Equation (19) can be simplified as follows:

$$\begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix}_{ref} = \frac{2}{3} \frac{P_{ref}}{\left[\left(u_d^+\right)^2 + \left(u_q^+\right)^2 \right] - \left[\left(u_d^-\right)^2 + \left(u_q^-\right)^2 \right]} \begin{bmatrix} u_d^+ \\ u_q^+ \\ -u_d^- \\ -u_q^- \end{bmatrix}. \tag{24}$$

The controller designed for the FSTPR is shown in Figure4. As it turns out, instead of the two loops in the CCFSTPR shown in Figure 3, there are four loops designed for the positive and negative components for the dq axes, with reference values obtained through equation (20). Also, as mentioned in Figure 5, the real reference power, i.e., p_{ref}, is determined by a separate loop by the voltage fluctuation of DC capacitors.

After calculating the positive and negative components of the current in the dq axes, i.e., i_{dq}^+ and i_{dq}^-, which are considered the current reference value, the positive and negative components of the dq axes must be determined by the separating method introduced in the last part. According to Figure 4, four control loops are designed on dq axes for the positive and negative components, which are selected as reference voltages: v_{dP}^*, v_{qP}^*, v_{dN}^*, and v_{qN}^*. Another contribution in the proposed controller is the auxiliary voltage balancing signal, which will be introduced in the following.

Note that the constraint of equation (21) is applied to avoid occurring over modulation.

$$\left| \overrightarrow{V_d^+} + \overrightarrow{V_d^-} + \overrightarrow{V_q^+} + \overrightarrow{V_q^-} \right| < V_m. \tag{25}$$

The design of an auxiliary signal so as to balance the voltage of the capacitor voltages in phase C is another critical point. As it is evident in Figure 5, unlike the previous auxiliary control signals, shown in Figure 6, the proposed signal, $i^+_{d\text{-}aux}$ and $i^+_{q\text{-}aux}$, resulting from the voltage difference of DC capacitors and by converting dq signals for positive components are designed and added to the control loop. Using this approach and strategy, it is expected to balance the input currents of the converter as well as suppress the deviation of capacitor voltage.

4. Simulation

To test how the proposed controller works under asymmetric voltage, a FSTPR with the proposed controller is simulated in Simpower at discrete step-size = $5e-5$. The parameters of a FSTPR considered for simulation study are shown in Table 2.

In this section, simulation cases have three definitions as mentioned below:

(1) First: simulation of four key three-phase rectifiers with suggested controller in at unbalanced section voltage condition named Scen1.

(2) Second: Simulation of four key three-phase rectifiers with suggested controller in [17] at normal section voltage condition named Scen2.

(3) Third: simulation of four key three-phase rectifiers with suggested controller at unbalanced section voltage condition named Scen3.

In this section, three cases are defined for the simulation study.

(i) Simulation of a FSTPR with a controller presented in [17] under unbalanced grid voltage conditions, given in the simulation results as case 1.

(ii) Simulation of a FSTPR with a controller presented in the reference [17] under balanced voltage conditions, given in the simulation results as case 2.

(iii) Simulation of a FSTPR with the proposed controller under unbalanced grid voltage conditions, given in the simulation results as case 3.

It should be noticed that because the acceptable amount of unbalanced for voltage surface is 380 or 2% [27], the simulation in the unbalanced case is performed by adding 8% negative item, V_i to the main section voltage that the forms, Figures7(a) and 7(b), show three-phase section voltage in normal and unbalanced conditions.

It is noteworthy that, given that the acceptable value of the voltage imbalance for the 380 V voltage level is about 2% [27], the simulation in the unbalanced condition is performed by adding 8% of the negative sequence V_1^- to the fundamental component of the grid voltage. Figures 8(a) and 8(b) show the three-phase voltage of the grid under balanced and unbalanced conditions, respectively.

Figure 9 shows the switching time for each voltage vector, which is calculated by the calculation block and the relationships related to the switching time of each vector.

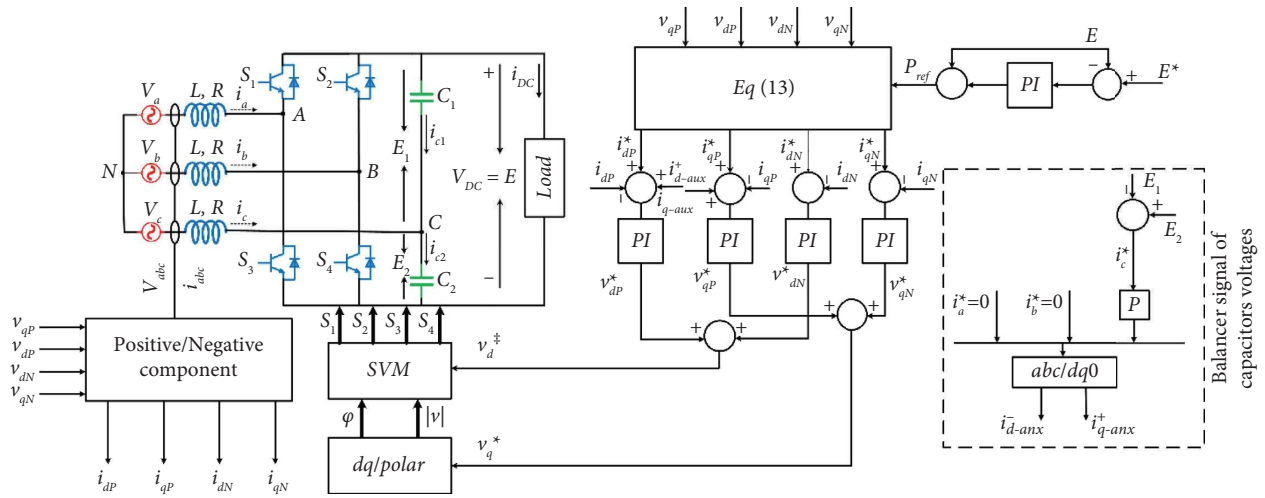

Figure 4: Block diagram of the proposed controller for FSTPR under unbalanced grid voltage.

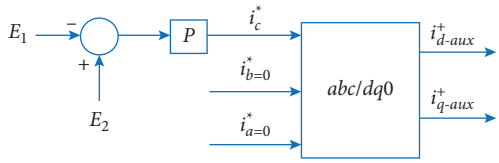

Figure 5: A novel deviation suppression signal for DC-link capacitor voltage.

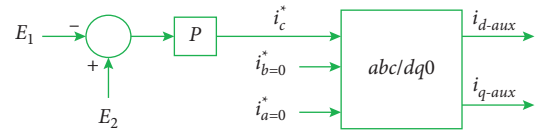

Figure 6: The deviation suppression signal for DC-link capacitor voltage proposed in [17].

Each of these times is a proportion of a switching period (50 μsec) at a frequency of 20 kHz. If the SSVM control method works in saturation mode, the calculated value will be negative for some of these times, which is unacceptable. Therefore, according to the values obtained for these quantities during the simulation period, which are positive values and less than 50 sec, it can be concluded that SSVM operates under normal conditions and saturation has not occurred.

Figure 8 shows the input current waveforms with the proposed and conventional controller. According to Figure 8(b), the input current imbalance is evident when the controller is used for balanced conditions. While using the proposed controller for unbalanced conditions, the currents are perfectly balanced.

Figure 10 shows the reference values of the *dq* components for the current's positive and negative sequences. As can be seen, the results are in accordance with the values calculated in Table 2. On the other hand, according to the figure, the reference value of the negative and positive components on the *q*-axis are zero, which is due to the design of the converter for operation in the unity power factor.

Figure 11 shows the negative component of the three-phase input current with the proposed controller. As it turns out, the switching ripple is more noticeable owing to the amplitude of the negative sequence current being smaller.

The shape of output voltage wave (E) and condenser voltage (E_1 and E_2) are described as three forms, old controller at unbalanced condition (Scen1), old controller at normal condition (Scen2), and new suggested controller at the unbalanced state, which can be seen at Figures 12 and 13.

Table 2: Simulation parameters for FSTPR.

Variable	Value
P_{out}	6 kW
V_{in}	380 V L-L
f	50 Hz
DC-link voltage	1200 V
f_s	20 kHz
C_1	600 μf
C_2	600 μf
L	4 mH
R_S	0.2 Ω

It is shown that by using the proposed controller at unbalanced conditions (Scen3), condensers voltage are concurrent, and output voltage has less ripple and 1200 v average. Due to Figure 12, output voltage (E) in Scen2 has curve 4 v and in Scen1 and abnormal condition the curve arise to 40 v. Finally, by applying the suggested controller in this article for unbalanced conditions (Scen3), the voltage curve is less than 1 v, which is an acceptable and predictable performance for the recommended controller.

Output voltage waveform (E) and capacitor voltages (E_1 and E_2), with three mentioned scenarios, case 1, case 2, and case 3, are seen in Figures 12 and 13, respectively. It can be seen that using the proposed controller in unbalanced conditions (case 3), the voltage of the capacitors is symmetric, and the output voltage with low ripple has an average value of 1200 V. According to Figure 12, the output voltage (E) in case 2 has a distortion of 4 volts, which in case 1 and unbalanced conditions, its distortion reaches about 40 volts. Finally, by applying the proposed controller in this paper for

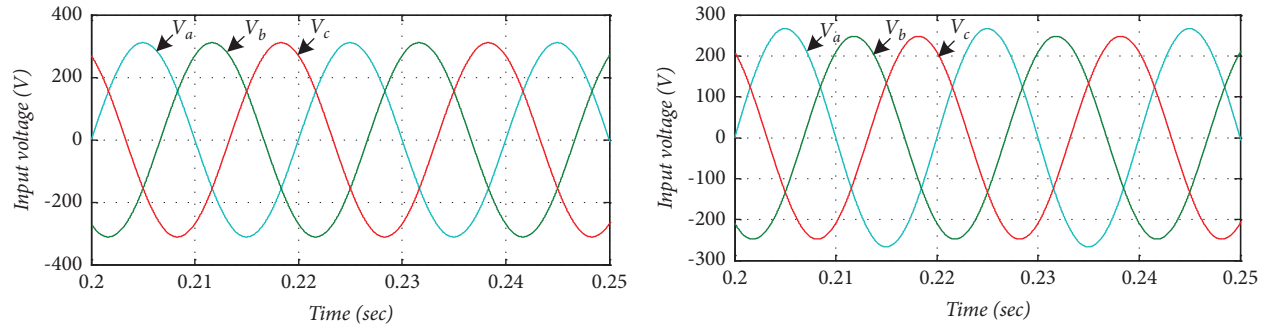

Figure 7: Grid input voltage; (a) balance and (b) unbalance condition with 8% negative sequence component.

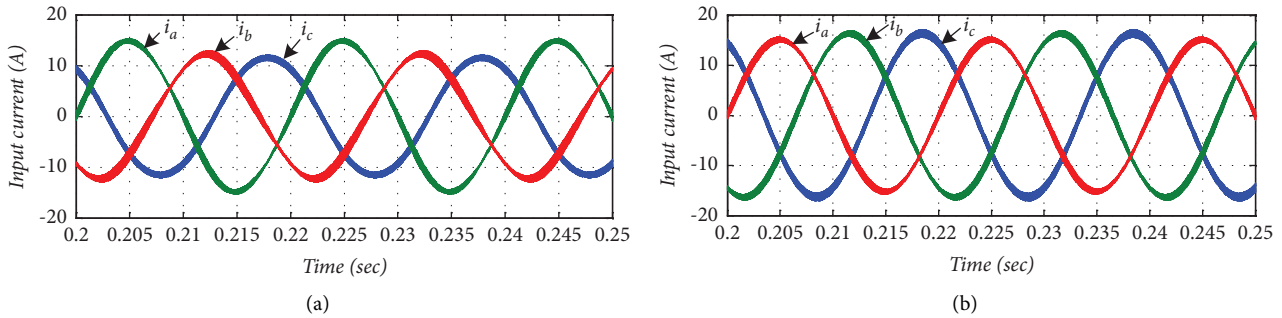

Figure 8: Three-phase input current under unbalanced grid voltage with a different controller; (a) proposed and (b) conventional.

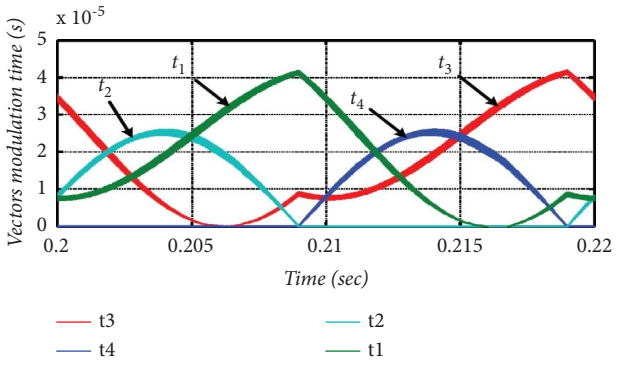

Figure 9: Switching time of voltage vectors in different regions for proposed controller under unbalanced grid voltage.

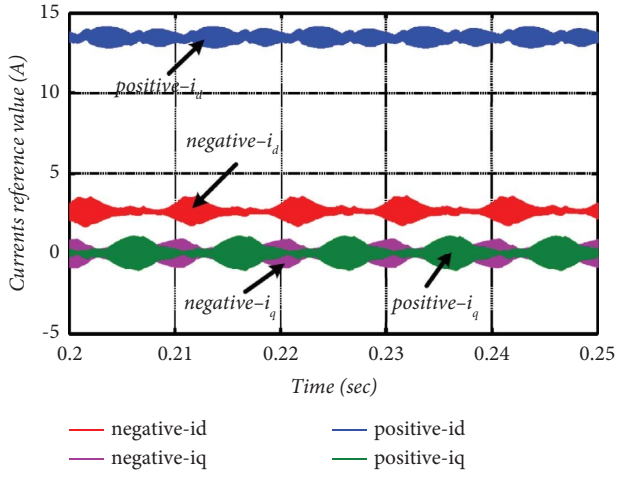

Figure 10: Positive and negative components on dq axis of input current using proposed controller under unbalanced grid voltage.

unbalanced conditions (case 3), the voltage distortion is less than 1 V, which shows the acceptable and expected performance of the proposed controller.

The capacitor voltages (E_1 and E_2) for the three defined cases are shown in Figure 13. On the other hand, the maximum voltage that can be generated is defined through $V_m = \min(E_1/\sqrt{3}, E_2/\sqrt{3})$. Therefore, the larger the capacitor voltage value in a method, the lower the probability of saturation in SSVM. Thus, according to Figure 13, this value for the proposed controller is 585 volts, about 30 volts more than the CCFSTPR.

Figure 14 shows the input currents on dq axis for the three cases studied. As can be seen from the figure, the performance of the proposed controller in the unbalanced condition is similar to (somewhat better) the performance of the conventional controller in the balanced condition. The CCFSTPR in the unbalanced condition has fluctuations caused by terms $\sin(2\theta)\cos(2\theta)$ and around the value of dc. Also, the currents of the q-axis have an average value of zero for all three states, which indicates the performance of the rectifier in the unity power factor.

Figure 15 shows the input current of each three-phase and its THD frequency spectrum for proposed and conventional controllers. Two points from this figure can be mentioned. First, the proposed controller's input current has

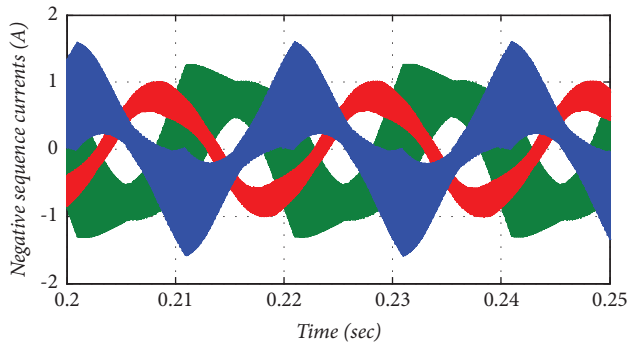

Figure 11: Negative sequence component of three-phase input current using proposed controller under unbalanced grid voltage.

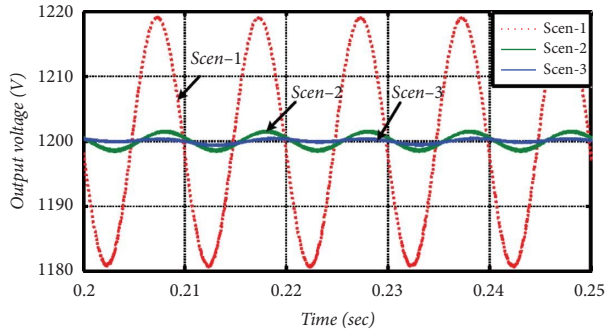

Figure 12: Output voltage for both old and suggested controller in normal and unbalanced condition.

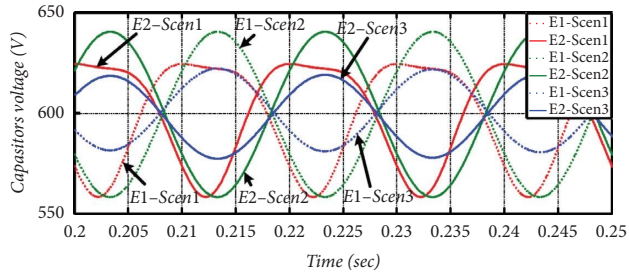

Figure 13: DC-link capacitor voltages for both proposed and conventional controller in various scenarios.

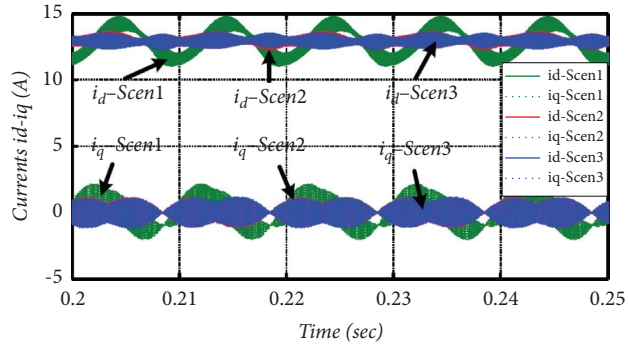

Figure 14: *dq* axis input current for both proposed and conventional controller in various scenarios.

a lower THD and a larger fundamental component value than that of the CCFSTPR. Second, the frequency range of the rectifier input current with the proposed controller is wider than the frequency spectrum of the rectifier input current with the CCFSTPR. Also, the THD of output current with the proposed controller is reduced by about 1% in each phase compared to the case where the conventional controller is used.

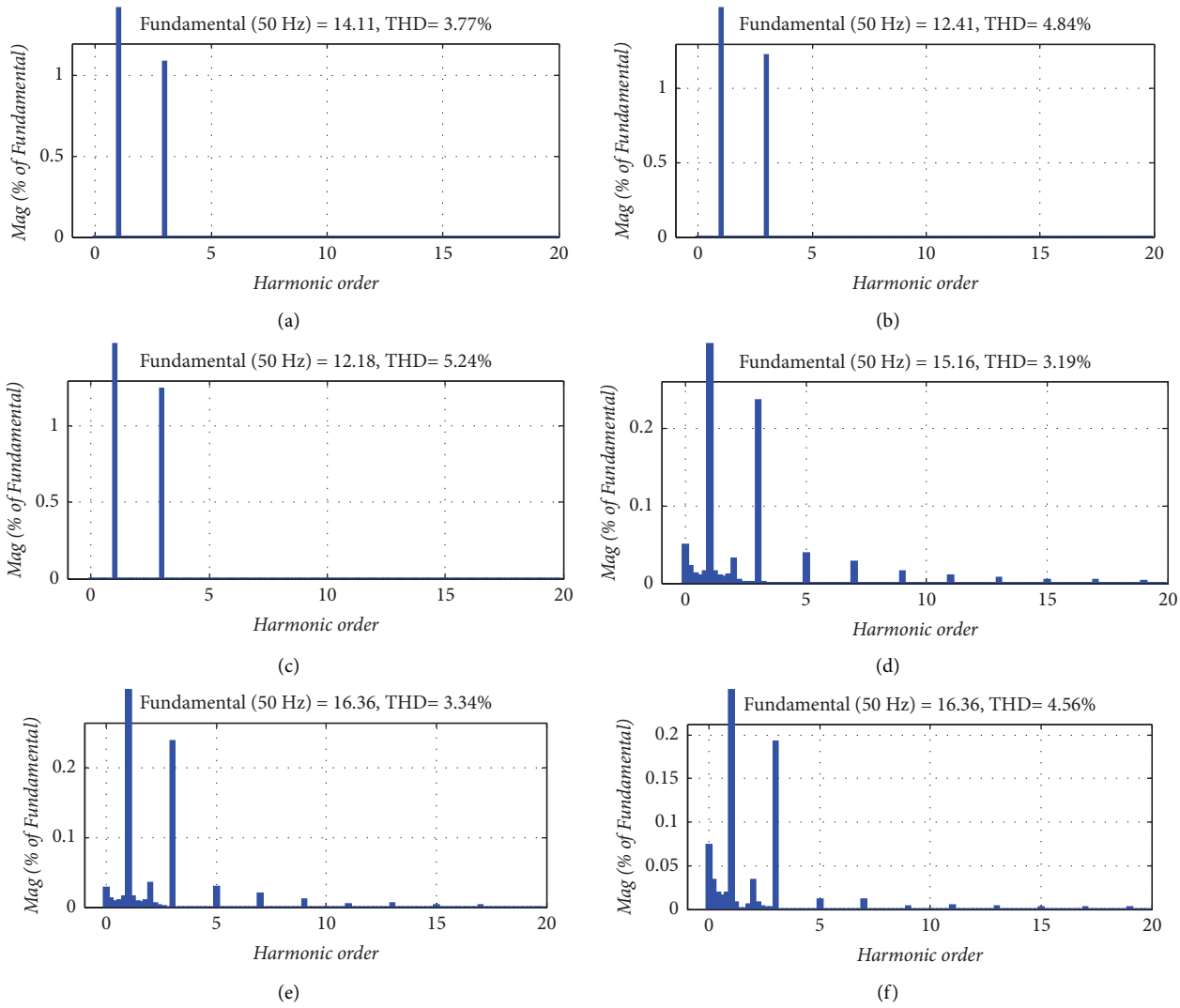

Figure 15: Harmonic distortion of three-phase input current under unbalanced condition; (a–c): current for phase a, b, and c with the proposed controller; (d–f): current for a, b, and c with the conventional controller.

Table 3: Main components and DC value in the positive and negative sequence of currents and voltages and their THD value for the proposed controller.

Amounts	Variable	Amounts	Variable	Variable	Variable
3.19%	THD_{i_a}	15.7∡0 (A)	i_a	13.49 (A)	i_d^+
3.34%	THD_{i_b}	16.9∡250.9 (A)	i_b	0	i_q^+
4.56%	THD_{i_c}	17.1∡120 (A)	i_c	1.35 (A)	i_d^-
600 (V)	E_2	600 (V)	E_1	−2.34 (A)	i_q^-

According to Table 2, for a 4 kW three-phase rectifier with a 6 kW load at DC 1200 V voltage level, the values of positive and negative sequence components for dq current components are shown in Table 3.

5. Conclusion

In this paper, the performance of a FSTPR in unbalanced conditions was investigated. The results show that due to the negative components in the dq axis of the converter input voltage, the real and unreal power received by the rectifier have oscillating parts, which causes distortion of the rectifier output voltage and uneven distribution of capacitor voltage, which cannot be ignored in unbalanced conditions. Finally, selecting the appropriate method, the positive and negative components are separated, and the reference control signal is designed and extracted. From the analysis of the results of the conventional and proposed controller simulations in balanced and unbalanced conditions, the following conclusions can be drawn:

(i) The conventional controller in balanced conditions has balance capacitor voltages and low output voltage ripple, but both are not acceptable in

unbalanced conditions. However, the proposed controller in unbalanced conditions can eliminate the oscillating active and reactive power components, suppress imbalance capacitor voltages, and lower the distortion of rectifier output voltage.

(ii) The larger the capacitor voltage value in the proposed controller, the lower the probability of saturation in SSVM.

(iii) The THD output current with the proposed controller is reduced by about 1% in each phase compared to the case where the conventional controller is used.

(iv) Using the proposed controller in a FSTPR under unbalanced conditions balances the converter's input current compared to the CCFSTPR. This can be attributed to the application of the capacitor voltage balancing signal with the proposed controller, which in the case of unbalanced voltage, the signal is applied only to the positive components of the *dq* axis. The second reason that can be mentioned is the elimination of oscillating components in the real and unreal power to determine the reference values of currents.

Finally, it should be noted that the proposed controller will need a microcontroller at a higher cost due to the adoption of a direct method using mathematical equations to derive current reference values from positive and negative components, which can be more complicated. For future work, the implementation of the converter with the proposed controller can be considered.

Data Availability

The entire data used to support the findings of this study are included within the article.

Additional Points

It is possible to access the whole of simulation's codes if needed.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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