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Research Article

A Three-Phase Reduced Switch Count Multilevel Inverter Topology

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Multilevel inverters play a vital role in the industrial and renewable energy sectors due to their flexibility in synthesizing sinusoidal waveforms using a low-pass filter with a medium voltage range. It has several drawbacks, such as a higher number of power component requirements and voltage balancing problems. In this study, a new structure for multilevel inverters has been developed to offer good power quality with minimum number of switching devices and gate driver circuits. The proposed structure is configured to operate in symmetrical and asymmetrical configurations for single/three-phase versions. A simulation study using MATLAB/Simulink has been utilized to study the operating characteristics under both configurations. A laboratory prototype has been built to check the feasibility of the proposed structure for real-time applications.

1. Introduction

In recent years, multilevel inverters (MLI) have been used in industrial, utility, and renewable energy applications due to their lower voltage stress, bringing the output voltage nearer to sinusoid and resulting in lower harmonic distortion [1, 2]. Multilevel inverters have three basic structures such as neutral point clamped, flying capacitor, and cascaded type [1, 3–5]. Several efforts have been put forth to accomplish stepped voltage waveform through reduced component count topologies [1, 3–13]. In the abovementioned topologies, cascaded-type topologies have been considered as they are free from capacitor balancing issues and do not use flying capacitors or clamping diodes. An MLI topology has been developed with a perspective to increase the voltage levels with the combination of three-leg inverter and H-bridge inverter sharing a common dc-link, but it requires a high-capacity isolation transformer to isolate the three-phase voltages [14]. A three-phase topology using several half-bridge cells is developed to synthesize stepped voltage waveform. The topology is designed only for 19-level devices and requires switching devices with different blocking voltages [15]. A cascaded connection of two three-leg inverters and multiphase inverters sharing a common dc-link through a three-phase high frequency transformer is formulated to draw sinusoidal output voltage. The topology requires a large number of transformers to couple the generated voltage for active power filter applications [16]. A generalized three phase structure using a diode-clamped H-bridge inverter is presented to appeal to three-phase output voltage. The topology suffers from unbalanced capacitor voltages [17, 18]. Two hybrid asymmetric cascaded multilevel inverters for driving medium-voltage open-end winding motors have been developed using three and nine levels H-bridge cells connected in series. The topologies of the nine-level H-bridge cells are constituted using a modular multilevel cascade converter with double-star chopper cells (DSCC), and the three level H-bridge cells are fed by a floating capacitor. However, the topology is having unbalancing voltage issues [19–21]. A hybrid topology using half-bridge cells is devised for battery management systems. The functionality of the topology for battery management applications is well

demonstrated [22]. A photovoltaic inverter architecture comprises stackable dc to three-phase ac converter blocks with a converter power stage and controls which are connected in series on their AC sides to obtain transformerless medium-voltage AC interfaces for PV power plants [23]. A three-phase topology using half-bridge structures and a common dc-link is developed to offer good quality output voltage. However, the topology requires more number of switching devices [24]. A three-phase MLI topology is constituted using two half-bridge cells connected across split-capacitors and an H-bridge inverter. Both basic units are equally shared by the three phases maintaining symmetry among the phases. The topology requires tedious control circuits and inability in fault operation due to outage of switching devices [25]. An asymmetrical three phase topology is formulated using a level doubling network (LDN) that comprises of asymmetric voltage sources with half-bridge cells for doubling the number of levels in the output voltage. The topology requires separate circuitry for charging the floating capacitors [26]. A three-phase topology using solid state transformer is developed to generate three-phase output voltages. The topology requires independent control strategies to regulate the dc-link voltages and balance the three-phase grid currents [27]. A three-phase modular multilevel inverter consists of repeated modular primary cells that are connected in series configuration to generate stepped output voltage. The topology looks simple in structure [28]. An asymmetric MLI topology having a ratio of $1:4^n$ is presented to improve the number of levels in the output voltage, where "n" is the number of H-bridges. However, the topology uses conventional three level (H-bridge) inverters as basic power module and claims only the number of level increase with high device voltage blocking capability [29]. A two stage MLI with AC-DC-AC conversion topology is devised to provide good quality output voltage. The topology involves capacitors and clamping diodes for their operation, and unbalanced output voltage may occur [30]. A multistage MLI topology using one two-level inverter and the remaining modules as H-bridge inverters is devised to synthesize stepped voltage waveforms. The two-level inverter has to withstand a high blocking voltage [31]. A hybrid structure using flying capacitors and diode clamped inverters has been formulated to generate multilevel waveforms. The topology is a hybrid form of basic topologies and requires capacitor balancing circuits [32]. An inverter to drive an open-winding induction motor has been designed using two level inverters with a capacitor-fed H-bridge cell. The topology is specifically designed for open-end winding induction motors [33]. A dual dc source with four switch modules shown in Figure 1 is developed for three phase applications, which is an optimized recent modular topology with the advantage of reduced component count [34]. A three-phase grid tie inverter using three-leg inverter is developed with built in function of boost mode. The topology requires complex control for current injection into the grid [35]. A five-level inverter scheme using cascading of traditional two-level and three-level neutral point clamped inverters for an induction motor drive is developed to eliminate common-mode voltage [36].

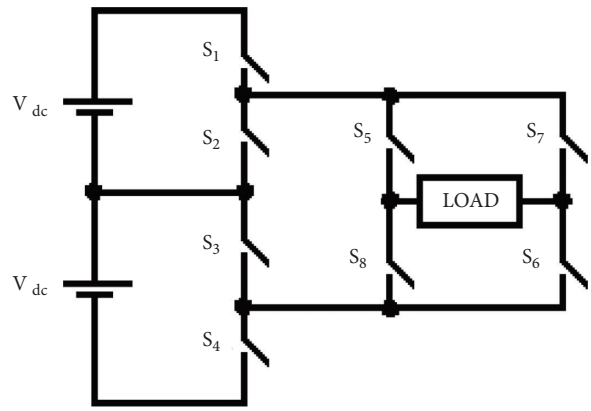


Figure 1: MLI topology presented in [34].

From the aforesaid detailed review of recent literature, the topologies presented above have different perspectives in terms of structure, modularity, and total power components. However, the traditional topologies require a large number of power components for three phase topology configurations. This paves a way to devise a new modular topology with reduced power components and dc sources compared with traditional topologies. This study proposes a new reduced switch count three-phase MLI topology for medium voltage applications. The detailed operating modes and comparison with recent topologies have been forayed to fore fit its advantages in real-time applications. A laboratory prototype has been developed to test the viability of the proposed topology.

2. Proposed Topology

A significant research study has been conducted in developing topological structures in multilevel inverter topologies due to their inherent characteristics of synthesizing stepped voltage waveforms to offer better quality output voltage waveform. In this perspective, an attempt has been made to carve out fresh three-phase MLI from single-phase topology for the same number of dc sources. A generalized structure for three-phase topology is pictured in Figure 2 comprising of series connection of five-level (0, V_{dc}, $2V_{dc}$, $3V_{dc}$, and $4V_{dc}$) voltage generation modules associated with switching devices and coupling transformer having a ratio of 1:1. To understand the operating characteristics, a generalized single-phase topology is portrayed in Figure 3 to solicitude stepped voltage waveform. In Figure 4, the switches (S_{r31}, S_{r41}) and (S_{r11}, S_{r41}) are conducted to pump the voltage from the voltage sources (V_{11}) and (V_{21}) to generate (V_{dc} and $2V_{dc}$) levels in the output voltage. Similarly, in Figure 5, the switches (S_{r11}, S'_{r21}) and (S_{r11}, S_{r21}) are switched to draw out the voltage from the voltage sources (V_{11}, V_{21}) and (V_{31}) to generate ($3V_{dc}$ and $4V_{dc}$) levels in the output voltage. The switches (S'_{r11}, S_{r41}) are required to be turned ON to generate zero voltage in the output voltage as portrayed in Figure 6.

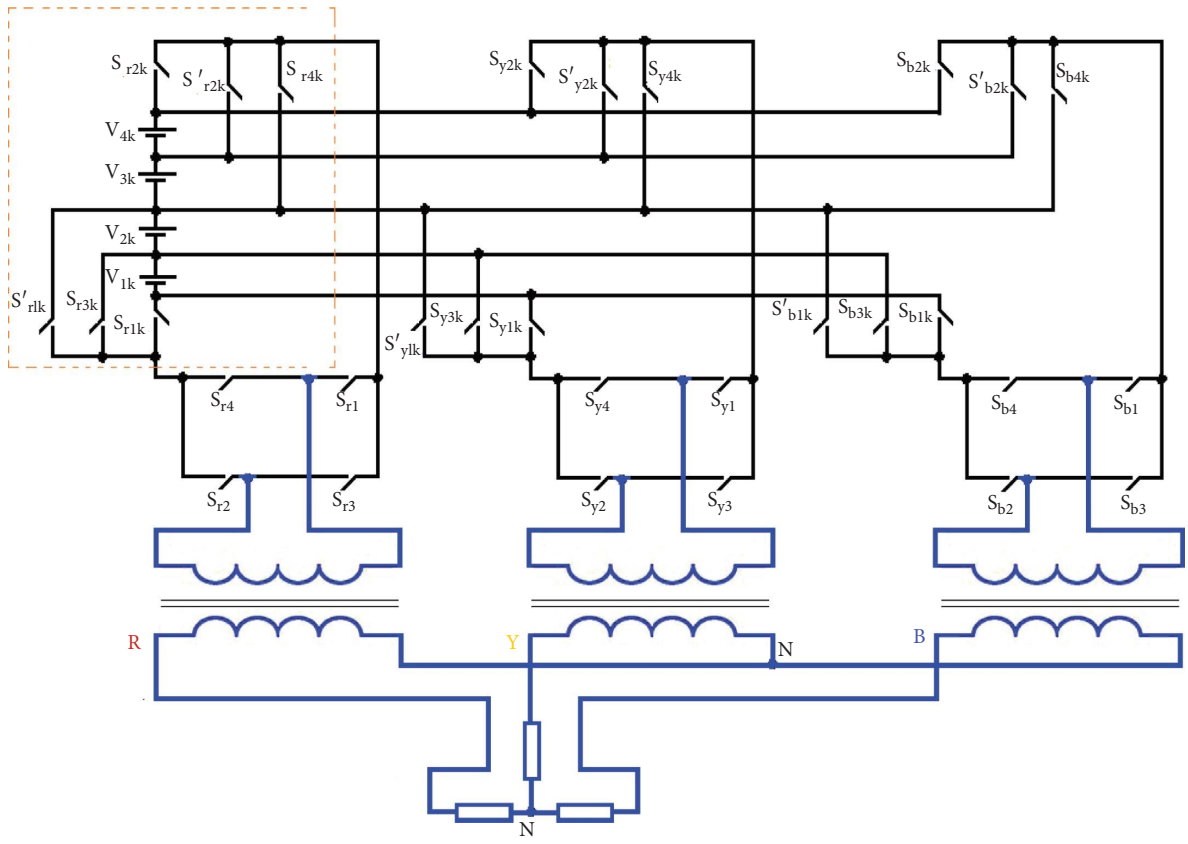


Figure 2: Proposed three-phase topology.

The topology presented by Ruiz-Caballero et al. [34] is composed of cascading connections of several full-bridge modules with two dc sources and four switches used to generate (0, V_{dc}, and $2V_{dc}$). Two modules are required to generate five levels (0, V_{dc}, $2V_{dc}$, $3V_{dc}$, and $4V_{dc}$) with four dc sources and eight switches. The proposed voltage generation module requires the same number of dc sources and switching devices with 6 gate driver circuits. The reduction in gate driver circuits in the MLI topology is a greater advantage while increasing the number of levels. In addition, the proposed topology exhibits an added advantage of reduced number of switching devices in the conduction path that offers reduced power loss. The proposed topology needs only 2 switching devices, while the topology presented by Ruiz-Caballero et al. [34] requires 4 switching devices to produce 5 level in the inverter output voltage. This advantage is more apparent while increase in number of voltage generation modules. Table 1 provides the comparison between proposed topology, cascaded H-bridge multilevel inverter (CHBMLI), and topology presented by Ruiz-Caballero et al. [34]. For instance, to produce 9 level, the topology presented by Ruiz-Caballero et al. [34], CHBMLI, and proposed topology requires "k" as a value of 2, 4, and 1. The switching device variation between conventional topologies and proposed MLI topology is 12, 16 and 12, while the gate driver requirements are 12, 16, and 10, respectively. These mathematical relations show the ease of power component requirements for the proposed topology for "m" voltage levels. Table 2 tabulates comparison between the proposed three-phase topology and conventional topologies. It is observed that the proposed topology requires one-third of dc sources as compared to conventional topologies.

2.1. Selection of Magnitude of Voltage Sources. It is worthwhile noted that the proposed topology has the merit of operating with different voltage magnitudes resulting in increased number of voltage levels. An optimized method is presented in this section to determine the values of voltage sources:

$$V1(n) = V2(n) = V3(n) = V4(n) = (2n - 1 \times V\mathrm{dc}). \quad (1)$$

Then, the number of voltage levels and switches is given by

$$m = 8 \times \left[\sum_{k=1}^{n} 2^{n-1}\right] + 1,$$
$$N_{sw} = \left[\sum_{k=1}^{n} (4 \times k)\right] + 4. \quad (2)$$

2.2. Comparison Study. It is worthwhile to demonstrate the merits of the proposed single- and three-phase topologies by comparing the recent topologies in terms of power component requirements. In this study, a comparison has been

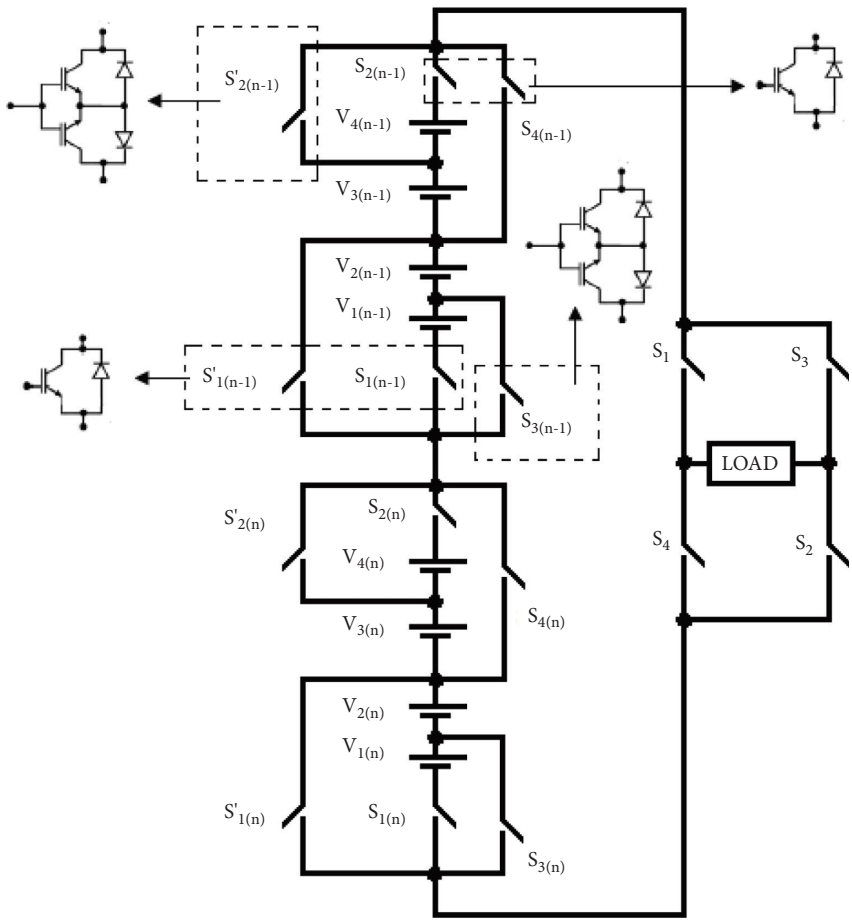


Figure 3: Proposed single-phase topology.

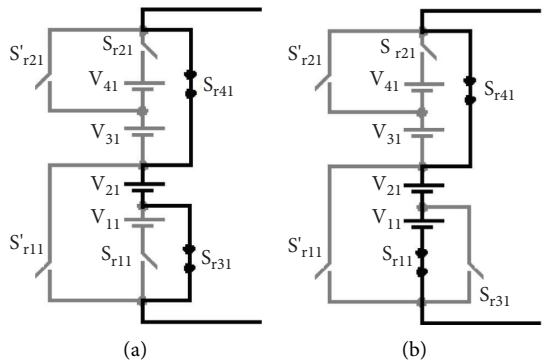


Figure 4: Operating mode: (a) V_{21} and (b) $V_{11} + V_{21}$.

made for single-phase topologies, since the proposed topology requires one-third of dc sources as that for conventional topologies. Figures 7–9 represent the comparison chart between recent and proposed topologies in terms of switching devices, gate driver units, and conducting devices in the current path against topologies for 33-level inverter. In Figure 7, the proposed topology requires only two switching devices higher than the topology presented in [37], and it exhibits lower number of switches compared to the topologies in [38–40]. However, the proposed topology requires only 28 gate driver circuits, while the topology in [37] needs 34 gate driver circuits which is represented in Figure 8. The proposed topology offers lesser switching devices in current conduction path compared with recent topologies as evident in Figure 9.

Figures 10–12 carves out the detailed chart for variation of switching devices, gate drivers, and current conducting devices compared to various voltage levels.

The other important parameter used to understand the performance of the developed topology is the power loss. The proposed topology offers lesser power loss and hence attains better performance indices. The power loss is

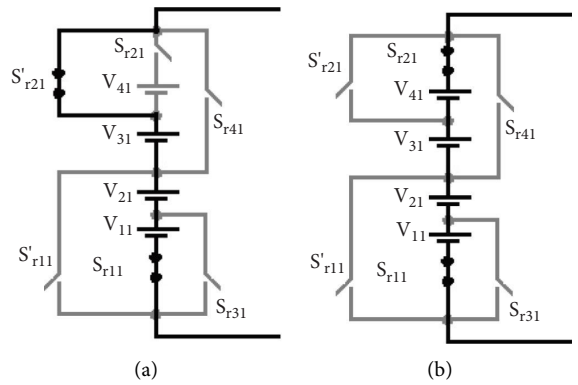


Figure 5: Operating mode: (a) $V_{11} + V_{21} + V_{31}$ and (b) $V_{11} + V_{21} + V_{31} + V_{41}$.

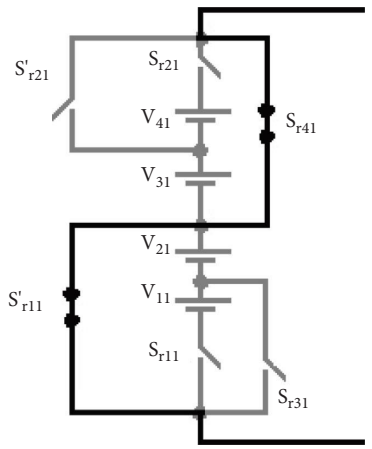


Figure 6: Operating mode for zero level.

basically comprised of switching and conduction loss. The methodology pertaining to compute switching and conduction losses is obtained from the device characteristic curves. The experimental prototype avails IGBTs (IRG4BC20SD, International rectifier manufacturer) as switching device, which has a maximum forward current of 10 A and a blocking voltage of 600 V. The characteristics curves are plotted between ON-state saturation voltage (V_{ce} (θ) for the IGBT and V_F (θ) for the diode) and load current I_L (θ). E (θ) denotes the energy loss during a single commutation (E_{ON} (θ) and E_{OFF} (θ) are turn-ON and turn-OFF commutations, and E_{rec} (θ) owes for the diode reverse recovery process, where "θ" is the load current phase angle). The curves are approximated using nonlinear least square curve-fitting tool by an exponential equation (1) to (6).

The mathematical models obtained for the IGBTs are given by

$$V_{ce} = 0.96e^{0.0016I}L^{(\theta)} - 0.4654e^{-0.044I}L^{(\theta)}, \quad (3)$$

$$V_F = 0.6e^{0.002I}L^{(\theta)} - 0.4258e^{-0.0275I}L^{(\theta)}, \quad (4)$$

$$E_{rec} = 0.00806e^{-0.000322I}L^{(\theta)} - 0.0057e^{-0.00446I}L^{(\theta)}, \quad (5)$$

$$E_{ON} = 0.0041e^{0.0044I}L^{(\theta)} - 0.0037e^{-0.008I}L^{(\theta)}, \quad (6)$$

$$E_{OFF} = 0.0443e^{0.00021I}L^{(\theta)} - 0.0547e^{-0.00107I}L^{(\theta)}, \quad (7)$$

$$I_{L(\theta)} = I_{max}\sin(\theta - \varphi), \quad (8)$$

where I_L (θ) is the load current and φ is the load-displacement angle.

The switching loss happens during turn-ON and turn-OFF, and for every power device (P_{sw}), it is obtained by identifying the corresponding turn-ON and turn-OFF instants during one reference period as follows:

$$P_{sw} = \frac{1}{T}\sum(E_{ON} + E_{OFF} + E_{rec}). \quad (9)$$

The conduction loss is calculated when the device is in current conduction path, and it is a product of ON-state voltage and current.

The calculation of conduction losses for each semiconductor device is given by

$$P_{con,T} = \frac{1}{2\pi}\int_0^{2\pi} V_{ce}(\theta)I_L(\theta)d\theta,$$
$$P_{con,D} = \frac{1}{2\pi}\int_0^{2\pi} V_f(\theta)I_L(\theta)d\theta. \quad (10)$$

Figure 13 illustrates the plot in terms of normalized power loss between the proposed and traditional topologies by Su [9] and Cascaded H-Bridge MLI. It is observed from Figure 13 that the developed MLI attains lesser power loss than the topologies by Daher et al. [12] and CHB. For understanding the total devices in current conduction path to attain 9 level, the developed topology has 4 switching devices, while, the topologies by Su [9] and CHB have 6 and 8 switching devices. It is inferred from Figure 13, the developed topology claims minimum power loss in comparison with traditional topologies with increase in voltage levels.

3. Simulation Results

The simulated response of the proposed topology is studied in Matlab/Simulink platform with RL-load of 100 Ω and 100 mH and input dc voltage sources of 75 V each. The proposed topology is configured to operate in both single

Table 1: Comparison between proposed and conventional single-phase topologies for "k" cells.

Multilevel inverter structure	Topology presented in [34]	CHB topology	Proposed
No. of voltage levels	$(4\times k)+1$	$(2\times k)+1$	$(8\times k)+1$
Max. output voltage	$(2\times k)\times V_{dc}$	$(k)\times V_{dc}$	$(4\times k)\times V_{dc}$
Main switches	$(4\times k)+4$	$(4\times k)$	$(8\times k)+4$
Gate drivers	$(4\times k)+4$	$(4\times k)$	$(6\times k)+4$
Max. device count in conduction path	$(2\times k)$	$(2\times k)$	$(2\times k)+2$
SDCs	$(2\times k)$	(k)	$(4\times k)$
Total standing voltage on switches Voltage-level generation part	$(4\times k)\times V_{dc}$	$(4\times k)\times V_{dc}$	$(10\times k)\times V_{dc}$
Polarity reversal part	$(8\times k)\times V_{dc}$		$(16\times k)\times V_{dc}$

Table 2: Comparison between proposed and conventional three-phase topologies for "k" cells.

Multilevel inverter structure	Topology presented in [34]	CHB topology	Proposed
No. of voltage levels	$(4\times k)+1$	$(2\times k)+1$	$(8\times k)+1$
Main switches	$3\times((4\times k)+4)$	$3\times((4\times k))$	$3\times((8\times k)+4)$
Gate drivers	$3\times((4\times k)+4)$	$3\times((4\times k))$	$3\times((6\times k)+4)$
SDCs	$3\times(2\times k)$	$3\times(k)$	$(4\times k)$

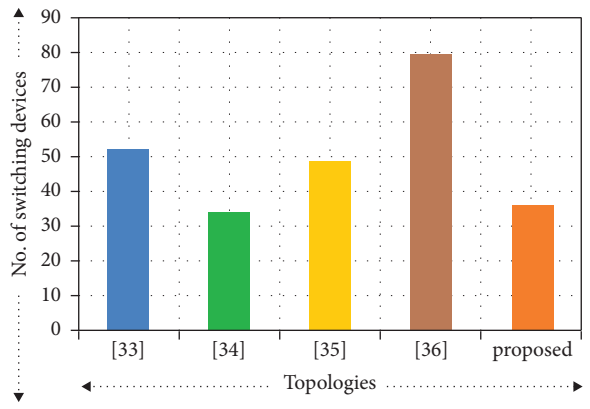


Figure 7: Comparison of number of switching devices required in recent topologies vs. proposed topology.

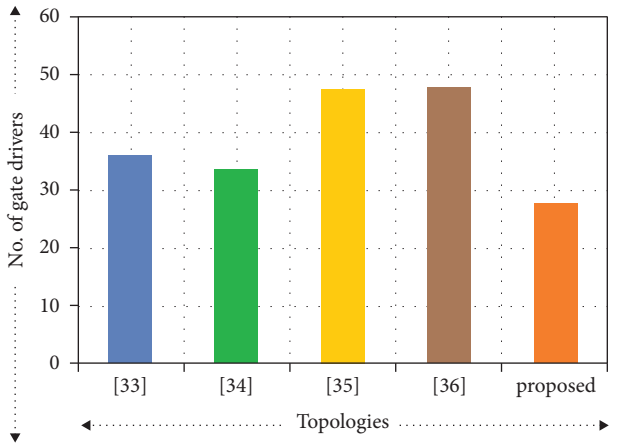


Figure 8: Comparison of number of gate drivers required in recent topologies vs. proposed topology.

and three-phase 9-level inverters. The switching scheme MCPWM with carrier frequency of 2 kHz is used to generate PWM pulses to acquire 9-level output voltage in proposed

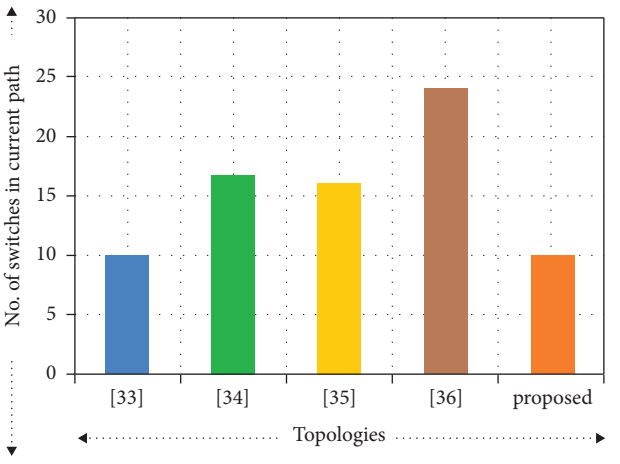


Figure 9: Comparison of number of current conducting devices required in recent topologies vs. proposed topology.

topology. The PWM generation scheme for simulation study is portrayed in Figures 14 and 15, respectively. The PWM generation scheme is explained for single 9-level inverter. It consists of 4-triangle carrier and single modulating waveform to buffer positive and negative cycle pulses. The sine and each triangle carrier are compared and suitably logically XOR to acquire base PWM pulses. The base PWM pulses are given to the switches of the proposed topology to synthesize each level of output voltage.

Figures 16 and 17 represent the output voltage and inductive current waveform for single-phase 9-level inverter. Similarly, Figure 18 represents phase voltages for three-phase 9-level inverter. Figure 19 depicts inductive load current for 9-level inverter.

4. Experimental Results

The performance of the proposed topology is validated using the experimental results by constructing a laboratory

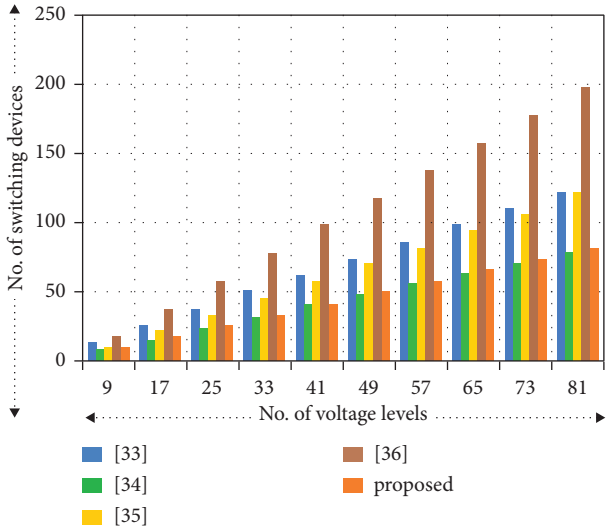


FIGURE 10: Comparison of number of switching device required for various voltage levels in recent topologies vs. proposed topology.

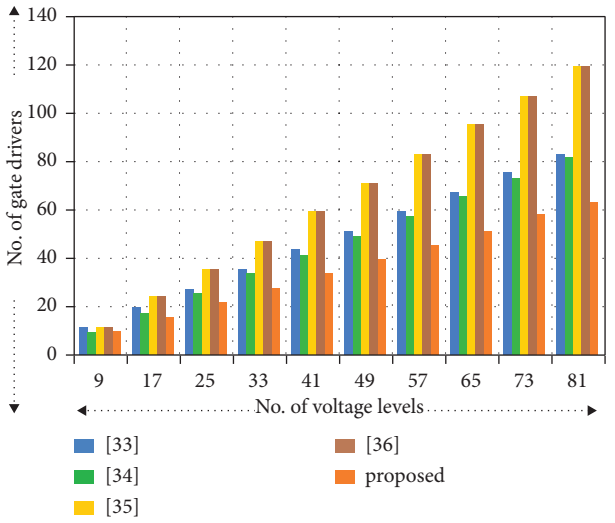


FIGURE 11: Comparison of number of gate drivers required for various voltage levels in recent topologies vs. proposed topology.

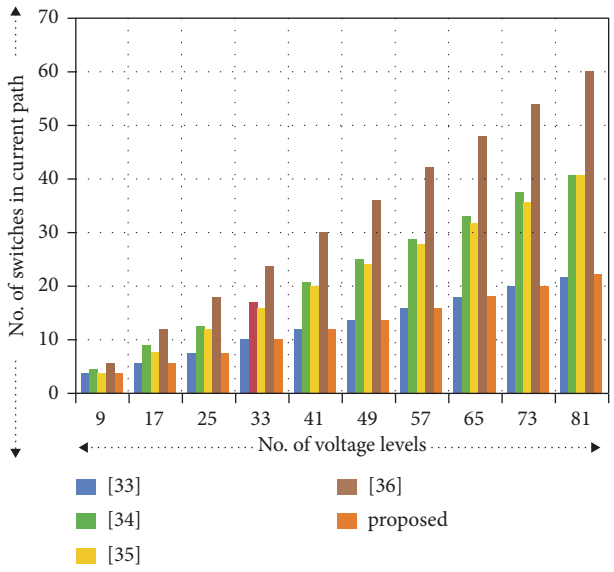


FIGURE 12: Comparison of number of current conducting devices required for various voltage levels in recent topologies vs. proposed topology.

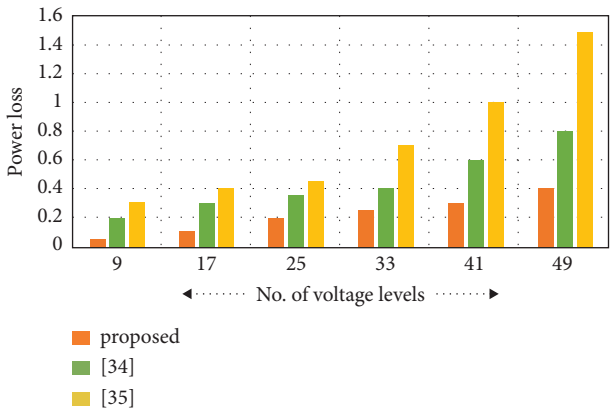


FIGURE 13: Comparison of device power loss for various voltage levels in recent topologies vs. proposed topology.

prototype with a dc-link voltage of 70 V to acquire a three phase voltage of 280 V (Per phase) to feed a RL load of 150 Ω and 106 mH, respectively. The experimental prototype shown in Figure 20 avails insulated gate bipolar transistor (FSBB20CH60 IGBT) as switching device to constitute the power module with assorted gate drive units of 6N137 opto-isolator. The structure utilizes multicarrier PWM strategy to synthesize three-phase PWM modulated voltage waveform with carrier frequency of 2 kHz and modulation index of 1. The proposed topology uses Xilinx Spartan 3E-500 FG320 controller for generating PWM pulses to synthesize PWM modulated output voltage waveform. The FPGA controller has inbuilt 50 MHz clock, 16MByte flash, and 16 Byte SDRAM memories to re-configure for any applications. The flowchart for PWM generation is represented in Figure 21. The flowchart has been given for base PWM generation for 9-level output voltage per phase. The flowchart has three folds: the first one is reference wave generation, the second is carrier wave generation, and the last is base PWM generation. Firstly, the amplitude of sine wave is calculated at an interval of 400 samples and formed as look up-table. The count for fetching the sine data from memory address is calculated in terms of FPGA clock frequency. For sine wave

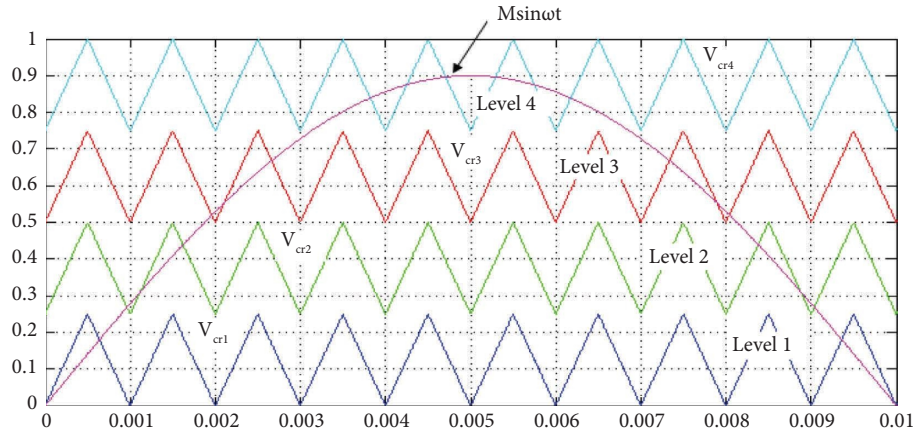


Figure 14: Pulse width modulation phase disposition technique (PD-PWM).

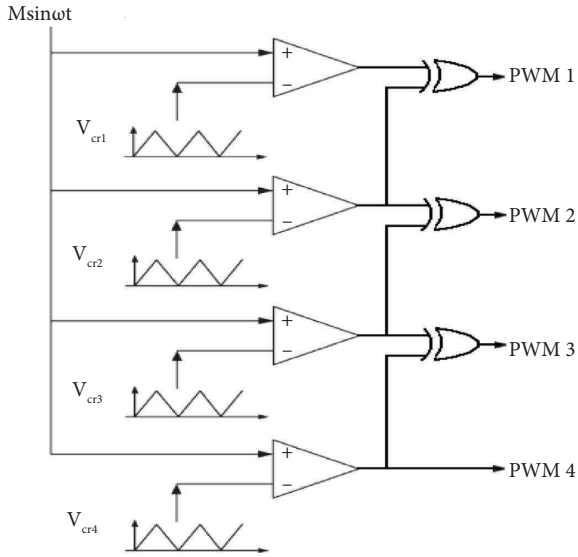


Figure 15: Simplified modulation scheme for single-phase 9-level inverter.

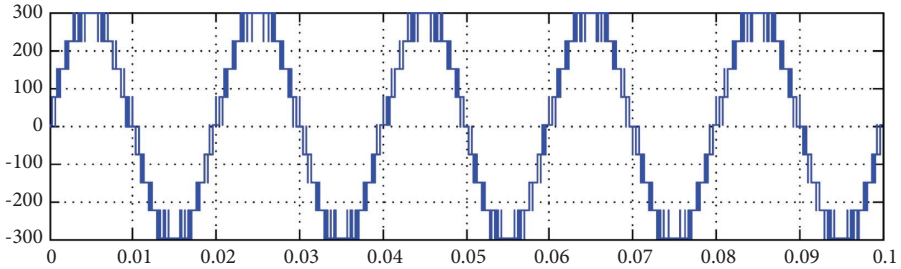


Figure 16: Output voltage for 9-level inverter.

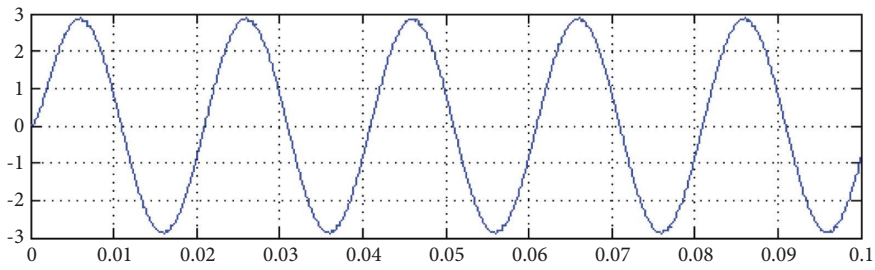


Figure 17: Inductive load current for 9-level inverter.

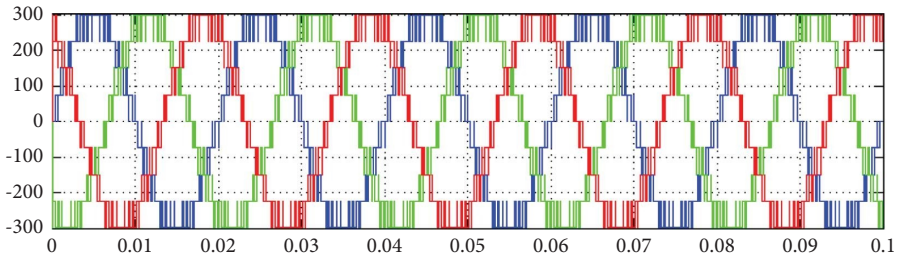


Figure 18: Phase voltages for three-phase 9-level inverter.

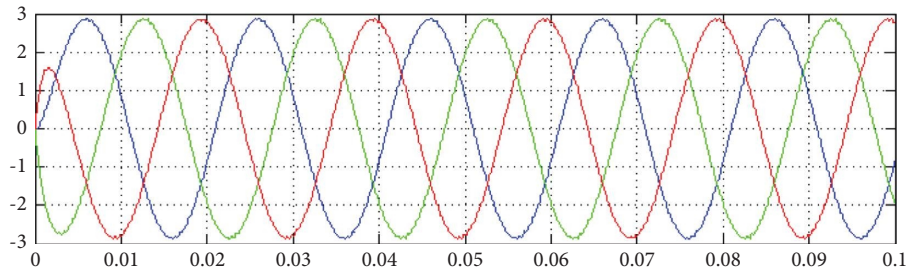


Figure 19: Inductive load current for three-phase 9-level inverter.

Figure 20: Experimental prototype.

frequency of 50 Hz and 400 samples with FPGA clock frequency of 50 MHz, the count for the fetching the data is 2500. The clock is initialized; the count has been updated at every leading edge of clock and fetches the sine data from the memory address. Similarly, for triangle wave generation, the count for carrier frequency in terms of FPGA clock is computed and then divides the clock for rising/falling slope to acquire triangle waveform. For example, the carrier frequency is 1 kHz; the total count for wave generation is 50000. At every clock cycle, the sine and carrier data are compared to get base PWM for each level. The FPGA controller has high storage capacity to store the samples data which generates accurate PWM pulses as that of simulation. The algorithm is written using VHDL language

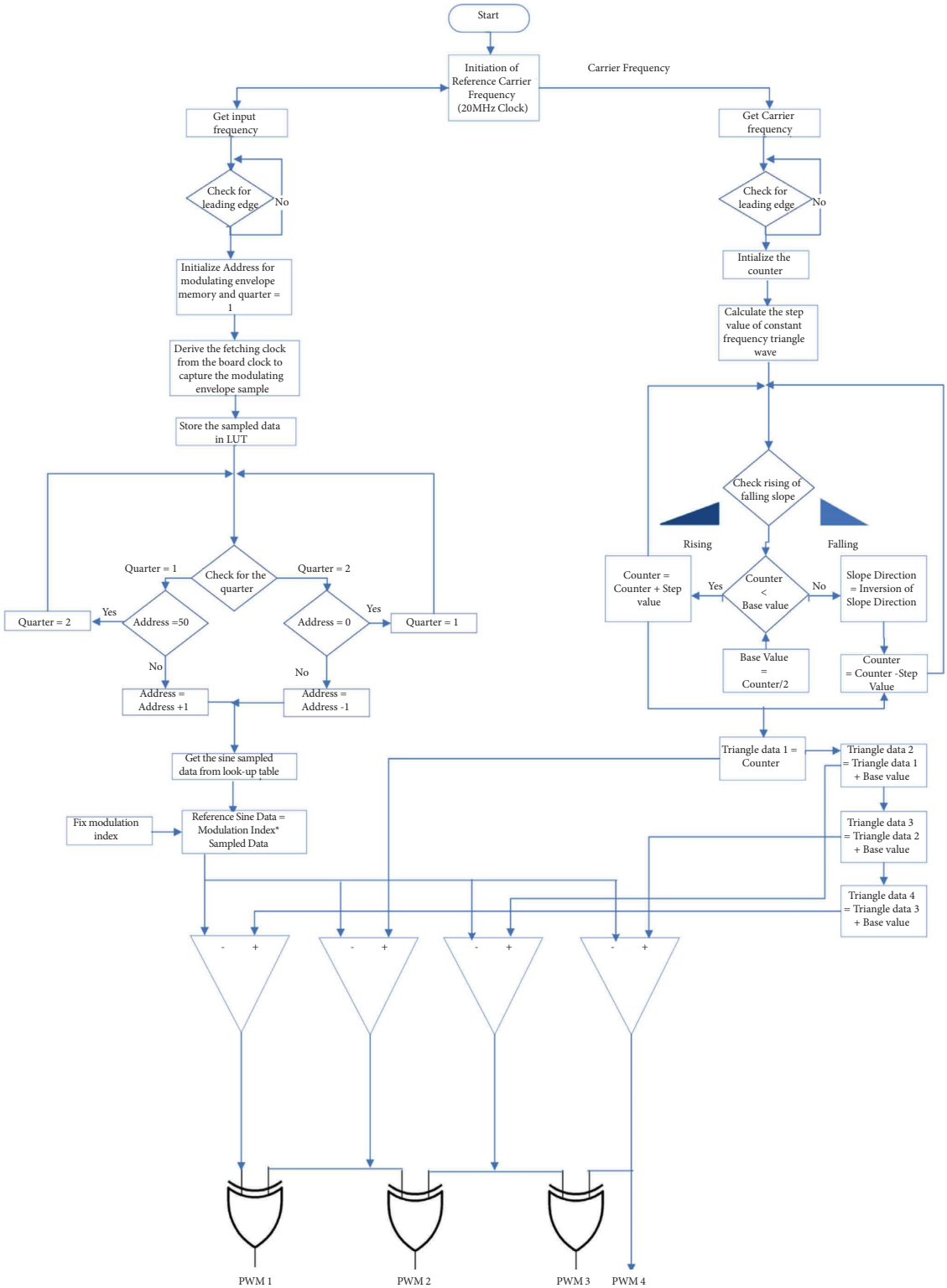
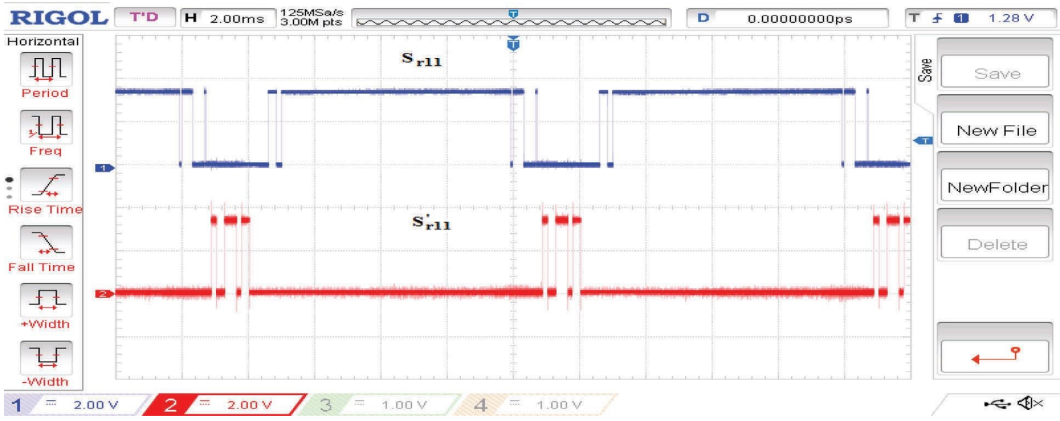
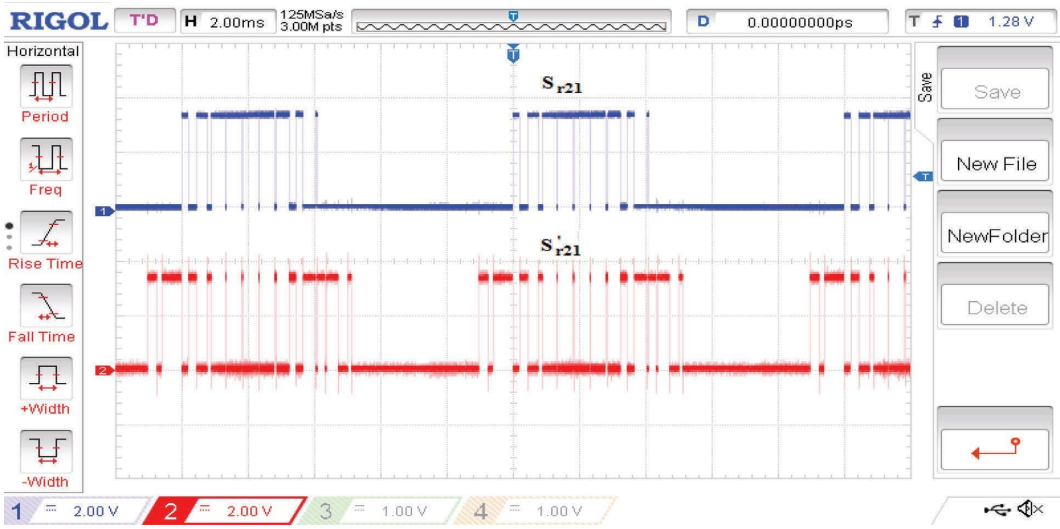


Figure 21: Flowchart for FPGA implementation.

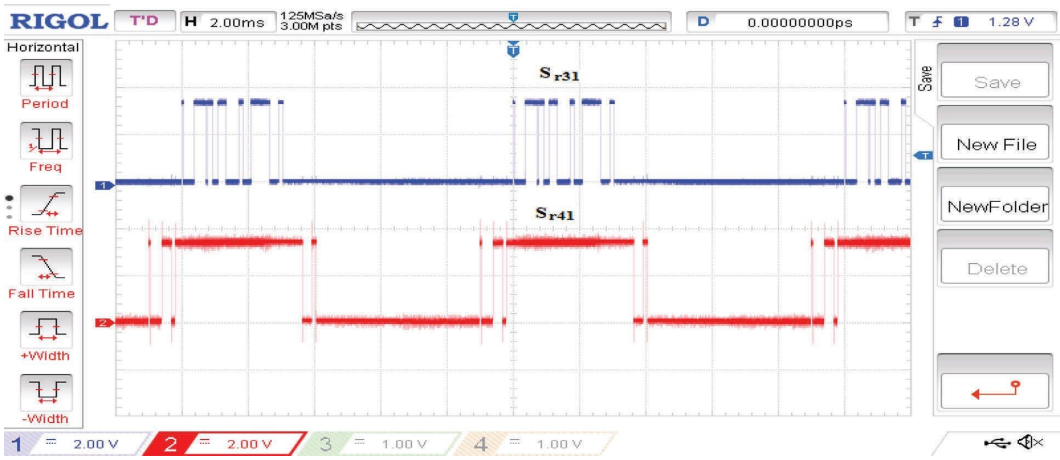
and the same is verified using ModelSim software. The specimen excels that FPGA controller exactly replicates the simulated pulses in real time and proved its capabilities for power converter applications. The PWM generation for phase voltage is included in Figures 22(a)–22(d), while the phase shifting between the phases is represented in Figures 22(e) and 22(f). The output voltage, inductive load current, and dynamic variations of M_a at constant load conditions



(a)

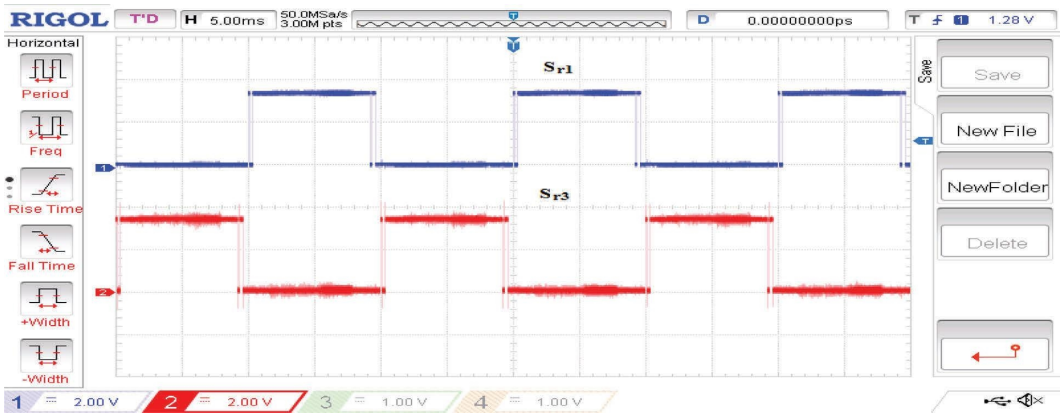


(b)

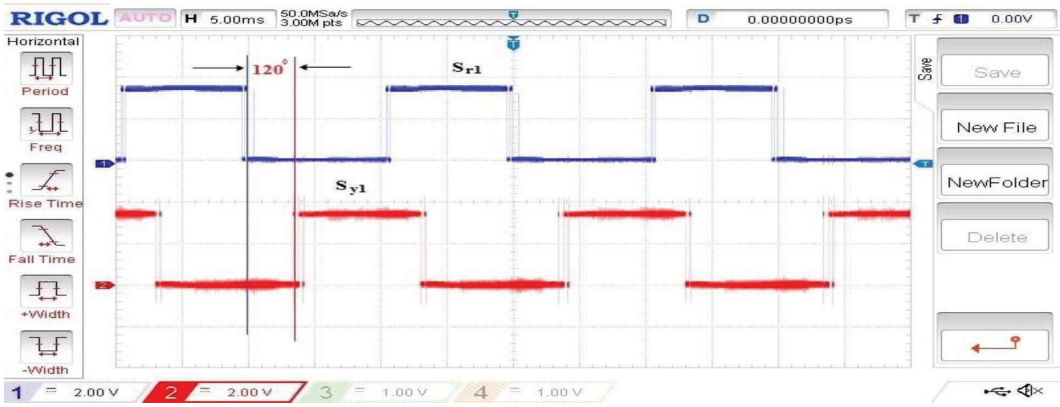


(c)

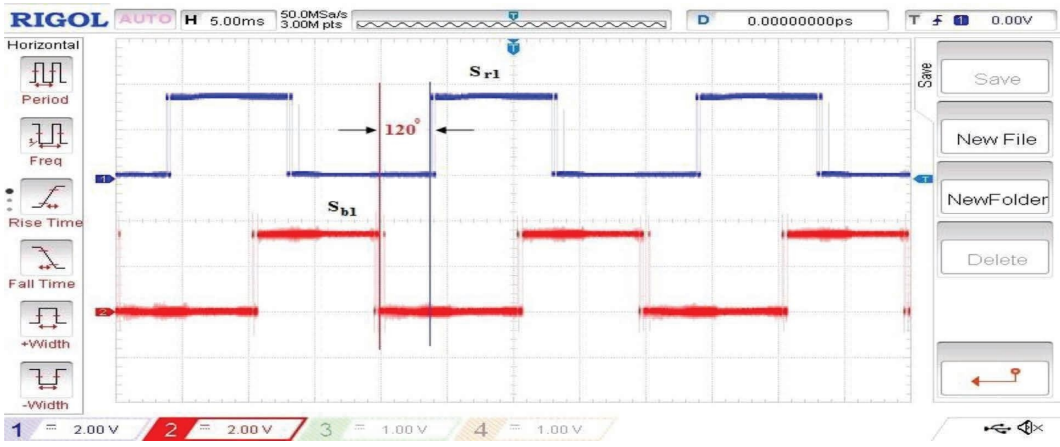
Figure 22: Continued.



(d)



(e)



(f)

FIGURE 22: Experimental gating pulses for proposed three-phase topology. (a)–(d) Pulses for phase-R; (e) H-bridge pulses for phase-Y; (f) H-bridge pulses for phase-B.

are shown in Figures 23 and 24, respectively, where "M_a" is the amplitude modulation index. The phase voltage, line voltage, and line current waveform are shown in Figures 25–27, respectively. The experimental results recognize that the proposed topology is well suited for real-time applications.

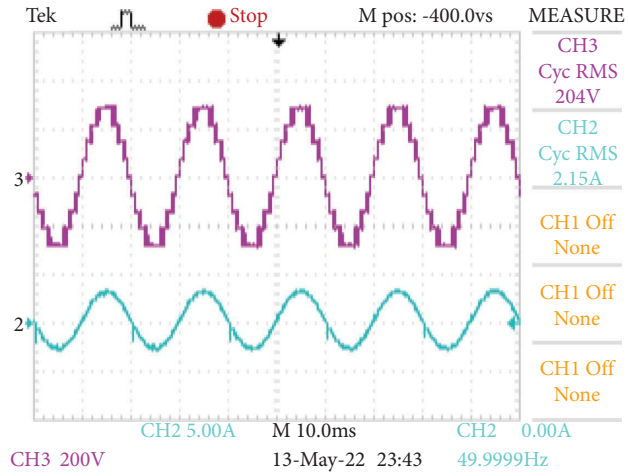


Figure 23: Output voltage and inductive load current for 9-level inverter.

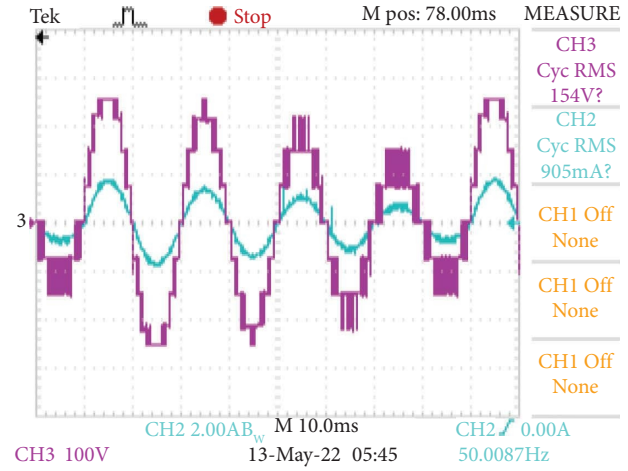


Figure 24: Dynamic variation of M_a under constant load condition.

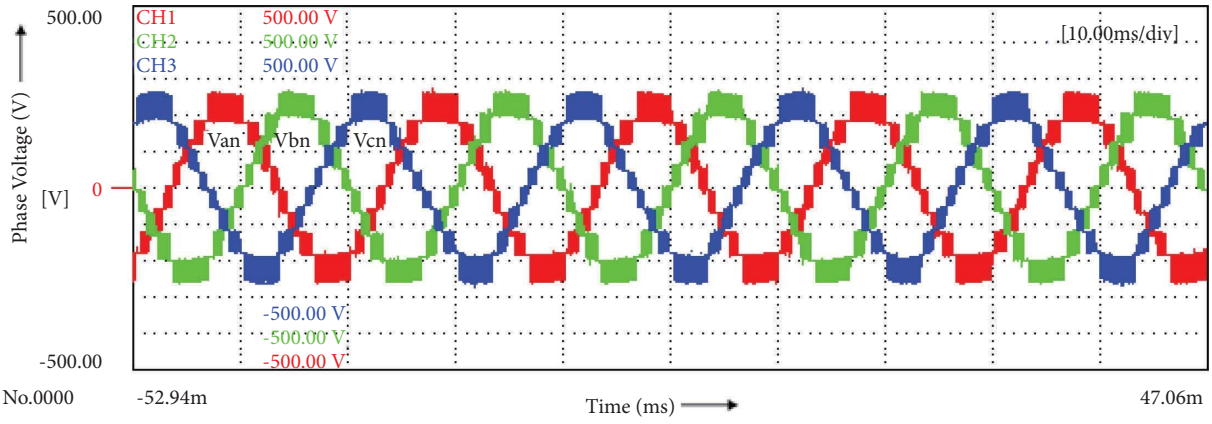


Figure 25: Phase voltage waveform.

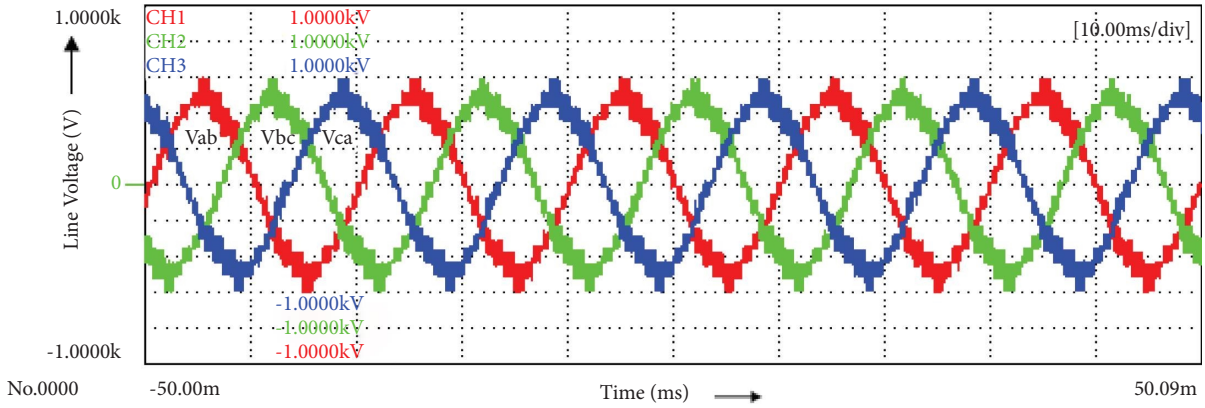


Figure 26: Line voltage waveform.

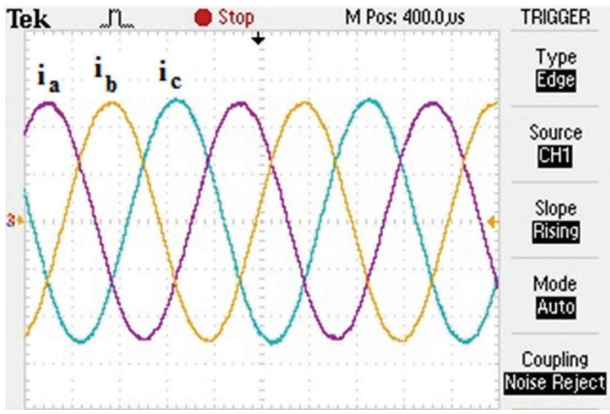


Figure 27: Line current waveform.

5. Conclusion

A new MLI topology has been developed for high power medium voltage applications with a view to reduce total power components for higher voltage levels. The new MLI structure constituted using four dc sources as single power module which has been developed to operate with reduced switch count in the path of current. The proposed topology requires one-third of input dc sources in total source count as needed for recent cascaded topologies. The switching devices associated with gate driver units are greatly reduced in par with recent topologies. The concept of generating pulses has been divined using the FPGA controller that makes a flexible path for generating PWM pulses for three-phase cascaded MLIs. The simulation response observed from MATLAB/Simulink platform toils future scope in developing new topologies for high power applications. The experimental results from laboratory prototype reveal easier implementation for higher voltage levels. The proposed topology is well suited for renewable and variable speed drive applications due to one-third of input dc source requirements with reduced power components.

Abbreviations

MLI: Multilevel inverters
DSCC: Double-star chopper cells
LDN: Level doubling network
CHBMLI: Cascaded H-bridge multilevel inverter
MCPWM: Multi carrier pulse width modulation
FPGA: Field programmable gate array
SDRAM: Synchronous dynamic random-access memories
LTUs: Look-up tables
VHDL: Very high-speed integrated circuit hardware description language.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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