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Research Article

Non-Isolated Power Factor Corrected AC/DC Converter with High Step-Down Voltage Ratio for Low-Power Applications

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This paper proposes a high step-down ratio AC-DC converter employing a quadratic buck converter with power factor correction. Conventional active power factor correction topologies employ boost-based correction schemes for unity power factor operation. This will require a steeper step-down ratio and higher switch voltage stress apart from complexity in the control scheme with sensors. The structure of the proposed topology is developed by combining the power factor correction stage with a high step-down stage. The passive input filter is split up into two for the purpose of reducing the thermal heating apart from offering a higher power factor. A single switch operation reduces the complexity of the control scheme. In addition, the number of conducting devices during the current path is also the same as the conventional buck converter due to cascading and hence offers lower conduction losses. The need for the converter to operate at an extremely low duty cycle is reduced due to the quadratic stage structure. The proposed converter operates at a moderate duty cycle, offering higher step-down voltage apart from reducing filtering requirements. MATLAB R2020b is used for carrying out simulation studies. Xilinx FPGA-based controller using system generator is implemented for the generation of pulses of appropriate duty cycle. Simulation and experimental results for a 150 W prototype are presented. An investigation and comparative evaluation of the conventional bridgeless buck system with the quadratic buck converter are carried out. The proposed structure offers the benefit of a higher step-down voltage ratio incorporating an inherent power factor correction stage along with the AC/DC stage.

1. Introduction

Fuel scarcity, rising oil prices, poor air quality, and an increase in demand for personal transportation have paved the way for battery electric vehicles (BEVs). To charge these batteries from the conventional grid supply, AC/DC chargers are required, which meet the IEC 61000-3-2 standards. Single-phase AC/DC converters were widely employed in applications such as uninterruptible power supplies and battery chargers. Conventional bridge rectifiers have over 55% total harmonic distortion (THD) and a poor power factor. These converters necessitate power factor correction (PFC) due to their poor power quality. The absence of PFC would result in poor efficiency, higher current pulses being drawn at the source side, higher peak ratings of the devices, and hence increased losses. To reduce the peak currents and improve the input side power factor, filters were employed. Inductive and capacitive filters conventionally used for this application are very bulky as these need to be designed for power frequency. Inductor opposes the instantaneous change in currents, and therefore inrush current during turn-on can be reduced. The capacitor and inductor behave as complementary potential and kinetic energy storage elements, respectively, such that the input sees an impedance that is close to a resistive load. Power factor topologies could be active or passive. Passive PFC incorporates LC filters at the source side. These filters provide reduced EMI but the size of converter increases due to the bigger size of inductorThe advantage of such schemes is simpler control and inexpensive construction. Active PFC requires complex

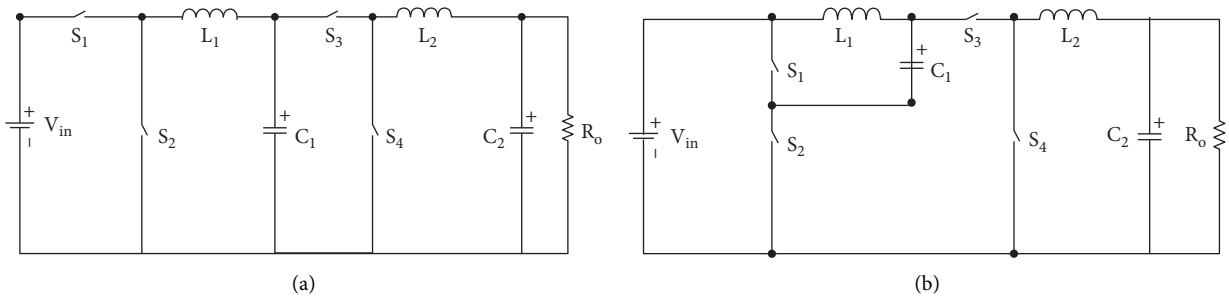

Figure 1: (a) Cascaded buck converter. (b) Realization of QBC [7].

control, hence more sensors resulting in increased cost but lower weight and size due to the absence of source filters. The simplest configuration of an AC/DC converter consists of a bridge rectifier with a chopper. These choppers could be either buck or boost types. Boost converters require larger electrolytic capacitors for filtering requirement. The output voltage of the buck-based scheme would be lower than the peak of the input voltage, which can lead to a reduction of costs in terms of reduced ratings. But buck-based choppers require larger inductances to reduce the power pulsations. Buck converter-based PFC provides an alternate option for low-voltage applications.

To incorporate PFC, a family of unidirectional/bidirectional, active/passive, boost, buck, buck-boost, isolated, and multi-level-based PFC topologies was reported in the literature [1]. The other kind of PFC topologies proposed in the literature is bridgeless. These bridgeless converters have reduced the number of devices in the current path achieving higher efficiency and lower losses. These can be further categorized into boost and buck-boost [2, 3]. A bridgeless Cuk-flyback converter has been reported operating in discontinuous mode with a very high power factor and lower loss [4]. Though the system reports high efficiency and smaller size, the system is complex with more components.

A bridgeless buck topology is presented through a power factor corrected rectifier coupled with the buck topology [5]. The conventional $230V_{rms}$ system would need a higher step-down ratio to obtain 48 V_{dc}. The conventional buck converters cannot be employed as they need to be operated at a very low duty ratio of twenty percent. The size of the components will become bulkier with lower switching frequency limitations considering the slower charging and discharging, apart from the switch constraints. Converters are investigated for stepup as a quadratic boost converter for charging a battery from solar PV application [6]. There are also bidirectional converters for returning power to the grid for power stability.

If two buck converters are connected in cascade, the converter, as shown in Figure 1(a), would be realized with a wide step-down ratio [7]. The disadvantage of the cascaded converter is that the number of active switches in the power path is more, resulting in increased switching losses. Reducing redundant states, a converter with a quadratic relationship between the output and input is realized as shown in Figure 1(b).

The converters have the cascaded buck arrangement with twice the number of inductors and capacitors and hence exhibit fourth-order dynamics. These converters were studied for lower input voltages and wider step-down ratio with an average mode of current control with *DC* input source and for lower power requirements of less than 20 W applications [8, 9]. A bidirectional converter with a quadratic relationship for the battery was investigated [10]. The experiment has been verified with resistive loads of 7 Ω and 330 Ω for a buck and boost operation. The conversion ratio had been 24 V/180 V. The isolated two-stage PFC rectifiers have a reported efficiency of 70 to 80%. DICM and DVCM-based topologies are reported to have higher power factors [11].

Buck converter at a very low duty cycle can yield high power factor correction [12]. A series of boost and buck-boost topologies for PFC were investigated [2, 13]. Quadratic gain bidirectional converters for regenerating braking application were investigated for battery/supercapacitor storage applications [14]. Topologies using transformer/coupled inductor for high step up/step down were discussed[15–18]. A bridgeless SEPIC converter with coupled inductor topology for high step up was investigated for motor drive application [19]. A modified SEPIC converter for higher gain was investigated [20]. Cascaded Cuk-buck and quadratic buck-boost topologies were designed and reported for low voltage stress and reduced ripple conditions [21]. Performance evaluation of PFC boost was investigated [3]. However, many of these topologies are for step-up/step-down DC/DC conversion. Traditionally, boost topologies are preferred for power factor correction, but the high output voltage stage which is above the peak of supply voltage makes the system more complex. There is also a requirement of feedback and multiple sensors and switches for a low-voltage step-down application [22]. Interleaved converters were investigated for a higher step-down ratio. Studies were conducted to increase the power rating of the load, improve the efficiency, and lower switching losses using interleaved QBC topology [23]. The literature proposes quadratic converters interfaced with forward/flyback topology to provide isolation requirements. Interleaving reduces the current stress and offers lower loss. The proposed converters have multiple switches switching at 180-degree phase shifts [24, 25]. Multi-phase interleaved converters were presented [26].

Table 1: Comparison studies with the literature.

Topology	Ref. [34] Quadratic buck series resonant PWM	Ref. [35] BB-QB single-stage PFC rectifier	Ref. [36] Bridgeless flyback	Ref. [37] Bridgeless Cuk-flyback	Ref. [38] Boost buck cascaded	Ref. [24] Interleaved transformerless	Proposed QBC PFC (passive)
No. of switches	3	1	2	3	2	4	1
Diodes	4	9	3	5	5	2	7
Inductors	4	4	Flyback	Flyback along with 4 normal	3	2	4
Capacitors	4	3	1	4	3	5	4
Efficiency	91	83	90	55%–90%	94	93	80%
Conversion ratio	180/60 V	85/5 V	(110–220)/48 V	(160–260)/48 V	110/216	400/25	230/54 V
Remarks	DC-DC	Low power (20 W) High component count (AC-DC)	Power factor of 0.92 (3-winding). 50 W application (48 V, 1 A) (AC-DC)	At 125 W, efficiency is 55%, 90% at 900 W (motor)	60 W (LED application)	DC-DC conversion	150 W

To increase the conversion ratio, delayed quadratic buck converters and semiquadratic buck converters have been presented. However, these are for only DC-DC conversions with a high step-down ratio for low-power applications [27, 28]. Switched capacitor-based quadratic buck converter was discussed, but the limitation of this topology has been an increased component count [29]. If a non-cascading connection was used, high step-down topologies can be realized with reduced redundant power processing stages [30]. Investigations were carried out to reduce the dead zone and improve PF in a QBC by cascading a buck cell with a buck-boost cell [31]. Considering the ESR, size of the inductor, and capacitor, it was investigated and reported [32] that the buck converter operated at a very low efficiency of 40% when the duty cycle was 20%, and the efficiency increased to above 80% when the duty cycle reaches 50%.

In multi-phase buck converter circuits, series capacitors are used for the purpose of combining the phases, and modified topologies are proposed in the literature in order to reduce the switching losses [33]. The conduction losses of switches in such topologies are high, whereas the switching losses are low [39]. These topologies have a switching limitation of 50% of the duty cycle. The topologies having Cuk and SEPIC variations also employ series capacitors, and capacitor becomes major storage element instead of inductors, and the size of the capacitor increases [4, 37]. In a boost converter-based topology, the capacitor supplies the load current during the process of charging the inductor when the switch is closed. In such a scenario, the design of the capacitor is important and has to be rated for supplying load current. Comparative studies relating to various topologies, power ratings, and component count are presented in Table 1.

When there is a coupled inductor or transformer in the system, the entire flux does not link to secondary and there is a corresponding loss due to the same. In systems where parallel windings are present, such as flyback, SEPIC, Cuk, and so on [19, 20, 37], the design is based on coupled inductors. The advantages of coupled inductors are that by varying the turn ratio, voltage gain can be varied. But the disadvantage is the stress on the switch due to leakage reactance. In topologies such as interleaved, the literature reports that by switching the devices 180 degrees out of phase, the effect of leakage reactance is annulled.

The topologies of QBC have been conventionally evaluated for low-power and high step-down applications. Interleaved topologies were investigated for 400 W and higher power applications. The present work investigates the performance characteristics of bridgeless/PFC QBC for a 150 W system. The converter operates in discontinuous inductor current mode (DICM), which is reported to have an inherent PFC operation.

The rest of the paper is organized as follows. Section 2 gives the description and presents the operating modes of the converter. Section 3 presents the design of the converter. Simulation and hardware results of the proposed prototype of the passive PFC QB converter are presented in Section 4. Comparative results of the proposed converter with a bridgeless buck system are also discussed. Section 5 concludes the paper with final remarks.

2. Proposed Bridgeless QBC Topology

Figure 2 shows the proposed bridgeless QBC PFC topology. Converters need to operate at an extremely low duty cycle in applications that require a low output from higher input. Due to the limitation of the turn-on/off of the devices, the switching frequency needs to be reduced, and hence the size of the inductors and capacitors becomes bulkier. It can be observed that compared to the conventional PFC of using a single inductor and capacitor at the input side, this system uses twice the inductors and capacitors, a disadvantage in terms of size and cost. At the same time, two inductors at the source yield better thermal performance and low EMI and reduce the filtering requirement.

The following assumptions are made:

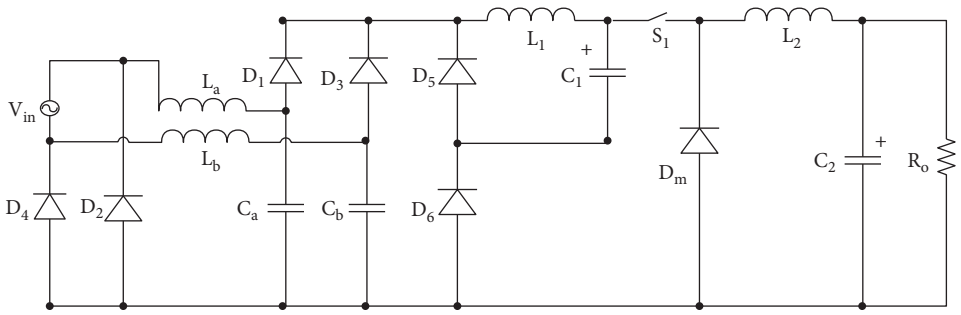

Figure 2: Proposed bridgeless QBC with AC source and PFC.

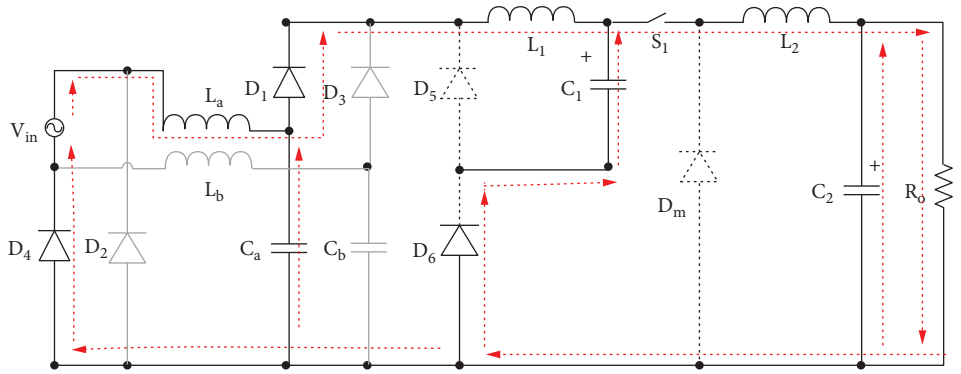

Figure 3: Operating mode of the converter when S1 is closed (positive half cycle).

(i) The source is purely sinusoidal.

(ii) The filter capacitors C_a and C_b are very small such that the voltage is discontinuous.

(iii) MOSFET and diodes are ideal.

(iv) Ripples in the inductor and capacitor are negligible.

To the AC source, a pair of inductors and capacitors is connected across the phase and the neutral for acting as an input filter. To this system, diodes are connected which are conducting at high frequency of 50 kHz by the turn-on/off action of the switch. When the switch is open, these high-frequency diodes do not conduct and the current through the inductor gets interrupted. To avoid this interruption, a pair of diodes is connected providing a return path. The QBC stage has two LC filters, one active switch, and three passive devices. It can be assumed to be a cascaded stage of passive buck stage (L_1, C_1,D_5, and D_6) with an active buck stage (L_2, C_2,D_m, and S_1). During the positive line voltage cycle, the devices L_a, C_a,D_1, S_1, L_1, and L_2 are active through the diode D_4, which closes the path. During the negative half cycle of the line voltage, the devices L_b, C_b,D_3, S_1, L_1, and L_2 are active through the diode D_2 for the circuit to complete. Due to the symmetry of the system, analysis of one-half cycle would represent the complete converter. The operating modes of the converter can be described as follows under the assumption of a constant input voltage over a cycle.

Mode 1. When the switch S_1 is closed, the freewheeling diode D_m and the diode D_5 are reverse biased by the source and do not conduct. The diode D_6 conducts as shown in Figure 3. The current through the inductors i_{L1} and i_{L2} begins to rise. The current through the switch is the same as i_{L2}. $i_{L1} = i_{L2}$-i_{C1}. The input filter capacitor C_a and the buck stage capacitor C_1 begin to discharge. The diode D_4 provides a return path to the source and conducts throughout the positive half cycle.

$$V_{in}(t) = V_m \sin(2\pi f_L t). \tag{1}$$

Converter is considered to operate at a duty cycle of k, where f_L is the line frequency of supply and V_m is the peak of the input supply voltage. In practice, the switching frequency f_S and hence the rectified input voltage can be considered as constant for a small interval of time denoted as V_{ac}. The voltage across the filter capacitor is denoted as V_{Ca}.

$$\begin{aligned}
V_{ac} - V_{Ca} &= L_a \frac{di_{La}}{dt}, \\
i_{La} - i_{L1} &= -C_a \frac{dV_{Ca}}{dt}, \\
V_{Ca} - V_{C1} &= L_1 \frac{di_{L1}}{dt}, \\
i_{L1} - i_{L2} &= -C_1 \frac{dV_{C1}}{dt}, \\
V_{C1} - V_{C2} &= L_2 \frac{di_{L2}}{dt}, \\
i_{L2} - \frac{V_{C2}}{R} &= -C_2 \frac{dV_{C2}}{dt}.
\end{aligned} \tag{2}$$

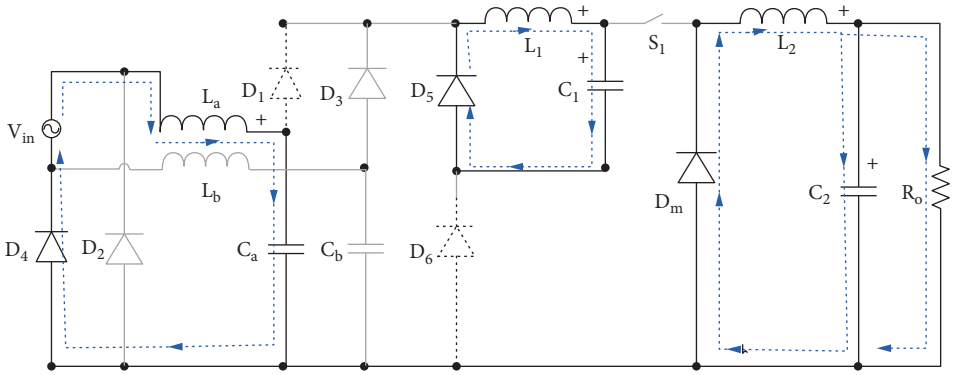

FIGURE 4: Operating mode of the converter when S1 is open (positive half cycle).

Considering the current through the inductors and voltage across the capacitors as state variables, $i_{La} = x_1$, $i_{L1} = x_2$, $i_{L2} = x_3$, $V_{Ca} = x_4$, $V_{C1} = x_5$, and $V_{C2} = x_6$.

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \\ \dot{x_4} \\ \dot{x_5} \\ \dot{x_6} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{La} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ -\frac{1}{C_a} & \frac{1}{C_a} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2} & 0 & 0 & \frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{ac}. \tag{3}$$

Considering the voltage across the capacitor and current through the inductor L_2, the output equation can be written as

$$\begin{bmatrix} v_O \\ i \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix}. \tag{4}$$

Mode 2. The operating mode of the converter when the switch is open is shown in Figure 4. The energy stored in the inductor L_2 is discharged through the filter capacitor, the load, and the freewheeling diode D_m. The energy stored in the inductor L_1 charges the capacitor C_1 with a constant current. As the current through the inductor L_1 cannot be interrupted, the diode D_5 provides the path for the circuit. Hence, D_1 and D_6 do not conduct. The energy stored in inductor L_a is transferred to the capacitor C_a through the path L_a, C_a, and the diode D_4, and the capacitor C_1 charges with the constant current i_{Ca}.

$$i_{La} = C_a \frac{dV_{Ca}}{dt},$$

$$V_{ac} - V_{Ca} = L_a \frac{di_{La}}{dt},$$

$$i_{L1} = C_1 \frac{dV_{C1}}{dt},$$

$$V_{C1} = -L_1 \frac{di_{L1}}{dt},$$

$$i_{L2} = C_2 \frac{dV_{C2}}{dt} + \frac{V_{C2}}{R},$$

$$V_{C2} = -L_2 \frac{di_{L2}}{dt},$$

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \\ \dot{x_4} \\ \dot{x_5} \\ \dot{x_6} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_a} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_a} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_2} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{ac}. \tag{5}$$

The operating modes are analyzed and state matrices are formed and expressed through equations (1)–(5).

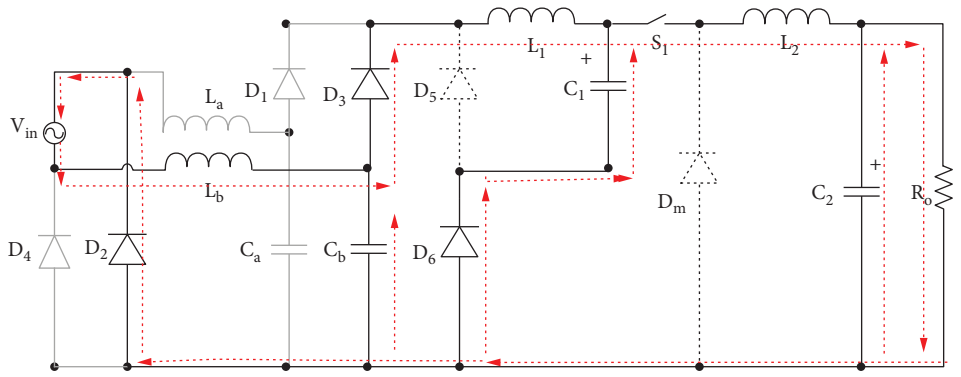

FIGURE 5: Operating mode of the converter when S1 is closed (negative half cycle).

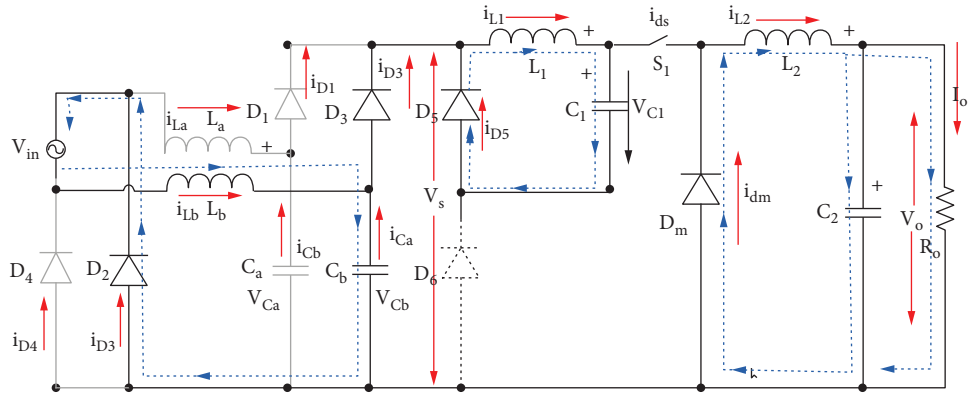

FIGURE 6: Operating mode of the converter when S1 is open (negative half cycle).

Mode 3. When the supply voltage reverses and the switch S_1 is closed, the input current flows through L_b, D_3,L_1,L_2, filter capacitor C_2, and the load resistor R_o. Only the QBC input current shifts through the inductor L_b. Hence, the quadratic stage equations remain the same. The freewheeling diode D_m and the diode D_5 are reverse biased by the source and do not conduct. The diode D_6 conducts as shown in Figure 5. The current through the inductors i_{L1} and i_{L2} begins to rise. The current through the switch is the same as i_{L2}. The current (through the inductor L_1) $i_{L1} = i_{L2} - i_{C1}$. The input filter capacitor C_b discharges. The voltage through the capacitor begins to fall.

$$V_{ac} - V_{Cb} = L_b \frac{di_{Lb}}{dt},$$
$$i_{Lb} - i_{L1} = -C_b \frac{dV_{Cb}}{dt}. \tag{6}$$

Mode 4. The energy stored in the inductor L_2 is discharged through the filter capacitor, the load, and the freewheeling diode D_m. The energy stored in the inductor L_1 charges the capacitor C_1. As the current through the inductor L_1 cannot be interrupted, the diode D_5 provides the path for the circuit. Hence, D_3 and D_6 do not conduct as shown in Figure 6.

The energy stored in inductor L_b is transferred to the capacitor C_b through the path L_b, C_b, and the diode D_2, and the capacitor charges with the current $I_{Lb} = I_{Cb}$. The cycle continues till S_1 is switched on again after the time $T_s.D_2$ provides a path for the return in the negative half cycle and conducts during the entire half cycle. D_1/D_3 switches at a high frequency, and therefore fast recovery diodes have to be used. D_2 and D_4 switch at a power frequency which is 50 Hz for the proposed study.

$$V_{ac} - V_{Cb} = L_b \frac{di_{Lb}}{dt},$$
$$i_{Lb} = C_b \frac{dV_{Cb}}{dC}. \tag{7}$$

The operating current waveform across the various devices for the proposed prototype is presented in Figure 7. When the switching pulse is applied, the current through the switch increases. The inductors L_1 and L_2 and the capacitor C_2 begin to charge through the diode D_1 and the switch S_1 as shown by rising i_{ds}, i_{L1},i_{L2},i_{C2}. When the pulse is withdrawn, the freewheeling diode begins to conduct, indicated by the i_{dm} rising. The inductors L_1 and L_2 begin to discharge, indicated by the falling i_{L1},i_{L2},i_{C2}. The QBC stage capacitor C_1 charges quickly through the diode D_5. The filter inductors L_a/L_b charge alternately during this mode. The operating modes as discussed conform to the simulation waveforms obtained.

The size of electrolytic capacitor in a conventional PFC using boost converter with diode bridge-based rectification schemes is heavy. For step-down applications, single-stage

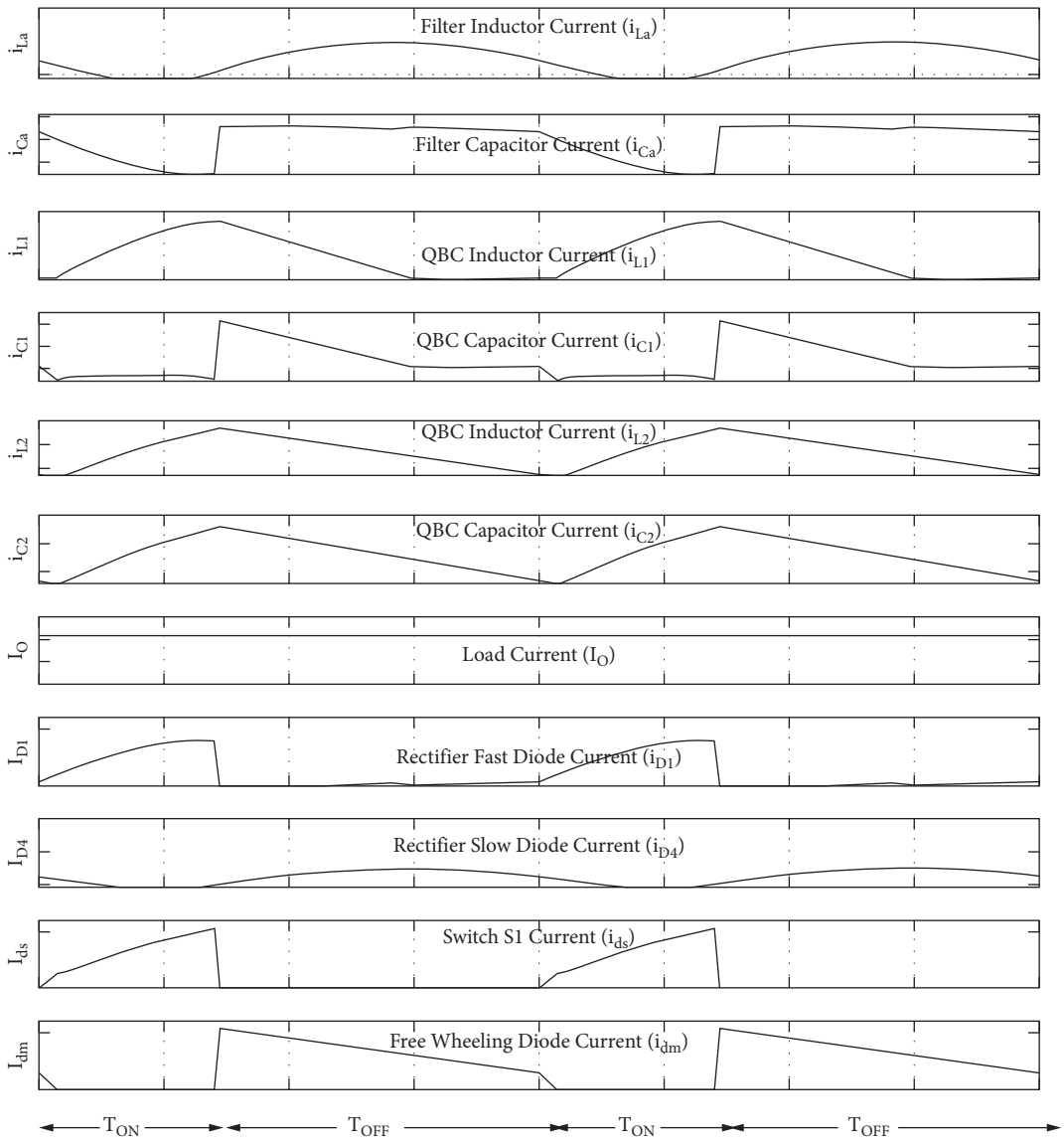

Figure 7: Key waveforms of the various components of the proposed QBC PFC converter.

buck conversion imposes the burden having to operate at 25% duty cycle. Here load side inductor would also be heavy, having to supply load current for 75% of the time. Hence, losses will also increase, resulting in lesser efficiency, whereas the present scheme has the advantage of offering high step-down ratio at a moderate 45% duty cycle. Hence, filtering requirement is reduced. Rectifier stage electrolytic capacitor is eliminated. Requirement of costly sensors for closed-loop control is reduced compared to boost topology-based schemes. The inherent passive PFC takes care of power factor correction, and only output voltage/current control will be required to be processed. The size of the components also reduces, resulting in more economy and indirect increase in efficiency, apart from the benefit of thermal cooling due to current sharing (similar to interleaved topologies). Further reduction in size can be obtained by increasing switching frequency, but due to the limitations of available components, frequency was limited to 50 kHz.

3. Design of Components

Considering *AC* supply of 230V_{rms}, 50 Hz, the rectified output voltage of a full-bridge is given by $2V_m/\pi$. As per the standards of IS 12360 (1988) [40], 10% voltage variation at the source side, the *AC* supply voltage varies between 207 and 253V_{rms}. The corresponding *DC* voltage varies from 186 V to 227 V. Considering a 48 V battery charging application with a load current of 2.5 A, equivalent load resistance R_O is estimated as 20 Ω. The maximum power output is P_o which is assumed to be 150 W. The relation between output and input for a quadratic converter is given by $V_O = k^2 V_S$, where k is the duty cycle, and therefore $k = \sqrt{V_o/V_s}$. Assuming V_S as the rectified DC voltage, the voltage across the capacitors can be computed as $V_{C1} = k * V_s$, $V_{C2} = k^2 * V_s$. The load current $I_O = V_O/R_O$, $I_O = k^2 * V_s/R_o$, and an average of the current through the inductor L_2 (i_{L2}) is the same as the load current I_O, Therefore,

Table 2: Estimated device voltage and current ratings.

Device V/I	Estimated value
$V_S = 2V_m/\pi$	207 V
$V_{C1} = kV_S$	104 V
$V_{C2} = k^2V_S$	52 V
$i_{L2} = I_O = k^2V_S/R_O$	2.6 A
$i_{L1} = ki_{L2} = k^3V_S/R_O$	1.3 A

$i_{L1} = k_3 * V_s/Ri_{L1} = k^3 * V_S/R$. The duty cycle is minimum (0.45) when the output voltage is minimum and source voltage is at maximum (48, 227), and the duty cycle is maximum (0.55) when the output voltage is maximum with source voltage minimum (54, 186).

Substituting the values, the theoretical limits of the duty cycle (k) vary between 0.45 and 0.55 and are assumed as 0.5 for computation. The average value of inductor current i_{L2} will be the same as that of the load current. The computed values with a moderate duty cycle of 50% are presented in Table 2.

3.1. Design of Filter Capacitor (C_a, C_b). For the higher values of constant "p," the capacitor current is continuous for a longer period of time, and the input current is distorted. For shorter values of "p," there would be higher voltage stress on the switch.

$$C_a, C_b = \frac{pTs}{2R_e}. \tag{8}$$

A value of $p = 0.03$ was considered for design [5]. f_L is the line frequency of 50 Hz, and the switching frequency f_S is 50 kHz. C_a and C_b are estimated to be 15 nF from equation (8). A 47 nF capacitor was used for the study based on the component availability. As the capacitors are subjected to voltage stress of $2V_m$, the voltage rating should be above 650 V.

3.2. Design of Filter Inductor (L_a, L_b). There is LC loop with equivalent inductance L_e and C_a, and hence resonance can occur. In order to avoid resonance, the constraints to be met are given in the equations below.

$$f_r \ll f_s, \tag{9}$$

$$L_{\min} \gg \frac{1}{C}\left[\frac{(1-k)T_s}{2\pi}\right]^2, \tag{10}$$

$$L_{\max} \ll \frac{1}{C}\left[\frac{(1-k)2T_s}{4\pi f_L}\right]. \tag{11}$$

Substituting the values in equations (10) and (11), the filter inductor can be estimated to be between 54 μH and 169 mH, and the resonating frequency of the equivalent inductance with filter capacitance is estimated as 13.3 kHz using equation (12). The value of filter inductance used is 2.6 mH. The RMS value of source current at the input side is around 1A, so that the filter inductor can be selected which can have a 2A rating. It was observed that inductor ESR increases with an increase in switching frequency. To reduce the size of the inductor, higher frequency is required. There could be losses due to the internal resistance of various components. Hence, lower ESR components are desirable. The inductor was wound in lab using toroid core and the value of inductance and ESR is measured with the help of LCR meter.

$$f_r = \frac{1}{2\pi\sqrt{(L_eC_a)}}. \tag{12}$$

3.3. Design of QBC Inductors L_1 and L_2. Following the conventional buck converter, the inductor is designed using equation (13), which gives a value of 384 μH for the continuous current mode. If the inductor L_1 operates in discontinuous mode, the component used should be lesser than 384 μH, and the estimated value for L_2 is 190 μH. Duty cycle $k_{\min} = 0.45$, and the peak-to-peak ripple currents were limited to 3 A.

$$\begin{aligned} L_1 &= \frac{V_{C1}(1-k)}{\Delta i_{L1} f_s}, \\ L_2 &= \frac{V_{C2}(1-k)}{\Delta i_{L2} f_s}, \\ L_1 &= \frac{104(1-0.45)}{3*50000} = 384\mu H, \\ L_2 &= \frac{52(1-0.45)}{3*50000} = 190\mu H. \end{aligned} \tag{13}$$

3.4. Design of Output Capacitors. Using the output ripple constraints and the load power requirement from equation (14), the critical value of capacitor C_C is greater than 763 μF. Consider the output voltage ripple ΔV_o as 10 mV.

$$\begin{aligned} C_C &= \frac{(1-k)}{16L_2 f_s^2}, \\ C_2 &= \frac{P_o}{V_o \Delta V_o 4 f_s}, \\ C_2 &= \frac{150}{54*0.01*4*50000} = 1388\mu F. \end{aligned} \tag{14}$$

3.5. Diodes and Switch. The rectifier stage diodes are expected to withstand a peak input voltage of 2Vm and hence are rated above 650 V. There are two slow switching diodes at 50 Hz and 5 fast switching diodes at 50 kHz in the designed prototype. The voltage across the switch is desired to withstand $2V_m + V_o$ VO. Though rectifier stage diodes have a low current rating requirement as the current drawn from the source is low, the QBC stage diodes have a higher current rating. As the entire inductor current is carried by these diodes during freewheeling operation, diodes of rating 8 A were chosen.

Table 3: Parameter values used for simulation and experimental study.

Device	Component value
L_a, L_b	2.6 mH, 0.05 Ω (toroidal core inductor, wound in lab and tested with LCR meter)
L_1	274-10 L, PCV2 inductor, (270 μH, DC resistance 0.06 Ω, 7.2 A i_{rms}) (coil craft)
L_2	184-10 L, PCV2 coil inductor (180 μH, DC resistance 0.048 Ω, 8 A i_{rms}) (coil craft)
C_a, C_b	0.047 μF, Wima capacitors, 1600 V_{dc}, 650V_{ac}
C_1	Two electrolytic capacitors of 100 μF, and 400 V (series to obtain 50 μF, 800 V)
C_2	Two 3300 μF electrolytic capacitors, 200 V (parallel to obtain 6600 μF).
D_1–D_6,D_m	MUR 880, 800 V, 8 A
Switch	(MOSFET)17N80C3. $V_{ds} = 800$ V, $R_{ds} = 0.29$ Ω, $i_d = 17$ A/(IGBT15N120), $V_{ce} = 1200$ V, $i_{ce} = 15$ A

The components are designed based on equations derived through available literature resources. While selecting components, the nearest values available in the laboratory were chosen, keeping the literature as reference.

4. Simulation and Experimental Results

4.1. Comparative Results of Buck and Quadratic Buck Converter with DC Source. Advances in semiconductor technology have motivated the development of integrated circuits, which require 3.3 and 1.5 V power supplies. At the same time, the battery technology is upgrading from 12 V to 36/48 V systems. To obtain such low voltages, conventional DC-DC converters do not offer a high step-down ratio. The relation between the input and output of a conventional buck converter is given by $k = V_o/V_s$ where k is the duty cycle, V_O is the output, and V_S is the *DC* input voltage. When a wider conversion ratio is required, the conventional buck converter fails due to the limitation of the T_{ON} requirement of a switch. As switching frequency increases, there exists a limitation due to the minimum duty cycle of the switch. Quadratic buck converters satisfy the requirements. The quadratic converters can be single-stage or multi-stage, isolated/non-isolated. Single-stage conversion is always more efficient compared to multistage conversions. An increase in the number of stages leads to increase in the number of components in the power path and hence less efficiency apart from complexity in the control scheme. Quadratic converters have the relation of duty cycle as $V_O = k^2 V_S$.

To test the quadratic stage of the prototype, the simulation studies of the conventional buck converter and quadratic buck converter as represented in Figure 1 were conducted using MATLAB/Simulink with parameters as shown in Table 3. A *DC* source of 30 V was used to apply a variable *DC* input voltage. A 20 Ω resistor was used as a load. The duty cycle is varied from 25% to 50%, and the variation in output voltage for a conventional buck converter with QBC is plotted as shown in Figure 8. The experimental and comparative results for the buck and QBC are shown in Figures 9(a)–9(d) which depict a higher step-down ratio for the same duty cycle.

The efficiency of the conventional buck converter was observed to be over 94% with a *DC* source. An extra stage of cascaded combination gives lower efficiency of 70% for light loads. Efficiency increases with an increase in load current.

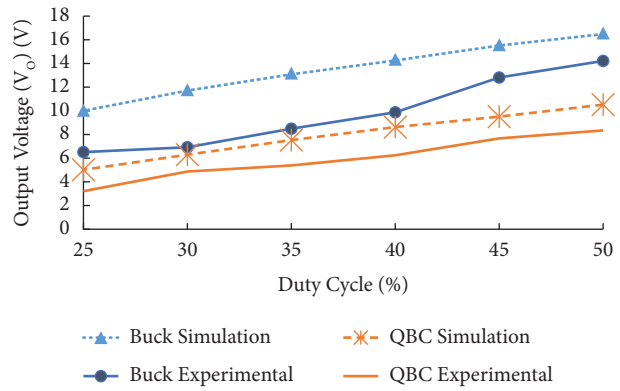

Figure 8: Comparative study of variation of output voltage with duty cycle.

5 V power supplies have applications with relays, mobile charging, stepper motors in 3D printers, robotics, and surveillance cameras.

4.2. Simulation Results of QBC with AC Source. The circuits of conventional buck and QBC as shown in Figure 2 are simulated with parameters as presented in Table 3 using MATLAB R2020b. The source is varied from 30 V–230 V. Figure 10(a) indicates the V, I stress of the rectifier stage diodes. The fast diodes (D_1, D_3) are operated at 50 kHz as expected, and the slow diodes (D_2, D_4) operate at 50 Hz. Both the inductors charge and discharge together, as discussed in modes of operation indicated by Figure 10(b). Inductor L_1 current is discontinuous, and this is due to the small size of the inductor. The voltage stress across the switch is also pulsating, and instantaneous stress of 400 V is indicated in Figure 10(c). Figure 10(d) represents the voltage and current waveforms of the input filter capacitors C_a and C_b. Figure 11 shows the input voltage and the sinusoidal current drawn through the rectifier circuit, which indicates a higher power factor compared to the bridge rectifier circuit with a capacitive filter. The V, I stress of the switching device and the freewheeling diode are not constant due to pulsating *DC* being applied.

4.3. Hardware Results of QBC. The experimental prototype is rigged up as shown in Figure 12. MATLAB is interfaced with a system generator tool for the transfer of logic. Previous

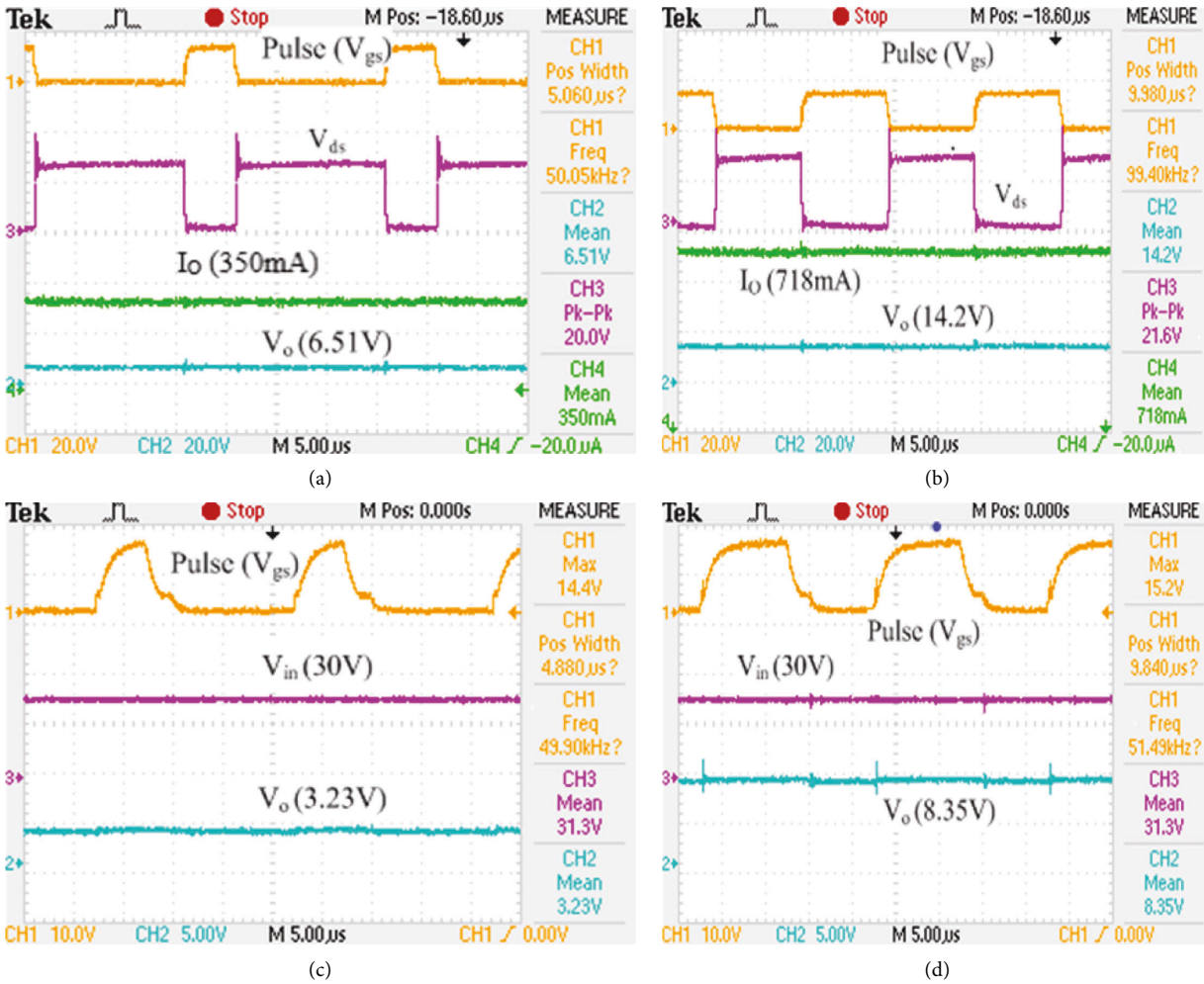

FIGURE 9: (a) Buck converter with 25% duty cycle. (b) Buck converter with 50% duty cycle. (c) QBC with 25% duty cycle. (d) QBC with 50% duty cycle.

working experience of register transfer logic (RTL) is not required when the system generator is interfaced with MATLAB. Simulink block sets such as waveform generators and comparators can be used. It has "gateway in" and "gateway out" ports helping to transfer generated logic into a controller. An "xpr" file is generated, which is further processed using Vivado design suite. This project is opened using the Vivado interface, and several steps such as block design, adding sources and sinks, selecting clock, and so on are performed. The generated design is simulated, run, and implemented using the appropriate features available. Once the simulation runs smoothly, a bit stream is generated. This bit stream is transferred to FPGA using the hardware manager.

For the duty cycle generation, pulses are generated by using a comparison of a constant with a sawtooth wave of 50 kHz. The magnitude of "constant" is varied to obtain pulses of 25–50% using a system generator for the MATLAB interface. These pulses were sent to the output ports of Basys3, which is an Artrix-7 35T-based FPGA from Xilinx using the "Vivado design suite" as the user interface. "Pmod" ports J_1, L_2, J_2, H_1, K_2, and H_2 are used as the output ports with each duty cycle assigned with the specific port for convenience and faster analysis.

As the output of FPGA is 3.6 V, a MOSFET driver would be required. An isolator is required to help in the protection of the low-voltage control circuit from high power load. TLP 350, an 8 pin opto isolator and driver is used to step up the pulses to 15 V. TLP 350 was the opto isolator and driver which facilitates driving the power switch and offers isolation. The embedded figure describes source voltage, load voltage, the voltage across the switch, and the freewheeling diode for a duty of 35%. The fast charge and discharge at 50 kHz operation of the switching diodes (D_1 and D_3), 50 Hz switching of the slow diodes (D_2 and D_4), the filter capacitor voltages, and the inductor current are illustrated in Figures 13(a)–13(d). The applied voltage is varied in steps of 20 V from 30 V to 230 V, and the variation in output voltage is studied.

Figure 14 depicts the output voltage (with a QBC converter giving a low voltage of 54 V at a medium duty of 50%), voltage across the switch (V_{ds}), load voltage, and current for the 150 W application QBC stage inductor L_2 which was not accessible for the current measurement.

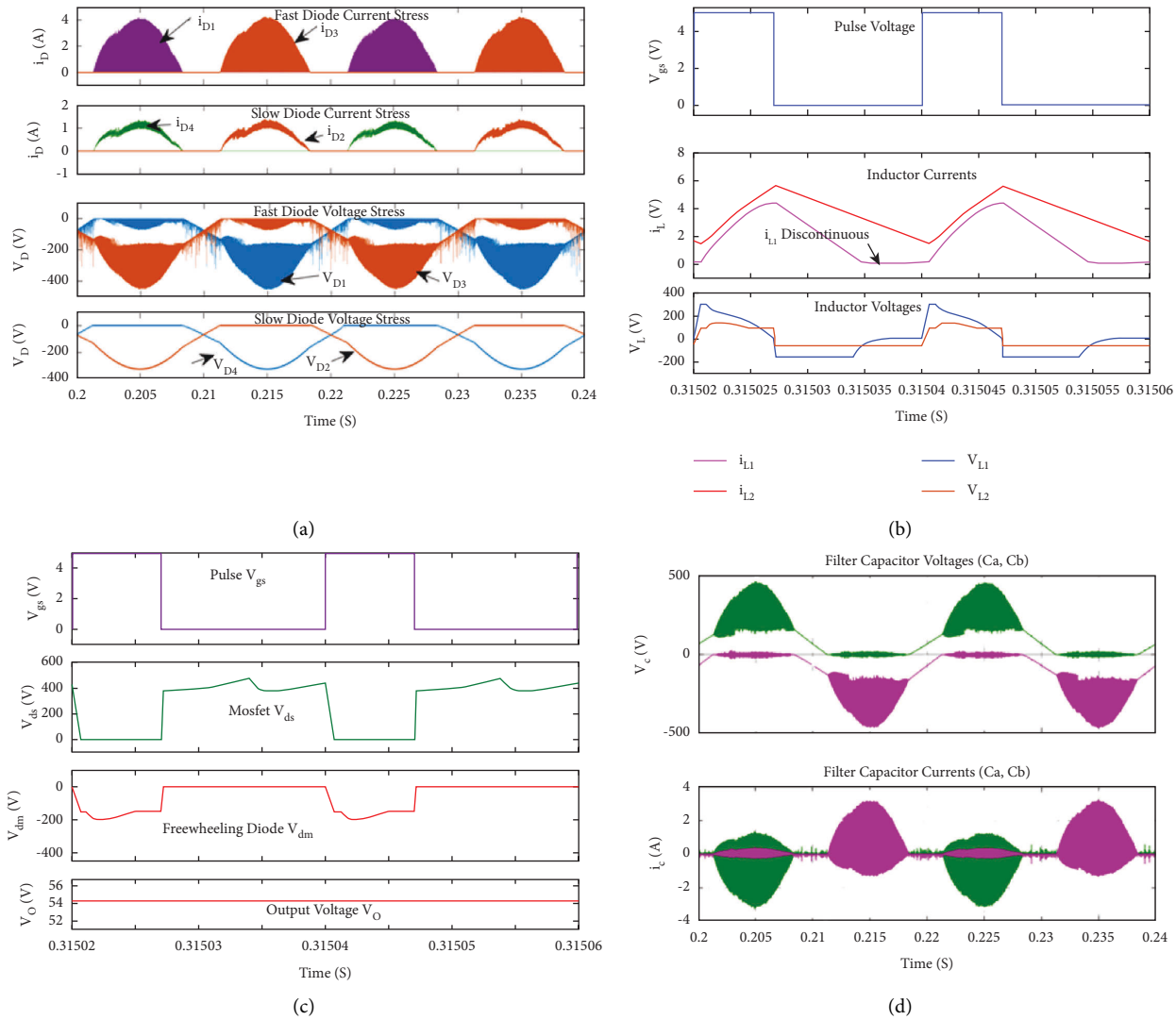

FIGURE 10: (a) Fast and slow diode stress. (b) V,I across the QBC stage inductor. (c) Voltage stress across the switch and freewheeling diode. (d) Input filter capacitor voltage and current.

Figure 15 indicates the source current being sinusoidal, and the power factor as estimated from the dead band between the voltage and the current is 0.89. Figure 16 presents the comparative results between the simulation and the experimental results. The representative hardware results agree with the modes of operation as discussed and simulation results. Voltage stress across the switch is observed to be high due to DICM with passive PFC topology and selection of the small size of inductors. For a 150 W operation, peak stress was observed to be over 740 V, and it increases with an increase in the load currents. Protection was incorporated by using an RCD snubber. As the MOSFET samples were limited in number and IGBT was compatible at the switching frequency, it was used at a later stage. There is a difference in the simulation and practical results beyond 35%. For a moderate duty cycle of 25% to 35%, the results show a linear relationship, and thereafter the simulation and hardware results deviate. With a higher duty cycle, there is a higher current being drawn from the source, resulting in higher i^2r losses across the series resistance of the components, inductors, and capacitors. As the resistance increases with frequency for inductors, the additional loss could have resulted in a lowered voltage at the load side. It was observed that the ESR of the inductor core is not constant but increases with the frequency of operation, which could have led to the difference in the simulation and hardware studies.

4.4. Comparative Evaluation of PFC Converters (Buck Converter vs. QBC). The hardware circuit of the buck converter was rigged up, and the output of the rectifier stage PFC was connected to compare the conventional buck circuit with the proposed QBC topology. It was observed that the switching capacitors exhibited DCVM as against CCVM in the QBC converter. The stress of the capacitors was around 324 V at 110 V_{rms} source, increasing to beyond 510 V at 200 V_{rms}. Figure 17 represents the pulse of 25% across the switch giving 48 V output with a 2.4 A load current. Figure 18

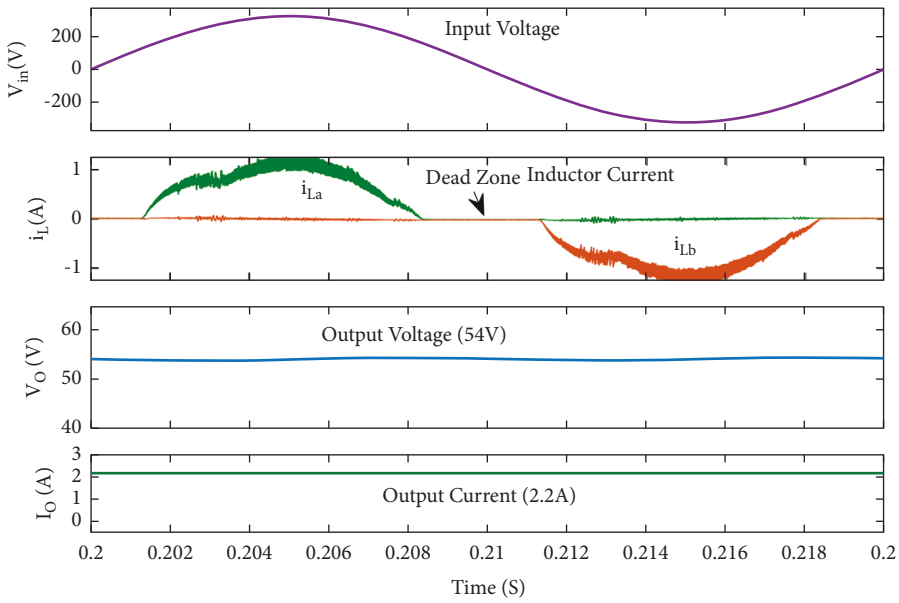

Figure 11: Simulation results of QBC with PFC for an input of 230 V AC at 35% duty cycle with output of 54 V and 2.2 A.

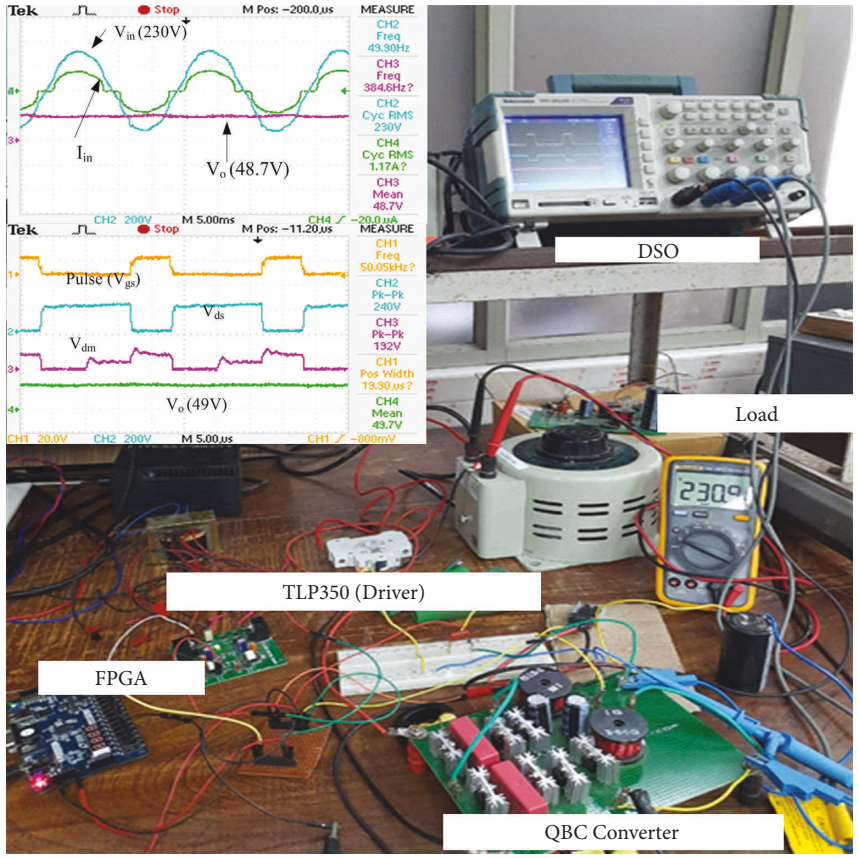

Figure 12: Prototype for QBC with PFC converter with 230 V input and 48 V output.

presents the variation of output voltage with load. Load resistance is varied to study the nature of output voltage variation with load. There has been a decrease in voltage.

Figure 19 presents the experimental results with the variation of output voltage with duty cycle from 25% to 35% for both QBC and conventional buck converter [5] for a load of 20 Ω. The experimental results indicate the variation of output voltage for QBC topology but lesser response with a change in duty cycle in buck converter-based system. This shows better control of load voltage by the proposed QBC scheme.

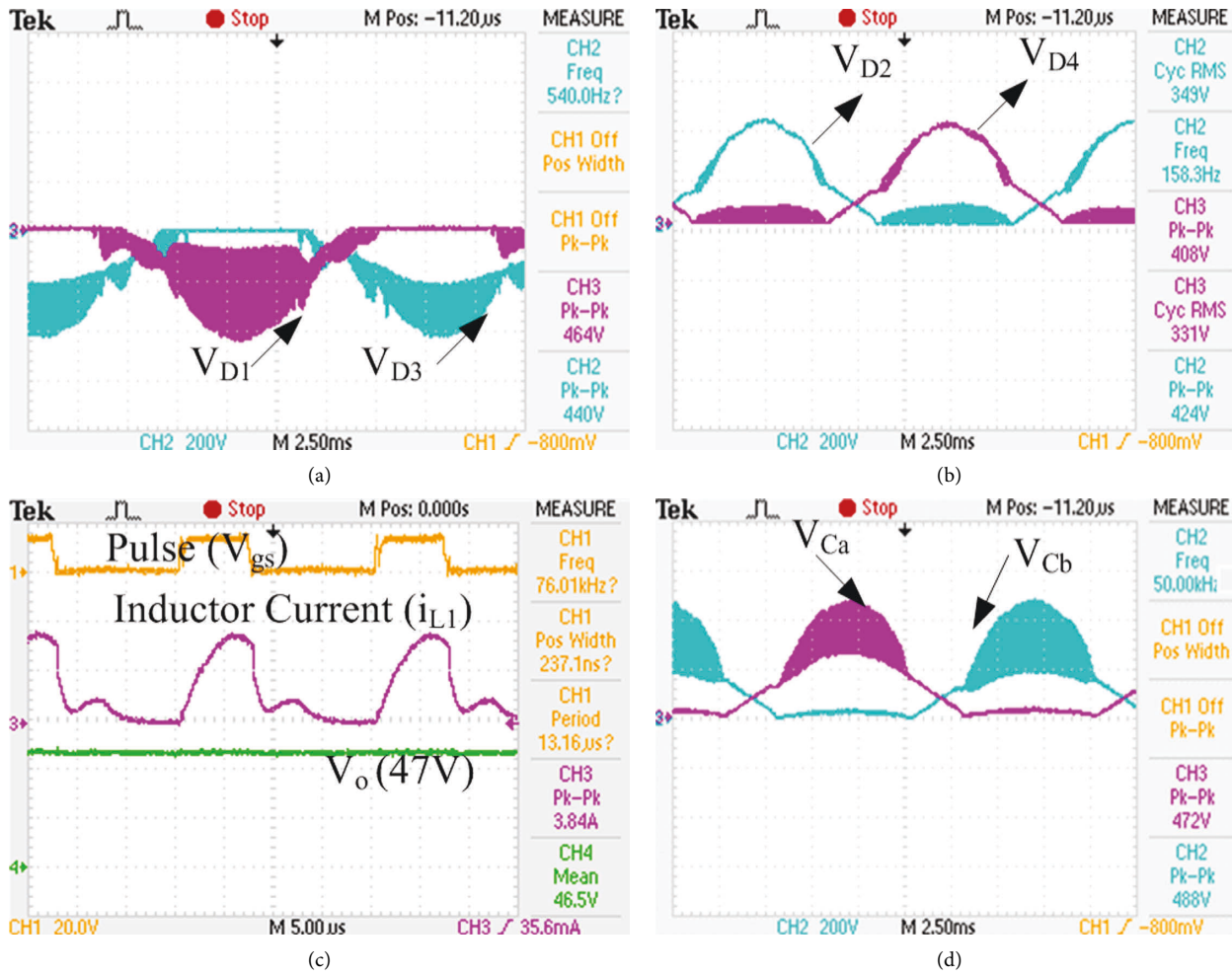

Figure 13: (a) Rectifier stage fast diode stress. (b) Slow diode voltage stress. (c) Inductor current. (d) Voltage across the filer capacitors.

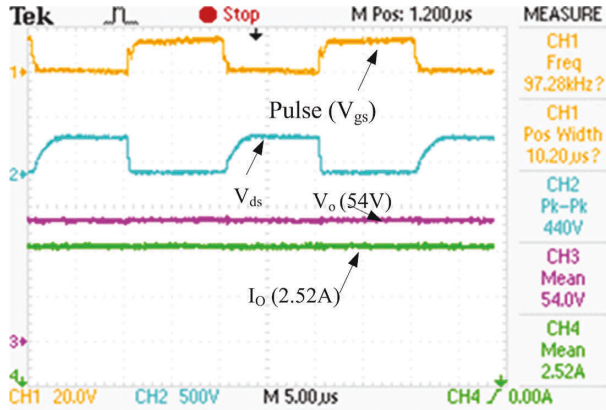

Figure 14: Experimental results of QBC with PFC for an input of 230 V AC at 50% duty cycle with output of 54 V and 2.2 A.

Comparative studies with existing literature as in Table 1 indicate that conventionally QBC was used for low-power, high step-down applications. The existing literature survey indicates that most of the topologies offer a lower efficiency for low-power applications, and efficiency increases with an increase in the rated power of the application. The presented prototype offers an alternative with a reduced number of switches and a comparable efficiency. Hence, the proposed high step-down ratio converter facilitates improved efficiency as the individual stages switch at a moderate duty cycle of 45%, whereas due to the cascaded stage, the desired high step-down voltage ratio is obtained by the proposed converter.

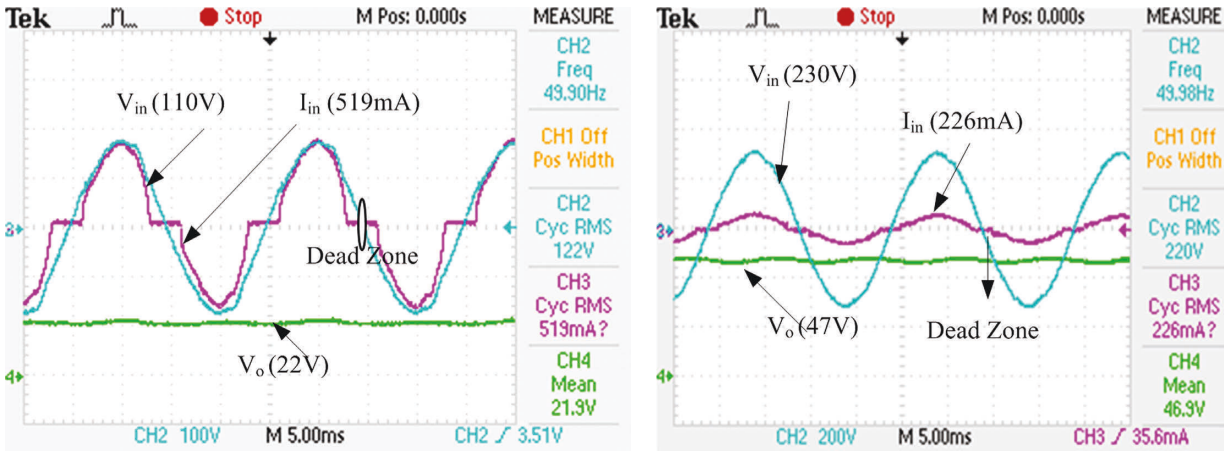

Figure 15: Source voltage and current waveform. (a) 110 V input voltage. (b) 230 V input voltage.

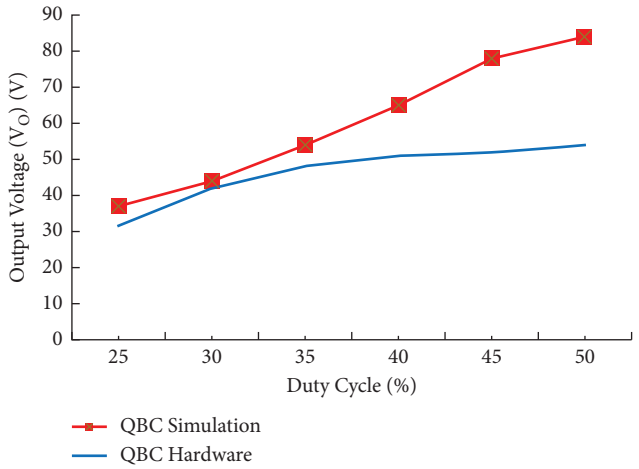

Figure 16: Comparative study of variation of output voltage with duty cycle for QBC with PFC Converter.

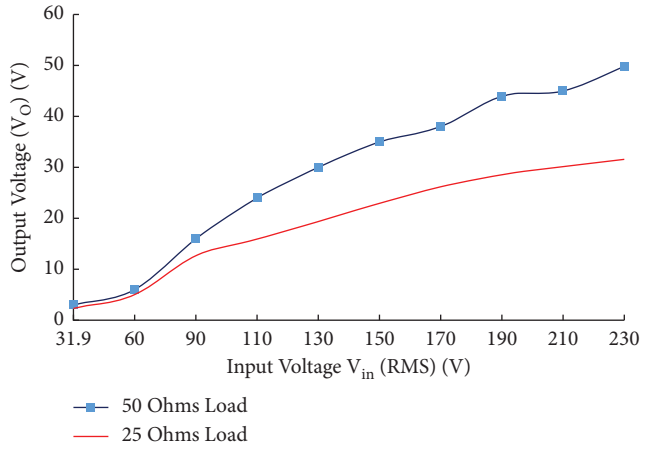

Figure 18: Comparative study of variation of PFC QBC with load.

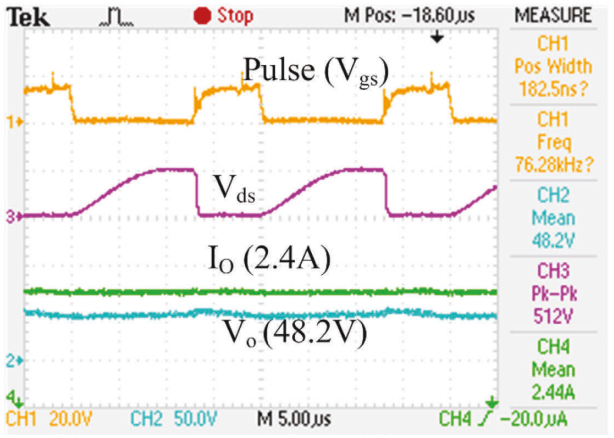

Figure 17: Buck converter with PFC at 25% duty cycle duty.

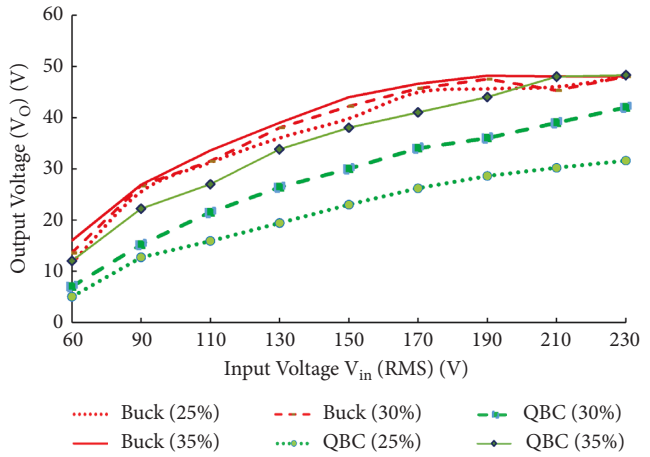

Figure 19: Comparative study of variation of output voltage for the conventional buck and proposed quadratic PFC buck converter.

5. Conclusion

A modified power factor corrected quadratic buck converter is proposed and described in this paper. The prototype of 150 W was rigged up in the laboratory and tested. The different operating modes of the operation of the converter are discussed and presented. The proposed converter has the benefit of single switch operation and reduced component counts comparable with the existing literature. The presented topology offers an improved power factor of over 0.89 at 110 V and 0.95 at 230 V. The study of variation of the output with variation in load, duty cycle, and source was carried out experimentally, and the results are presented. The efficiency of the converter was observed to be over 80%. By using low ESR components and better assembly techniques, the efficiency could be further improved.

Comparative studies of conventional and quadratic buck topologies for *DC* loads are conducted and presented. Though conventional buck operates at a higher efficiency due to the reduced total number of components, quadratic topology offers a higher step-down ratio for a moderate duty cycle with equivalent components in the power path. The proposed converter is suitable for 24–48 V DC power requiring applications such as small motors and UPS/battery charging applications. It provides a high step-down voltage ratio and inherent power factor correction without the requiring closed-loop control and complex sensor control.

The present work focused on open-loop control and investigated for power applications of 150 W. The study indicates higher stress on the switch during commutation with increasing load power. A passive RCD clamp was used for the reduction of the same. Further work is required in exploring closed-loop control for the system and investigations for higher power applications.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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