

## Retraction

# Retracted: Simulation of Multisensor Energy Data Fusion Transformer Acquisition System Based on FPGA

### International Transactions on Electrical Energy Systems

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This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

- (1) Discrepancies in scope
- (2) Discrepancies in the description of the research reported
- (3) Discrepancies between the availability of data and the research described
- (4) Inappropriate citations
- (5) Incoherent, meaningless and/or irrelevant content included in the article
- (6) Peer-review manipulation

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.


The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

### References

- [1] L. Luan and D. Hu, "Simulation of Multisensor Energy Data Fusion Transformer Acquisition System Based on FPGA," *International Transactions on Electrical Energy Systems*, vol. 2022, Article ID 7612674, 7 pages, 2022.

## Research Article

# Simulation of Multisensor Energy Data Fusion Transformer Acquisition System Based on FPGA

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In order to solve the problems of small signal acquisition range and poor acquisition accuracy of the existing multichannel acquisition system, a multisensor energy data fusion transformer acquisition system simulation method based on FPGA is proposed, and key hardware functions are designed and implemented. The system uses FPGA to control the core logic, synchronously collects and controls the energy data of the CCD camera and the laser rangefinder, organizes and uses an external large-capacity SDRAM group for buffering, and uses a dedicated PCI interface chip PLX9656 to achieve high-speed data transmission. Two pieces of sensor energy data and PCI bus energy data are stored in real time using a large-capacity disk array composed of multiple SATA hard disks. The function and performance of the energy data acquisition and storage system were tested. After the actual system test, the experimental results show that the transmission speed of the system through the PCI bus exceeds 200 MB/s, the writing speed of the continuous disk array is 240 MB/s, and the real-time acquisition and recording speed is 100 MB/ss. *Conclusion.* The system effectively solves the problems of high-speed data acquisition and storage and large capacity data transmission of key sensor nodes.

## 1. Introduction

In the research of aerospace, geological exploration, satellite navigation, and other fields, it is necessary to collect and record some important energy data parameters for energy data analysis and research, which has important reference value for the next experiment improvement and result analysis and is also more important for the result analysis of scientific research energy data. Therefore, the research and design of energy data acquisition memory is of great significance for these fields [1]. The main application of data acquisition memory in these fields is to collect and record the data collected by various sensors during the working process of aircraft, such as vibration signal, noise signal, image signal, and other key data. These energy data play a key role in the monitoring of aircraft operation status, fault analysis, environmental energy data acquisition, and so forth; it is very important to accurately collect and record

energy data. With the increase of the amount of energy data to be tested and the types of test energy data, it is necessary to collect and store multiple energy data signals at the same time, which puts forward higher requirements for the performance of the energy data acquisition and storage system. Because FPGA can process a large amount of parallel data at the same time, the current mainstream data acquisition memory design schemes use FPGA as the control module, write logic circuit programs in FPGA to control, receive the data signals sent from the outside, and save them in the memory. In recent years, with the rapid development of semiconductor technology and the maturity of production technology, energy data acquisition memory has ushered in new development. As the main control module of energy data acquisition memory, large-scale integrated circuits such as PGA and single chip microcomputer make energy data acquisition and storage more complex and functional by software programming. The products

developed in recent years have made great progress in multichannel energy data acquisition, large-capacity storage, high-speed storage, and so forth [2].

Therefore, it is of great significance to improve the collection and storage of real-time energy data by using emerging technologies.

## 2. Literature Review

For real-time energy data collection and storage, Miao et al. proposed realizing feeder automation FA by building distribution automation system (DAS) [3]. The meaning of feeder automation is to monitor the status of current, voltage, interconnection switch, and section switch on the feeder remotely. Yarlagadda et al. proposed updating the solid-state storage technology in the aerospace energy data storage system, changed the previous method of using tape storage, and improved the stability and reliability of the energy data storage technology [4]. Kumar et al. proposed the integration of FPGA technology and ASIC technology, so as to reduce its disadvantages of large volume, insufficient capacity, and larger power consumption than ASIC and then optimize energy data transmission [5]. He et al. proposed that FPGA chip is the core device, and online driving fatigue detection can be realized only by matching with appropriate digital image algorithm. The design omits the DSP control chip and expands the memory to form a simplified minimum system. Reprogrammable features and highly integrated features can greatly reduce the design cycle and design cost [6]. Tappari proposed designing the internal logic circuit of FPGA and creating the firmware program of FX3. It realizes the receiving and storage of LVDS energy data and the reading of energy data in memory by computer [7]. Kowalczyk et al. proposed using multiple hard disks to form a RAID array (cheap redundant disk array). High-end storage functions and redundant energy data security were provided for large servers. Raid combines multiple independent hard disks (physical hard disks) in different ways to form a hard disk group (logical hard disk), thus providing higher storage performance than a single hard disk and providing energy data redundancy technology.

According to the requirement of real-time energy data acquisition and storage of key sensor nodes, this paper proposes a solution of real-time energy data acquisition and high-speed storage based on FPGA and designs and implements the key hardware functions. The system uses FPGA for core logic control, synchronously collects and controls the energy data of CCD camera and laser rangefinder, sorts out and uses external large capacity SDRAM group for cache, uses a special PCI interface chip PLX9656, realizes the high-speed transmission of two pieces of sensor energy data and PCI bus energy data, and uses a large capacity disk array composed of multiple SATA hard disks for real-time storage. The function and performance of the energy data acquisition and storage system are tested to prove the real time, stability, and efficiency of the real-time energy data acquisition and storage of key nodes.

## 3. Research Methods

*3.1. Main Functions and Technical Indicators.* In the measurement system, in order to accurately measure the jitter of the flexible baseline and the change of the relative attitude of the two antennas in real time, it is necessary to select a CCD camera with high frame rate and large array and a high-precision laser rangefinder for combined measurement, which will produce a large amount of high-speed image energy data and distance energy data output by the laser rangefinder [8]. Therefore, the main function of the high-speed acquisition and storage system designed in this paper is to control the time synchronization between the measurement sensors, complete the real-time energy data acquisition of each sensor, and shunt the collected energy data. One channel of energy data is stored at high speed; another channel of energy data is output to another real-time processing system. According to the requirements of flexible baseline measurement system, the system in this paper should be able to collect and store the measurement energy data of two sensors in real time. The technical indicators to be achieved mainly include continuous acquisition speed, continuous storage speed, and minimum storage capacity. The CCD camera in the system adopts a high-resolution, high frame rate area array digital camera, the image resolution is 1608 columns  $\times$  1208 rows, and the maximum frame rate of the camera is 30 Hz. The AD sampling of the camera energy data is 10 bits, and the energy data acquisition is only 8 bits high, so the energy data volume generated by the CCD camera per second is about 55.57 MB [9]. LRFS-0040-2 laser rangefinder is used as the laser rangefinder. The measurement rate can reach 50 Hz at most. RS422 interface is used as the energy data interface, and the amount of energy data generated is 9.6 kB/s. The energy data volume of the two sensors per second is about 56 MB/s, so the continuous acquisition speed of the acquisition system must be greater than 56 MB/s before real-time energy data acquisition of the two sensors can be carried out. Only when the continuous storage rate is greater than the acquisition speed can the energy data be stored in real time and accurately. Therefore, the continuous storage speed should be greater than 56 MB/s, and the maximum theoretical read-write speed of SATA hard disk can reach 150 MB/s. Using multiple SATA hard disks to form a RAID array can provide higher storage performance than a single hard disk. According to the requirements of the flexible baseline measurement system, the longest continuous working time of the acquisition storage system is about 2 h, and the minimum storage capacity required is about 390.76 GB [10]. According to the demand analysis of the above energy data acquisition system and considering the scalability of the system and the needs of actual energy data transmission and terminal processing, it is required that the energy data acquisition and recording speed should reach 70 MB/s, the continuous disk array writing speed should reach 120 MB/s, and the storage capacity should reach 2 TB. For the 32-bit/33 MHz PCI bus, it can generally reach 80 MB/s in actual use. The energy data in and out of the system memory must pass through the PCI bus, which will reduce the efficiency of the bus by half. The

acquisition speed of the system must be greater than 56 MB/s, so the 64-bit/66 MHz PCI bus is selected, and the peak speed of energy data transmission can reach 528 MB/s. The existing system shows that the actual transmission speed of the 64-bit/66 MHz PCI bus can reach more than 200 MB/s, so the transmission speed of the PCI bus fully meets the system requirements [11].

The whole system is mainly composed of CCD camera, laser rangefinder, PCI energy data acquisition card, SATA disk array, and computer. The PCI image acquisition card is mainly composed of sensor energy data interface, FPGA logic control chip, cache, and PCI interface chip. The principle of the scheme is as follows: Firstly, the host sends commands to configure the CCD camera and laser rangefinder. After the configuration is completed, the acquisition is started. The high-speed image energy data output by the CCD camera and the synchronous control signal are sent to the FPGA and cached in the FPGA. The energy data of the laser rangefinder is also sent to the dual-port RAM of the FPGA through the serial port for caching. After the FIFO is half full, the energy data of the CCD camera and the laser rangefinder are shunted under the control of the FPGA, one of which is sent to the external SDRAM group for caching. After the SDRAM is stored in the set image frame number, it is sent to the PCI for interruption. The host responds to the interruption, reads the data from the SDRAM to the memory for processing, and writes the data to the hard disk to complete real-time storage. The other way is sent to the relevant real-time processing system for processing. The block diagram of the whole design scheme is shown in Figure 1.

The design of data real-time acquisition and storage system applied to flexible baseline measurement system includes the following key technologies: CameraLink interface technology, multisensor synchronization technology, real-time acquisition and cache of multisensor data, and real-time storage of multisensor data.

**3.2. Key Design and Implementation of Real-Time Energy Data Acquisition and Storage System.** The experimental camera adopts CameraLink standard interface, and the basic configuration adopts standard MDR26 connector output. The system uses FPGA as the main control chip of the acquisition card, and the i/o standard supported by FPGA is LVCMOS/LVTTL signal [12]. The main function of DS90CR288A is to complete the conversion from LVDS to TTL level signals and the conversion of serial signals into parallel signals. In order to set parameters and trigger control of the camera, it is necessary to convert the camera control signals (CC1-CC4) and signal SerTC (serial to camera) output from FPGA into LVDS signals through level conversion chip ds90lv047 and send them to the receiver. In order to receive the response signal (SerTFGserial-to-frame-grabber) sent by the camera to the acquisition card, ds90lv048 is used to convert the LVDS signal into TTL signal, which is sent to FPGA and sent to the host for display.

The system adopts 64-bit/66 MHz PCI bus to realize high-speed energy data transmission. PCI interface is the

communication interface between PCI bus and external bus to realize the communication between them. In this system, PLX9656 is used to design high-speed PCI card to realize the functions of setting camera parameters, setting laser ranging parameters, setting sampling parameters, reading image energy data, and so on. PLX9656 is the PCI interface controller with the highest performance at present. It has the performance of 66 MHz and 64 bits at PCI end and 66 MHz and 32 bits at local end and conforms to PCIV2.2 specification. The key point of PCI interface design in this system is the setting and implementation of PLX9656 local bus working mode and energy data transmission mode. The local bus of PLX9656 can be set to three modes: M mode, C mode, and J mode. According to the characteristics of the system, C mode can be selected, and the working mode of C mode can be realized by pulling down the pins of mode1 and mode0. In C mode, the energy data transmission mode is divided into master mode operation, slave mode operation, and DMA operation. The DMA working mode can realize the fast transmission between high-level peripherals and memory without CPU intervention, so it is more suitable for the transmission of CCD camera energy data and laser rangefinder energy data. The DMA transmission mode can be realized by setting dmamode0/1 and PCICR of the internal registers of PLX9656 [13].

### 3.3. FPGA Core Logic Control

**3.3.1. Sensor Trigger Setting.** In this design, the working modes of the two sensors are set through the host terminal, the mode setting string is transmitted to the FPGA through the PCI bus, and the communication with the camera and the laser rangefinder is realized through the serial port controller, so as to complete the configuration of the camera and the laser rangefinder. After the camera and the laser rangefinder receive the configuration command, the response information is also transmitted to the FPGA through the serial port controller and then transmitted to the host through the PCI bus. In order to realize the synchronous control with the laser rangefinder, the camera selects the software external trigger mode. In this mode, an EXSYNC trigger signal with a frequency of 20 Hz needs to be generated in the FPGA and sent to the CCD camera for exposure reading energy data. The low-level width of EXSYNC is 10  $\mu$ s, and the exposure time of the camera is set by the host terminal.

**3.3.2. Energy Data Synchronization Control.** The EXSYNC trigger signal is sent to the laser rangefinder and camera at the same time to realize the output synchronization of the two sensors. Because the measurement speeds of the two sensors are different, the output frame rate of the camera is 20 frames/s, and the output frequency of the laser rangefinder is 50 Hz, so the key to the design of data synchronization is how to record the single frame image data and the laser rangefinder data at the same time. The timing diagram of the synchronous acquisition of the two sensors is shown in Figure 2(a). Clk100 Hz is the least common multiple of

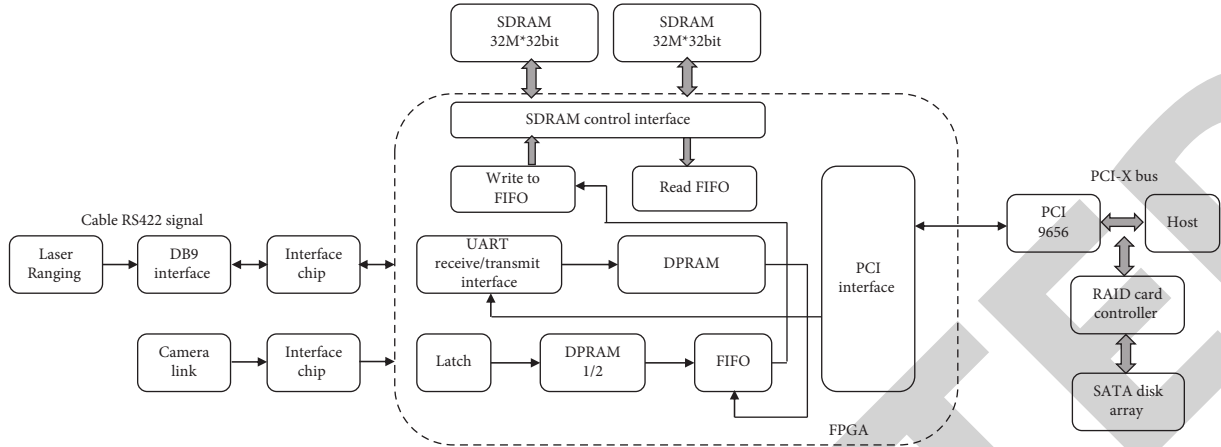


FIGURE 1: Design scheme block diagram of real-time energy data acquisition and storage system.

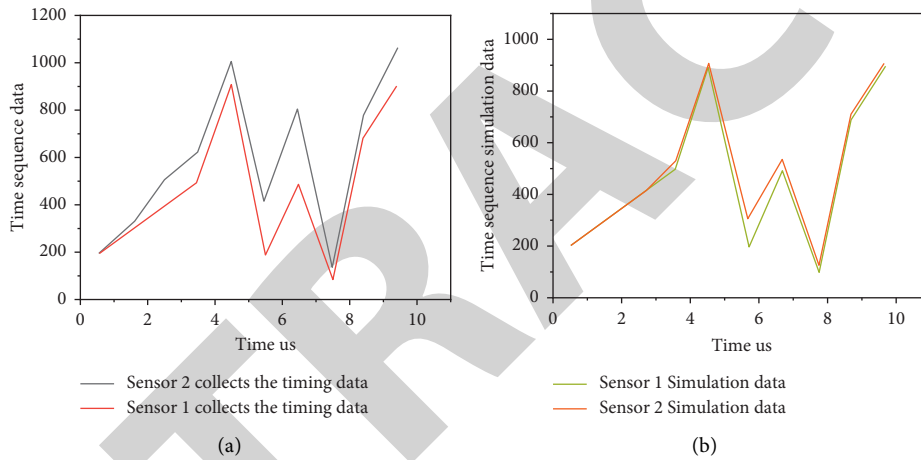


FIGURE 2: Synchronous acquisition design and simulation sequence diagram of CCD camera and laser rangefinder. (a) Collect energy data. (b) Simulation energy data.

two frequencies, which can be set according to the internal resource usage of FPGA. energy data\_lrf\_sel is the selected laser energy data, where  $I$  indicates that the energy data at this time is invalid, and  $V$  indicates that the energy data at this time is valid [14]. The energy data synchronization scheme is that after the camera energy data enters the FPGA, it is sorted and cached in two dual-port RAM, and the laser rangefinder sends the energy data into the FPGA through the serial port receiver. The serial port receiver of this design has FIFO cache, and the energy data is sent to the dual-port RAM for further cache after caching. The write enable  $Wen$  signal of the dual-port RAM is generated according to the timing diagram shown in Figure 2(a), and the laser energy data is written at this time into the dual-port RAM when the  $Wen$  signal is valid. When the read enable signal is valid, first the laser rangefinder energy data in the dual-port RAM is read into FIFO, and then the image energy data of the corresponding frame is read into FIFO. After the FIFO is half full, the laser rangefinder energy data and camera energy data are sent to the external SDRAM for further caching. The

simulation sequence diagram is shown in Figure 2(b) [15]. According to the simulation results in Figure 2, the synchronization design scheme in this paper can effectively reduce the delay between the two sensors and collect the relative synchronization energy data of the two sensors. Although it is not strictly synchronous, it can meet the requirements of the flexible baseline measurement system.

**3.3.3. Energy Data Caching and Collation.** The caching scheme adopted in this system is to firstly latch the image energy data and control signal at three levels, because the image energy data output by the experimental camera is the energy data of two taps, and the energy data of the two taps are, respectively, sent to the two dual-port RAM inside the FPGA for caching. The energy data of the left tap is stored according to the sequential address, and the energy data of the right tap is stored according to the reverse address, so as to splice the energy data of the two taps into a complete image. When the enable signal is valid, the data of the two dual-port RAM is sent to FIFO for further caching. When

the FIFO data is half full, the FIFO data is sent to the external SDRAM memory through the SDRAM interface controller.

**3.3.4. PCI Logical Interface.** The system completes the communication between FPGA and PLX9656 through PCI local logic interface. After the system is powered on, the internal register of PLX9656 is reset by the RST. At the same time, PLX9656 outputs local reset signal LRESET and checks whether EEPROM exists [16]. If the local DMA mode is used for control, the whole handshake process is as follows: First, when the energy data in the SDRAM cache reaches the set value, the signal is valid, and the PLX9656 sends an interrupt request signal to the host. If the CPU responds to the interrupt, it will issue the DMA read command, the number of bytes to be read, and the address information in the corresponding program of the interrupt. PLX9656 applies for the local bus to make the LHOLD signal valid. Once again, the FPGA effective ready signal is enabled, and the SDRAM control interface read enable effective signal is enabled, and the energy data begins to appear on the LD energy data bus. When the last byte of energy data starts to be transmitted, the PLX9656 drives the blast signal to be valid, and the FPGA has no ready signal [17]. Finally, the SDRAM read enable signal is made invalid, PLX9656 drives LHOLD to be invalid, the local bus is released, and then FPGA also drives LHOLDA to be invalid, ending the primary energy data transmission. The design of DMA transmission is shown in Figure 3.

**3.4. Cache Design and Real-Time Cache Design.** Because the internal cache capacity of PCI interface chip is too small, the cache must be used to cache the energy data in the process of real-time collection and then sent to the host through PCI bus to improve the transmission speed and performance of the system [18]. Large-capacity and high-speed SDRAM is easy to buy and the price is moderate. The system uses SDRAM for caching. Windows is a multithreaded and preemptive operating system. In order to reduce the interruption of threads due to the end of CPU occupation time, the interruption interval should be greater than the maximum thread execution time of 20 ms, so the cache capacity should be at least  $20 \text{ ms} \times 70 \text{ MB/s} \times 2 = 2.8 \text{ MB}$ . The caching scheme adopted by the system is to connect 2 groups of 32 m \* 32-bit SDRAM to FPGA, which is configured by 4 pieces of SDRAM, and is used for energy data buffering from camera to PCI. The SDRAM is encapsulated into the FIFO interface through the controller, the camera energy data is written into the FIFO, the interrupt is sent to PCI according to the set number of images, and then the camera energy data is read by PCI, thus overcoming the shortcomings of complex SDRAM structure and difficult switching control circuit [19, 20].

Real-time streaming disk has always been the biggest bottleneck of high-speed energy data acquisition technology, which directly restricts the real-time storage capacity of acquisition and storage devices [21]. The system adopts PCI-X bus motherboard supporting 66 MHz, 100 MHz, and 133 MHz/64 bits. It consists of 8 high-speed SATA hard

disks with a capacity of 1 TB, which are configured into raid0 mode through raid card to maximize disk access rate and form a high-speed and large capacity storage device. The design block diagram of the entire digital camera energy data acquisition and storage device is shown in Figure 4. The system uses the interface chip PLX9656 to send the energy data output from the real-time acquisition module to the system memory through the PCI bus and then writes the energy data in the memory into the SATA hard disk array through the PCI bus under the control of the raid card. The theoretical continuous disk writing speed can reach more than 400 MB/s [22].

## 4. Result Analysis

In the experiment, the function and performance of the system are tested, respectively. Performance test mainly includes real-time acquisition and recording speed test, continuous disk array writing speed test, and stability test. For the function test of the system, the simulation image and the actual image energy data acquisition test are carried out, respectively. The analog image is the energy data with regular circulation generated in FPGA, and the corresponding image is the stripe image. The function of the acquisition system is verified according to whether the collected energy data is correct. Then switch to the actual energy data source and collect the moving image of the cooperative target. The test results of simulated and measured image energy data show that the system can collect and store energy data correctly without image dislocation, which verifies the correctness of the system function.

The test method for the real-time acquisition and recording speed of the system is as follows: because the output frequency of the sensor in the system is limited, it cannot reflect the maximum acquisition and recording speed of the system. Analog images of different frequencies are generated in FPGA, real-time acquisition and disk writing are carried out through the system, and the image is played back by the upper computer software to check whether there is frame loss and dislocation. The measured results show that when the output frequency exceeds 50 Hz, if only the image is collected and not saved, the image acquisition is correct, but when the disk is saved at the same time, the image dislocation and frame loss begin to occur. There are two main reasons: One is that when the frequency is greater than 50 Hz and the amount of energy data is greater than 100 MB/s, the theoretical reading and writing speed of the external cache of the system is 133 MHz. Because the FIFO interface is made to read while writing, the transmission speed is halved, which may lead to the cache energy data not being read in time, resulting in image dislocation and loss. The other is that the read and write of the system in the host memory is a thread, which reads and writes energy data at the same time, resulting in the rate falling behind. To sum up, the acquisition and recording speed of the system can reach 100 MB/s, meeting the index requirements of 70 MB/s.

The speed test method of continuous writing disk array is to use a special hard disk read-write speed test software to write energy data of different capacities from the host

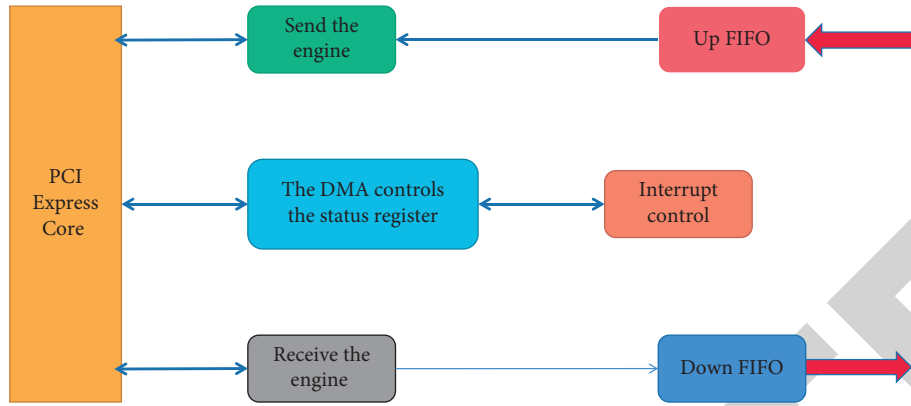


FIGURE 3: DMA transmission design.

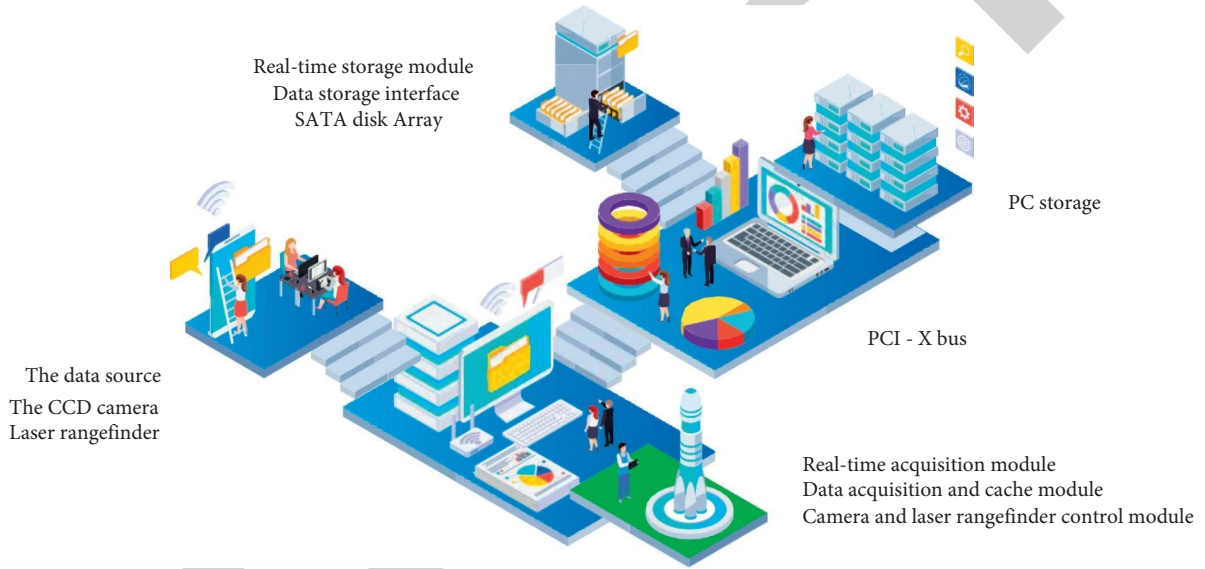


FIGURE 4: Design of real-time high-speed storage scheme.

TABLE 1: System stability test results.

Working hours (h)	2	2	4	4	6	6
Operating mode	Free running	Software external trigger	Free running	Software external trigger	Free running	Software external trigger
Frame loss rate (%)	0	0	0	0	0.03	0.01

memory to the disk array and average the speed of software statistics. The measured results show that the real-time storage speed of the system can reach more than 240 MB/s in different acquisition times, meeting the requirements of the system index of 120 MB/s. In addition, the system uses 8 1 TB SATA hard disks, with a total recording capacity of 8 TB, which meets the index requirement of 2 TB minimum recording capacity of the system.

The stability test method of the system is as follows: under different working modes, collect the energy data of two sensors for many times, verify the energy data packet header counter through the verification program, count the number of energy data lost frames, and then calculate the

frame loss rate of the system. The actual test results are shown in Table 1. It can be seen from Table 1 that, within the required working time of the system, the system has no frame loss under different modes, and the performance is very stable. Even if the working time is 3 times the required time, the maximum frame loss rate of the system is only 0.03%, which can meet the requirements of the measurement system.

### 5. Conclusion

Based on FPGA + PCI energy data acquisition and storage hardware design, this paper adopts a high-speed storage

system composed of high-performance FPGA logic devices and multiple disk arrays to realize high-speed acquisition and real-time storage of the output of the flexible measurement system. This paper introduces the working principle and key module design of this design in detail and focuses on the process of setting CCD camera and laser rangefinder with FPGA, synchronous acquisition and energy data cache, and high-speed real-time transmission through PCI special interface chip and PCI bus.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## Acknowledgments

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