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Research Article

A Nonlinear Controller for Neutral Point Piloted (T-Type) Multilevel Inverter-Based Three-Phase Four-Wire DSTATCOM

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In recent times, neutral point piloted (NPP) or half-leg T-type multilevel inverter (MLI) becomes a promising topology for medium-voltage high-power applications. This T-type MLI is the best substitute for diode clamped multilevel inverter (DCMLI) due to its simple structure and absence of clamping diodes. However, the neutral point voltage control or dc bus capacitors' balance of NPP T-type MLI is a challenging task. Therefore, this paper presents a nonlinear sliding mode controller (SMC) for dc-link voltage balance and reference current control in distribution static compensator (DSTATCOM). For this, a three-level T-type MLI-based three-phase four-wire DSTATCOM is considered to eliminate current-related power quality issues such as harmonics, reactive power, load unbalance, and neutral current. The proposed NPP T-type-based DSTATCOM is compared with DCMLI and active DCMLI-based DSTATCOMs in terms of switching losses and cost. Simulation studies are carried out in MATLAB Simulink environment and further corroborated with experimental studies. Furthermore, the ability of the proposed SMC-based controller is compared with the PI controller under different operating conditions.

1. Introduction

One of the best methods to improve the power quality is by using a distribution static compensator (DSTATCOM). DSTATCOM can eliminate current harmonics, compensate reactive power, and balance the three-phase load currents in a three-phase four-wire system. DSTATCOM is used to generate compensating currents and added with distorted current consumed by nonlinear loads, to eliminate the harmonics present in the source currents [1]. DSTATCOM can be realized with a two-level or multilevel inverter (MLI); however, a two-level inverter-based DSTATCOM requires a large filter size and is unsuitable for medium-voltage applications. Therefore, MLIs are suitable due to their advantages like low THD, high efficiency, and reduced electromagnetic interference (EMI) compared with a two-level inverter [2]. However, switching losses are a major factor in an MLI-based DSTATCOM.

To reduce power loss in the inverter, circuits with reduced power electronic components are preferred [3]. Among those reduced power electronic component-based topologies, T-type inverters also known as neutral point piloted (NPP) inverters are popular. T-type inverters have lower conduction losses at medium switching frequency ranges. Power loss is a combination of switching losses and conduction losses. Switching losses depends on switching frequency and conduction losses mainly depend on modulation index and power factor, but the advantage of the T-type inverter has a small conducting path and less number of switches and no clamping diodes; these all effects reduce the power loss when compared with two-level VSI [4]. Si IGBTs are replaced with SiC MOSFETs in T-type inverters because of the low switching loss of MOSFET which will improve the efficiency and power density [5]. Extended T-type construction is used in boost converter to improve the efficiency of the inverter circuit, in general, T-type inverters have step-down voltage performance, the output of T-type inverter is connected to boost converter to improve grid peak to peak voltage, and diodes are replaced with SiC MOSFET to get bidirectional output. Mainly T-type is used to connect low

voltage sources to a three-phase grid having a lower number of passive components [6]. Based on the histogram pattern method used to detect the faults in T-type inverters for grid-connected systems because of low computational problems, based on inverter output voltage pattern analysis, an open switch fault will be diagnosed. Here, the algorithm is used at pattern mass centers to detect the inverter output; to implement this algorithm inverter voltage does not depend on load parameters; this easily identifies the open switch faults in T-type [7]. T-type is preferred over diode clamped voltage source inverter for reducing the converter's switching losses and thus makes the converter best suitable for high switching frequency applications as compared to diode versions. It can be able to balance the neutral point voltage and reduce the leakage current to a minimal level. These arrangements are able to produce better stabilized during load disturbance conditions with low total harmonic distortion. They are better suitable for sudden load variant applications, which reduce the voltage stress and allow for the implementation of higher efficiency power switches on the dc side [8].

To control the inverter, multiple controllers are present [9, 10] in this particular paper focusing on the conventional PI controller and sliding mode controller (SMC). In a three-phase four-wire system, a neutral point current analysis is very important for a three-level T-type inverter [11]; if the neutral current is not balanced which will affect the neutral potential, indirectly supply current may have an effect, here by using nonlinear sliding mode controller neutral current compensation provided. There are two major benefits of SMC. The first one is improvement in the dynamic performance of the system by the precise selection of sliding function. Secondly, the response of the system becomes entirely unaffected by specific uncertainties. This principle ranges to system parameter uncertainties, nonlinearity, and disturbance which are bounded. From a real-time point of view, SMC permits for control of nonlinear closed-loop systems under exterior disturbances and heavy system uncertainties. In general, in SMC, the Lyapunov stability method is applied to keep the nonlinear system under control [12]. Generally, SMC is used to generate reference magnitudes of supply currents as proposed in [13]; however, in this paper, an SMC is proposed to control the unbalance in dc voltage of a three-level NPP-based DSTATCOM.

This paper focuses on different types of controllers like PI controller and SM controller for T-type and diode clamped inverters having three-phase four-wire arrangements. Section 2 explains three-phase four-wire DSTATCOM with T-type topology, Section 3 gives comparisons of NPC, ANPC, and NPP (T-type) in terms of efficiency and power loss, Section 4 discusses reference current generation with PI and SM controllers, and Sections 4 and 5 discuss the simulation and experimental results.

2. A Three-Level Neutral Point Piloted Inverter-Based DSTATCOM

The neutral point piloted (NPP) or Mixed Voltage Neutral Point clamped (MNPC) or T-type topology-based three-phase four-wire (3P4W) DSTATCOM is shown in Figure 1 [14, 15]. The DSTATCOM is connected at the point of common coupling (PCC). It consists of a conventional half-bridge with a bidirectional switch which clamps the output to the DC middle point, respectively, ground to achieve zero voltage. Discrete semiconductor devices are incorporated to construct a switch with bidirectional voltage blocking and current-conducting capability or a reverse blocking insulated gate bipolar transistor (RBIGBT) is used [14]. Compared to the other topologies, the lowest number of semiconductors is required. The designation Mixed Voltage NPC illustrates that the used semiconductors must be rated for two different blocking voltages.

The outer devices (S_{1a} and S_{2a}) have to block the full dc-link voltage (V_{dc}) while the inner devices (S_{2c} and S_{1b}) have to block only half of the dc-link voltage. A phase-leg of a three-level NPP consists of only 8 semiconductors: 4 IGBTs ($S_{1a} - S_{2a}$) and 4 antiparallel free-wheeling diodes ($D_{1a} - D_{2a}$). Similar to three-level NPC, the NPP is connected to the split dc-link at DC+, N, and DC−. The midpoint of S_1 and S_4 provides the AC output. The three switching states of this inverter are given in Table 1. This topological configuration produces lower conduction losses and blocking voltages compared to DCMLI and ANPC. This topology is reported for various PV and grid-connected applications [15]. Fault-tolerant strategies and reconfiguration of this inverter for OC switch faults are also reported in [15]. This topology does not possess switching redundancies, operates with unequal device blocking voltages, does not facilitate uniform power distribution, and mandatorily requires dc voltage ratios to be symmetrical. However, the charge balance among the dc-link voltages can be obtained by equalizing the rate of charge over a fundamental cycle [16] or by involving modulation techniques such as space vector modulation (SVM).

3. Power Loss Calculation in Three-Level Neutral Point Piloted Inverter

During the active state (P and N) outer IGBTs S_{1a} or S_{2a} will carry the current, whereas the current passes through inner IGBTs S_a' and S_a" during the zero state. The outer switches S_{1a} and S_{2a} commutate in hard switching conditions. The turn-off losses during a passage from a zero state to an active state must be considered, but the turn-on losses at the beginning of a zero state can be neglected, as well as the low-frequency switching losses of the inner IGBTs. All the above considerations yield the total power loss over a grid voltage period. The power losses of the eight semiconductors in 3-level ANPC topology are different from those of 3-level NPC and can be calculated as follows:

$$P_{\text{cond}} = V_{ce} * I_{\text{avg}} + R_{ce} * I_{\text{RMS}}^2. \quad (1)$$

When S_{1a} or S_{2a} in conduction,

$$I_{\text{avg}} = \frac{1}{2 * \pi} * \int_{\varphi}^{\pi} \left(I_m \sin(\omega t - \varphi) * M \sin(\omega t)\right) * \mathrm{d}\omega t, \quad (2)$$

$$I_{\text{RMS}} = \sqrt{\frac{1}{2\pi} \int_{\varphi}^{\pi} \left(I_m \sin(\omega t - \varphi)\right)^2 * M \sin(\omega t) * \mathrm{d}\omega t}. \quad (3)$$

Integrating equation (2) and equation (3) and substituting in equation (1), we get equation (4):

$$P_{\text{cond}} = \frac{MI}{12\pi}\left(3 * V_{ce} * [(\pi - \varphi) * \cos\varphi + \sin\varphi] + 2 * R_{ce} * I * [1 + \cos\varphi]^2\right), \tag{4}$$

$$P_{sw} = F_{sw} * \left(E_{\text{on}} + E_{\text{off}}\right) * \frac{I}{I_{\text{ref}}} * \frac{V_{cc}}{V_{\text{ref}}} * \left\{\frac{1}{2\pi}(1 + \cos\varphi)^2\right\}. \tag{5}$$

When S_a in conduction,

$$I_{\text{avg}} = \frac{1}{2 * \pi} * \left[\int_{\varphi}^{\pi}\left(I_m \sin(\omega t - \varphi)\mathrm{d}\omega t\right) + \int_{\pi}^{\pi+\varphi}\left(\left(I_m \sin(\omega t - \varphi)\right) * (1 + M\sin(\omega t))\right) * \mathrm{d}\omega t\right], \tag{6}$$

$$I_{\text{RMS}} = \sqrt{\frac{1}{2\pi}\left[\int_{\varphi}^{\pi}\left(I_m \sin(\omega t - \varphi)\right)^2 * \mathrm{d}\omega t + \int_{\pi}^{\pi+\varphi}\left(\left(I_m \sin(\omega t - \varphi)\right)^2 * (1 + M\ \sin(\omega t)) * \mathrm{d}\omega t\right]}. \tag{7}$$

Integrating equation (6) and equation (7) and substituting in equation (1), we get equation (8):

$$P_{\text{cond}} = \frac{I}{12\pi}\left\{V_f\left[12 + 6M(\varphi\cos\varphi - \sin\varphi) - 3M\pi\cos\varphi\right] + R_{ce}I\left[3\pi - 4M\left[1 + \cos\varphi^2\right)\right]\right\}, \tag{8}$$

$$P_{sw} = F_{sw} * \left(E_{\text{on}} + E_{\text{off}}\right) * \frac{I}{I_{\text{ref}}} * \frac{V_{cc}}{V_{\text{ref}}} * \left\{\frac{1}{2\pi}\{(1 - \cos\varphi)\}\right\}. \tag{9}$$

When D_a in conduction,

$$I_{\text{avg}} = \frac{1}{2 * \pi}\left[\int_{\varphi}^{\pi}\left(I_m \sin(\omega t - \varphi)(1 - M\sin(\omega t))\mathrm{d}\omega t\right) + \int_{\pi}^{\pi+\varphi}\left(\left(I_m \sin(\omega t - \varphi)\right)(1 + M\sin(\omega t))\right)\mathrm{d}\omega t\right], \tag{10}$$

$$I_{\text{RMS}} = \sqrt{\frac{1}{2\pi}\left[\int_{\varphi}^{\pi}\left(I_m \sin(\omega t - \varphi)\right)^2(1 - M\sin(\omega t))\mathrm{d}\omega t + \int_{\pi}^{\pi+\varphi}\left(\left(I_m \sin(\omega t - \varphi)\right)^2(1 + M\sin(\omega t))\right)\mathrm{d}\omega t\right]}. \tag{11}$$

Integrating equation (10) and equation (11) and substituting in equation (1), then, equation (12) is obtained:

$$P_{\text{cond}} = \frac{I}{12\pi}\left\{V_f\left[12 + 3M(2\varphi\cos\varphi - 2\sin\varphi) - 3M\pi\cos\varphi\right] + R_f I\left[3\pi - 4M\left[1 + \cos\varphi^2\right)\right]\right\}, \tag{12}$$

$$P_{sw} = F_{sw} * E_{\text{rec}} * \frac{(0.45I + 0.55)}{I_{\text{ref}}} * \frac{V_f}{V_{\text{ref}}} * \left\{\frac{1}{2\pi}\{(1 + \cos\ \varphi)\}\right\}. \tag{13}$$

When D_{1a} and D_{2a} in conduction,

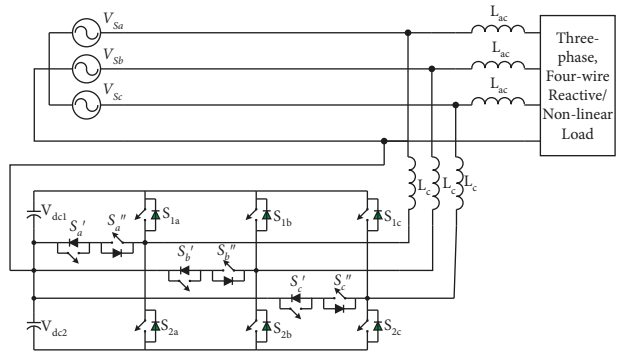
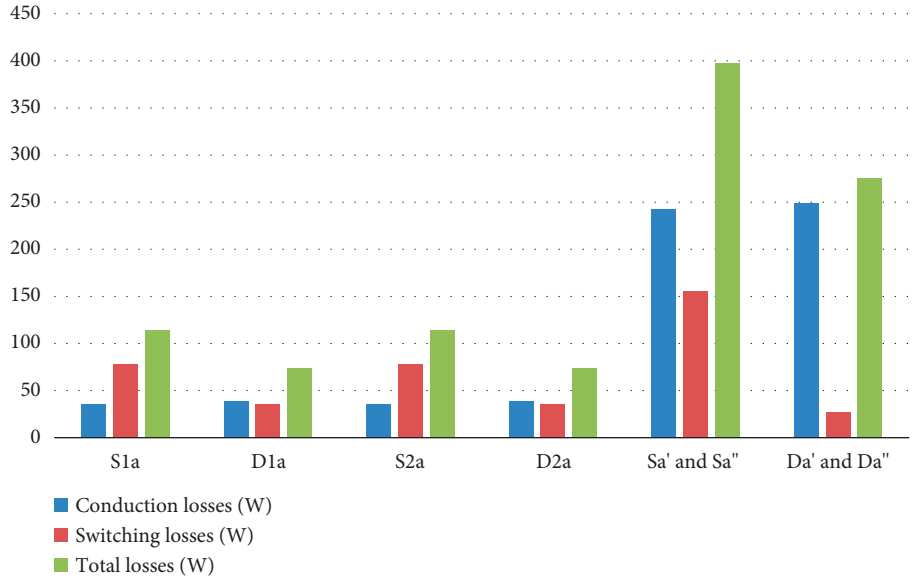


Figure 1: A three-phase four-wire three-level neutral point piloted-based DSTATCOM.

Table 1: Switching sequence of 3L-NPP.

Generation of level	Switching state	S_{1a}	S_a'	S_a"	S_{2a}	Output voltage
$+V_{dc}/2$	P	On	Off	On	Off	+1
0	O	Off	On	On	Off	0
$-V_{dc}/2$	N	Off	On	Off	On	−1

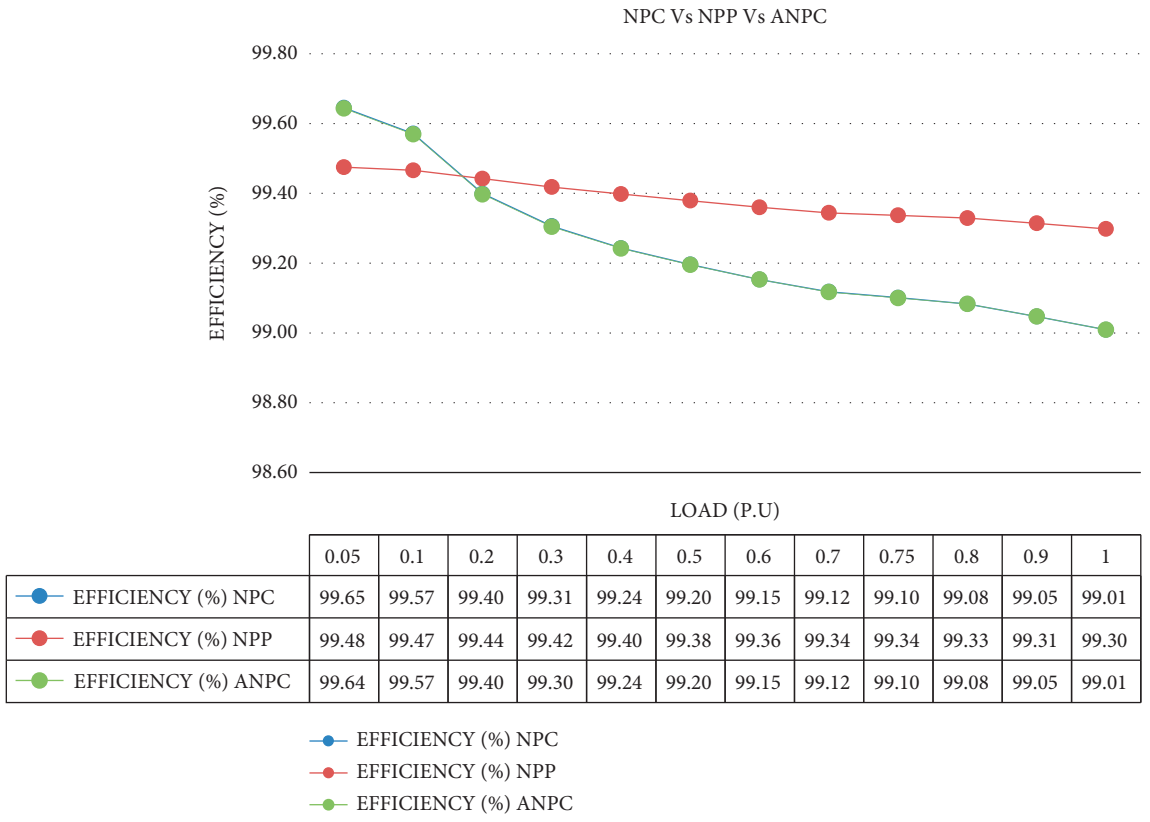


Devices	S_{1a}	D_{1a}	S_{2a}	D_{2a}	S_a' and S_a"	D_a' and D_a"
Conduction losses (W)	36	39	36	39	243	249
Switching losses (W)	78	35	78	35	155	27
Total losses (W)	114	74	114	74	398	276

Figure 2: Power losses of different switches in three-level NPP T-type MLI.

Table 2: Parameters used for simulation study of 3P4W NPP T-type DSTATCOM.

Parameters	Values
AC line voltage	Three-phase, four-wire, 415 V, 50 Hz
Line impedance	$Rs = 0.01\ \Omega$, $Ls = 1$ mH
DC bus voltage of 3P4W DSTATCOM	350 V (for each capacitor)
DC bus capacitance of 3P4W DSTATCOM	2200 μF (for each capacitor in the H-bridge cell)
DSTATCOM coupling inductor	$Lc = 4.8$ mH
PWM switching frequency for 3P4W DSTATCOM (f_{cr})	5 kHz
Load	Three-phase controlled rectifier, $R_{dc} = 30\ \Omega$, $L_{dc} = 10$ mH, firing angle = 20°, commutation inductance = 1.5 mH; single-phase universal rectifier connected between the b–phase and the neutral, $R_{dc} = 5\ \Omega$, $L_{dc} = 50$ mH, commutation inductance = 1.5 mH; single-phase universal diode rectifier connected between the c phase and the neutral, $R_{dc} = 5\ \Omega$, $L_{dc} = 50$ mH, commutation inductance = 1.5 mH
Sampling time	$T_s = 5e{-}6$ s.



	0.05	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.75	0.8	0.9	1
EFFICIENCY (%) NPC	99.65	99.57	99.40	99.31	99.24	99.20	99.15	99.12	99.10	99.08	99.05	99.01
EFFICIENCY (%) NPP	99.48	99.47	99.44	99.42	99.40	99.38	99.36	99.34	99.34	99.33	99.31	99.30
EFFICIENCY (%) ANPC	99.64	99.57	99.40	99.30	99.24	99.20	99.15	99.12	99.10	99.08	99.05	99.01

Figure 3: Power losses of different switches in three-level NPP T-type MLI under different loading conditions.

$$I_{\text{avg}} = \frac{1}{2 * \pi} * \left[\int_0^{\varphi} \left(I_m \sin(\omega t - \varphi) * M \sin(\omega t) \right) * \mathrm{d}\omega t \right], \tag{14}$$

$$I_{\text{RMS}} = \sqrt{\frac{1}{2\pi} \left[\int_0^{\varphi} \left(I_m \sin(\omega t - \varphi) \right)^2 * M \sin(\omega t) * \mathrm{d}\omega t \right]}. \tag{15}$$

Integrating equation (14) and equation (15) and substituting in equation (1), then we get equation (16):

$$P_{\text{cond}} = \frac{M * I}{12\pi} \left\{ 3 * V_f * [-\varphi * \cos\varphi + \sin\varphi] + 2 * R_f * I * [1 - \cos\varphi]^2 \right\}, \tag{16}$$

$$P_{sw} = F_{sw} * E_{\text{rec}} * \frac{(0.45I + 0.55)}{I_{\text{ref}}} * \frac{V_f}{V_{\text{ref}}} * \left\{ \frac{1}{2\pi} \{(1 - \cos\ \varphi)\} \right\}. \tag{17}$$

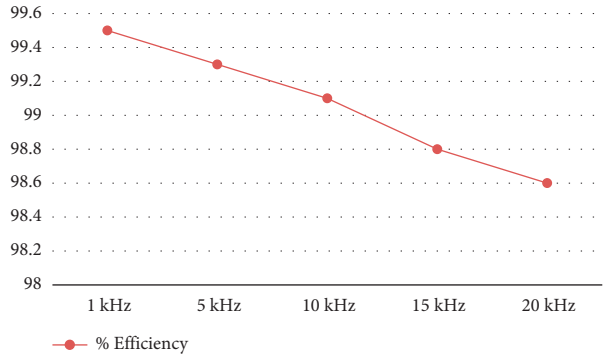


Figure 4: The efficiency of NPP with change in PWM switching frequency.

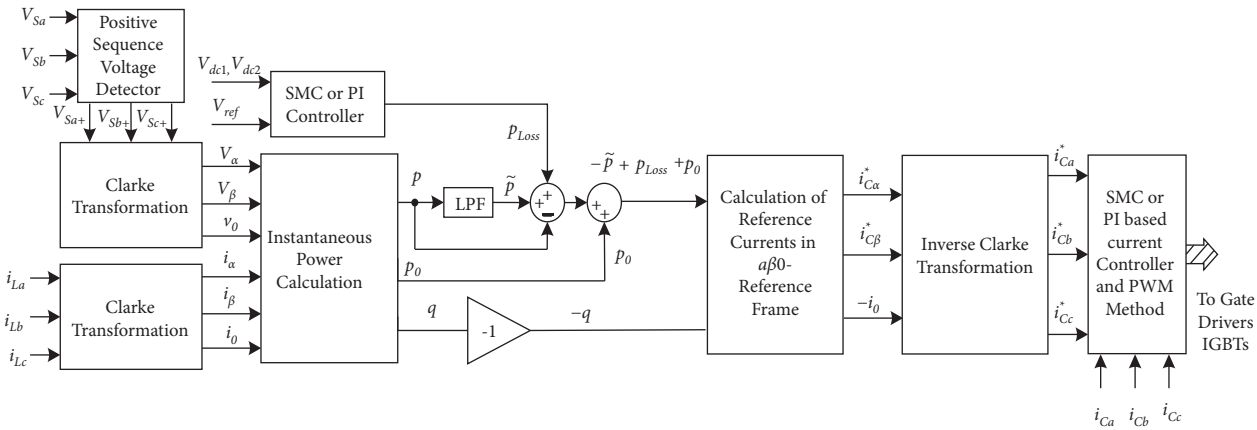


Figure 5: Sliding mode controller with *pq* theory.

3.1. Losses Comparison. In this section, a loss comparison between the NPP topology NPC and ANPC has been done, and NPP has less losses compared to the other two topologies. The following section gives the information for conduction and switching and total losses for NPP, NPC, and ANPC.

Figure 2 depicts the conduction and switching losses in each IGBT and its antiparallel diode in the NPP inverter. For the calculation of the losses, a neutral point piloted (T-type) multilevel inverter is simulated in the MATLAB/SIMULINK environment with the PLECS toolbox. For NPP Topology Fuji, 1MBI2400VAC-120P and 2MBI1800XXF170-50 modules are used. The load conditions are given in Table 2 of the revised manuscript. In the case of NPC topology, the losses across the inner switches S_a' and S_a" are more compared to outer switches in the compensator mode of operation. The antiparallel diodes across S_a' and S_a" are denoted with D_a' and D_a". In the case of NPP topology, the losses across inner switches S_a' and S_a" are more compared to outer switches in the compensator mode of operation.

3.2. Efficiency Comparison. In this section, an efficiency comparison between the NPP topology NPC and ANPC has been done, with NPP having good efficiency compared to the other two topologies. The following section gives the information on efficiencies between NPP, NPC, and ANPC.

The efficiency comparison between the NPC, NPP, and ANPC topologies with respect to different loading conditions is shown in Figure 3. The efficiency of NPC and ANPC is the same. The efficiency of NPP topology is higher than NPC and ANPC. The efficiency of NPP with change in switching frequency is shown in Figure 4. As the switching frequency increases, a slight reduction in efficiency is observed.

4. A Sliding Mode Controller for DSTATCOM

4.1. Sliding Mode Controller. Here, reference signals and DSTATCOM currents are given as inputs of the error detector; the detector output connected to the sliding mode controller based on the difference value reference signals will generate to turn on the IGBT of the inverter circuit. SMC is used in the current control loop to get a fast approach [17]; it is also used to minimize supply current harmonics by controlling power factor under constant switching frequency of operation; under system parameters variations, also it will give good performance [18]. This is also helpful to decrease phase-shifting problems at broad bandwidth, but high-frequency switching application switches may have a drawback of SMC which is chattering noise; this can be

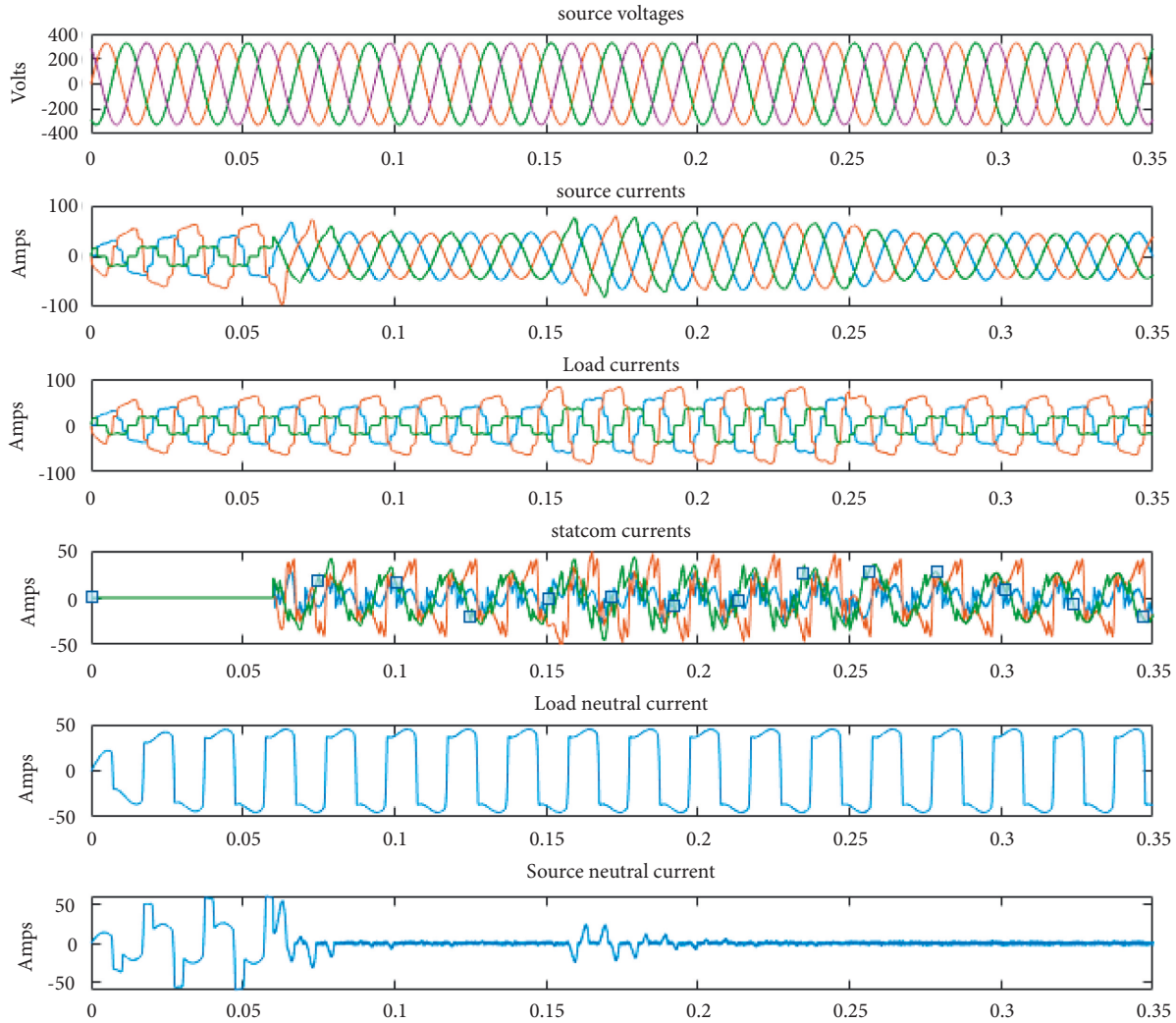


Figure 6: Performance of three-level NPP-based DSTATCOM with PI controller.

overcome by placing sigmoid function instead of sign function [19]. SMC has a vital role in enhancing the power quality by decreasing THDs in source current basically used to generate reference signals for PWM inputs [20]; this controller helps to control the dc bus voltage in shunt active power filter to calculate reference currents by using self-tuning filters [21]. An adaptive sliding mode controller is used to calculate the real and reactive powers of the system, also applicable for renewable energy systems and PV systems [22]. Using sliding mode theory simple form of the control action is a relay function which is given by

$$s(x) = k.\text{sign}(s(x)),$$
$$s(x) = k.\tanh(s(x)). \tag{18}$$

To generate gating pulses, the controller plays a vital role. This particular paper focuses on two controllers named proportional and integral controller and sliding mode controller. Out of these two controllers, the sliding mode controller is having more advantages and features:

(i) Increase the system robustness

(ii) Parameter insensitivity

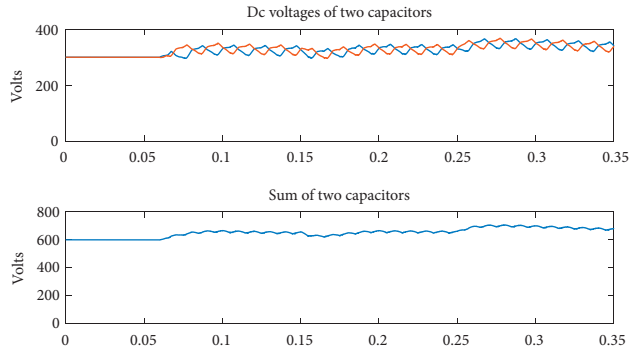
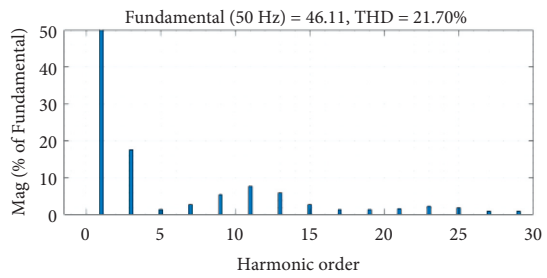


Figure 7: DC-link capacitor voltages in three-level NPP-based DSTATCOM with PI controller.

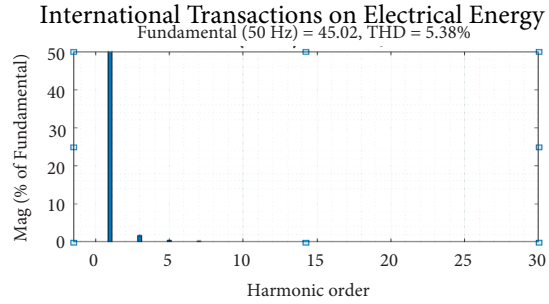
(iii) Realization simplicity

(iv) Stability under variations and external disturbance

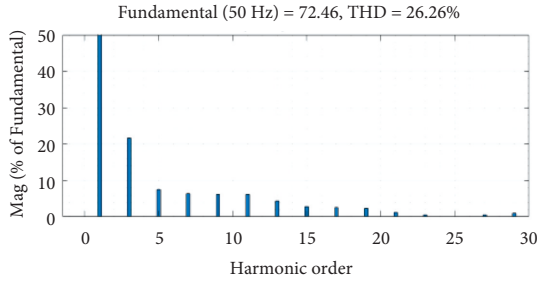
For reference current generation, the authors used Akagi's instantaneous reactive power theory (PQ theory). It works in the time domain and is applicable for three-phase



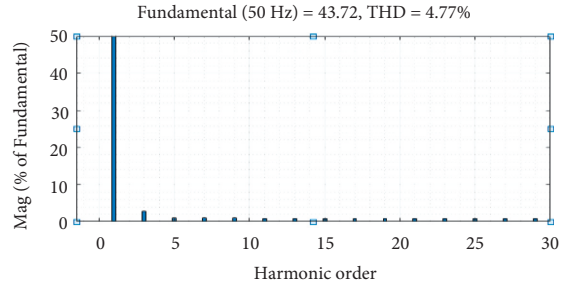
(i) phase-*a*load current harmonic spectrum



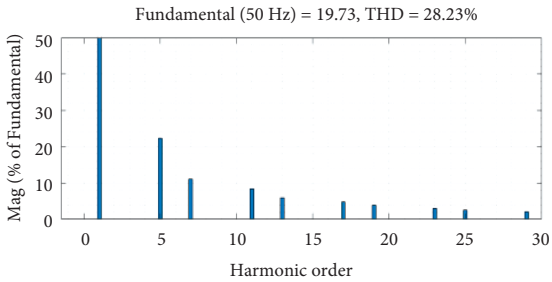
(iv) phase-*a* source current harmonic spectrum with PI controller



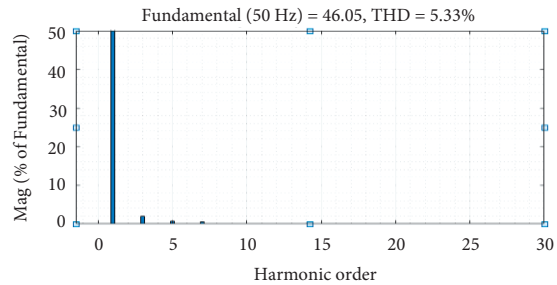
(ii) phase-*b* load current harmonic spectrum



(v) phase-*b* source current harmonic spectrum with PI controller



(iii) phase-*c* load current harmonic spectrum



(vi) phase-*c* source current harmonic spectrum with PI controller

FIGURE 8: Harmonic spectra of load currents and compensated source currents with PI controller. (a) Phase *a* load current harmonic spectrum. (b) Phase *b* load current harmonic spectrum. (c) Phase *c* load current harmonic spectrum. (d) Phase *a* source current harmonic spectrum with PI controller. (e) Phase *b* source current harmonic spectrum with the PI controller. (f) Phase *c* source current harmonic spectrum with the PI controller.

three-wire systems and three-of-phase four-wire systems and also it is effective for steady-state and transient state applications. It transforms initially abc to $\alpha\beta o$ coordinates: Clarke transformation (see Figure5).

$$\begin{bmatrix} V0 \\ V\alpha \\ V\beta \end{bmatrix} = \sqrt{\left(\frac{2}{3}\right)} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} Vsr \\ Vsy \\ Vsb \end{bmatrix}. \tag{19}$$

Next instantaneous load currents are

$$\begin{bmatrix} I0 \\ I\alpha \\ I\beta \end{bmatrix} = \sqrt{\left(\frac{2}{3}\right)} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} Ilr \\ Ily \\ Ilb \end{bmatrix}. \tag{20}$$

Instantaneous powers are P, Q, and P0. P0 is the instantaneous zero-sequence power:

$$\begin{bmatrix} P0 \\ P \\ Q \end{bmatrix} = \begin{bmatrix} V0 & 0 & 0 \\ 0 & V\alpha & V\beta \\ 0 & V\beta & -V\alpha \end{bmatrix} \begin{bmatrix} I0 \\ I\alpha \\ I\beta \end{bmatrix}. \tag{21}$$

Power in three phases can be written as

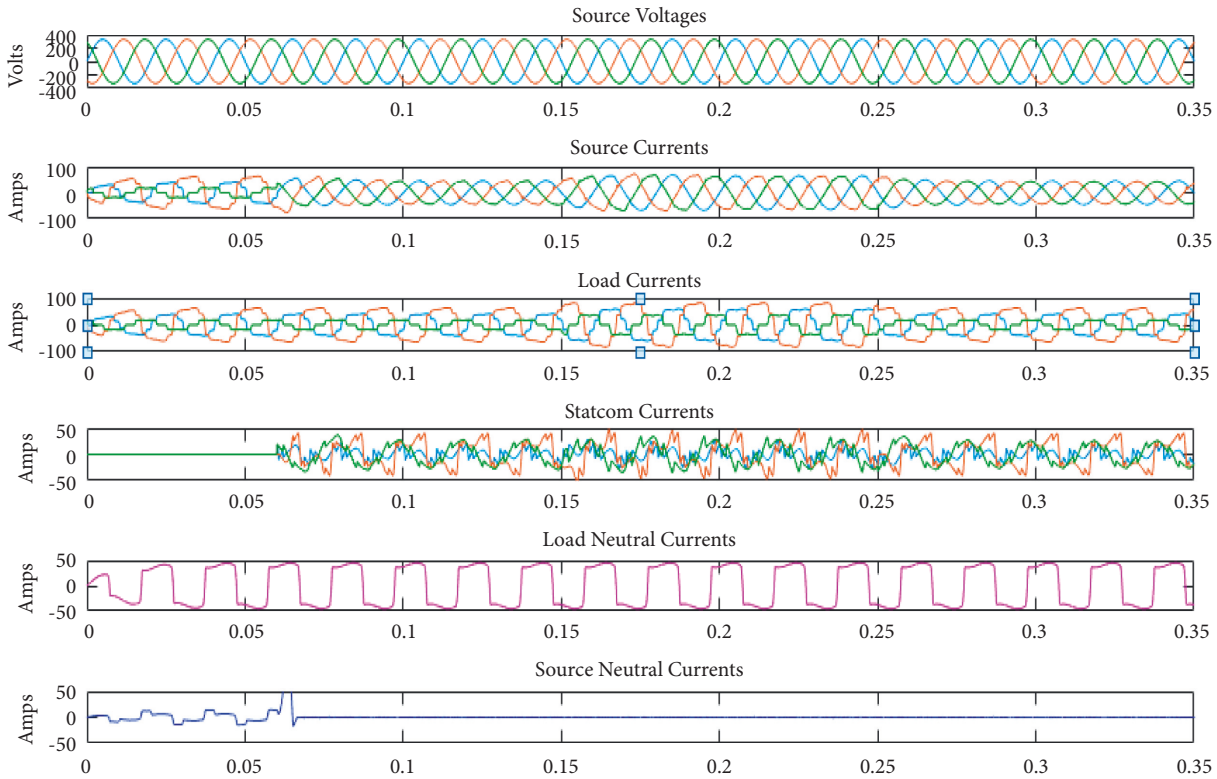


Figure 9: Performance of three-level NPP-based DSTATCOM with SMC controller.

$$P3\varnothing = V\alpha I\alpha + V\beta I\beta + V0I0 = P0 + P. \quad (22)$$

4.2. DC Capacitor Selection. The selection of capacitance depends mainly on the Unit Capacitance Constant (UCC) [23], which is the ratio between the power conversion capacity of the inverter circuit measured in watts and energy stored in the capacitor measured in joules:

$$\text{UCC} = \frac{1}{2}C_{dc}\frac{V_{dc}^2}{Q},$$

$$Q = \frac{\text{Power conversion capacity of the inverter}}{\text{Number of phase in the inverter} * \text{Number of capacitors}}. \quad (23)$$

Considering $V_{dc} = 350$ V, the number of capacitors (N) = 2 and $UCC = 35$ ms (for a ripple voltage in the range of 10%) and with a power conversion capacity of 25 kVA of the inverter C_{dc} calculated as 2400 μF.

For optimum performance of DSTATCOM, the value of reference dc voltage must be carefully selected. Since the DSTATCOM injects maximum reactive power at $V_{\text{dc}} = 2V_{\text{pcc}}$, from the power flow between DSTATCOM and PCC. However, for optimum selection of switching devices, a factor of 1.6 to 1.7 times the PCC voltage is used. In this paper, 1.7 is used. From this, for a 415 V supply, a dc link of 700 V is chosen, which will be equally shared between two capacitors. To balance the capacitor voltages, two sliding mode controllers (SMCs) are used. One SMC controls the sum of dc-link voltages to its reference value and the other SMC controls the difference of two capacitor voltages to zero. This ensures the tight control of capacitor voltages under all loading conditions.

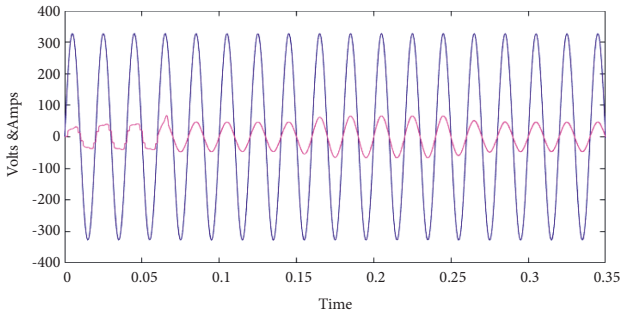


Figure 10: PCC voltage and source current of phase a.

4.3. Coupling Inductor Selection. The requirement of the coupling inductor is to filter out the harmonics produced by the converter and inverter circuits. This is the most important component to determine the performance of DSTATCOM. Inductance selection especially depends on the switching frequency of the converter and current ripple.

$$Lc = \frac{\sqrt{3}MaVc}{12af_cI_{cr}}. \quad (24)$$

To control the converter, the PWM method used switching frequency depending on this, by using Carrier frequency switching frequency calculated:

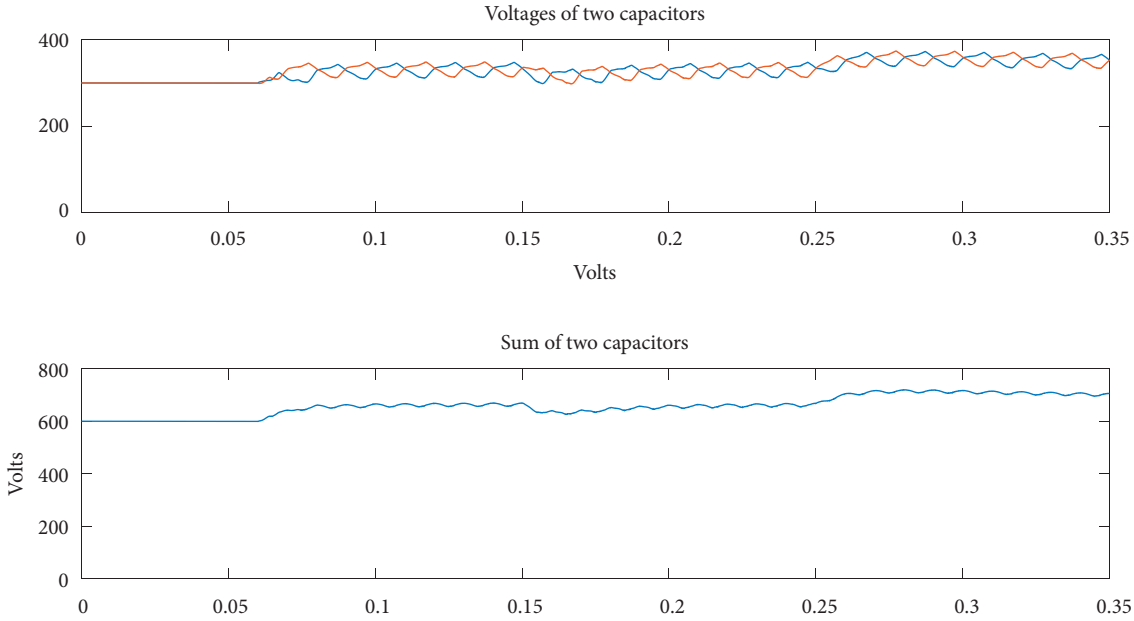
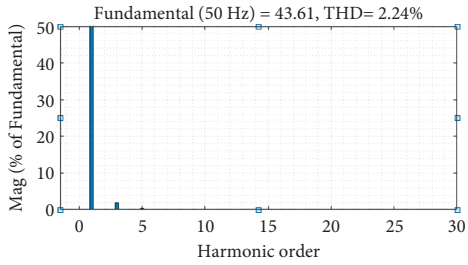
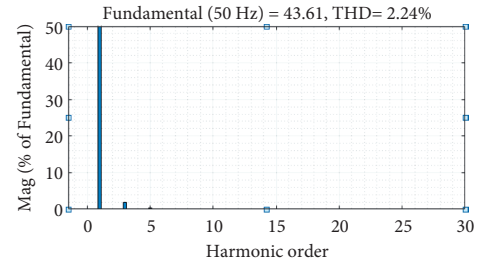


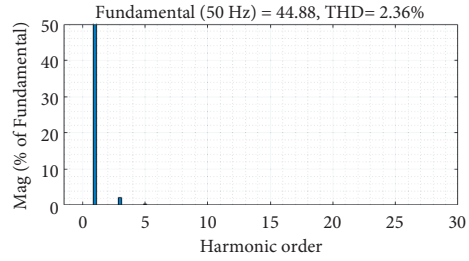
Figure 11: DC-link capacitor voltages in three-level NPP-based DSTATCOM with SMC controller.



(i) phase-*a* source current harmonic spectrum with SMC controller



(ii) phase-*b* source current harmonic spectrum with SMC controller



(iii) phase-*c* source current harmonic spectrum with SMC controller

Figure 12: Harmonic spectra of compensated source currents with the SMC controller. (a) Phase *a* source current harmonic spectrum with the SMC controller. (b) Phase *b* source current harmonic spectrum with SMC controller. (c) Phase *c* source current harmonic spectrum with the SMC controller.

$$f_c = N f_{cr}. \tag{25}$$

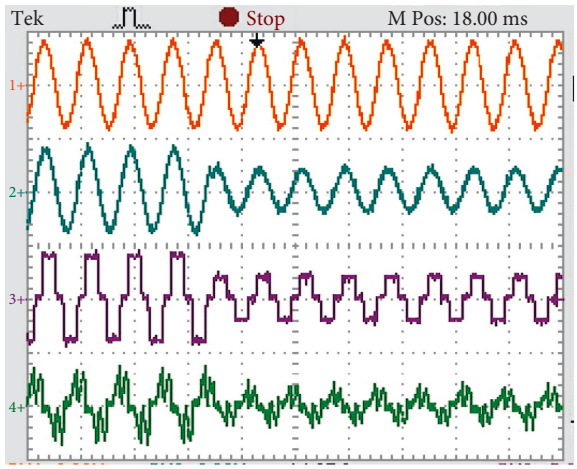
Peak to peak current ripple can be 5% of current value, i.e., 1.75 A·rms, switching frequency is 10 kHz, phase to neutral voltage is 700, overload factor "*a*" is 1.2, and then the calculated inductance is 4.8 mH.

5. Simulation Results of NPP-Based DSTATCOM with PI and SMC

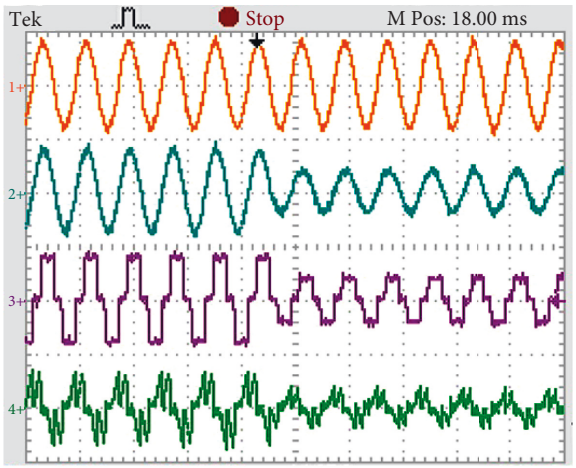
The simulation waveforms of 3P4W NPP along with load and source harmonic spectra with unbalanced nonlinear loads below waveforms explain source voltages, source phase

Table 3: The performance of DSTATCOM under different loading conditions.

Load (%)	Load power factor	Load side currents (rms, A)			Load side (%) THD			Source power factor	Source side currents (rms, A)			Source side (%) THD		
		I_{la}	I_{lb}	I_{lc}	a phase	b phase	c phase		I_{sa}	I_{sb}	I_{sc}	a phase	b phase	c phase
100	0.8 lagging	40	60	20	21.7	26.26	28.23	Unity	45	45	43	2.28	2.5	3.02
	0.5 lagging	30	50	10	27.7	31.27	29.03	Unity	36	37	37.5	2.93	3.8	4.15
	0.3 lagging	22	48	8	31.85	33.86	29.43	Unity	33	34	35	3.41	5.2	4.75
60	0.8 lagging	25	37	13	22.3	28.62	29.28	Unity	26	25	25	3.13	3.7	4.01
	0.5 lagging	20	32	10	27.7	31.27	30.67	Unity	20	21	22	3.79	4.5	4.53
	0.3 lagging	18	29	8	32.58	35.80	29.56	Unity	17	18	17	4.40	5.4	6.15
30	0.8 lagging	13	19	8	23.9	26.26	28.23	Unity	14	12	14	3.43	3.9	4.02
	0.5 lagging	11	17	6	29.2	33.26	31.30	Unity	11	10	11	3.99	4.8	4.65
	0.3 lagging	9	14	5	34.82	39.23	34.43	Unity	9	8	9	4.46	5.8	6.35

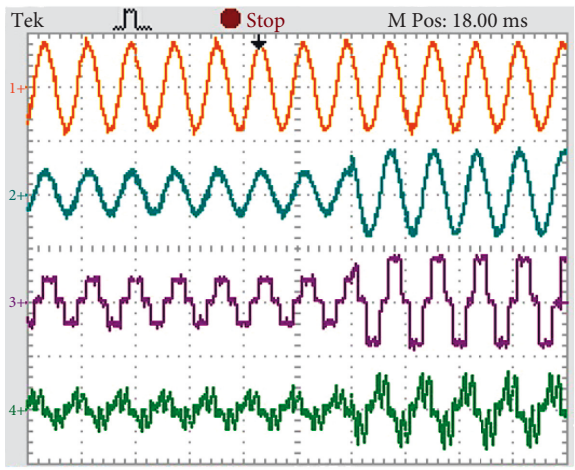


(a.1) With PI

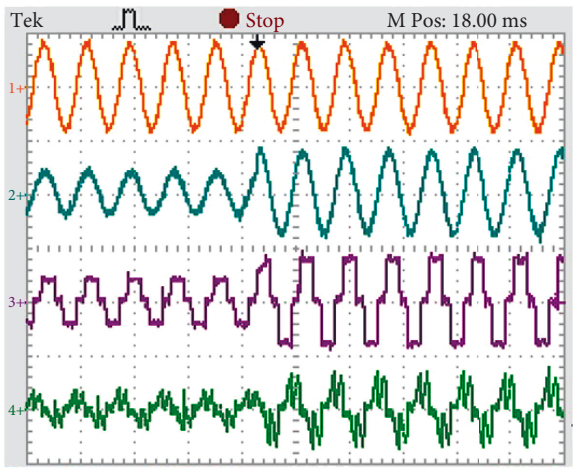


(a.2) With SMC

(a)



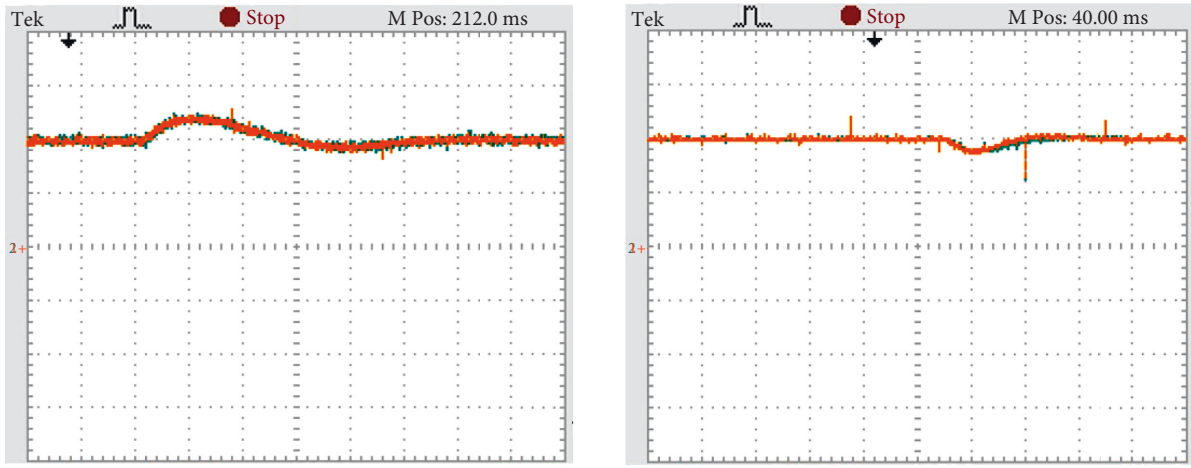
(b.1) With PI



(b.2) With SMC

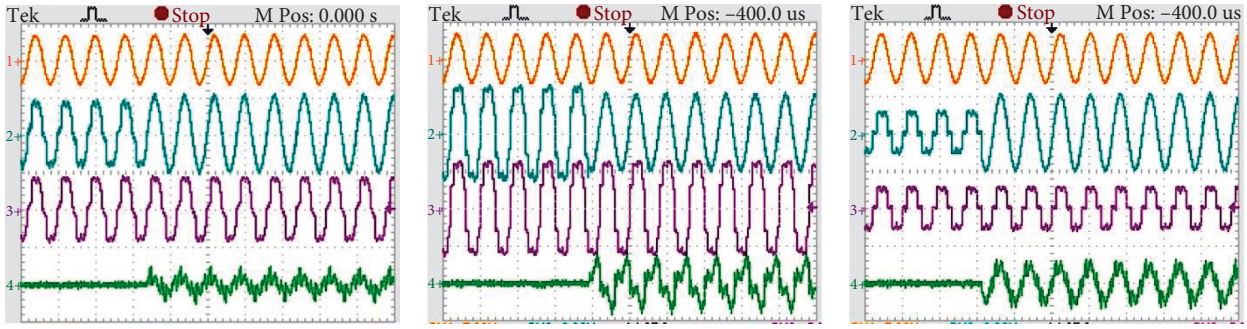
(b)

Figure 13: The performance of DSTATCOM for an RL-load on the dc side of a phase-controlled rectifier with PI and SMC. (a) with a 50% reduction in load current. (b) With a 50% increase in load current.



(a) (b)

Figure 14: Experimental results of capacitor voltages of NPP-based DSTATCOM. (a) with PI. (b) with SMC.



(a) (b) (c)

Figure 15: Switching-in response of SMC-based 3P4W DSTATCOM. (a) phase a waveforms, (b) phase b waveforms, and (c) phase c waveforms.

currents, three-phase load currents, filter currents, load neutral currents, and source neutral currents. In order to study the performance of 3P4W NPP T-type MLI-based DSTATCOM, the following things are (see Figure 6) considered for simulation studies.

(i) Before the start of simulation studies, the circuit breaker is open at that point; DSTATCOM is not connected to the system

(ii) At $t = 0.06$ s, the breaker is closed and 3P4W DSTATCOM is connected to the system

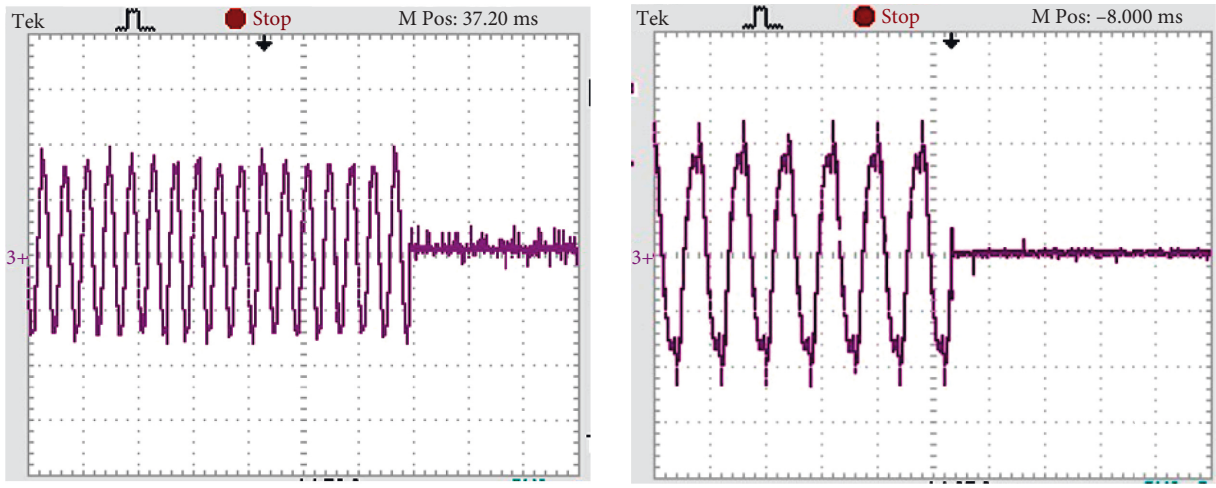
5.1. Following Observations are Made from Figures of PI Controller

(1) Before compensation, three-phase load current (rms) values are 41.1 A, 62.3 A, and 18.3 A, and their corresponding (%) THD values are 21.70%, 26.26%, and 28.23% for phase a, phase b, and phase c, respectively, as shown in Figure 6.

(2) The load neutral current and its (%) THD values are 45.0 A·rms and 38.73%, respectively, as shown in Figure 6.

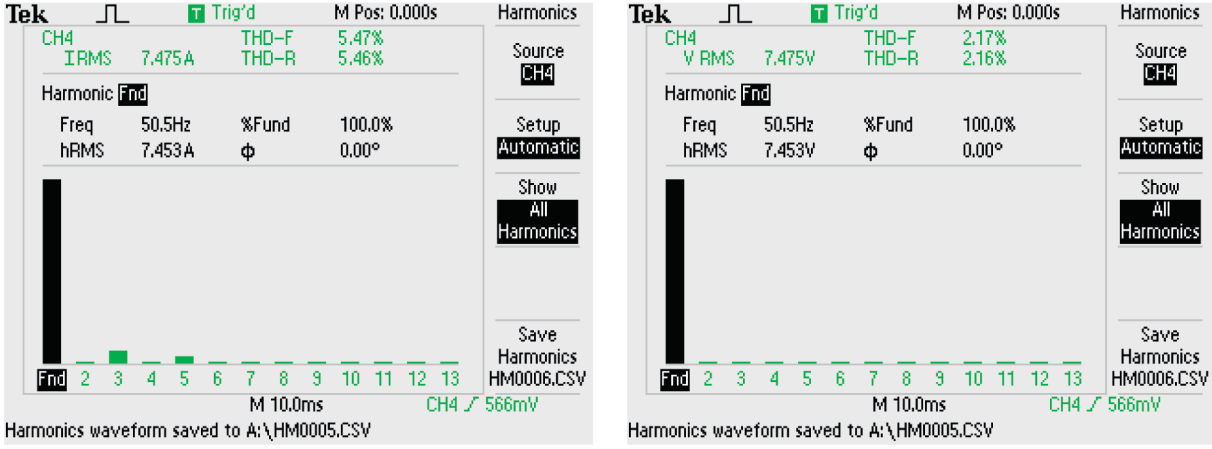
(3) At $t = 0.06$ sec, when breakers on 3P4W DSTATCOM are acting as compensators (switch S closed), the source neutral current is reduced from 50.0 A·rms to 4.18 A·rms only. Thus, the DSTATCOM with PI is the source neutral current to a large extent. Therefore, after compensation with 3P4W DSTATCOM, the source phase currents may become sinusoidal but unbalance in their magnitudes still exists. The observed source phase current (%) THD values are 5.38%, 4.77%, and 5.33% for phase a, phase b, and phase c, respectively, of source phase currents reduced to a large extent but they have small amounts of lower-order harmonic currents.

(4) At $t = 0.06$ s, when the single-phase DSTATCOM is switched on, the compensator almost completely eliminates the source neutral current, and the source phase currents become almost balanced (46.7 A, 46.8



(a) (b)

Figure 16: Source neutral current of 3P4W DSTATCOM with PI and SMC controller. (a) with PI. (b) with SMC.



(a) (b)

Figure 17: Harmonic spectra of source currents (phase a) with PI and SMC-based DSTATCOM. (a) with PI. (b) with SMC.

A, and 47.3 A·rms for phase a, phase b, and phase c, respectively) and in phase with their respective voltage waveforms, which ensures the compensation of load reactive power.

(5) The dc-link voltages of NPP are shown in Figure 7 consisting of a small amount of ripple which may deviate from the performance of DSTATCOM.

5.2. Performance of DSTATCOM SMC Controller

(1) Before compensation, three-phase load current rms values are 41.1 A, 62.3 A, and 18.3 A, and their corresponding (%) THD values are 21.70%, 26.26%, and 28.33% for phase a, phase b, and phase c, respectively, as shown in Figure 9.

(2) The load neutral current and its (%) THD values are 45.0 A·rms and 38.73%, respectively.

(3) At $t = 0.06$ sec, when the breaker on 3P4W DSTATCOM is acting as a compensator (switch S closed), the source neutral current is reduced from 50.0 A·rms to 3.25 A·rms only. Thus, the DSTATCOM with SMC of the source neutral current is reduced to a large extent. Therefore, after compensation with 3P4W DSTATCOM, the source phase currents may become sinusoidal but unbalance in their magnitudes still exists.

(4) In Figure 10, PCC voltages along with source currents are shown, where both waveforms are in-phase and the source current is sinusoidal. This indicates the complete compensation of load reactive power.

(5) The dc-link voltages of NPP are shown in Figure 11 consisting of a very small amount of ripple compared to Figure 7, which improved the performance of DSTATCOM.

Table 4: Cost comparison of 3P4W NPC, ANPC, and NPP-based DSTATCOMs.

Configuration	NPC	ANPC	NPP (T-type)
IGBT semipack switch (SKM300GB12T4, 1200 V, and 50 A)	4462 * 4 * 3 = 53544	4462 * 6 * 3 = 80316	4462 * 4 * 3 = 53544
DC capacitors with voltage sensor (4700 μF/450 V) B43743A5478M000	7288 * 2 = 14,576	7288 * 2 = 14,576	7288 * 2 = 14,576
Heat sink cost (KL-2855, P3/300 mm)	3000	4000	3000
Skyper board (SKHI 10/12R, 1200 V and 8 A)	9600 * 4 * 3 = 1,15,200	9600 * 6 * 3 = 1,72,800	9600 * 3 * 3 = 86,400
Snubber capacitor (MP-4 1F/1200 V dc H1 AD)	400 * 4 * 3 = 4,800	400 * 6 * 3 = 7,200	400 * 4 * 3 = 4,800
Coupling inductors (3 mH, 10 A)	2400 * 3 = 7,200	2400 * 3 = 7,200	2400 * 3 = 7,200
Clamping diodes (IXYS 1.2 kv, 109 A, 1.55 V, 60 ns, 600 A)	6 * 465 = 2790	18 * 465 = 8370	Not required
Total cost (INR) (as on May 2022)	2,01,110	2,94,462	1,69,520

Table 5: Comparison between NPP-based DSTATCOM with two-level capacitor midpoint and four-leg topologies.

Active filter topology	NPP (three-level)	Capacitor midpoint (two-level)	Four-leg APF (two-level)
Number of switching devices	12	6	8
Number of capacitors	2	2	1
DC voltage sensor requirement	Two	Two	One
DC-side voltage (V_l = line-to-line voltage)	$\geq\sqrt{2}V_l$	$\geq\sqrt{2}V_l$	$\geq\sqrt{2}/0.87V_l$
Need of coupling transformer	Not necessary	Necessary	Necessary
Control over neutral current	Indirect	Indirect	Direct (using 4th leg)
Main advantage	Reduced dc voltage requirement. high voltage capability, improved performance	Reduced number of switching devices	Better controllability than capacitor midpoint
Main disadvantage	Capacitor unbalance problem due to voltage difference across two capacitors	Capacitor unbalance problem due to voltage difference across two capacitors	Additional control circuit for 4^{th} leg
Application and topology selection	Suitable for high voltage, medium to high-power Applications	Suitable for low-power applications	Suitable for low-power applications

(6) The observed source phase current (%) THD values are 2.24%, 2.24%, and 2.36% for phase a, phase b, and phase c, respectively, as shown in Figure 12. With SMC, source phase currents are reduced to a large extent but they have small amounts of zero-sequence harmonic currents.

The performance of DSTATCOM under different loading conditions is shown in Table 3. From this table, it is observed that under all loading conditions the proposed DSTATCOM compensated the load current harmonics and achieved a unity power factor.

6. Experimental Results of NPP-Based DSTATCOM with PI and SMC

In this experimental study, the developed prototype inverter has been used as a DSTATCOM to verify the viability and effectiveness of the NPP-based DSTATCOM for harmonic elimination and reactive compensation. The DSTATCOM is connected to the PCC with a series of connected coupling inductors in each output phase of the inverter. The PQ theory-based controller of the DSTATCOM has been implemented in dSPACE. To verify the viability and effectiveness of the NPP-based DSTATCOM for harmonic elimination and reactive compensation, experimental investigations have been conducted with nonlinear/reactive loads.

6.1. Performance under Balanced Load Condition. The performance of the compensator with normal voltage conditions is presented in this section. Figure 13 (a)shows the experimental results of source voltage, source current after compensation, load current, and compensating currents for phase *a* with PI and SMC control techniques with a 50% reduction in the load current under normal source voltage conditions, while Figure 13(b) shows these results with 50% increase in load current.

In Figure 13(a), the load current rms value has been decreased from 3.3 A to 1.7 A and the corresponding change in the source current is from 2.9 A to 1.5 A in PI and 2.8 A to 1.4 A in the SMC control technique, respectively. It is also observed that the change in source current is very smooth in

SMC when compared to the PI-based controller. In Figure 13(b), the load current rms value has been increased from 1.7 A to 3.3 A and the corresponding change in the source current is from 1.5 A to 2.9 A in PI and 1.4 A to 2.8 A in the SMC control technique, respectively. In this case, also the observed change in source current is very smooth in SMC when compared to PI, which ensured the fast dynamic response of the controller.

Figure 14 shows the experimental results of dc capacitor voltages with PI and SMC control methods of a 50% increase in the load current. In both cases, at the instant when load current increases, the dc capacitor voltage drops from its reference value to accommodate the enhancement in the load current. These drop-in capacitor voltages are restored in 2-3 cycles in the PI-based technique but with an SMC-based controller; the drop-in capacitor voltages are restored in 1-2 cycles only, which demonstrates its superior dynamic response. It is further observed that the inclusion of a sliding mode controller in DSTATCOM control will reduce the voltage ripples in dc-link capacitor voltages when compared with the conventional PI controller. This helps in minimizing the source current overshoots during transients and harmonics.

6.2. Performance of SMC under Unbalanced Load Condition. The source voltage, source current after compensation, load current, and compensating currents before and after compensation with 3P4W DSTATCOM for phases *a*, *b* and *c* are shown in Figures 15(a)–15(c), respectively. In these figures, the different waveforms are identified as source voltage, source current after compensation, load current, and compensating current injected by DSTATCOM. It is observed that at the instant when 3P4W DSTATCOM is switched "ON", the source currents become balanced and sinusoidal and in phase with their respective voltage waveforms. From Figure 16, it is observed that at the instant when 3P4W DSTATCOM is switched "ON", the source currents become balanced and sinusoidal and in phase with their respective voltage waveforms. The THDs of the compensated source currents are 2.17%, 2.6%, and 3.0%, respectively, which are well within the limits of IEEE–519–1992 standard recommended value of 5%. The source displacement and power factor after compensation are almost unity. The experimental results are observed to be in good agreement with the simulation results.

Figure 16 shows the neutral current before and after compensation with DSTATCOM. The results are shown for PI and SMC-based controllers. From Figure 16, is observed that in the source neutral current when DSTATCOM is ON, with PI controller, a small value of neutral current still exists but with SMC the source neutral current is almost zero.

The harmonic spectra of source currents with PI and SMC control are shown in Figure 17. From this figure, it is observed that lower-order harmonics are still present in conventional PI-controlled DSTATCOM. However, with the adoption of SMC in DSTATCOM control, the lower order harmonics are reduced, and (%) THD value is 2.17%, which is well within the limits of recommended value.

7. Cost Comparison

Table 4 gives the cost comparison among the NPC, ANPC, and NPP-based DSTATCOM topologies. NPP-based DSTATCOM has less cost when compared to ANPC and NPC. This is due to the fact that to realize an NPP topology only four switching devices per phase are required. In NPC, four switching devices plus two clamping diodes are required per phase, and in comparison with ANPC, six switching devices are required per phase. Furthermore, in NPP topology, the bidirectional clamping switches are realized with a common emitter antiseries connection of two switching devices, which requires only one gate driver circuit which further reduces the cost of the topology. Table 4 gives the cost comparison of 3P4W NPC, ANPC, and NPP-based DSTATCOMs. From this table, it is observed that NPP-based topology is much cheaper when compared to the other two. On the other hand, two-level capacitor midpoint and four-leg topologies are popular for the compensation of neutral current and load balancing. Therefore, a comparison between NPP-based DSTATCOM with two-level capacitor midpoint and four-leg topologies is given in Table 5.

8. Conclusion

In this paper, a sliding mode controller is proposed for 3P4W NPP-based DSTATCOM. Mathematical equations are provided to determine the losses and efficiency of the three-level NPP topology. When compared to conventional NPC and ANPC, this NPP requires the least number of semiconductor devices and has low switching losses and high efficiency. The cost of NPP-based DSTATCOM is less when compared to its counterpart inverter topologies NPC and ANPC. The performance of the proposed SMC-based controller is smooth when compared to PI in compensating load current harmonics and balancing capacitor voltages. The experimental results are in corroborate with simulation results.

Nomenclature

NPC: Neutral point clamped
ANPC: Active neutral point clamped
NPP: Neutral point piloted
MNPC: Mixed neutral point clamped
M: Modulation index
Cos φ: Power factor
P_{cond}: Conduction losses
P_{sw}: Switching losses
$V_{\text{ce/f}}$: Forward voltage drop
$R_{\text{ce/f}}$: Forward resistance
E_{on}: Turn-on energy
E_{off}: Turn-off energy
E_{rec}: Reverse recovery energy
F_{sw}: Switching frequency
I_{ref}: Reference or nominal current
V_{ref}: Reference or nominal voltage
V_{cc}: Operating voltage.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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