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Research Article

A New Continuous Input Current Nonisolated Bidirectional Interleaved Buck-Boost DC-DC Converter

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In this paper, a new interleaved bidirectional buck-boost DC-DC converter is proposed. The input current of this converter is continuous and has a low ripple, that cause reduction in the size of the input filter of the converter. Because of these features, this converter is appropriate for renewable applications such as fuel cells and photovoltaic (PV) panels for obtaining maximum power in which the continuity of the input current is essential. The operation principle of this converter is detailed, and its power losses calculation shows the positive effects of the low input current ripple on its efficiency. The input current ripple of the proposed converter and conventional interleaved buck-boost converter has been calculated in detail. In addition, the comparison results of this converter with conventional interleaved buck-boost converters and other similar structures confirm that the proposed converter without utilizing extra components achieves continuous input current with low ripple. Compared with other buck-boost structures, the low input current ripple in the presented converter causes an improvement in its efficiency. An experimental prototype is implemented in the laboratory to confirm the correctness of theoretical analyses.

1. Introduction

Today, bidirectional DC-DC converters are used in many applications, such as electric vehicles, solar panels, fuel cells, and other renewable energy sources. The used battery in renewable sources can be charged using a bidirectional converter and discharged in low and high loads, respectively [1–4]. In applications such as fuel cells, electric vehicles, and power factor correction, to increase the system's life, it is necessary to have a converter with a continuous input current with a small ripple [5–7]. The DC-DC converter plays a vital role in tracking the maximum power of a photovoltaic source. If the input current of this converter has a ripple, the obtained power from PV will fluctuate around the maximum PowerPoint. The value of this oscillation is directly related to the input current ripple of the converter. Therefore, as the currents ripple increases, power oscillation will be higher around the maximum power point [8, 9]. In the conventional buck-boost converter, the converter's input current has a pulse form, which reduces the life of the used components in the converter structure [10]. Usually, on the input side of the converter, an inductor can be used to reduce the ripple of the input current; because of the proper design of the inductor, the input current can be continuous. In converters such as Cuk, this method has been used to reduce the ripple of the current. However, the number of circuit elements is higher, and the resulting cost increases [11]. The interleaved converter is used to increase the power transferred, increasing the efficiency and reducing the current and voltage ripple [12–14]. The presented structure in [5] includes a two-phase interleaved buck converter and a two-phase boost converter that has been connected in series together. The input and output current ripple can be reduced by using the boost and buck converter. Therefore, the structure presented in [5] has a continuous input/output current with low ripple. However, due to the series

connection of the two interleaved converters, the efficiency of the proposed converter in [5] decreases because the number of converter elements is high, and additional conductive losses in the converter are created [15]. In [16], a converter has been introduced in a hybrid source storage system with low input and outputs current ripple. This converter can only operate in step-up mode and is not applicable for both step-up and step-down applications. In [17, 18], additional elements are used to reduce the ripple of the converter's current; however, due to the increase in the number of elements in the current path, the power losses and cost of the converter increase and the efficiency decreases. In [19], an interleaved buck-boost converter has been presented. The presented converter is constructed of two parallel conventional buck-boost converters, and the input current ripple of this converter is considerable, and this is in discontinuous mode. Also, this converter is not capable of operating as a bidirectional converter, and this issue makes it is not a suitable interface device between the battery port and other ports. The presented structure in [20] operates as an interleaved buck converter. In the structure of this converter to achieve soft switching for one of the switches, an inductor has been used, but the efficiency improvement is not considerable. Also, like other mentioned converters, this converter has a ripple in its input current. By switching the switches in the input side of the converter, the input current gets in discontinuous mode. The presented converter in [21] operates as a buck converter, and this converter has more elements in its structure and has five switches that cause the conduction losses, and the switching losses of the converter increase, so its efficiency decreases.

An interleaved buck converter is presented in [22], in which the step-down ratio is improved. Still, the input current is discontinuous, and the input current ripple ratio is close to the conventional one. In [23], a ZCS interleaved bidirectional buck-boost DC-DC converter is presented, appropriate for energy storage applications. Although the conventional interleaved converter has been improved with the auxiliary resonant cells, the input current ripple is still not improved. In addition, the power loss of the converter is not much increased compared with similar structures. According to [24, 25], the large current ripple causes to increase in its RMS value, which produces extra power losses, so the low input current has a vital role in the converter losses. In [26], a SEPIC-based converter is proposed to increase the voltage gain without using any coupled inductors and isolated transformers. Nevertheless, this noncoupled inductor converter still has a low voltage gain, and its high number of passive components causes adverse effects on the dynamic response of the converter. A new buck-boost converter derived from conventional boost and buck-boost converter is proposed in [27], but the stress across one switch is high, and the voltage gain in the boost range is limited.

In this paper, a new interleaved bidirectional buck-boost DC-DC converter is presented in which, without using the additional elements, the ripple of the input current is reduced. Due to the lack of an auxiliary circuit to reduce the current ripple, the number of converter elements is less, and the losses of the converter get low. Due to the bidirectional operation of this converter, it can be used in renewable energy sources. The applied batteries in these sources can be charged and discharged using this converter. Because the battery is sensitive to currents ripple, the high-current ripple will reduce its life. It should be noted that increasing the gain is not the contribution of this paper. The paper detailed the different operation modes for the proposed structure for both forward and reverse power flow directions. In addition, the design of converter elements has been done, the input current ripple is calculated, and the converter efficiency is fully analyzed. The small-signal model of the proposed converter has been obtained, and the converter stability has been investigated. In addition, a comparison has been made between the proposed converter and other structures, and finally, the experimental results have been presented.

2. Structure of the Proposed Converter and Its Steady-State Analysis

Figure 1(a) shows the proposed bidirectional interleaved buck-boost DC-DC converter structure. This converter uses four switches with reverse-parallel diodes, two inductors, and a capacitor. The input and output voltages are shown, respectively, with V_{in} and V_o, and R represents the load resistance. The converter switches work with the duty cycle D, and the applied commands to the switches gate have a 180-degree phase difference with each other. The switches S_1 and S_2 and the reverse-parallel diodes of switches S_3 and S_4 are used to transmit the power from the input to the load. For power flow in the reverse direction, the switches S_3 and S_4 are used, and this power passes through the reverse-parallel diodes of switches S_1 and S_2. The operation of this converter in each direction of power flow has four modes; in the following, different modes are given.

2.1. Forward Operation. The power transmission is through the switches S_1 and S_2 and reverse-parallel diodes D_3 and D_4. In this case, the converter has four modes, all of which are listed in the following. The equivalent circuit for each mode and related key waveforms are shown in Figures 1 and 2(a), respectively.

Mode 1 $[t_0 < t < t_1]$: during this mode, the switch S_1 and diode D_3 are turned on, and the input voltage is applied to the L_1 via the switch S_1 and magnetized it, and the inductor current increases linearly. Also, the output voltage is inversely applied to L_2, and its current decreases linearly. The currents of the inductors are given by (1) and (2) (Figure 1(b)):

$$i_{L1}(t) = \frac{V_i}{L_1} t + i_{L1}(t_0), \tag{1}$$

$$i_{L2}(t) = -\frac{V_o}{L_2} t + i_{L2}(t_0). \tag{2}$$

The peak value of i_{L1} occurs at t_1; therefore, using (1), the value of the ripple of the i_{L1} is obtained as follows:

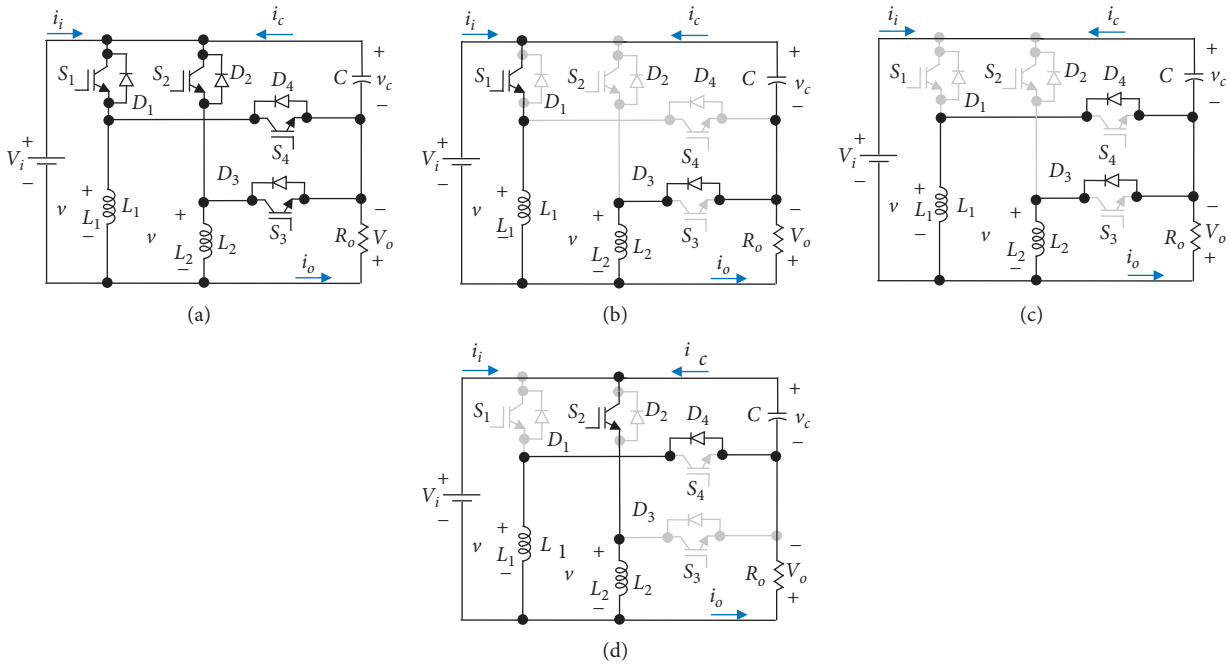

Figure 1: (a) Proposed converter and its equivalent circuits in different modes in forward operation: (b) mode 1, (c) modes 2 and 4, and (d) mode 3.

$$\Delta I_{L1} = \frac{V_i}{f_s L_1} D. \tag{3}$$

When the switch S_1 is turned off at t_1, this mode ends, and the next mode starts.

Mode 2 $[t_1 < t < t_2]$: in this mode, the switch S_1 is turned off, and the reverse-parallel diodes D_4 and D_3 are directly biased, and the stored energy in the inductors is demagnetized to the load through these diodes. V_{L1} and V_{L2} are equal to $-V_o$, and the currents i_{L1} and i_{L2} decrease linearly. The voltage of the switches S_1 and S_2 is clamped to $V_i + V_o$ (Figure 1(c)). When the switch S_2 is turned on at t_2, this mode ends, and the next mode starts.

Mode 3 $[t_2 < t < t_3]$: in this mode, the switch S_2 is turned on, the reverse-parallel diode D_4 is directly biased, the voltage of the inductor L_1 is equal to $-V_o$, and the current i_{L1} decreases linearly according to (4).

The input voltage is applied to the inductor L_2 via the switch S_2, and the current i_{L2} increases linearly according to (5) (Figure 1(d)):

$$i_{L1}(t) = -\frac{V_o}{L_1}(t - t_2) + i_{L1}(t_2), \tag{4}$$

$$i_{L2}(t) = \frac{V_i}{L_2}(t - t_2) + i_{L2}(t_2). \tag{5}$$

The peak value of i_{L2} occurs at t_3. Therefore, using (5), the value of the ripple of i_{L2} is obtained as follows:

$$\Delta I_{L_2} = \frac{V_i}{f_s L_2} D. \tag{6}$$

When the switch S_2 is turned off at t_3, this mode ends, and the next mode starts.

Mode 4 $[t_3 < t < t_4]$: at t_3, the switch S_2 is turned off, the reverse-parallel diode D_3 is directly biased, and D_4 still is in on state. Through these diodes, the inductors are demagnetized to the load. The voltages v_{L1} and v_{L2} are equal to $-V_o$, and the currents i_{L1} and i_{L2} are decreased linearly. In this mode, the voltage of the switches S_1 and S_2 is clamped to $V_i + V_o$ (Figure 1(c)).

2.2. Reverse Operation. The load acts as an energy source in this mode, and the power is transferred from the output to the input source. For this purpose, the switches S_1 and S_2 are turned off, and the command signals are applied to the switches S_3 and S_4. The power transmission is through switches S_3 and S_4 and reverse-parallel diodes D_1 and D_2. Like the forward operation, the converter has four modes in this mode. Figure 3(a) shows the circuit related to this operation with the elements used to transfer power in the reverse direction. The equivalent circuit for buck operation and their key waveforms are shown in Figures 3(b) and 3(c) and Figure 2(b), respectively.

Mode 1 $[t_0 < t < t_1]$: during this mode, the switch S_4 and the diode D_2 are turned on and the voltage V_o is applied through the switch S_4 to the inductor L_1 and charges it. In this mode, the inductor current i_{L1} increases linearly according to (7). Also, the voltage V_i inversely is applied to the inductor L_2 and discharges it, and its current decreases linearly according to (8) (Figure 3(b)):

$$i_{L1}(t) = \frac{V_o}{L_1} t + i_{L1}(t_0), \tag{7}$$

$$i_{L2}(t) = -\frac{V_i}{L_2} t + i_{L2}(t_0). \tag{8}$$

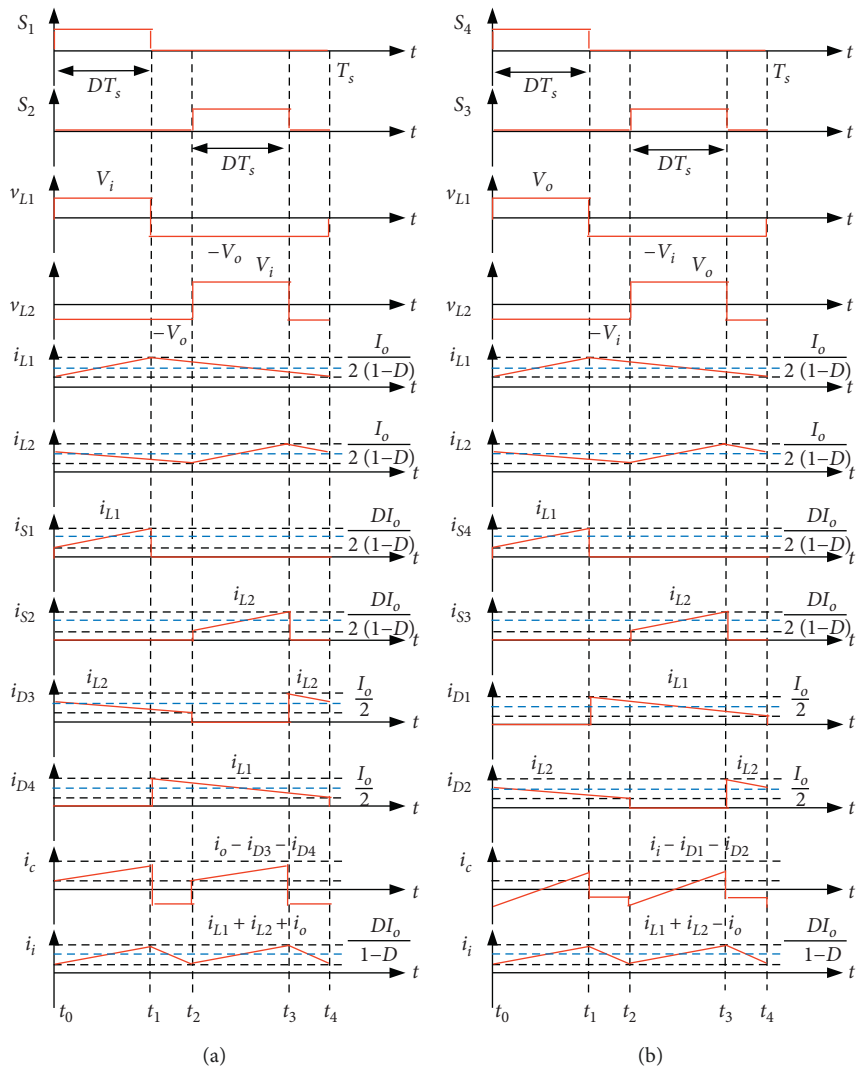

Figure 2: The key waveforms of the proposed converter elements in (a) forward buck operation and (b) reverse buck operation.

The peak value of i_{L1} occurs at t_1. Therefore, using (7), the value of the ripple of i_{L1} is obtained as follows:

$$\Delta i_{L_1} = \frac{V_i}{f_s L_1} D. \tag{9}$$

When the switch S_4 is turned off at t_1, this mode ends, and the next mode starts.

Mode 2 $[t_1 < t < t_2]$: the switch S_4 is turned off in this mode, and the reverse-parallel diodes D_1 and D_2 are turned on. The energy stored in the inductors is discharged to the input source through these diodes. The voltages v_{L1} and v_{L2} are equal to $-V_i$, and the currents i_{L1} and i_{L2} decrease linearly. The voltages of the switches S_3 and S_4 are clamped to $v_i + v_o$ (Figure 3(c)). When the switch S_3 is turned on at t_2, this mode ends, and the next mode starts.

Mode 3 $[t_2 < t < t_3]$: at t_2, switch S_3 turns on, and the diode D_1 is still in on state. The voltage V_i through this diode is inversely applied to the inductor L_1, and its current decreases linearly according (10). Applying the voltage V_o to the inductor L_2, its current increases linearly according (11) (Figure 3(d)).

$$i_{L1}(t) = -\frac{V_i}{L_1}(t - t_2) + i_{L1}(t_2), \tag{10}$$

$$i_{L2}(t) = \frac{V_o}{L_2}(t - t_2) + i_{L2}(t_2). \tag{11}$$

The peak value of i_{L2} occurs at t_3. Therefore, using (11), the value of the ripple of the i_{L2} is obtained as follows:

$$\Delta i_{L_2} = \frac{V_o}{f_s L_2} D. \tag{12}$$

When the switch S_3 is turned off at t_3, this mode ends, and the next mode starts.

Mode 4 $[t_3 < t < t_4]$: at t_3, the switch S_3 is turned off, the reverse-parallel diode D_2 is directly biased, and D_1 is still in on state. The energy stored in the inductors discharges to the input source through these diodes. The voltages v_{L1} and v_{L2}

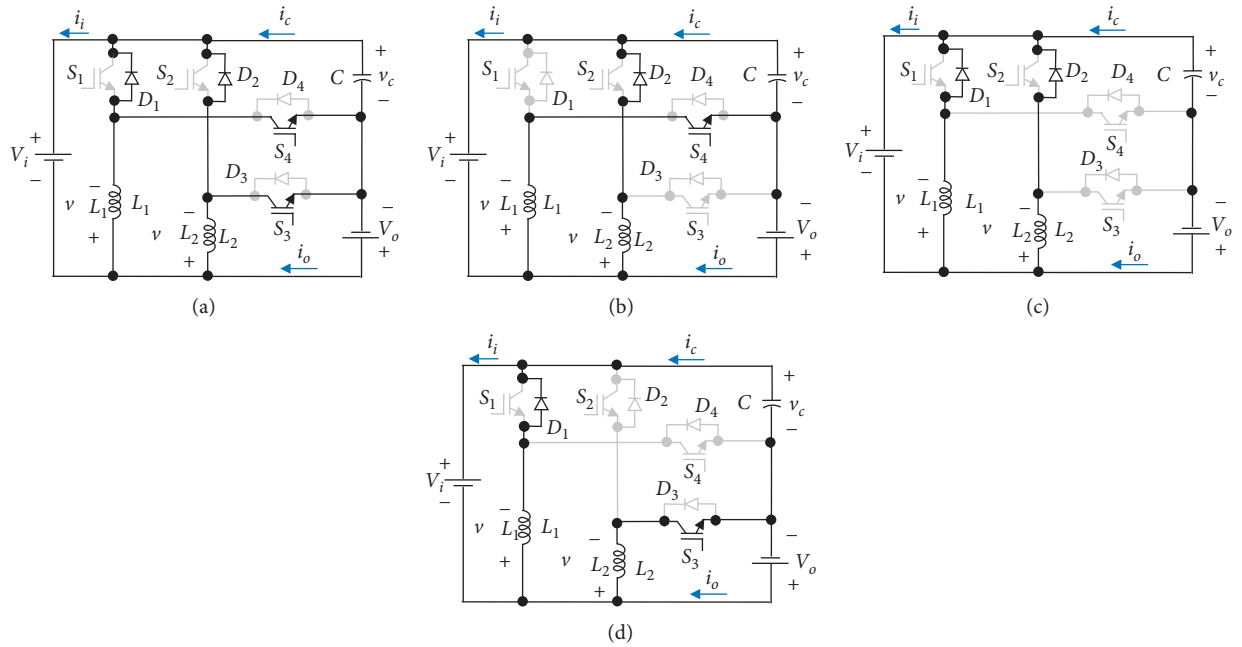

Figure 3: (a) The proposed converter and its equivalent circuit in different modes in reverse operation: (b) mode 1, (c) modes 2 and 4, and (d) mode 3.

Table 1: Inductors applied voltage in forward and reverse boost operation.

Case	Operation	Mode 1	Mode 2	Mode 3	Mode 4
v_{L1}	Forward	V_i	V_i	V_i	$-V_o$
	Reverse	V_o	V_o	V_o	$-V_i$
v_{L2}	Forward	V_i	$-V_o$	V_i	V_i
	Reverse	V_o	$-V_i$	V_o	V_o

equal $-V_i$, and the currents i_{L1} and i_{L2} decrease linearly. In this mode, the voltages of the switches S_3 and S_4 are clamped to $V_i + V_o$ (Figure 3(c)).

Also, in boost operation, the voltage and current of the inductors in each mode for forward and reverse operation are presented in Table 1. The key waveforms for these operation modes can be obtained using this table.

2.3. Voltage Conversion Ratio. The voltage conversion ratio of the proposed converter in both directions is similar to each other; therefore, in this section, voltage gain is obtained for one direction. In forward operation, using volt-second law for an inductor and taking into account that t_3-$t_2 = t_1$-$t_0 = D$, the voltage conversion ratio of the converter is obtained as follows:

$$\frac{V_o}{V_i} = \frac{D}{1-D}. \tag{13}$$

It can be seen from (13) that the voltage conversion ratio of the proposed converter is the same as a conventional buck-boost converter. Also, the voltage of the capacitor is obtained as follows:

$$v_c = \frac{1}{1-D} V_i. \tag{14}$$

2.4. Discontinuous Conduction Mode. The presented converter's operation is divided into four modes in this mode. Mode 1 and mode 3 in DCM, respectively, are the same as that of mode 2 and mode 4 in CCM, and in mode 2, the currents of switches S_1 and S_2 and diode D_3 are zero. In addition, in mode 4, the currents of semiconductors (except D_3) are zero. These modes and the related typical waveforms are shown in Figures 4 and 5, respectively. The current ripple of the inductors still is according to (9) and (12). If the average value of the inductor current is greater than half of its current ripple (according to equation (15)), then the current of the inductor would be continuous.

$$I_L = \frac{I_o}{2(1-D)} > \frac{\Delta i_L}{2} = \frac{V_i D}{2 L f_s}, \tag{15}$$

in which $I_L = I_{L1} = I_{L2}$ and $L = L_1 = L_2$. By replacing (12) in (15), the relationship between duty cycle (D) and constant parameters (L, f_s, and R_o) is obtained as follows:

$$(1-D)^2 < \frac{L f_s}{R_o}. \tag{16}$$

By considering the normalized inductor time constant as $\tau_b = L f_s / R_o$, according to equation (16), τ is a function of the duty cycle. If the value of τ is lower than its critical value (τ_b), the operation of the converter will be in discontinuous mode; otherwise, it will be in continuous mode. In Figure 6, the curve τ_b is shown. According to this figure, the operation region of the proposed converter in CCM is larger than DCM.

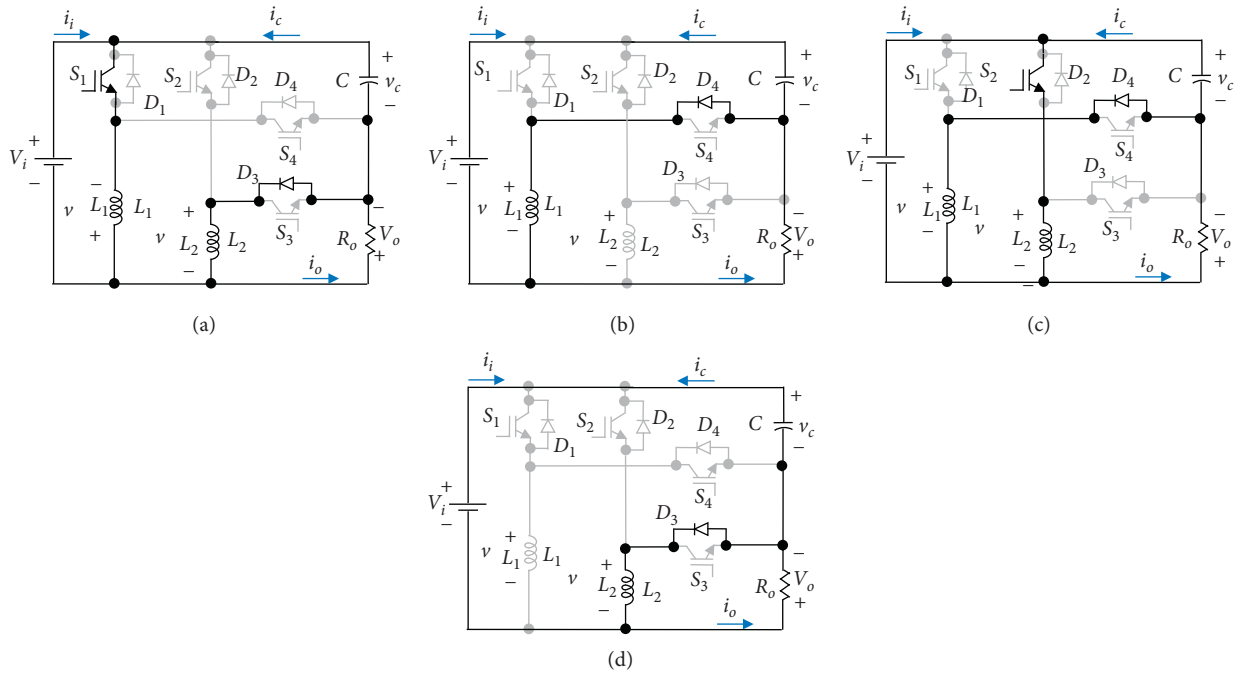

Figure 4: Different modes of the proposed converter in DCM: (a) mode 1, (b) modes 2, (c) mode 3, and (d) mode 4.

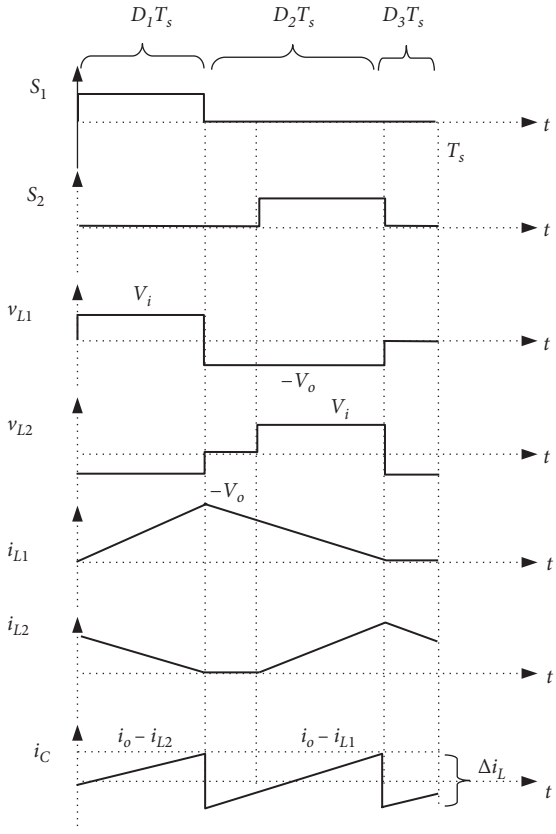

Figure 5: Typical waveforms of the proposed converter in DCM.

From Figure 6, it can be concluded that the boundary normalized inductor time constant (τ_b) for the presented converter is the same as the conventional interleaved buck-boost converter.

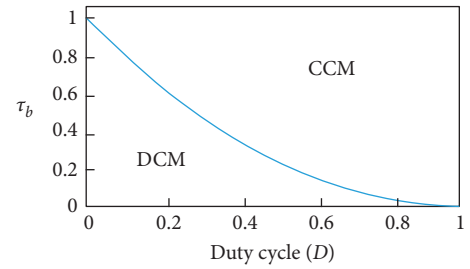

Figure 6: Normalized inductor time constant versus duty cycle D.

In order to calculate the voltage gain in discontinuous conduction mode, the volt-second balance principle of inductors is used. This principle for inductor L_1 can be expressed as follows.

$$\frac{1}{T_s}\int_0^T V_{L1}\,\mathrm{d}t = D_1V_i + D_2V_o + D_3(0) = 0. \tag{17}$$

Thus, the voltage conversion ratio is obtained as follows:

$$\frac{V_o}{V_i} = \frac{D_1}{D_2}. \tag{18}$$

According to Figure 5, in time interval D_2T_s, the capacitor, respectively, is charged and discharged by the inductor and load. The DC output current is calculated as follows:

$$I_o = \frac{1}{T_s}\int_0^{T_s}\left(i_{D3}(t) + i_{D4}(t)\right)\mathrm{d}t = 2\times\frac{D_2\Delta i_L}{2} = \frac{V_o}{R_o}. \tag{19}$$

Hence, by substituting (15) and (18) in (19), duty cycle D_2 in the second mode can be obtained as follows:

$$\frac{V_i D_1 D_2}{L f_s} = \frac{D_1 V_i}{D_2 R_o}, \tag{20}$$

$$D_2 = \sqrt{\frac{L f_s}{R_o}} = \sqrt{\tau_b}, \tag{21}$$

where $\tau_b = L f_s / R_o$. Using (18) and (21), the voltage conversion ratio can be derived as follows:

$$\frac{V_o}{V_i} = \frac{D_1}{\sqrt{\tau_b}}. \tag{22}$$

Thus, the voltage conversion ratio of the presented converter is the same gain as that of the conventional interleaved buck-boost converter in DCM.

2.5. Switches Voltage Stress. As shown in Figures 1 and 3, in forward and reverse operations, the voltage stress of switches S_1–S_4 is calculated as follows:

$$V_{sw} = \frac{V_o}{D}. \tag{23}$$

According to (23), it concluded that the voltage across switches in the proposed converter and the conventional buck-boost converter are equal.

3. Converter Design

3.1. Inductor Design. Since the average current of the inductors L_1 and L_2 are equal, the design for L_1 is given and the design of the L_2 is similar to L_1. In Figure 7, the waveform of the current of inductor L_1 is shown in a critical condition. By using this waveform, the minimum values of the inductors L_1 and L_2 can be obtained. As shown in Figure 7, the inductor current reaches its maximum value in time interval DT_s. Therefore, the maximum value of the current ripple of inductor L_1 will be equal to

$$\Delta I_{L_1,\max} = \frac{V_o (1 - D_{\min})}{f_s L_{1,\min}}. \tag{24}$$

As shown in (25), in the critical condition, the current of the inductor L_1 is equal to half of the current ripple.

$$I_{L_1,B} = \frac{V_o (1 - D_{\min})}{2 f_s L_{1,\min}}. \tag{25}$$

Since the average current of the inductors is equal and the average current of the capacitor C is zero,

$$I_i + I_o = I_{L1} + I_{L2}. \tag{26}$$

The average currents of I_{L1} and I_{L2} can be calculated as follows:

$$I_{L1} = I_{L2} = \frac{I_o}{2(1 - D)}. \tag{27}$$

Using (25) and (27), the critical output current $I_{o,B}$ is obtained by

$$I_{o,B} = \frac{V_o (1 - D_{\min})^2}{f_s L_{1,\min}}. \tag{28}$$

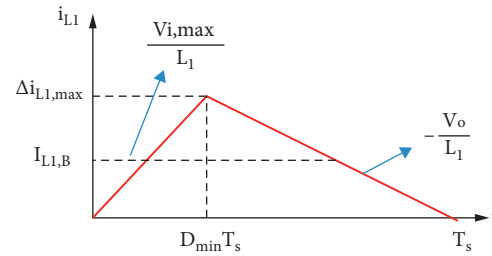

Figure 7: Current waveform of the inductor L_1 in boundary mode.

According to (28), the minimum values of the inductors L_1 and L_2 are given by

$$L_{1,\min} = L_{2,\min} = \frac{R_{o,\max} (1 - D_{\min})^2}{f_s}. \tag{29}$$

3.2. Capacitor Design. The design of capacitor C is based on the value of the voltage ripple of this capacitor so that the ripple does not exceed its maximum permissible value. Using (27) and (28), in the first mode of forward operation, the capacitor current is given by

$$i_c(t) = I_o - i_{L2}(t) = I_o + \frac{V_o}{L_2} t - i_{L2}(t_0). \tag{30}$$

The ac component of the output voltage is the sum of the voltage across the capacitor ESR (r_C) and the capacitance C. Using (6), (27), and (30), v_o can be calculated.

Using the derivative of the voltage v_o with respect to time, the minimum value of v_o is obtained. This occurs at a minimum capacitance, given by

$$C \geq \frac{2R_o (1 - D)^2 - f_s L_2 (1 - 2\ D)}{2 r_c R_o f_s (1 - D)}. \tag{31}$$

4. Input Current Ripple

For $D < 0.5$, in forward operation, the input current in different modes is a function of the current of the inductors and the load as described as follows:

$$i_i = i_{L1} + i_{L2} - i_o. \tag{32}$$

By using the currents equations of inductors L_1 and L_2 in various modes, the following equation is obtained:

$$i_i = \begin{cases} \left(\frac{V_i}{L_1} - \frac{V_o}{L_2}\right) t + i_{L1}(t_0) + i_{L2}(t_0) - i_o, & t_0 < t < t_1, \\ -\left(\frac{V_o}{L_1} + \frac{V_o}{L_2}\right)(t - t_1) + i_{L1}(t_1) + i_{L2}(t_1) - i_o, & t_1 < t < t_2, \\ \left(\frac{V_i}{L_2} - \frac{V_o}{L_1}\right)(t - t_2) + i_{L1}(t_2) + i_{L2}(t_2) - i_o, & t_2 < t < t_3, \\ -\left(\frac{V_o}{L_1} + \frac{V_o}{L_2}\right)(t - t_3) + i_{L1}(t_3) + i_{L2}(t_3) - i_o, & t_3 < t < t_4. \end{cases} \tag{33}$$

Using (33), the value of the input current ripple can be calculated as follows:

$$\Delta I_{i,\text{proposed}} = i_i(DT_S) - i_i(0) = \frac{V_o}{f_s}\left[\frac{L_2(1-D) - DL_1}{L_1 L_2}\right]. \tag{34}$$

If $L_1 = L_2 = L$, (26) can be simplified as follows:

$$\Delta I_{i,\text{proposed}} = \frac{V_o}{Lf_s}(1 - 2\ D). \tag{35}$$

For $D > 0.5$, in the case where the proposed converter acts as a step-up in the forward operation, the inductor L_1 and L_2 currents are given by the following equations, respectively:

$$i_{L1} = \begin{cases} \dfrac{V_o}{L_1}t + i_{L1}(t_0), & t_0 < t < t_3, \\ -\dfrac{V_i}{L_1}(t - t_3) + i_{L1}(t_3), & t_3 < t < t_4, \end{cases} \tag{36}$$

$$i_{L2} = \begin{cases} \dfrac{V_o}{L_2}t + i_{L2}(t_0), & t_0 < t < t_1, \\ -\dfrac{V_i}{L_2}(t - t_1) + i_{L2}(t_1), & t_1 < t < t_2, \\ \dfrac{V_o}{L_2}t + i_{L2}(t_2), & t_2 < t < t_4. \end{cases} \tag{37}$$

If $L_1 = L_2 = L$, then using (36) and (37), in one switching period, the input current equations can be calculated in all modes as follows:

$$i_i = \begin{cases} \dfrac{2V_o}{L}t + i_{L1}(t_0) + i_{L2}(t_0) - i_o, & t_0 < t < t_1 \& t_2 < t < t_3, \\ \dfrac{V_i - V_o}{L}(t - t_1) + i_{L1}(t_1) + i_{L2}(t_1) - i_o, & t_1 < t < t_2 \& t_3 < t < t_4. \end{cases} \tag{38}$$

For the proposed converter in step-up mode, by using (38), the input current ripple is obtained as follows:

$$\Delta I_{i,\text{proposed}} = \frac{2(1-D)(D-0.5)V_o}{DLf_s}. \tag{39}$$

In a conventional two-phase interleaved buck-boost converter, assuming $L_1 = L_2 = L$, the input current ripple for $D < 0.5$ and $D > 0.5$ is calculated according to the following equations:

$$\Delta I_{i,conv} = V_o\left[\frac{1}{R_o(1-D)} + \frac{1-D}{2f_s L}\right], \quad \text{for } D < 0.5, \tag{40}$$

$$\Delta I_{i,\text{conv}} = \frac{V_i}{f_s L}D, \quad \text{for } D > 0.5. \tag{41}$$

Using (35), (39), (40), and (41), the ratio of the input current ripple of the proposed converter to the input current ripple of the conventional interleaved buck-boost converter for $D < 0.5$ and $D > 0.5$ is obtained as (42) and (43), respectively. According to (42), in step-down mode, by increasing the power and frequency, the ratio of the input current ripple of the proposed converter decreases with respect to the conventional converter.

$$\frac{\Delta I_{i,\text{proposed}}}{\Delta I_{i,\text{conv}}} = \frac{1-2D}{(Lf_s/R_o(1-D)) + (1-D)/2}, \tag{42}$$

$$\frac{\Delta I_{i,\text{proposed}}}{\Delta I_{i,\text{conv}}} = \frac{2D-1}{D}. \tag{43}$$

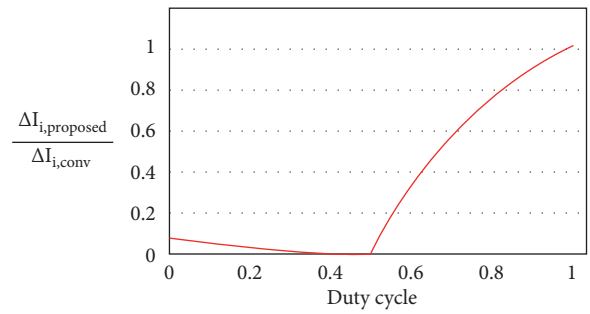

Figure 8: The ratio of the input current ripple of the proposed converter to the input current ripple of the conventional interleaved buck-boost converter.

The curve of the input current ripple ratio of the proposed converter to the input current ripple of the conventional interleaved buck-boost converter is shown in Figure 8. According to this figure, this ratio is less than 1 for all duty cycles, and the input current ripple of the proposed converter in buck mode is less than the conventional interleaved buck-boost converter.

According to the analyzes performed in Sections 2.5 and 4 and using equations (3), (15), (16), (42), and (43), the three-dimensional curve of normalized inductor time constant (τ_b) with respect to duty cycle (D) and input current ripple ratio ($\Delta i_{\text{Proposed}}/\Delta i_{\text{Conventional}}$) for the buck and boost operation modes is provided as shown in Figure 9. The upper and lower level of the surface corresponds to continuous conduction mode (CCM) and discontinuous mode (DCM), respectively. As can be seen, for different values of duty cycle and τ_b, the input current ripple ratio ($\Delta i_{\text{Proposed}}/\Delta i_{\text{Conventional}}$) is less than 1, representing that the presented converter's input current ripple is less than the conventional interleaved buck-boost converter.

5. Power Losses Calculation

The operation of the proposed converter in the forward mode is similar to the reverse mode. In other words, the currents of the elements are the same in two operations, and the same voltage is applied to the elements. Therefore, to calculate the losses of the converter and its efficiency, the equivalent circuit of the forward operation is used as shown in Figure 10. In this circuit, the parasitic components of all elements are shown. In this figure, R_F is equal to the resistance of the diode in conduction mode, V_F is the diode

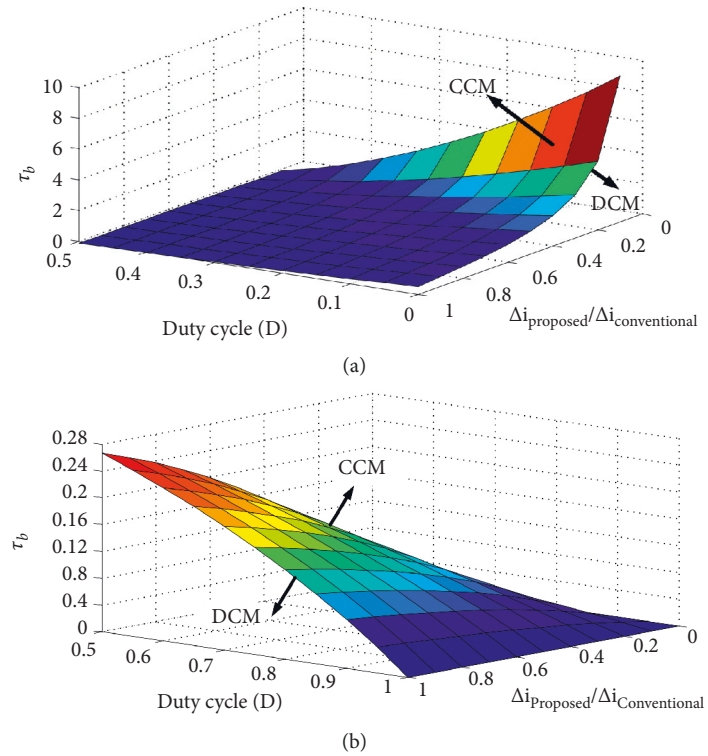

Figure 9: Normalized inductor time constant with respect to duty cycle and input current ripple ratio: (a) buck operation and (b) boost operation.

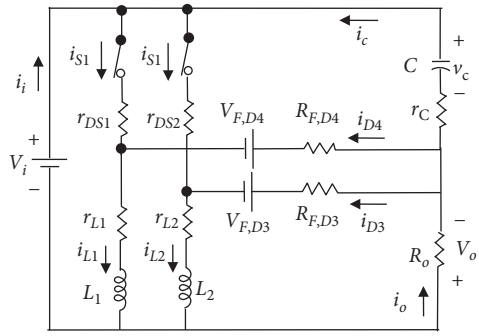

Figure 10: The equivalent circuit of the proposed converter with parasitic resistances and diodes conduction threshold voltage.

conduction threshold voltage, r_L is the equivalent series resistance of inductor L, r_c is the equivalent series resistance of capacitor C, and r_{DS} stands for the total resistance between the drain and source in a switch when the switch is on. Using definitions of the RMS and average values, the power losses of the switch, diode, inductor, and capacitor are obtained as listed in Table 2.

According to Figure 10, the total power loss is calculated as follows:

$$P_{\text{loss}} = 2\left(P_{\text{Switch}} + P_D + P_{rL}\right) + P_{rc}. \tag{44}$$

Using (44) and Table 2, the converter efficiency is equal to

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}}. \tag{45}$$

Table 2: Calculated losses of components.

Symbol	Losses
P_{Switch}	$P_o[(r_{DS_1}D/4R_o(1-D)^2) + (f_s C_{s_1} R_o/D^2)]$
P_D	$P_o[(R_{F,D_4}/4R_o(1-D)) + (V_F/2V_o)]$
$P_{r,L1}$	$r_{L_1}P_o/4R_o(1-D)^2$
$P_{r,C}$	$D(1-2D)r_c P_o/2R_o(1-D)^2$

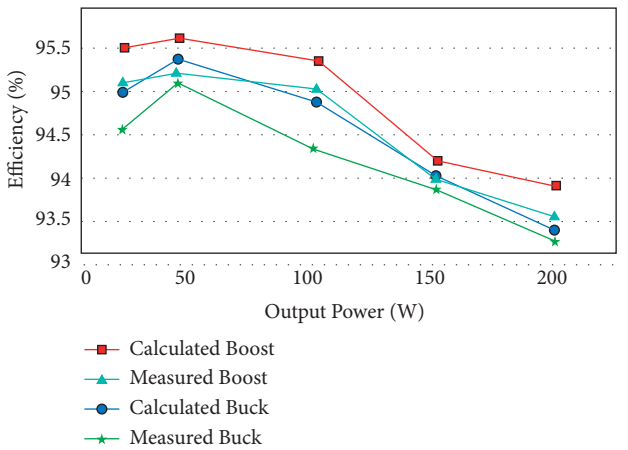

Figure 11: Converter efficiency curve versus output power.

The efficiency curves versus output power of the proposed converter in boost and buck modes are illustrated in Figure 11. As can be seen from this figure, the measured

efficiency is a little lower than the calculated losses. For boost and buck operation modes, this converter at 50 W load has a maximum efficiency of 95.6% and 95.4%, respectively. For smaller and larger loads than 50 W, the converter's efficiency decreases because for loads less than 50 W and the switching losses are high. For loads greater than 50 W, the conduction losses increase, and efficiency decreases. In the rated power, the efficiency in boost and buck modes is equal to 93.9% and 93.4%, respectively. According to Figure 11, the efficiency of the theoretical is slightly different with experimental one. In practice, due to conduction losses and differences in the performance of practical elements, different efficiencies will be obtained. In general, the value of this difference is not so great and for the presented converter is equal to 0.5%. For example, the performance of the same power components (diode and switch) cannot be exactly the same. This is related to the internal structure and factory production of the component. As a result of conduction losses, differences in the internal structure of exactly the same power components and errors due to measuring devices (such as internal resistances or some external conditions of the environment, such as pressure, temperature, humidity, or magnetic field) are the most important factors that cause differences between the experimental and simulation efficiency values.

6. Relation between Input Current Ripple and Converter Efficiency

In addition, in the following, the effects of the input current ripple on the converter efficiency are discussed, and the relation between these two parameters is derived. The current of inductor L_1, switch S, diode D, and capacitor C in different time intervals is as follows:

$$i_L = \begin{cases} \dfrac{\Delta i_L}{DT_s} t + i_{L1}(t_0), & 0 < t < DT_s, \\ -\dfrac{\Delta i_L}{(1-D)T_s}(t - DT_s) + i_L(DT_s), & DT_s < t < (1-D)T_s, \end{cases} \tag{46}$$

$$i_S = \begin{cases} \dfrac{\Delta i_L}{DT_s} t + i_{L1}(t_0), & 0 < t < DT_s, \\ 0, & DT_s < t < (1-D)T_s, \end{cases} \tag{47}$$

$$i_D = \begin{cases} 0, & 0 < t < DT_s, \\ -\dfrac{\Delta i_L}{(1-D)T_s}(t - DT_s) + i_L(DT_s), & DT_s < t < (1-D)T_s, \end{cases} \tag{48}$$

in which the amplitude of $i_L(0)$ and $i_L(DT_s)$ is obtained using

$$i_L(t_0) = \frac{I_o}{2(1-D)} - \frac{\Delta i_L}{2}, \tag{49}$$

$$i_L(DT_s) = \frac{I_o}{2(1-D)} + \frac{\Delta i_L}{2}. \tag{50}$$

Using (47), (49), and (50), the effective currents of the switches S_1 and S_2 are obtained as follows:

$$I_{S_{1,rms}} = I_{S_{2,rms}} = \sqrt{\frac{D\Delta i_L^2}{12} - \frac{DI_o\Delta i_L}{2(1-D)} + \frac{DI_0^2}{4(1-D)^2}}. \tag{51}$$

The switch losses of the converter include two components, including conduction losses and switching losses. The component losses of Figure 2 are calculated and then multiplied in 2 to obtain the proposed converter losses. The conduction losses of the switches can be calculated by the following:

$$P_{r_{DS_1}} = r_{DS_1}\left(\frac{D\Delta i_L^2}{12} - \frac{DI_o\Delta i_L}{2(1-D)} + \frac{DI_0^2}{4(1-D)^2}\right). \tag{52}$$

The switching losses are also obtained as follows:

$$P_{SW_{S_1}} == \frac{f_s C_{s_1} P_o R_o}{D^2}. \tag{53}$$

The losses of the switch are equal to the sum of the conduction and switching losses; therefore, the total losses associated with the switches are equal to the following:

$$P_{\text{Switch}} = 2\left(r_{DS_1}\left(\frac{D\Delta i_L^2}{12} - \frac{DI_o\Delta i_L}{2(1-D)} + \frac{DI_o^2}{4(1-D)^2}\right) + \frac{f_s C_{s_1} P_o R_o}{D^2}\right). \tag{54}$$

Using (47), (49), and (50), the effective currents of diodes D_3 and D_4 are obtained as follows:

$$I_{D_{3,rms}} = I_{D_{4,rms}} = \sqrt{\Delta i_L^2\left(\frac{5D-2}{12}\right) + \Delta i_L\left(\frac{1-I_o}{2}\right) + \frac{I_o}{2(1-D)}}. \tag{55}$$

The average currents of the diodes D_3 and D_4 are obtained as follows:

$$I_{D_3} = I_{D_4} = \frac{I_o}{2}. \tag{56}$$

The power losses in R_F of diodes are equal to the following:

$$P_{R_F} = R_{F,D_4}\left(\Delta i_L^2\left(\frac{5D-2}{12}\right) + \Delta i_L\left(\frac{1-I_o}{2}\right) + \frac{I_o}{2(1-D)}\right). \tag{57}$$

Using (55), the power losses associated with the diode conduction threshold voltage can be calculated as follows:

$$P_{V_F} == \frac{V_F P_o}{2V_o}. \tag{58}$$

The diode losses are equal to the sum of (57) and (58). Therefore, the overall loss of diodes is equal to the following:

$$P_D = 2\left[R_{F,D_4}\left(\Delta i_L^2\left(\frac{5D-2}{12}\right)+\Delta i_L\left(\frac{1-I_o}{2}\right)+\frac{I_o}{2(1-D)}\right)+\frac{V_F P_o}{2V_o}\right]. \tag{59}$$

Equation (60) is used to calculate the power losses of the equivalent series resistance of the inductance:

$$I_{L_{1,rms}} = \sqrt{\Delta i_L^2\left(\frac{6D-2}{12}\right)+\Delta i_L\frac{1-D-I_o}{2(1-D)}+\frac{DI_o^2}{4(1-D)^2}+\frac{I_o}{2(1-D)}}, \tag{60}$$

$$P_{r_{L_1}} = r_{L_1}\left(\Delta i_L^2\left(\frac{6D-2}{12}\right)+\Delta i_L\frac{1-D-I_o}{2(1-D)}+\frac{DI_o^2}{4(1-D)^2}+\frac{I_o}{2(1-D)}\right). \tag{61}$$

In order to calculate the equal series resistance losses of the capacitor C and the effective current of capacitor C, equation (62) is used, and this loss is calculated as (63).

$$I_{c,rms} = \sqrt{I_o^2-\Delta i_L^2\left(\frac{5D-2}{6}\right)+\Delta i_L(1-I_o)+\frac{I_o}{(1-D)}}, \tag{62}$$

$$P_{r_c} = r_c\left(I_o^2-\Delta i_L^2\left(\frac{5D-2}{6}\right)+\Delta i_L(1-I_o)+\frac{I_o}{(1-D)}\right). \tag{63}$$

The total power losses of the converter are obtained using the following:

$$P_{\text{loss}} = P_{\text{Switch}} + P_D + P_{r_L} + P_{r_c}. \tag{64}$$

Using (54), (59), (61), (63), and (64), the converter efficiency is equal to the following:

$$\eta = \frac{P_o}{P_o + P_{\text{loss}}} = \frac{P_o}{P_o + a\Delta i_L^2 + b\Delta i_L + c}, \tag{65}$$

where

$$a = \left(\frac{r_{DS_1}D}{6}+R_{F,D_4}\left(\frac{5D-2}{6}\right)+r_{L_1}\left(\frac{6D-2}{12}\right)-r_c\left(\frac{5D-2}{6}\right)\right), \tag{66}$$

$$b = \left(-r_{DS_1}\frac{DI_o}{(1-D)}+R_{F,D_4}(1-I_o)+r_{L_1}\frac{1-D-I_o}{2(1-D)}+r_c(1-I_o)\right), \tag{67}$$

$$c = \frac{DI_o^2}{2(1-D)^2}\left(r_{DS_1}+\frac{r_{L_1}}{2}\right)+\frac{I_o}{(1-D)}\left(R_{F,D_4}+\frac{r_{L_1}}{2}+r_c\right)+\left(\frac{2f_sC_{s_1}P_oR_o}{D^2}\right)+\frac{V_FP_o}{2V_o}+r_cI_o^2. \tag{68}$$

Using (33), the relation between input current ripple and inductor current ripple is obtained as follows:

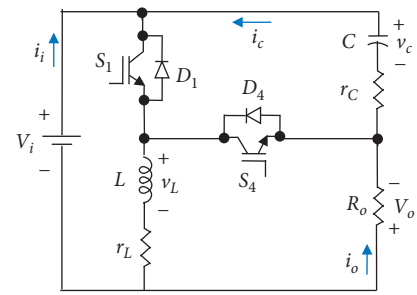

Figure 12: Single-phase equivalent circuit of the proposed converter with parasitic elements.

$$\Delta i_i = i_i(t_1)-i_i(t_0) = i_{L1}(t_1)+i_{L2}(t_1)-i_{L1}(t_0)-i_{L2}(t_0) = \Delta i_{L1}+i_{L2}(t_1)-i_{L2}(t_0). \tag{69}$$

According to Figure 2, $i_{L2}(t_1)-i_{L2}(t_0)$ has a negative value, so the input current is less than the value of the inductor current ripple. Also, according to equation (69), the input current ripple is directly related to the inductor current ripple. Therefore, with the increase in the input current ripple, the inductor current ripple also increases. The effective value of the component current increases, and as proved in equations (54), (59), (61), and (63), the converter losses increase, and according to (65), the converter efficiency decreases.

7. Dynamic Modeling

In this section, the dynamic model of the proposed converter is presented. Since the input current is divided equally between phases, the equivalent circuit is used to model the proposed converter [18]. Modeling for the equivalent circuit of the converter in forward operation is performed. For this purpose, according to Figure 12, a phase has been used in which the actual model of the inductor and capacitor is used. In Figure 12, $L = L_1/2$ and $r_L = r_{L1}/2$ and the switch S_1 is in on state for DT_s during a switching period and for $(1-D)T_s$ is in off state. In these intervals, the equations for the inductor voltages and capacitor currents are given by

$$v_L(t) = \begin{cases} V_i - r_L i_L, & 0 < t < DT_s, \\ -V_o - r_L i_L, & DT_s < t < T_s, \end{cases} \tag{70}$$

$$i_c(t) = \begin{cases} I_o, & 0 < t < DT_s, \\ I_o - i_L, & DT_s < t < T_s. \end{cases} \tag{71}$$

In order to achieve the average model of the converter, an average method for states variables is used. By applying this method on (70) and (71), the average model of the proposed converter is obtained as follows:

$$f_1(x) = \frac{d\langle i_L\rangle}{dt} = \frac{V_i}{L}-\frac{r_L}{L}\langle i_L\rangle-\frac{1-d}{L}\langle v_c\rangle, \tag{72}$$

$$f_2(x) = \frac{d\langle v_c\rangle}{dt} = \frac{1}{R_oC}\langle v_c\rangle-\frac{V_i}{R_oC}-\frac{(1-d)}{C}\langle i_L\rangle. \tag{73}$$

The relationship between the output voltage and the states variables is also in a steady state and is given by

$$V_o = \langle v_c \rangle - V_i. \tag{74}$$

To analyze the system's dynamic behavior, a small-signal model is used. To obtain the small-signal model, the following states space equations are used:

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} = f(x,u), \\ \tilde{y} = C\tilde{x} + D\tilde{u} = h(x,u), \end{cases} \tag{75}$$

where x, u, and y denote states variables, input, and output, respectively, and A, B, C, and D are matrices and calculated by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \left(\dfrac{\partial f(x,u)}{\partial x}\right)_{xe,ue} & \left(\dfrac{\partial f(x,u)}{\partial u}\right)_{xe,ue} \\ \left(\dfrac{\partial h(x,u)}{\partial x}\right)_{xe,ue} & \left(\dfrac{\partial h(x,u)}{\partial u}\right)_{xe,ue} \end{bmatrix}. \tag{76}$$

In (76), u_e and x_e represent the equilibrium points for state variables and inputs, respectively. Using (72)–(76), the following equations are obtained:

$$\begin{bmatrix} \dfrac{d\hat{i}_L}{dt} \\ \dfrac{d\hat{v}_C}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{r_L}{L} & -\dfrac{1-D}{L} \\ -\dfrac{1-D}{C} & \dfrac{1}{R_oC} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & \dfrac{V_c}{L} \\ -\dfrac{1}{R_oC} & \dfrac{I_L}{C} \end{bmatrix} \begin{bmatrix} \hat{v}_i \\ \hat{d} \end{bmatrix}, \tag{77}$$

$$V_o = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} -1 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_i \\ \hat{d} \end{bmatrix}. \tag{78}$$

Considering (75), the output-to-input transfer function is obtained as follows:

$$G = C(SI - A)^{-1}B + D. \tag{79}$$

Using (77)–(79) and Laplace transforms, the output voltage transfer functions to the input voltage and the output voltage to the duty cycle are obtained as follows, respectively:

$$G_{V_oV_i}(s) = \frac{L^2Cs + R_oL^2C^2 - (1-D)R_oLC - r_L}{R_oLC(1-D)^2s^2 + R_o(1-D)^2(r_cC-1)s - r_L(1-D)^2}, \tag{80}$$

$$G_{V_od}(s) = \frac{R_oCI_Ls + R_oCr_LI_L - R_oV_C(1-D)}{R_oLC(1-D)^2s^2 + R_o(1-D)^2(r_cC-1)s - r_L(1-D)^2}. \tag{81}$$

The amplitudes of the variables in equations (80) and (81) and the ESR of inductors L_1 and L_2 and capacitor C are listed in Table 3. The Bode diagram for transfer functions (56) and (57) is shown in Figure 13(a) and Figure 13(b), respectively. This figure shows that proposed converter has a positive phase margin and gain margin for all transfer functions that approve the proposed converter's stability.

Table 3: Used parameters in experimental prototype.

Parameters	Values
Input voltage (V_{in})	50 V
Output voltage (V_o)	Buck 35 V Boost 75 V
Output power (P_o)	200 W
Switching frequency (f_s)	30 kHz
Seri capacitance $C(r_C)$	100 μF (79mΩ)
Inductor L_1, L_2 (r_L)	450 μH (100mΩ)
Duty cycle (Buck), D	0.41
Duty cycle (Boost), D	0.6
Switches	IRFP260n

8. Comparison of the Proposed Converter with Other Structures

To confirm the advantage of the proposed converter, it has been compared with the conventional interleaved buck-boost converter (CIBBC) and other structures. Different indexes such as the number of components, input current ripple, and continuity or discontinuity of the input current are used for comparison, and the results are listed in Table 4.

As shown in Table 4, the proposed converter in all operation modes has a continuous input current. However, the input current of the conventional interleaved buck-boost converter and presented structure in [19] for buck operation is discontinuous, and the presented structures in [20–22] have a discontinuous input current for all duty cycles. In addition, the ratio of the input current ripple of the proposed converter versus other structures ($\Delta_{i,\text{proposed}}/\Delta_{i,x}$ $\{x = \text{CIBBC, [19, 20]}\}$) is provided in Figure 14, in which Figures 14(a) and 14(b) refer to the buck and boost mode, respectively.

A ratio of less than 1 indicates that the input current of the proposed converter is less than that of other converters. According to Figure 14(a), in the proposed converter, the input current ripple for $D < 0.5$ is minimal compared with other structures. As the duty cycle increases, the input current ripple ratio decreases so that the converter's input current ripple canceling capability occurs in the duty cycle equal to 50%. A ripple less current has been drawn from the power source in this duty cycle.

According to Figure 14(b), for $D > 0.5$, the input current of the proposed converter is minimal and close to zero in comparison with the structure [19], and this ratio of the input current compared with the conventional interleaved buck-boost converter is less than 1. Therefore, for all duty cycles, the input current ripple of the proposed converter is less than that of other converters. All components used in converters structures have internal resistance, which contributes to the losses and efficiency of the converter.

The higher the RMS values of current passing through the resistor, the greater the losses because the power loss in a resistor is directly related to the square of the current passed through it. As mentioned in [24, 25], the large current ripple causes the RMS value of the current to increase, which produces extra power losses. In structures presented in

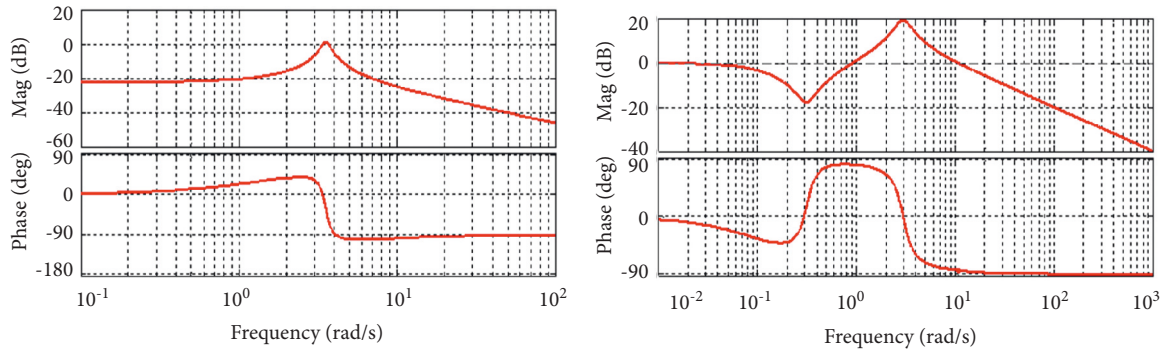

FIGURE 13: Bode diagram of the proposed converter for the output voltage transfer function to the (a) input voltage; (b) duty cycle.

[21–23], the input current is discontinuous, and the RMS value of current passing through the components increases. Since the number of components in the current path in structures [21–23] is more than the proposed converter and because of the high value of their RMS input current, the efficiency of the proposed converter is higher than that of the structures [21–23] and others except [19]. In the converter presented in [19], an additional inductor is used for soft switching, which reduces the switching losses and increases the converter's efficiency. However, the presented converter in [19] has a discontinuous input current for duty cycles less than 50%. The practical applications of the proposed converter are as follows: power supply for portable devices where the battery is discharging, obtaining the I-V curve in PV panels. In addition, the proposed converter can be used for renewable energy applications because of drawing continuous current from the DC source. Large current ripple causes, as a result, the RMS value of the current to increase that produces extra power losses and higher temperatures that advance the degradation of the renewable energy source. Furthermore, the maximum renewable source power can be extracted using a converter with a continuous input current [24, 25].

Figure 15 illustrates the normalized input current ripple with respect to the average value of the input current for all the converters. According to this figure, converter [21] has the highest input current ripple. For $D < 0.5$, the input current ripple of the proposed converter is lower than the converters [19–23] and CIBBC. Also, for $D > 0.5$, the input current ripple of the converter [26] gets higher than the presented converter and the presented converter acts better than others. In other words, as shown in Figure 15, the curve of the presented converter is placed lower than others; this illustrates that the presented converter has low input current ripple in comparison with [19–23] and CIBBC. The input current ripple ratio of the converter [27] in comparison with the proposed converter is less; however, the voltage conversion ratio of this converter in comparison with the presented converter and the conventional one for buck operation mode is not improved. Also, the high voltage stress in the components of the converter [27] causes a decrease in its efficiency.

In order to analyze the harmonic oscillation in the case of the presented converter and conventional interleaved buck-boost converter, the time-domain waveforms of $i_{i,\ proposed}$ and $i_{i,\ CIBBC}$ for the same condition are shown in Figure 16. One large DC component and the other smaller AC components from the provided frequency spectrums exist at the switching frequency and other frequencies. This indicates that except for switching frequency, more than one harmonic are distorted the waveforms. According to Figure 16(a), in the presented converter, besides fs, three new harmonics appear in the frequency spectrum, i.e., $f1 = 953$ Hz and $f2 = 2f1 = 1906$ Hz, and in frequency spectrum of the conventional converter as shown in Figure 16(b), $f1 = 714$ Hz, $f2 = 2f1 = 1428$ Hz, $f3 = f1 + f2 = 2142$, and $f4 = f1 + fs = 30714$ Hz. Among these harmonics, in the presented converter, $f1$ and fs have the most dominate role in the harmonic oscillation, whereas other harmonics do negligible role. However, in conventional interleaved buck-boost converter, the magnitude of harmonics in $f1$, $f2$, and fs is more than the presented one. Besides, two new harmonics at $f3$ and $f4$ appeared in the frequency spectrum of the conventional converter. The asymmetric waveform distortion in the conventional converter mainly results from $f3$ and $f4$ (the interactions between harmonics at frequencies $f1$, $f2$, and $f1$, fs). It is obvious that the harmonics $f1$ and $f2$ in waveform of $i_{i\ ,proposed}$ are dominated by both even and odd signal components. In the conventional converter, harmonics of $i_{i,CIBBC}$ are dominated by odd signal components.

Total harmonic distortion (THD) for the input current is defined as the effective value of all harmonics divided by the effective value of its fundamental current.

Distortion is defined as follows:

$$\text{THD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \ldots + I_h^2}}{I_1}, \tag{82}$$

where I_h is the effective current of the hth harmonics and I_1 is the effective value of the current in the fundamental frequency. In the case of harmonic absence, the THD will be equal to "0". Using (82) and the harmonics of Figure 16, the THD amplitudes for the presented converter and conventional interleaved buck-boost converter are obtained as 0.12

Table 4: Comparison of the proposed converter with other similar structures.

Case	No. of component					Maximum efficiency (%)	Normalized input current ripple ($\Delta Ii/\mathrm{Ii}$)		Input current
	Switch	Diode	Capacitor	Inductor	Total		$D > 0.5$	$D < 0.5$	
Proposed converter	4	0	1	2	7	95.6	$2(1-D)^2(D-0.5)R_o/D^2Lf_s$	$R_o(2D^2-3\ D+1)/DL\ f_s$	Continuous
CIBBC	4	0	1	2	8	88.6	$R_o(1-D)^2/Df_sL$	$(2f_sL+R_o(1-D)^2)/2\ Df_sL$	Discontinuous
[19]	2	2	1	3	8	97.7	$(2-D)/2\ D$	$(f_sL(2-D)+R_o(1-D)^2)/2\ Df_sL$	Discontinuous
[20]	2	2	1	3	7	94.7	$(f_sL(1-D)+R_o(2D^2-3\ D+1))/2\ Df_sL$		Discontinuous
[21]	5	0	3	2	10	91.5	$R_o(2D^2-5\ D+3)/3\ Df_sL$		Discontinuous
[22]	2	2	2	2	8	93	$(f_sL(1-D)+R_o(1-D)^2)/2\ Df_sL$		Discontinuous
[23]	6	0	3	4	13	90.3	$2(1-D)^2/Df_sL$		Continuous
[26]	1	3	6	4	14	94	$(9\ Df_sL_1R+(1-D)^2)/9\ Df_sL_1R_o$		Continuous
[27]	2	3	3	2	10	93.9	$((1-D)^4+4\ Df_sL_1R_o)/4\ Df_sL_1R_o$		Continuous

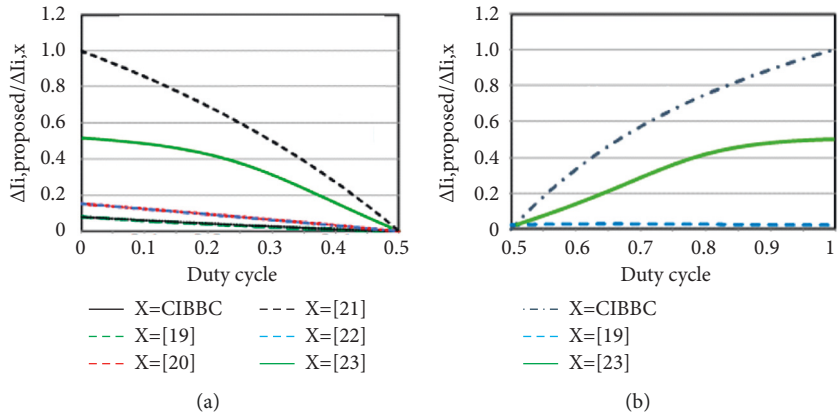

Figure 14: Input current ripple ratio in (a) buck operation and (b) boost operation.

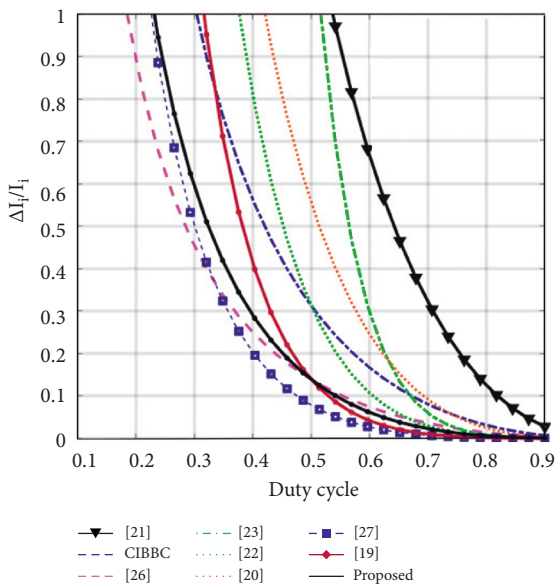

Figure 15: Normalized input current ripple to the average value of the input current.

and 0.277, respectively. So, the proposed converter's low THD amplitude compared with the conventional one confirms its better performance.

The practical THD value of the input current was obtained as 0.127. The slight difference in the practical and theoretical THD is because more numbers of harmonics are considered in the practical calculation.

9. Experimental Results

In order to confirm the theoretical analyses of the proposed converter, a 200 W prototype is built in the laboratory. This prototype is shown in Figure 17. The specifications of the circuit and components are presented in Table 3.

To calculate the practical value of inductances according to equation (29), the maximum value of load resistance and the minimum value of duty cycle are 35 ohms and 0.385, respectively. The operating frequency of the converter is also equal to 30 kHz. By substituting these values in equation (2), the minimum value of inductors is obtained as 440 μH, of which 450μH has been selected for the experimental prototype.

$$L_{1,\min} = L_{2,\min} = \frac{35 \times (1 - 0.385)^2}{30000} \simeq 440\,\mu\text{H}. \tag{83}$$

The value of capacitor C is obtained based on the minimum value of load resistance, which can be calculated using equation (31). Using this equation and the value of the parameters provided in Table 3, the minimum value of the capacitor C is equal to 86 μF.

$$C \geq \frac{2 \times 6.125 \times (1 - 0.385)^2 - 30000 \times 450 \times 10^{-6} \times (1 - 2 \times 0.385)}{2 \times 79 \times 10^{-3} \times 6.125 \times 30000 \times (1 - 0.385)} \simeq 86\,\mu\text{F}. \tag{84}$$

Therefore, for the implemented prototype, a 100 μF capacitor has been selected.

Figure 18(a) shows the PWM gate signals of the switches S_1 and S_2, and these switches operate with the duty cycle of 0.41.

The switches S_3 and S_4 are in the off state in forward buck operation, and their reverse-parallel diodes transfer the power to the load. Command signals for the gates of the switches S_1 and S_2 are shown in Figure 18(a). According to (13), for input voltage 50 V and duty cycle 0.41, the output voltage should be 35 V. The correctness of this analysis is confirmed in Figure 18(b). In addition, boost operation mode with 75 V output voltage is provided by the duty cycle of 0.6 of power switches. The experimental waveforms are given in Figures 18(c) and 18(d) that confirm the mentioned values.

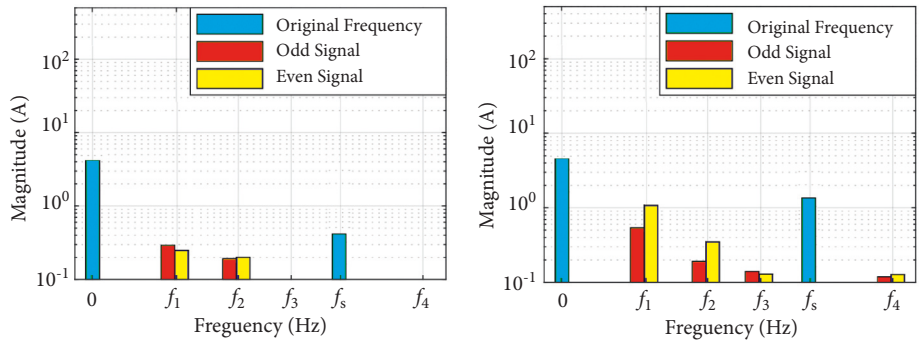

Figure 16: Frequency spectrum of input current in (a) proposed converter and (b) conventional interleaved buck-boost converter.

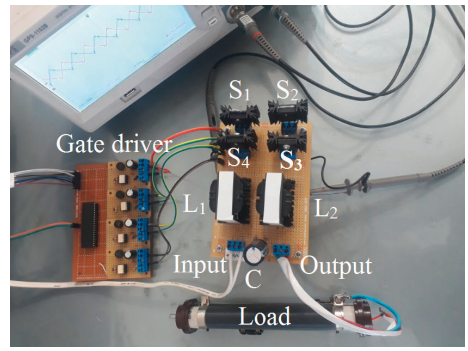

Figure 17: The experimental prototype of the proposed converter.

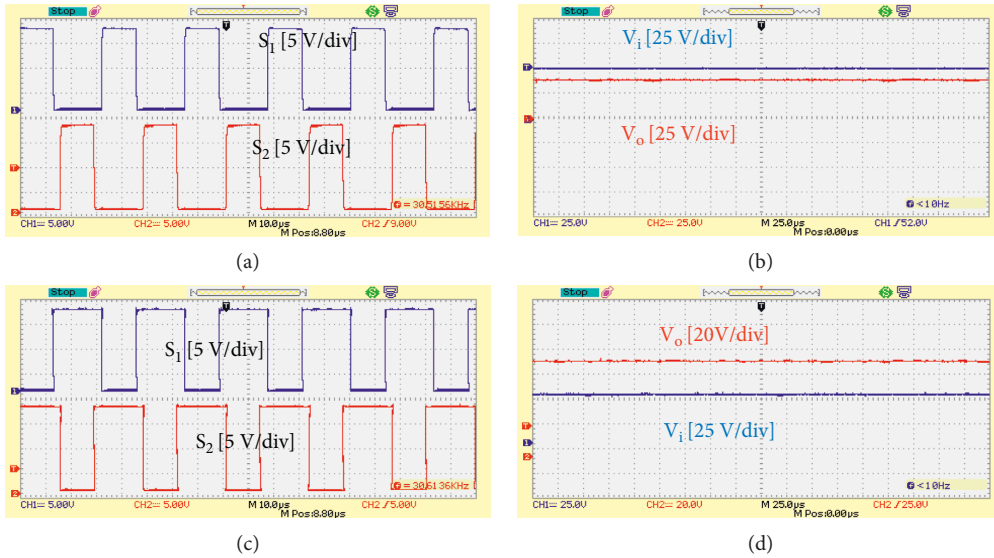

Figure 18: The experimental waveform for (a) V_{GS1} and V_{GS2} in buck mode; (b) the input and output voltages in buck mode; (c) V_{GS1} and V_{GS2} in boost mode; (d) the input and output voltages in boost mode.

As mentioned in previous sections, this converter has a continuous input current with low ripple. For duty cycle equal to 0.41, the input current ripple of this converter according to (35) is about 1 A which this ripple agrees with the experimental input current ripple at Figure 19. The conventional interleaved buck-boost converter has a closer input current ripple to the proposed one among the compared converters. The practical value of the input current ripple of conventional interleaved buck-boost converter is obtained as a coefficient of the proposed converter input

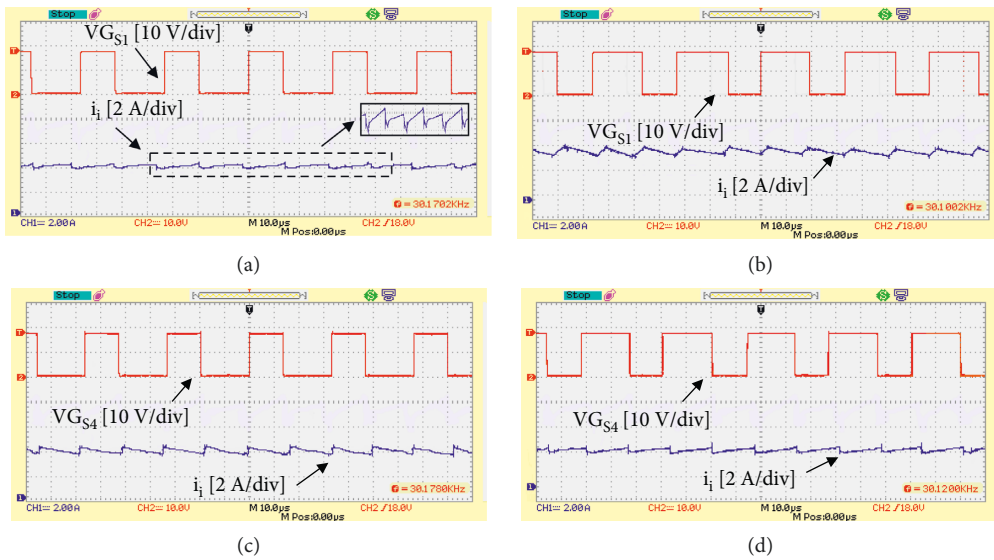

FIGURE 19: The experimental waveform of the input current for (a) forward buck operation, (b) forward boost operation, (c) reverse buck operation, and (d) reverse boost operation.

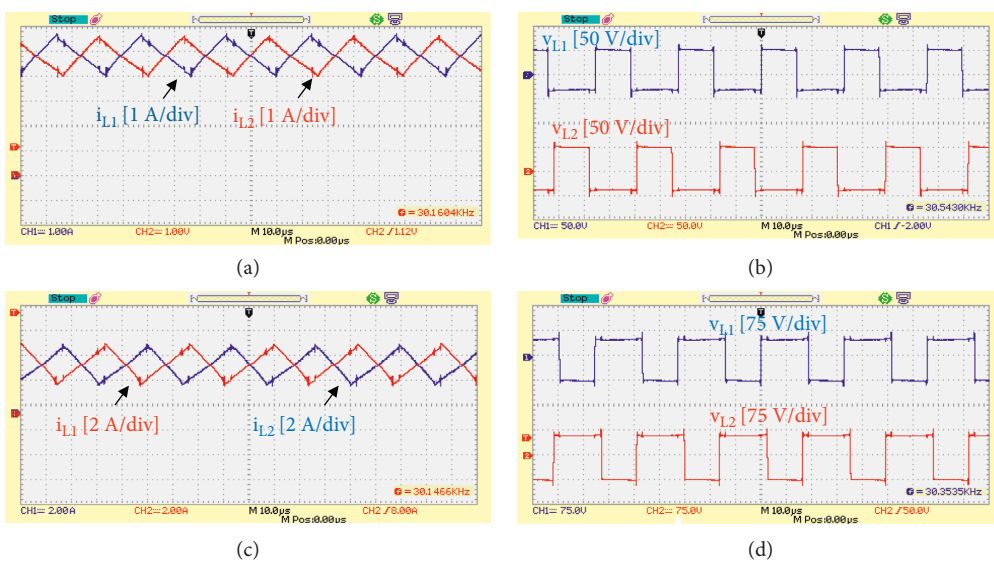

FIGURE 20: The experimental waveform of (a) inductors current in buck mode; (b) inductors voltage in buck mode; (c) inductors current in boost mode; (d) inductors voltage in boost mode.

current ripple. In the same condition, the ripple ratio of the input current in the conventional converter to the proposed converter is 2.5, which indicates that the proposed converter has less ripple than it. Also, the experimental results for forward boost, reverse buck, and reverse boost operation have been presented, respectively, in Figures 19(b)–19(d). In forward boost operation, the switches S_1 and S_2 operate with $D = 0.6$, and in reverse buck and reverse boost operation, the switches S_3 and S_4 operate with $D = 0.41$ and $D = 0.6$, respectively.

In forward buck operation, the current of the inductors L_1 and L_2 is equal to each other and, according to (27), is about 4.87 A, and the experimental results of Figure 20(a) reconfirm these amounts. As shown in this figure, the current i_{L1} increases and decreases linearly when switch S_1 is turned on and turned off, respectively, and the current i_{L2} vice versa. In boost operation mode, according to equation (27), the average value of inductor L_1 and L_2 should be equal to 3.3 A; the correctness of this current is demonstrated in Figure 20(c). In time intervals that switches are turned on, the currents of inductors increase, and in the off state of switches, the inductors' currents decrease (Figures 20(a) and 20(c)). The applied voltage to the inductors L_1 and L_2 in buck and boost operation modes is shown in Figures 20(b) and 19(d), respectively. The applied voltages to the inductors L_1 and L_2 are shown in Figure 20(b). According to theoretical

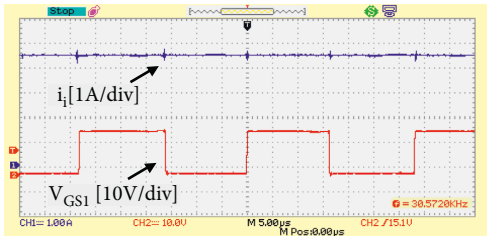

Figure 21: Input current ripple cancelation in selected duty cycle.

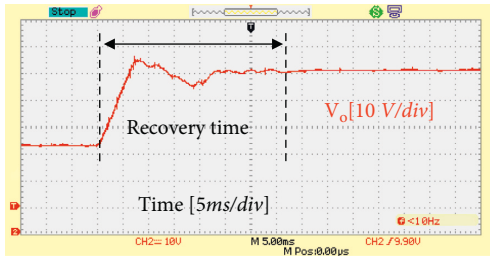

Figure 22: Output voltage changing in case of sudden changes of the duty cycle from 0.4 to 0.55.

analyses, when switch S_1 is turned on, the voltage applied to L_1 is $v_{L1} = 50$ V; otherwise, $v_{L1} = 35$ V. When S_2 is turned on, the voltage applied to L_2 is $v_{L2} = 50$ V, and in off-state time intervals of the mentioned switch, v_{L2} is equal to 35 V. Figure 20(b) confirms the correctness of these analyses.

According to equations (1) and (2), the proposed converter in the duty cycle of 0.5 has the property of eliminating the input current ripple. The switch's duty cycle has been set to the mentioned value to demonstrate this capability in the experimental prototype. Experimental waveforms of the switch's command and input current are shown in Figure 21. As can be seen, in this duty cycle, the input current ripple is zero, which confirms the theoretical analysis.

In order to observe the dynamic behavior of the proposed converter, the step response of the system is shown in Figure 22. This step response is obtained by changing the duty cycle suddenly from 0.4 to 0.55. It can be seen that the recovery time for the proposed converter is 35 ms.

10. Conclusion

In this paper, an interleaved nonisolated bidirectional buck-boost DC-DC converter is proposed. The operation principle of this converter, design consideration, and its dynamic modeling are detailed completely. Unlike conventional interleaved buck-boost converter that has discontinuous current for buck mode, the input current of this converter is continuous. It has a low ripple for both buck and boost modes. The analyses showed that the ratio of the input current ripple of the proposed converter to the conventional interleaved converter and other similar interleaved converters for all duty cycles is much less than 1. Also, this converter has low components in comparison with similar converters. Other properties of the proposed converter are low current stress of the components, the small size of the input filter, power flow in two directions, improved efficiency, and increased life of the component. This structure has a maximum efficiency of 95.6%, and finally, a prototype approved the theoretical analysis.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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