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Research Article

Performance Analysis of Diode-Assisted Switched LC qZSI Network-Based Multioutput Series-Parallel Topologies in Microgrid Application

Shri Prakash Sonkar, Vivek Nandan Lal, and Rajeev Kumar Singh

Department of Electrical Engineering, Indian Institute of Technology (BHU), Varanasi, Uttar Pradesh, India

Correspondence should be addressed to Shri Prakash Sonkar; shriprakashs.rs.eee16@iitbhu.ac.in

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In this paper, two (series and parallel versions) quasi *Z* source inverter (qZSI)-based multioutput series-parallel topologies capable of supplying multiple three-phase AC and single boost DC outputs simultaneously are presented. The proposed parallel version topology can supply *n* number of AC outputs along with one boost DC with constant voltage and variable current. Similarly, the series version topology can give *n* number of AC including one boost DC output with constant current and variable voltage. The outputs of the proposed topologies can feed directly to DC/AC microgrids and multiple residential loads simultaneously without using any extra adapter/regulator and thereby avoiding local power conversion to meet the load demand. A hybrid pulse width modulation technique with constant frequency is used to operate the proposed topologies. The performance of the proposed topologies is verified by developing the prototypes of 2.18 kW (for parallel version) and 2.02 kW (for series version) for two three-phase AC outputs and one boost DC output. The developed prototypes show measured efficiency of 90.01% for the parallel and 89.95% for the series version topology.

1. Introduction

In recent times, the idea of the AC/DC hybrid microgrid systems (HMGS), containing many electronically controlled strategies of parallel-connected distributed resources that are capable of functioning in both islanded and grid-connected modes, evolved rapidly. It is a systematic approach to interconnect various converter outputs, renewable energy sources, energy storage systems, and local loads within certain areas. The HMGS also provides reliable, low-cost, renewable energy, improves local resilience, and improves the regional electric grid's operation and stability [1, 2]. Moreover, the required prerequisite for futuristic houses with AC/DC loads is a hybrid microgrid. For modern electrical applications such as hybrid microgrids, hybrid electric vehicles, standby power supplies, etc., conventional single-output converters cannot fully meet the simultaneous requirements of different types of voltage outputs [3]. As a result, increasing hybrid microgrid applications and other residential loads need power converters that provide multiple outputs simultaneously. Hybrid multioutput converters (MOCs) are becoming prominent to achieve these requirements due to their ability to generate multiple AC and DC outputs simultaneously. Besides, MOCs are a cost-effective alternative to solve the power supply issue in remote areas far from the grid. There are several advantages of these converters, such as higher power density, compact size, lower costs, and better reliability [4].

Many studies are ongoing due to the demand and benefits of hybrid MOCs and the literature lists different hybrid MOCs. The MOCs discussed in [5–8] are primarily DC/DC converters able to supply dual DC output using single or dual DC input. However, it does not have any AC at the output. Literature [9] presents a *Z* source-based bidirectional multiport DC/DC converter that can produce only DC. It is unable to produce multiple AC at the output and requires an additional input filter as the proposed converter has a discontinuous input current. Paper [10] deliberates a *Z*

source-based converter capable of supplying dual AC using two DC inputs and nine switches. However, it is unable to produce DC at the output and needs an additional input filter to make the input current continuous. Topology [11] presents a DC-DC converter with a single input and multiple DC outputs having buck-boost capability with reduced switching losses, but no AC at the output. Article [12] presents a Z source-based dual-input single-output three-phase inverter with a high voltage gain. However, it is not equipped to produce multiple AC at the output. Paper [13] presents a DC-DC buck-boost converter topology with high voltage gain and dual outputs. However, it does not have any AC at the output. A high-efficiency coupled inductor-based DC-DC converter with single DC input multiple DC outputs is proposed in [14]. However, it does not have any AC at the output. Paper [15] proposed a novel nonisolated single-input dual output three-level DC-DC converter for medium and high voltage applications. However, it does not have any AC at the output. Manuscript [16] presents a novel integrated DC/DC topology with step-up and step-down outputs. Their output voltages are regulated simultaneously with no AC at the output. Articles [17, 18] presents single-inductor multi-input multioutput (SIMIMO) DC/DC converters with a high power density and low cost. However, it does not have any provision of AC at the output. Literature [19] discusses multi-input multioutput DC-DC converter with multiple DC outputs for hybrid renewable energy applications. However, it is unable to produce multiple AC. Papers [20, 21] propose DC-DC converters that can produce multiple high step-up DC outputs using a single input. However, they also do not have any provision of AC output. In paper [22], single-stage dual-input single-output high-gain three-phase inverter able to give only single three-phase AC output is proposed. However, it is unable to produce multiple AC at the output. Article [23] proposes a single-stage nonisolated bidirectional multiport DC-DC converter able to produce only DC output. However, it is unable to produce multiple AC at the output. Paper [24] proposes a high peak output power and high power conversion efficiency single-inductor multi-input multioutput (SIMIMO) converter for energy harvesting systems. However, it uses multiple inputs to produce multiple outputs. It is for low power applications and is unable to produce multiple three-phase AC outputs. Article [25] is a multicell multi-input multioutput reconfigurable converter that is unable to produce multiple AC at the output. In [26] a single-phase single-stage single-inductor multioutput DC-AC buck hybrid converter for battery charging application is proposed. It is can perform only buck operations at low power. It is unable to produce multiple three-phase AC at the output. Topology discussed in [27] is three-phase MOCs able to produce unregulated three-phase multiple AC outputs with no DC at the output. Hybrid MOCs discussed in [28] can produce a single DC and three-phase AC output simultaneously from a single DC input. Both the DC and three-phase AC outputs can be independently regulated. However, it is unable to produce multiple AC at the output. MOCs presented in [29] can supply single-phase regulated AC along with one DC output but not multiple AC. Paper [30] proposed a boost-derived converter that gives unregulated DC and AC outputs but not multiple AC. The topologies proposed in [31, 32] are an interleaved high-gain converter that gives simultaneous unregulated DC and AC outputs but not multiple AC. In [33], a minimum phase dual output hybrid converter with simultaneously regulated AC and DC outputs is presented. However, it is not equipped to offer multiple AC outputs. Hybrid MOC deliberated in [34] is a qZSI-based buck-boost MOC with dual DC and single AC outputs. With only one AC, it can supply two DC outputs in a wide range of output voltages.

In general, existing MOCs have various limitations such as the following: (1) some can produce only multi-DC outputs and cannot produce AC output, (2) some of them can produce both AC and DC having single DC or multiple DC with one AC output and cannot supply multiple AC outputs, (3) the existing hybrid MOCs are having only one AC output, that is single-phase, and thus, they are suitable only for low power application, and (4) no MOC provides multiple three-phase AC outputs and thus, they are not suitable for high power applications.

Therefore, to fulfil the abovementioned gap/limitations the qZSI network-based multioutput series-parallel topologies are proposed in this paper which have the following advantages:

(1) The proposed topologies can produce regulated multiple three-phase AC and single DC outputs simultaneously with different voltage/current

(2) The proposed topologies inherit all the features of the qZSI

(3) The suggested topologies have inherent shoot-through (ST) protection with buck and boost, AC as well as DC voltage capability

(4) Due to single-stage conversion, the proposed topologies have fewer losses and are compact, which results in higher power density and efficiency compared to the traditional multioutput converter

(5) It is less susceptible to electromagnetic interference (EMI)

(6) Like Z source inverter-based multioutput converters, the proposed topology does not require any input filter since it has continuous input current

(7) It has fewer voltage/current stresses on passive components compared to the Z source inverter

(8) For DC-DC and DC-AC power conversion in the hybrid microgrid, renewables, uninterrupted power supplies, and residential AC/DC loads, the proposed topologies outputs can be used

(9) Since it can supply multiple AC along with single DC outputs, the electricity bill can be saved and surplus power can be sold to the government

(10) The proposed topologies can operate at different voltages and frequencies, i.e., 50 and 60 Hz

The configuration of the proposed topologies and principles of operation are explained in Section 2. The hybrid PWM control strategy is explained in Section 3. The theoretical validation is done with hardware results in Section 4. Finally, Section 5 concludes the paper.

2. Proposed Series-Parallel Topologies

Figures 1(a) and 1(b) show the circuit diagrams of the proposed topologies in parallel and series versions. By replacing the inverter switch of qZSI with n number of parallel or series connected three-phase inverters, the proposed parallel or series version converter topologies are formed. The Z source network of the proposed topologies of both versions (i.e., parallel and series) has used the same number of components (three capacitors, two inductors, and two diodes). Figure 1(a) depicts the proposed parallel version converter, capable of supplying n number of three-phase AC outputs with the constant voltage and variable currents along with one boost DC simultaneously.

Similarly, the series version can give n number of three-phase AC outputs with different voltage and constant load current along with one boost DC. In addition, a circuit modification is done by inserting a parallel branch with a filter capacitor (C_{dc}) in series with a diode (D_y) across the dc-link voltage of the quasi Z source network to obtain the DC output. The suggested topologies are validated for ($n = 2$) two inverter units (i.e., for two three-phase AC) and one boost DC in this work. All the outputs can be independently regulated as they are working in voltage mode control.

2.1. Operation Principle, Derivation of Boost Actor, of the Proposed Topologies. The proposed topologies operate in the same way as traditional ZSIs, with shoot-through (ST) and non-shoot-through (NST) states [35].

2.1.1. Shoot-Through (ST) State. To illustrate the circuit behavior during the ST state, the circuit is simplified by replacing inverters with short circuit switches, as shown in Figure 2. All the power switches of all the legs are turned ON at the same time, and the inverter bridge operates in the short circuit mode; consequently, the dc-link voltage v_{inv} is equal to zero. Diodes D_x and D_y, are reverse biased and currents through them are zero. The reverse-biased diode D_y prevents a short circuit across the capacitor C_{dc} and thus protects against circuit damage. The source voltage v_{in} and capacitors C_a and C_b discharge the energy to inductors L_a and L_b. The time interval of this mode is D_sT_s, where D_s is the ST duty ratio during one switching period T_s. By applying KVL and KCL to Figure 2, the equations are given in

$$\left.\begin{aligned} &L_a\frac{di_{La}}{dt} = v_{in} + v_{ca}; C_a\frac{dv_{ca}}{dt} = -i_{La},\\ &L_b\frac{di_{Lb}}{dt} = v_{cb}; C_b\frac{dv_{cb}}{dt} = -i_{Lb},\\ &v_{inv} = 0; C_{dc}\frac{dv_{c\,dc}}{dt} = -i_{DC} = -\frac{v_{DC}}{R_{DC}},\\ &v_{Dx} = v_{ca} + v_{cb}; i_{Dx} = i_{Dy} = 0. \end{aligned}\right\} \quad (1)$$

2.1.2. Non-Shoot-Through (NST) State. Figure 3 depicts the proposed topologies corresponding circuit diagram in the NST state. An inverted current source (i_{inv}) with a potential v_{inv} represents the three-phase inverter units. None of the switches is triggered at the same time. The voltages through the diodes D_x and D_y are zero since they are forward biased. In this state, the inductors L_a and L_b discharge energy and capacitors C_a and C_b store it, and the dc-link voltage v_{inv} is not zero. This operating mode's time interval is $(1 - Ds)T_s$. The following equations are given by expression (2) by applying KVL and KCL to Figure 3.

$$\left.\begin{aligned} &L_a\frac{di_{La}}{dt} = v_{in} - v_{cb}; C_a\frac{dv_{ca}}{dt} = i_{La} - i_{dx},\\ &L_b\frac{di_{Lb}}{dt} = -v_{Ca}; C_b\frac{dv_{cb}}{dt} = i_{Lb} - i_{dx},\\ &v_{inv} = v_{Ca} + v_{cb}; C_{dc}\frac{dv_{c\,dc}}{dt} = i_{Dy} - i_{DC},\\ &v_{Dx} = v_{Dy} = 0; i_{Dx} = i_{La} + i_{Dy} - i_{inv}. \end{aligned}\right\} \quad (2)$$

2.2. Derivation of the Voltage Boost Factor. Based on the flux balance property of L_{a} and L_{b}, the average inductors voltage in steady-state over one switching period T_{s} is zero. Thus, from (1) to (2), we have

$$\left.\begin{aligned} &D_s(v_{in} + v_{Ca}) + (1 - D_s)(v_{in} - v_{Cb}) = 0,\\ &D_s(v_{Cb}) + (1 - D_s)(-v_{Ca}) = 0. \end{aligned}\right\} \quad (3)$$

Solving the above equation (3), the capacitor voltages v_{Ca}, v_{Cb} and the peak dc-link voltage v_{inv} of the proposed topology can be derived as

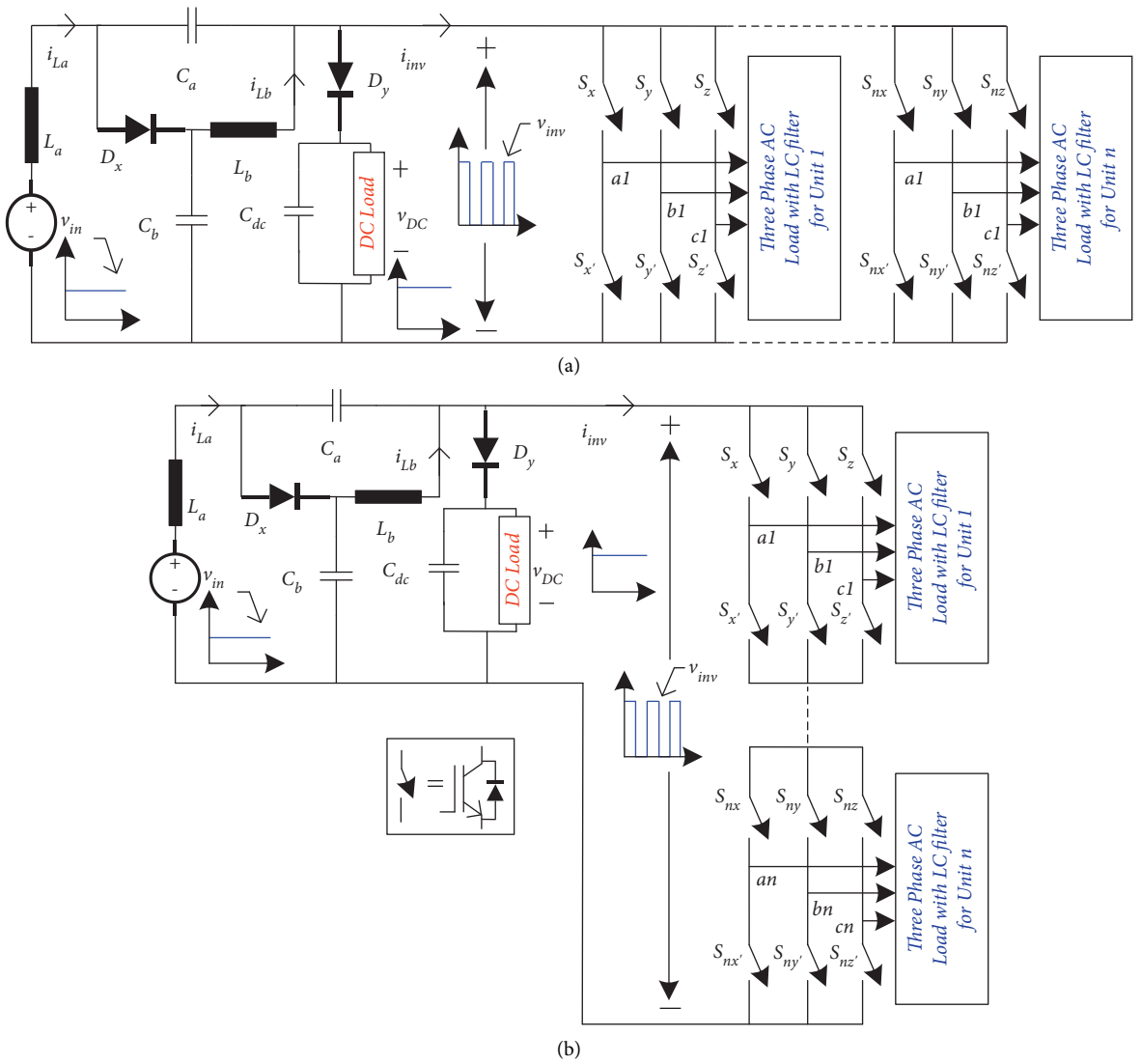
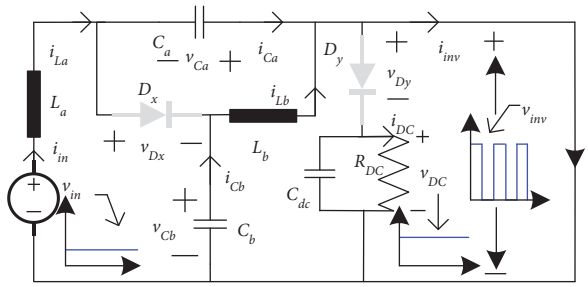


Figure 1: Proposed topologies in (a) parallel version and (b) series version.



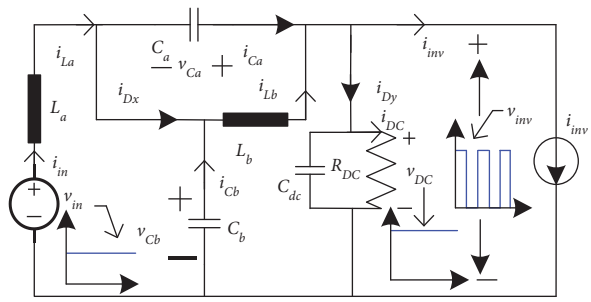
$$L_a \frac{di_{La}}{dt} = v_{in} + v_{ca}; \quad C_a \frac{dv_{ca}}{dt} = -i_{La};$$
$$L_b \frac{di_{Lb}}{dt} = v_{ca}; \quad C_b \frac{dv_{cb}}{dt} = -i_{Lb};$$
$$v_{inv} = 0; \quad C_{dc} \frac{dv_{cdc}}{dt} = -i_{DC} = -\frac{v_{DC}}{R_{DC}};$$
$$v_{Dx} = v_{ca} + v_{cb}; i_{Dx} = i_{Dy} = 0; \quad (1)$$

Figure 2: Equivalent circuit diagram in ST state of the proposed series and parallel topology.

$$v_{Ca} = \frac{D_s}{1-2D_s} v_{in}; v_{Cb} = \frac{1-D_s}{1-2D_s} v_{in},$$
$$v_{inv} = v_{DC} = \frac{1}{1-2D_s} v_{in}. \quad (4)$$

Similarly, according to the charge balance principle, the average capacitor current in C_a and C_b in steady-state over one switching period T_s is zero. Therefore, from (1) and (2),

$$D_s(-i_{La}) + (1-D_s)(i_{La} - i_{dx}) = 0,$$
$$D_s(-i_{Lb}) + (1-D_s)(i_{Lb} - i_{dx}) = 0. \quad (5)$$



$$\left.\begin{aligned} & L_a \frac{di_{La}}{dt} = v_{in} - v_{cb}; C_a \frac{dv_{ca}}{dt} = i_{La} - i_{dx}; \\ & L_b \frac{di_{Lb}}{dt} = -v_{ca}; \quad C_b \frac{dv_{cb}}{dt} = i_{Lb} - i_{dx}; \\ & v_{inv} = v_{ca} + v_{cb}; C_{dc} \frac{dv_{cdc}}{dt} = i_{Dy} - i_{DC}; \\ & v_{Dx} = v_{Dy} = 0; i_{Dx} = i_{La} + i_{Dy} - i_{inv}; \end{aligned}\right\} \quad (2)$$

Figure 3: Equivalent circuit diagram in NST state of the proposed series and parallel topology.

Solving equation (5), the inductor currents i_{La} and i_{Lb} of the proposed topologies can be derived as

$$i_{La} = \frac{(1 - D_s)}{(1 - 2D_s)} i_{dx}; i_{Lb} = \frac{(1 - D_s)}{(1 - 2D_s)} i_{dx}. \quad (6)$$

From (4), the voltage boost factor (B) of the proposed topologies can be obtained as

$$B = \frac{\hat{v}_{inv}}{v_{in}} = \frac{1}{1 - 2D_s}. \quad (7)$$

From equation (7), as the shoot-through duty ratio (D_s) increases the denominator term $(1 - 2D_s)$ decreases; consequently the boost factor B increases in a rectangular hyperbola manner (Figure 4(a)) and finally becomes infinite at $D_s = 0.5$.

The peak-phase output voltage ($\hat{v}_{AC}$) of the three-phase inverter is

$$(\hat{v}_{AC})_{fun\ da\ mental} = \hat{v}_{AC} = \frac{m_a}{2} v'_{inv} = \frac{m_a}{2} \left(\frac{1}{1 - 2D_s} \right) v_{in}, \quad (8)$$

$$(\hat{v}_{AC})_{fun\ da\ mental} = \hat{v}_{AC} = \frac{m_a}{2} v'_{inv} = \frac{m_a}{2} \left(\frac{1}{2m_a - 1} \right) v_{in}. \quad (9)$$

$v_{inv}{}'$ is the input voltage of each converter unit and is equal to v_{inv} and $v_{inv}/2$ for parallel and series versions, respectively, and m_a is the modulation index of the inverter.

The modulation index (m_a) controls the inverter output voltage. The ratio of peak output voltage ($\hat{v}_{AC}$) to the DC input voltage (v_{in}) is known as gain (G) of the three-phase inverter and given by

$$G = \frac{(\hat{v}_{AC})_{fun\ d}}{v_{in}} = \frac{m_a}{2} \left(\frac{1}{1 - 2D_s} \right). \quad (10)$$

$$G = \frac{(\hat{v}_{AC})_{fun\ d}}{v_{in}} = \frac{m_a}{2} \left(\frac{1}{2m_a - 1} \right). \quad (11)$$

From (10), it is clear that the AC gain (G) is directly proportional to modulation index (m_a) and inversely proportional to D_s. It increases as the m_a increases at constant D_s. The D_s must be less than 0.5 because, at $D_s = 0.5$, the G will become infinite. The gain of the proposed topologies is the same as the gain of conventional qZSI. Equation (11) represents the relation between G and m_a, and as the m_a increases, the G also increases. The value of m_a cannot be equal to 0.5 because, at $m_a = 0.5$, G will become infinite. For better performance, high efficiency, and ripple-free sinusoidal AC output of the proposed topologies, the value of D_s should be small and m_a should be large.

Note that the hybrid PWM used for this proposed topology has the following limitations for the m_a and duty ratio (D_s).

$$D_s + m_a \leq 1. \quad (12)$$

Figure 4(a) shows the variation of boost factor (B) with respect to D_S. As the D_S increases the denominator term, $(1 - 2D_s)$ decreases which is inversely proportional to the B. Therefore, as the D_S increases the B increases in a rectangular hyperbola manner, which can be seen and verified from Figure 4(a) and equation (7). Figure 4(b) shows the variation of AC gain (G) with respect to modulation index (m_a) since G is directly proportional to m_a; therefore, as the m_a increases G also increases in a straight-line manner, which can be justified from Figure 4(b) and equation (10). Figure 4(c) shows a graphical 3D representation of the variation of the gain G with D_s and m_a, where G is the ratio of peak v_{AC} and input DC voltage v_{in}. The operating region of the proposed topologies is shown in Figure 4(d). As D_s and m_a increase, the operating region also increases of the proposed topologies; however, the sum of D_s and m_a cannot be more than 1.

2.3. Mathematical Expression for AC and DC Power. The following sections give the AC and DC power expressions for the parallel and series versions of the proposed topologies with two inverter modules.

2.3.1. Proposed Parallel Version Topology. The input voltage for both the inverter units in the parallel version will be the same and equal to v_{inv}. For the same reference voltages (v_{ref}) and balanced AC loads, the peak AC voltages ($\hat{v}_{\text{AC1}}$ and $\hat{v}_{\text{AC2}}$) will be equal, as v_{inv} for both inverter units will be equal and expressed by (8). The $\hat{v}_{\text{AC1}}$ and $\hat{v}_{\text{AC2}}$ will be different for different v_{ref} to the inverter modules. v_{ref} is the peak value of the inverter unit's required AC output voltage ($\hat{v}_{\text{AC}}$). For both converters, the gain G will be the same and expressed by (10) and (11).

From (8), the rms AC output voltage ($v_{AC,rms} = \hat{v}_{AC}/\sqrt{2}$) is given as

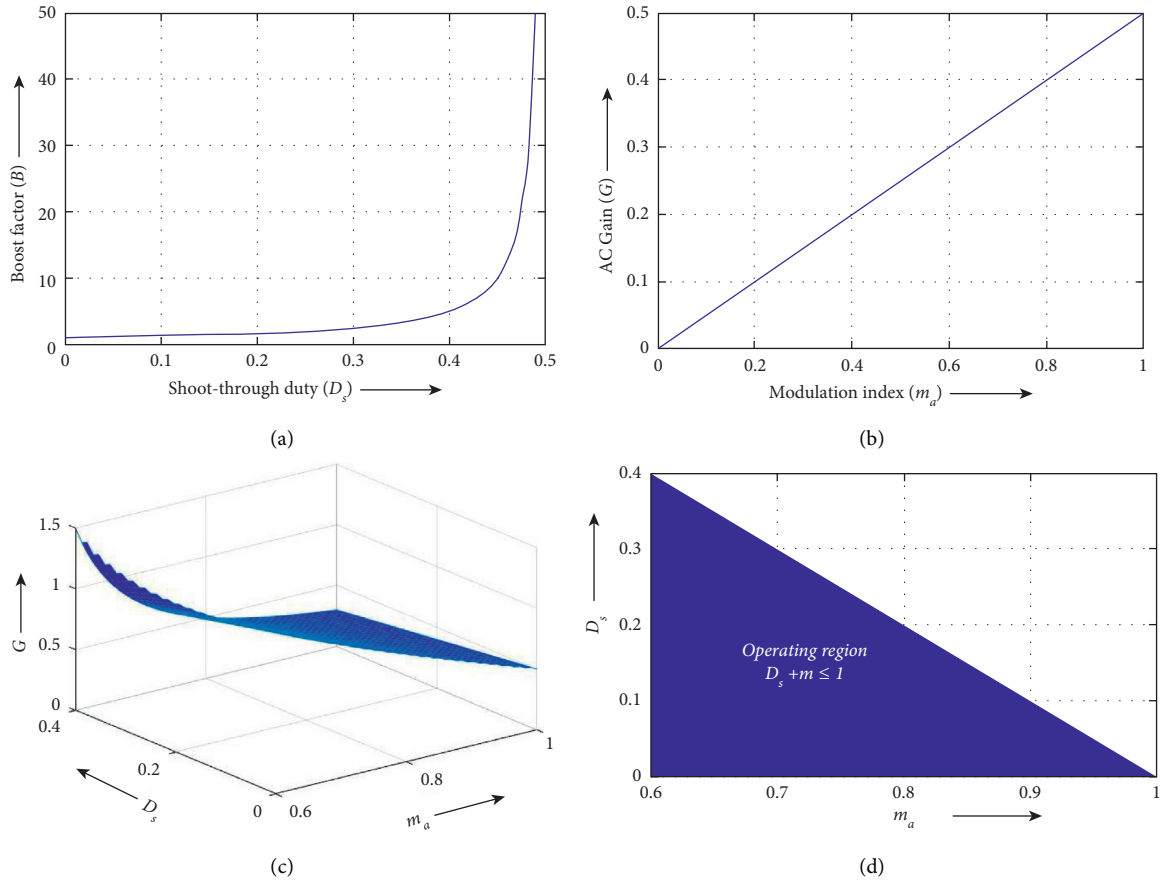


FIGURE 4: Different plots among B, D_s, m_a, and (G). (a) The plot between (G) and m_a, (b) graph between (B) and D_s, (c) 3D plot between AC voltage gains (G), D_s, and m_a, and (d) operating region of the proposed converter topologies.

$$v_{AC,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}} = \frac{GV_{in}}{\sqrt{2}} = \frac{m_a}{2\sqrt{2}}\left(\frac{1}{1-2D_s}\right)v_{in}. \tag{13}$$

The three-phase AC power output ($P_{3\text{-}\varnothing}$) of both units at the same v_{ref} is

$$P_{3-\varnothing} = 6\frac{v_{AC,rms}^2}{R_{AC}} = 6\frac{m_a^2 B^2 v_{in}^2}{8R_{AC}}. \tag{14}$$

Similarly, the three-phase AC power output $P_{3-\varnothing}$ of both units at different v_{ref} is

$$P_{3-\varnothing} = 3\frac{\left(m_{a1}^2 + m_{a2}^2\right)B^2 v_{in}^2}{8R_{AC}}, \tag{15}$$

where m_{a1} and m_{a2} are the modulation indices of inverter units 1 and 2, respectively, and R_{AC} is the AC load resistance.

The DC output power P_{DC} of the proposed topology in parallel version is

$$P_{DC} = \frac{v_{DC}^2}{R_{DC}} = \frac{v_{in}^2}{R_{DC}\left(1-2D_s\right)^2}, \tag{16}$$

where R_{DC} is the DC load resistance of the proposed topologies. It is clear from (15) and (16) that $P_{3\text{-}\varnothing}$ depends on m_a and D_s both whereas P_{DC} depends only on D_s.

2.3.2. Proposed Series Version Topology. In a series version with two units, the dc-link voltage (v_{inv}) is equally divided across the inverter units for a balanced AC load. The peak AC voltages ($\hat{v}_{AC1}$&$\hat{v}_{AC2}$) will be equal for the same voltage reference (v_{inv}) and given as (from (8)):

$$\hat{v}_{AC1} = \hat{v}_{AC2} = \frac{m_a}{2}\frac{v_{inv}}{2} = \frac{m_a}{4}\left(\frac{1}{1-2D_s}\right)v_{in}. \tag{17}$$

The rms AC output voltage ($v_{AC,rms}$) for both units is given as

$$v_{AC,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}} = \frac{m_a}{4\sqrt{2}}\left(\frac{1}{1-2D_s}\right)v_{in}. \tag{18}$$

The three-phase AC power output $P_{3-\varnothing}$ of a single unit is given as

$$P_{3-\varnothing} = 3\frac{v_{AC,rms}^2}{R_{AC}} = 3\frac{m_a^2 B^2 v_{in}^2}{32R_{AC}}. \tag{19}$$

The three-phase AC power output ($P_{3-\varnothing}$) of both units is given as

$$P_{3-\varnothing} = 6\frac{v_{AC,rms}^2}{R_{AC}} = 6\frac{m_a^2 B^2 v_{in}^2}{32R_{AC}}. \tag{20}$$

The DC output power P_{DC} of the series version is the same as that of the parallel version expressed in (16). Since $\widehat{v}_{\mathbf{AC}}$ is directly proportional to m_a of the inverter and equal to the peak value of v_{ref} in voltage control mode, as the v_{ref} is increased, the m_a increases due to which output power increases and vice versa.

2.4. Voltage and Current Stresses of the Components of the Proposed Topologies. The voltage and current stresses of each component of the proposed topologies are shown in Table 1. In the case of parallel version, if the number of converter units increases the current stress on L_a, L_b, and D_x increases, since these elements are dependent on i_{in} and i_{inv}. As the input voltage (i.e., switch node voltage v_{inv}) depends only on constant ST duty D_s, the v_{inv} remains constant consequently; there will be no voltage stress. However, in the series version, as the number of inverter units increases, v_{in} also increases to get the desired output voltage; therefore, the voltage stresses on capacitors and diodes increase, and current stresses remain constant.

With the increase in the stress of the front-end passive components (inductors, diodes, and capacitors of the impedance network), the rating will increase and so the cost of individual components increases. However, as the passive components counts are fixed irrespective of the number of units, the overall cost of the proposed topologies for more number units will be less in comparison with the same number of converters connected independently even for three-phase loads. Therefore, it is worthwhile and justified to use the proposed topologies with multiple units for practical applications.

Figures 5(a) and 5(b) show the variation of voltage and current stress with respect to D_S. From (21) as the D_S increases the voltage stress across the capacitors (C_a and C_b) and diodes (D_x and D_y) increases. Similarly, the current stress of inductors (L_a and L_b) increases (6).

$$V_{Ca} = \frac{(D_s)v_{in}}{(1-2D_s)},$$

$$V_{Cb} = \frac{(1-D_s)v_{in}}{(1-2D_s)}, \tag{21}$$

$$V_{Dx} \text{ and } V_{Dy} = \frac{v_{in}}{(1-2D_s)}.$$

Cost analysis of two single-unit individual converters and the proposed topologies with two units connected in parallel for the same power (total 2.18 kW) is carried out as shown in Tables 2 and 3, respectively. The total number of components (passive elements and switches) is 26 and the cost is 130.36 (USD) in the case of two single-unit individual converters. However, in the case of the proposed topology with two units, the number of components is 19 and the cost is 116.74 (USD). The number of components is less in the proposed topologies with two units, because the passive components are fixed. It is clear from Tables 2 and 3 that, for proposed topologies with two units, the price per component is high due to increased stress/rating. However, the overall cost is less as compared with its counterparts, i.e., two single-unit individual converters.

2.5. Comparative Analysis among Existing Topologies and Proposed Topologies. The proposed topologies are compared with the closely related topologies in Table 4. The table demonstrates some meaningful merits of the proposed topologies in comparison with the existing converter topologies.

3. Control Strategy for the Proposed Topologies

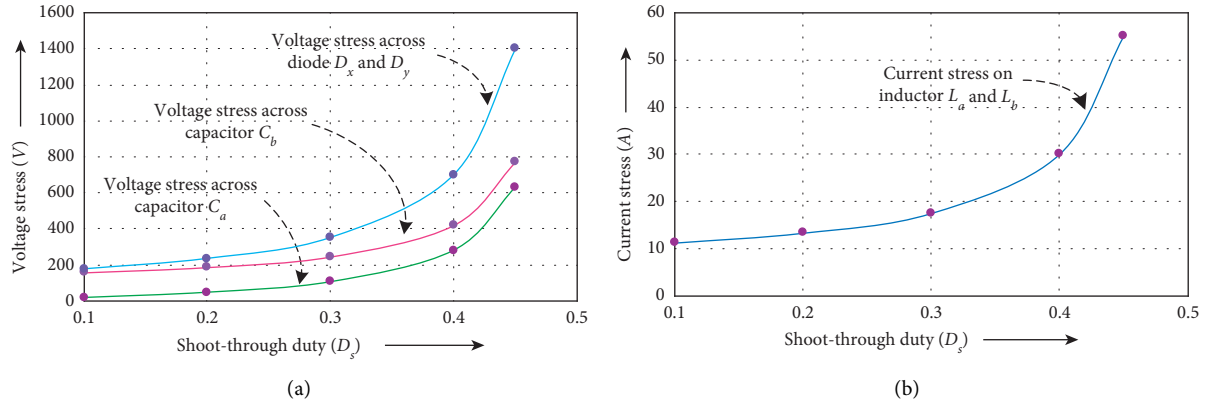
For the proposed topologies, the control strategy to control the DC/AC power flow is defined in the following sections.

3.1. Hybrid Pulse Width Modulation (PWM) Scheme for the Proposed Topologies. A hybrid sinusoidal pulse width modulation scheme with constant frequency shoot-through is implemented on the DSP board to control the proposed topologies. Using the hybrid PWM modulation method, the switching signals for NST and ST state for Z source inverters are obtained [36]. The complete modulation scheme of the proposed switching signal topology is shown in Figure 6. The modulation scheme's logic diagram is shown in Figure 6(a) and the corresponding switching signals are shown in Figure 6(b). For switches 1 to 6 of unit 1, sx to sz' are corresponding switching signals. By comparing the reference triangular waves with three-phase modulating sinusoidal signals ($\mathrm{m_a}$, $\mathrm{m_b}$, and $\mathrm{m_c}$) and their complementary signals, the switching signals are generated. The magnitudes of the modulating sinusoidal signals are as per the reference AC output voltages. The ST periods are decided by comparing the reference triangular waves with two constant $\mathrm{d_c}$ signals (upper $v_{\mathrm{u(dc)}}$ and lower $v_{\mathrm{l(dc)}}$), the magnitude of which is decided by the required DC output voltage. When the triangular carrier wave is higher than the upper constant dc signal $v_{\mathrm{u(dc)}}$ or less than the lower dc signal $v\mathrm{l}_{\mathrm{(dc)}}$, ST signals are generated. In the ST condition, switches of all the legs are ON at the same time. The signal for the first leg of the inverter is produced by comparing $\mathrm{m_a}$ and its complement with the triangular carrier wave. With the addition of the ST switching signals, signals sx and sx' are generated for upper and lower first leg switches, respectively. Comparing the carrier wave with $\mathrm{m_b}$ and $\mathrm{m_c}$, respectively, as well as dc modulating signals, produces switching signals for the second and third legs (sy, sy') and (sz, sz').

Figure 6(b) shows the PWM signals with the modulation index $m_{\mathrm{a}} = 0.3684$ and $D_{\mathrm{st}} = 0.3158$ for inverter unit 1 (Figure 7(d)) with v_{ref} 70 V and v_{dcref} 380 V. However, the PWM signals with $m_{\mathrm{a}} = 0.2631$ and $D_{\mathrm{st}} = 0.3158$ for inverter unit 2 with $v_{\mathrm{ref}} = 50\,\mathrm{V}$ and $v_{\mathrm{dcref}} = 380\,\mathrm{V}$ are shown in Figures 6(c) and 8(a). From equation (8) $\widehat{v}_{AC}$ is directly proportional to m_a and in voltage mode control, the $\widehat{v}_{AC}$ is equal to v_{ref}. Therefore, by varying the v_{ref} the m can vary; consequently the output power can be varied. Since the proposed topologies use two inverter units, it is possible to operate both units independently by giving them separate switching signals with a single DSP kit as shown in Figures 6(b) and 6(c).

Table 1: Voltage and current stresses of the components.

Parameter	Voltage stress	Parameter	Current stress
C_a	$(D_s)\, v_{in}/(1-2D_s)$	L_a	i_{in}
C_b	$(1-D_s)v_{in}/(1-2D_s)$	L_b	$(1-D_s)i_{inv}/(1-2D_s)$
C_{cdc}	$v_{in}/(1-2D_s)$	D_x	$i_{inv}/(1-2D_s)$
D_x, D_y	$v_{in}/(1-2D_s)$	D_y	$i_{DC}/(1-D_s)$



(a) (b)

Figure 5: (a) Diodes, capacitor voltage, and (b) inductor current stresses with respect to ST duty cycle (D_s) of the proposed series and parallel topology.

Table 2: Cost of two single-unit individual converters.

Component name	Item no./rating	Price per component	No. of components required	Total price (USD)
Inductors	3.5 mH, 15 A	7.15	4	28.6
Capacitors	470 μF, 250 V	4.66	6	27.96
Diodes	40EPF06	4.56	4	18.24
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			26	---
		Total cost		130.36

3.2. Closed-Loop Control Strategy for the Proposed Topologies. The block diagram of the closed-loop control strategy for the suggested topologies is shown in Figure 6(d). The three-phase output voltages (v_a, v_b and v_c) of the inverter units are controlled by a PI compensator using the $d-q$ control mode. Using the Park and Clark transformations, the sensed AC output voltages are transformed into their $d-q$ components and compared with the $d-q$ components of the reference voltage. Finally, from the controller, sinusoidal modulating signals (m_a, m_b, and m_c) are obtained. The required DC voltage (v_{dcref}) is compared with the actual DC voltage and the error is passed through the PI controller. Consequently, DC modulating signals are obtained for ST cycles. By using these modulating signals with a triangular signal for PWM operation, the switching signals are produced. Figure 9 displays the block diagram of the overall implementation of the proposed topologies.

4. Verification of the Proposed Topologies

To check the effectiveness of the proposed topologies, they are validated experimentally for $n=2$ (i.e., for two simultaneous AC outputs and one DC output). A hardware prototype is fabricated using the same parameters as given in Table 5. The hybrid PWM signals to control the switches of the proposed topologies are generated by a 32-bit TMS320F28335 DSP operating with a clock frequency of 150 MHz. The full steady-state and dynamic results of the proposed parallel and series version topologies are shown in Sections 4.1 and 4.2. Figure 10 provides a photograph of the experimental setup installed in the laboratory to test proposed topologies. The hardware system consists of an impedance network, DC network, two three-phase inverters, LC filter, and a DSP kit. The three-phase AC outputs are loaded with six 20 Ω loads in a Y-connection and DC output is loaded with a 100 Ω.

4.1. Validation of Parallel Version (Regulated Dual AC and Single DC Outputs). In the parallel version, the proposed topology is tested for 2.18 kW with DC power $P_{DC}=1444$ W and AC power $P_{AC}=735$ W.

4.1.1. Steady-State Result of the Proposed Parallel Version. Figure 11 shows the simulation results and Figures 7, 12, and 13 show the hardware results for the steady-state response of the parallel version of the proposed topologies for AC and DC voltage reference $v_{ref}=70$ V (peak AC for both units)

Table 3: Cost of proposed converters with two units.

Component name	Item no./rating	Price per component	No. of components required	Total price (USD)
Inductors	5.3 mH, 20 A	12.66	2	25.32
Capacitors	470 μF, 400 V	8.28	3	24.84
Diodes	DWD10G120C5XKSA1	5.51	2	11.02
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			19	---
Total cost				116.74

Table 4: Comparison among previously reported and proposed multioutput converters.

Reference	No. of outputs	Advantages	Disadvantages
[11]	3 (extendable)	(i) Multiple DC outputs (ii) One step-up DC output (iii) Other outputs are step-down DC	(i) Unable to produce AC (ii) Not suitable for high power application
[14]	2	(i) Produces more than one DC outputs (ii) Uses only one power switch to achieve high efficiency (iii) Soft switching and voltage clamping used to reduce switching and conduction losses	(i) Unable to produce AC output (ii) High number of passive elements: four inductors, four diodes, and three capacitors for two DC outputs (iii) Power density is low
[15]	2	(i) Simultaneous two buck and boost DC outputs (ii) Less voltage stress across the switches due to three-level structure	(i) No AC output (ii) The number of switches is high for two DC outputs, four switches are required
[16]	2	(i) Zero voltage switching (ii) Less switching loss (iii) One buck and one boost DC output simultaneously	(i) No AC output (ii) Large number of components: four inductors, three switches, four capacitors, and two diodes for two DC outputs (iii) Low power density
[21]	2	(i) High step-up voltage gain converter (ii) Produces two DC outputs at a different voltage level (iii) Continuous input current with low ripple due to use of interleaved connection	(i) No AC output (ii) Large number of the inductors, coupled inductors, and capacitors are used: four inductors, four coupled inductors, and nine capacitors are used for two DC outputs (iii) Low power density
[31]	2	(i) Inherent ST protection (ii) Continuous input current (iii) Two simultaneous DC and AC outputs	(i) No multiple AC output (ii) Only single-phase AC output (iii) Not suitable for high power application
[32]	2	(i) Inherent ST protection (ii) Two simultaneous DC and AC outputs (iii) Can operate for condition $(D+M)\geq 1$, M is AC modulation index, D is the duty ratio	(i) No multiple AC output (ii) Only single-phase AC output (iii) Closed-loop control is not implemented (iv) Not suitable for high power application
[33]	2	(i) Minimum phase converter (ii) Continuous input current (iii) Two simultaneous AC and boost DC outputs	(i) No multiple AC output (ii) No three-phase output (iii) Because damping resistance losses are increased
Proposed topologies	3 (Extendable)	(i) Multiple three-phase AC with one boost DC output simultaneously (ii) Less number of passive components (two inductors and two capacitors) irrespective of the number of AC outputs (iii) Higher power density (iv) Suitable for high power applications (v) Inherent ST protection (vi) All the outputs are independently regulated	Remark: the limitations given above in the previous topologies have been taken care of in the proposed converters

and $v_{\mathrm{dcref}} = 380$ V, respectively. Figure 11 shows the simulation results for the steady-state response of parallel version of the proposed topologies for AC and DC voltage references $v_{\mathrm{ref}} = 70$ V (Peak AC for both units) and $v_{\mathrm{dcref}} = 380$ V, respectively. With the input voltage $v_{\mathrm{in}} = 140$ V, the DC load resistance is 100 Ω and the AC load resistance for both the inverter units is 20 Ω. Figure 12(a) shows the input voltage ($v_{\mathrm{in}} = 140$ V), capacitors voltages ($v_{Ca} = 125$ V and $v_{Cb} = 255$ V), and inductor (L_{a}) current ($i_{\mathrm{La}} = 16$ A). Figure 12(b) shows inductor (L_{b}) current ($i_{\mathrm{Lb}} = 16$ A), dc-link voltage ($v_{inv} = 380$ V), and diode voltages ($v_{Dx} = 380$ V and $v_{Dy} = 380$ V). Figure 11(c) shows DC output current and

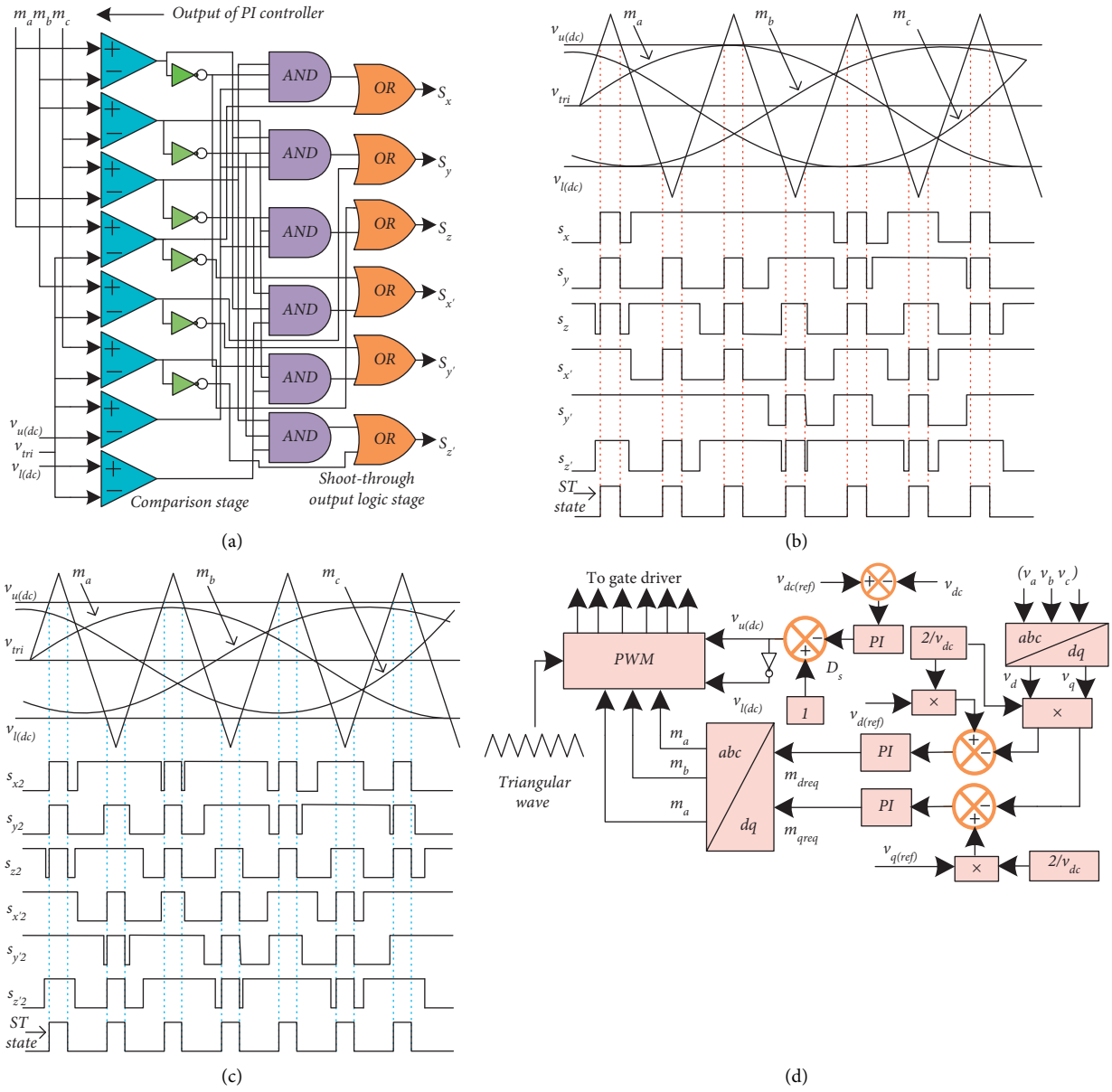


FIGURE 6: (a) Hybrid PWM control logic, (b) PWM switching signal of converter unit 1, (c) switching signal of converter unit 2, and (d) close-loop control strategy for the proposed topologies.

voltage ($i_{DC} = 3.8$ A and $v_{DC} = 380$ V and) along with three-phase voltages (140 V peak-peak) of unit 1. Figure 12(d) shows three-phase currents (7 A peak-peak) of unit 1, three-phase voltages (140 V peak-peak), and currents (7 A peak-peak) of unit 2. All the values are equal to the respective theoretical values.

Figure 13(a) shows the input voltage ($v_{in} = 140$ V), dc-link voltage (v_{inv}) 380 V which is equal to the theoretical value, and inductor currents i_{La} and i_{Lb} which are equal to the input current ($i_{in} = 16.5$ A). Figure 13(b) shows input voltage, the voltage across the capacitors C_a ($v_{Ca} = 125$ V) and C_b ($v_{Cb} = 255$ V), and DC output voltage ($v_{DC} = 380$ V). Figure 12(c) shows the input voltage, capacitor voltage ($v_{Ca} = 125$ V), DC output voltage ($v_{DC} = 380$ V), and DC output current ($i_{DC} = 3.8$ A) with DC load resistance of 100 Ω. Hence the DC power (P_{DC}) output is equal to 1444 W. Figure 12(d) shows the dc-link voltage, DC output voltage, and current with v_{in}. As the v_{inv} and DC network are in parallel, $v_{inv} = v_{DC} = 380$. Figure 12(e) shows the diodes (D_x and D_y) voltage waveforms v_{Dx}, v_{Dy} and capacitor voltage v_{Ca} along with input voltage v_{in}. The diodes D_x and D_y are forward biased during the NST state; therefore, the voltage across it (v_{Dx} and v_{Dy}) is zero. Further, during the ST state, both are reverse biased; consequently, the v_{Dx} and v_{Dy} are negative (-380 V). Figure 12(f) shows $v_{in} = 140$ V, DC output voltage ($v_{DC} = 380$ V), dc-link voltage ($v_{inv} = 380$ V), and voltage waveform across diode D_y. The diode D_y is also forward biased during the NST state; therefore, the voltage across v_{Dy} is zero; at the same time the dc-link voltage $v_{inv} = 380$ V. Further, during the ST state, D_y is reverse biased and the v_{Dy} is negative (v= -380 V).

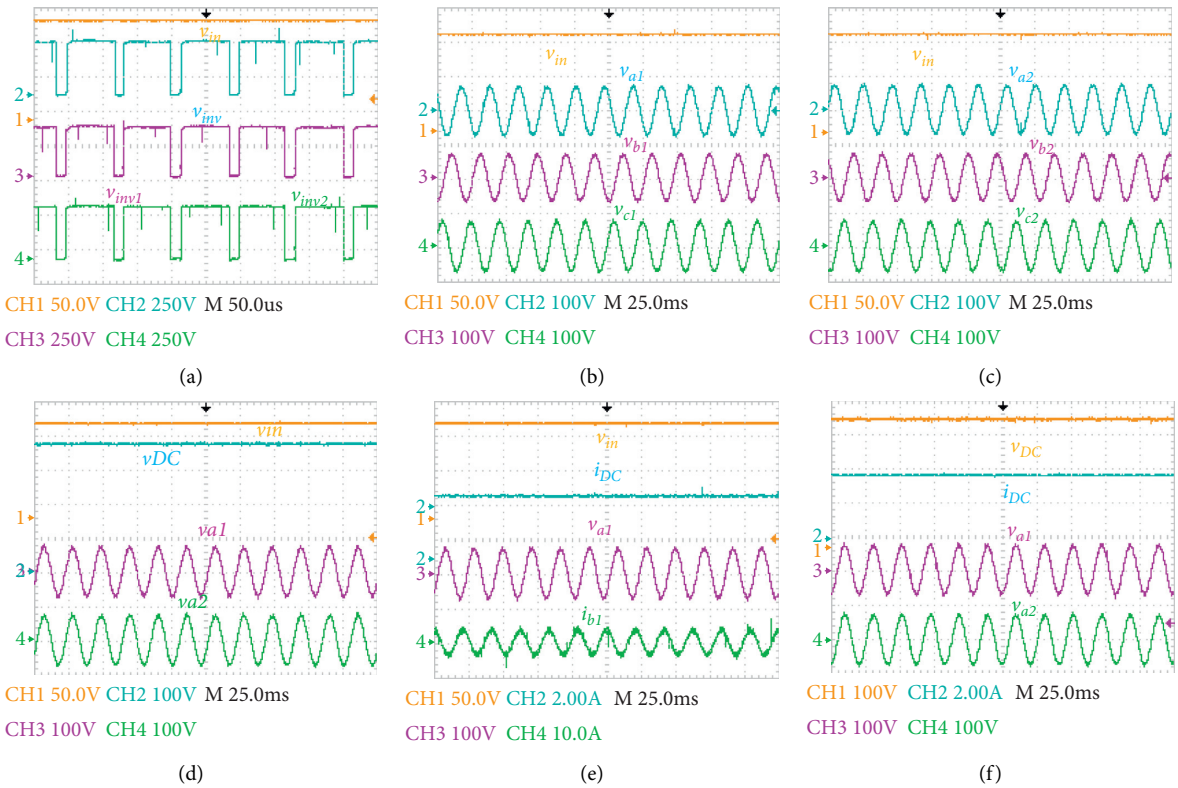


FIGURE 7: (a) dc-link voltages, (b) three-phase voltages of unit 1, (c) three-phase voltages of unit 2, (d) v_{DC} with phase a voltages v_{a1} and v_{a2} of inverter units 1 and 2, (e) i_{DC} with v_{a1} and phase b current (i_b), and (f) i_{DC}, v_{a1}, and v_{a2} of units 1 and 2 with $v_{dcref} = 380$ V and $v_{acref} = 70$ V.

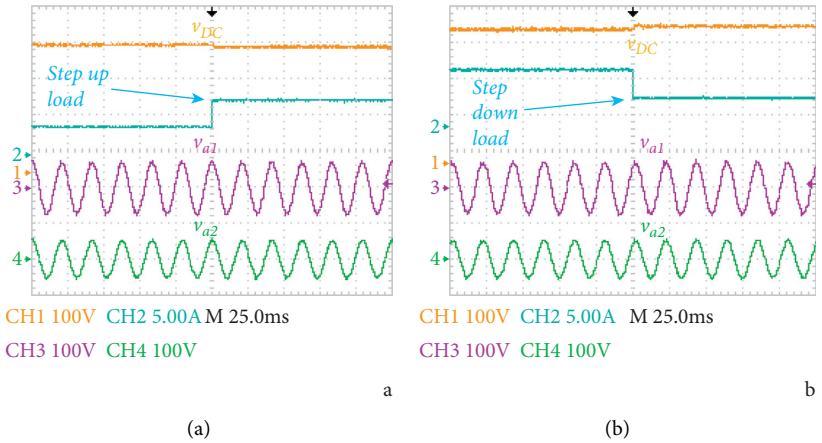


FIGURE 8: Dynamic result of the proposed parallel version topology. (a) Step-up dynamics with v_{DC}, v_{a1}, and v_{a2} and (b) step-down dynamics with v_{DC}, v_{a1}, and v_{a2}.

Figure 7(a) shows the input voltage v_{in}, dc-link voltages of converter units 1 and 2, i.e., $v_{inv1} = v_{inv2} = 380$ V, which is equal to the output of the impedance source network (i.e. v_{inv}) as the inverter units are connected in parallel. Figures 7(b) and 7(c) show input voltage $v_{in} = 140$ V and three-phase output voltages of converter units 1 and 2 which have a magnitude of 140 V (peak-peak) while the reference voltage v_{ref} is 70 V. Figure 7(d) shows v_{in}, output DC voltage ($v_{DC} = 380$ V with $v_{dcref} = 380$ V), and phase a voltages (140 V peak-peak) of converter units 1 and 2 with a reference voltage (v_{ref}) of 70 V for both units. Figure 7(e) shows output DC currents $i_{DC} = 3.8$ A, phase a voltage (140 V peak-peak), phase b current $i_{b1} = 7$ A peak-peak of converter unit 1 along with v_{in}. Figure 7(f) shows the output DC voltage, current, and phase a voltage (140 V peak-peak) of inverter units 1 and 2. The output DC voltage and currents are 380 V and $i_{DC} = 3.8$ A as the DC load resistance is 100 Ω while $v_{dcref} = 380$ V and $v_{acref} = 70$ V. For AC reference voltage $v_{ref} = 70$ V, all the three phases have the same magnitude (i.e., 140 V peak-peak) and 120° phase difference showing the stable and balanced system.

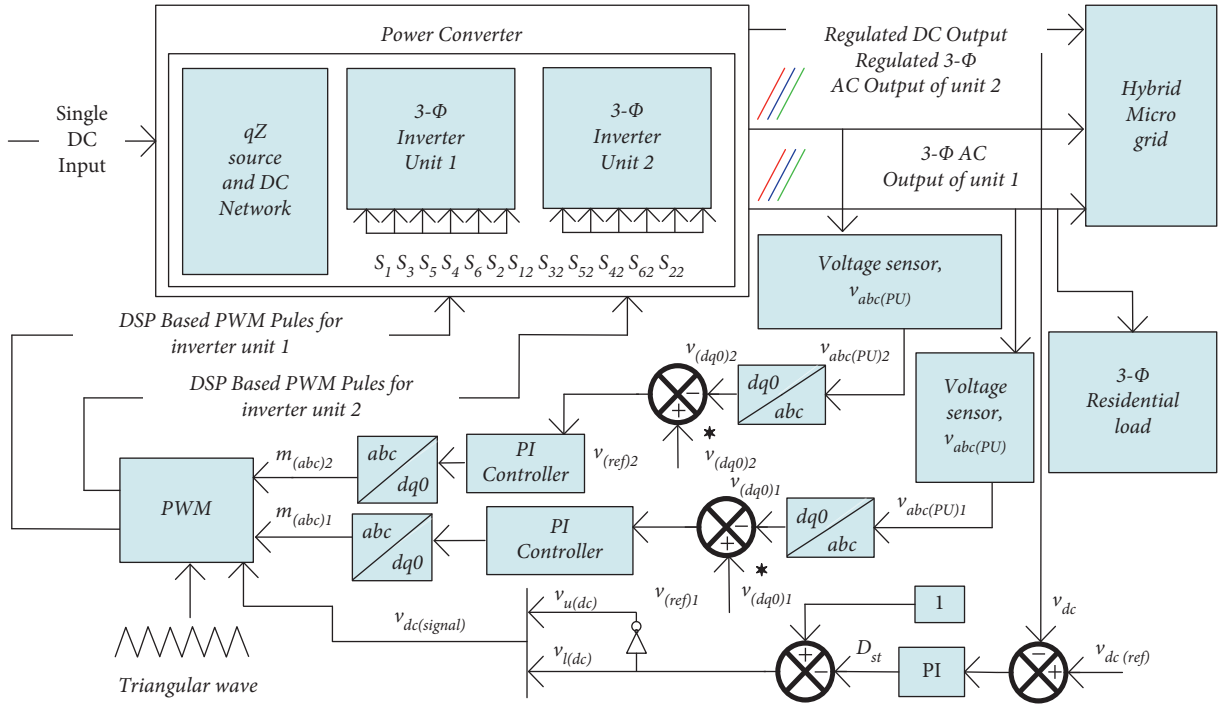


Figure 9: Overall implementation of the proposed topologies.

Table 5: Components list of the proposed topologies.

Parameter	Value
Rated output power $(P_o)/(W)$	2.18 and 2.02 kW (for parallel and series)
Input voltage, $v_{in}/(V)$	140 (for parallel and series version)
Switching frequency, fsw/(kHz)	10
Z source capacitor $(C_a, C_b, C_{dc})/(uF)$	470
Z source inductor $(L_a, L_b)/(mH)$	5
Output filter inductor $(L_f)/(mH)$	2
Output Filter Capacitor $(C_f)/(Uf)$	10
Power IGBTs (IKW15N120H3FKSA1)	1200 V, 30 A
Diodes (D_x, D_y) (RURG80100)	1000 V, 80 A
Output frequency, $f_o/(hz)$	50
Three-phase resistive load $(R_{AC})/(\Omega)$	20/phase
DC load resistance $(R_{dc})/(\Omega)$	100

Figure 12(a) shows output DC voltage $v_{DC} = 380$ V, output DC current $i_{DC} = 3.8$ A, phase *a* voltage (140 V peak-peak), and phase *a* current (7 A peak-peak) as the AC load resistance is 20 Ω of the converter unit 1 while $v_{\text{dcref}} = 380$ V and $v_{\text{acref}} = 70$ V. Phase *a* voltage and current are 0° phase apart from each other. Output DC voltage, current, and phase *a* voltage of unit 2 with the input voltage ($v_{\text{in}} = 140$ V) are shown in Figure13(b)which is equal to the theoretical value.

4.1.2. Dynamic Response of the Proposed Parallel Version with the Same AC Reference Voltages. Figure 14 shows the dynamic response of the proposed topologies for DC and AC load transients with the same AC reference voltages. Figures 14(a) and 14(b) show step-up and step-down DC load change in DC network with phase *a* voltage (140 V peak-peak) of converter unit 1 while the v_{ref} is 70 V and v_{dcref} is 380 V. As the DC load current is changed from 3.8 A to 7.6 A, the dc-link voltage v_{inv} slightly decreases and finally, it restores its original position very quickly (within one cycle) and vice versa. Figures 14(c) and 14(d) show DC output voltage (v_{dc}), the step-up and step-down load change in DC network, and phase *a* voltage (140 V peak-peak) of converter units 1 and 2 while the v_{ref} is 70 V and v_{dcref} is 380 V. As the DC load current is changed from 3.8 A to 7.6 A, v_{dc} slightly decreases and finally it restores its original position very quickly (within one cycle) and vice versa. Figures 14(e) and 14(f) show step-up and step-down AC load change in converter unit 1. In Figure 14(e) the load current of converter unit 1 changes from 7 A to 14 A (peak-peak). As the load current increases the corresponding voltage of phase *a* (v_{a1}) slightly decreases and it restores its original position within very little time. The DC output voltage (v_{DC}) remains unaffected by AC load change. Similarly, in Figure 14(f) the load current of converter unit 1 changes from 14 A

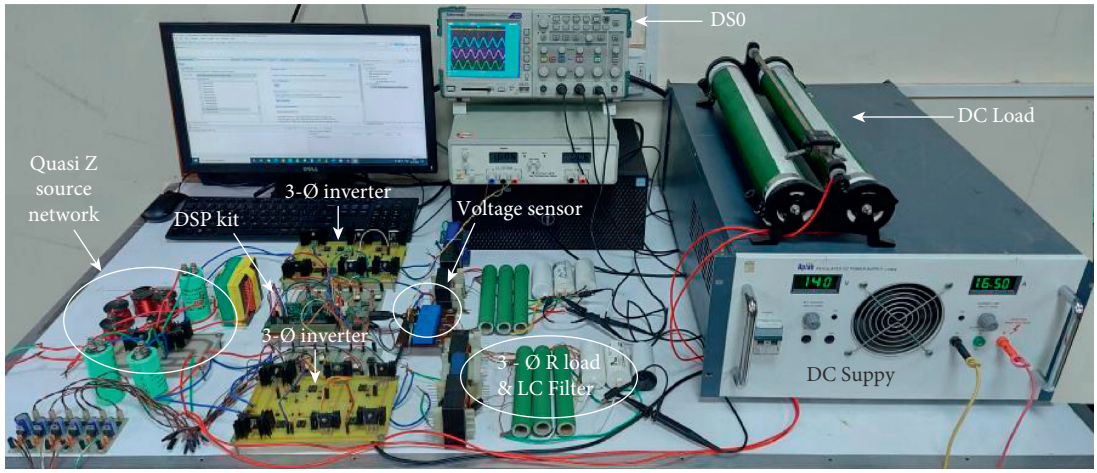


Figure 10: Experimental setup.

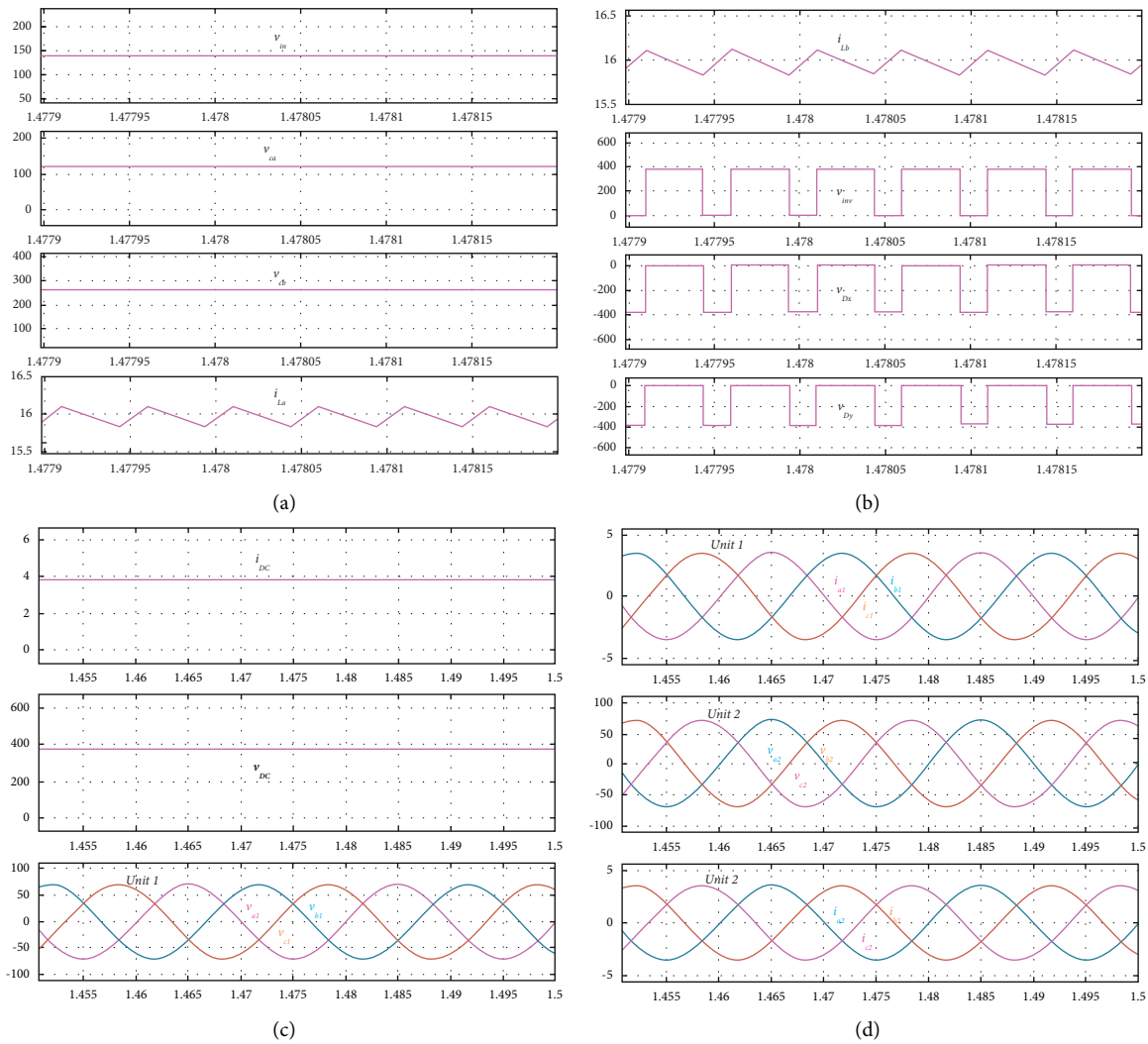


Figure 11: Steady-state simulation result of the proposed parallel version converters. (a) Input voltage, capacitor voltages, and inductor current i_{La}, (b) inductor currents i_{Lb}, dc-link voltage v_{inv}, and diode voltages, (c) output DC current and voltage along with three-phase voltage of unit 1, and (d) three-phase currents of unit 1 and three-phase voltages and currents of unit 2 with $v_{dcref} = 380$ V and $v_{acref} = 70$ V.

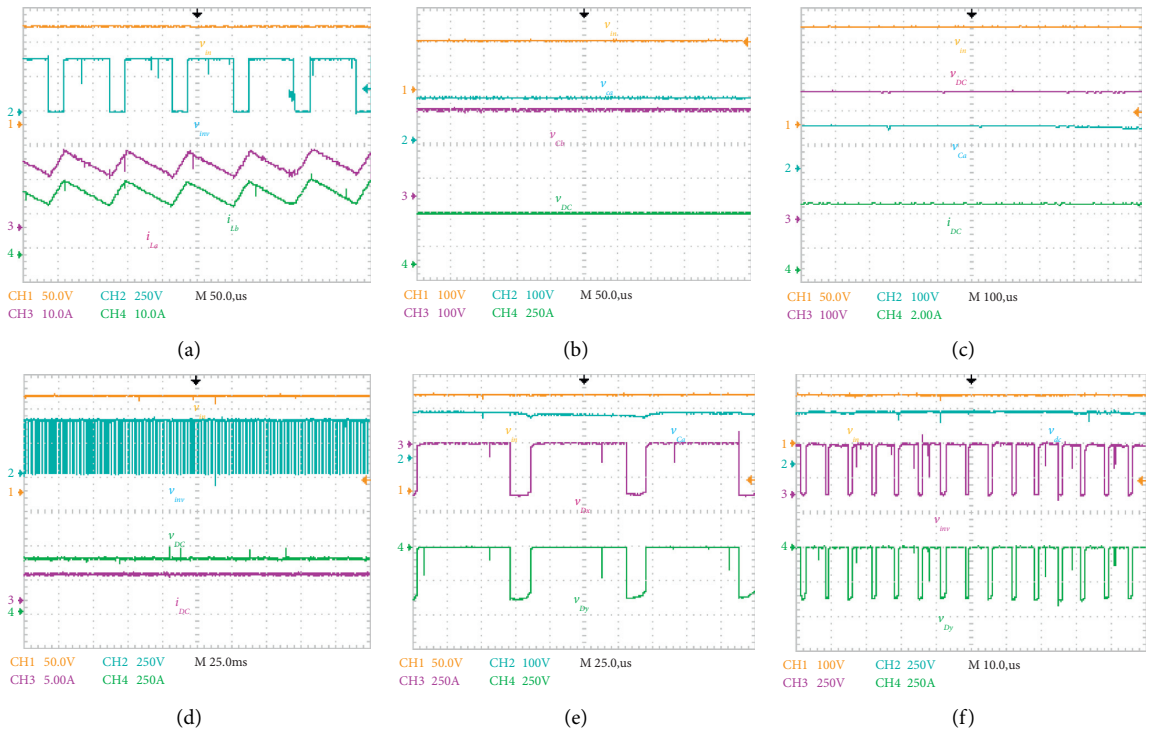


FIGURE 12: Steady-state result of the proposed parallel version converters. (a) Inductors current, (b) capacitors voltages, (c) output DC voltage (v_{DC}) and current (i_{DC}), (d) dc-link voltage (v_{inv}) and v_{DC}, (e) diode voltages (v_{Dx} and v_{Dy}), and (f) v_{inv}, v_{DC}, and v_{Dy} with $v_{dcref} = 380$ V.

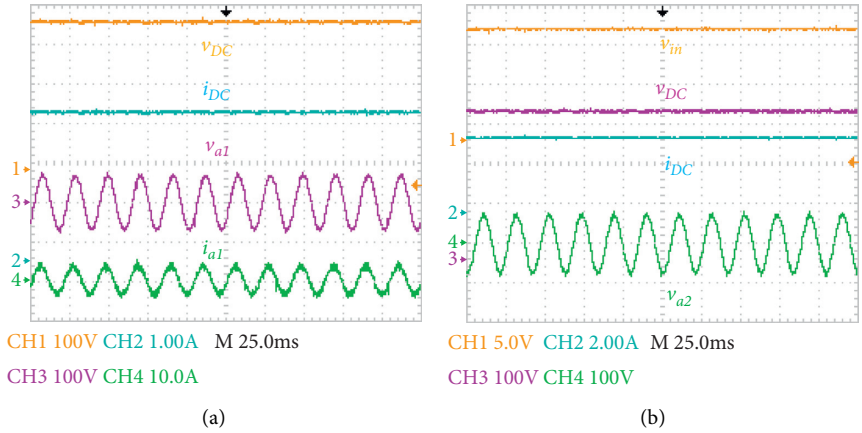


FIGURE 13: (a) Output DC voltage (v_{DC}) and currents (i_{DC}) with v_{a1} and phase a current (i_a) of the inverter unit 1 and (b) DC output voltage (v_{DC}) and i_{DC} with v_{a2} of the inverter unit 2.

(peak-peak) to 7 A. As the load current decreases the corresponding voltage of phase a (v_{a1}) slightly increases and it restores its original position within very less time (in one cycle) and the DC output voltage (v_{DC}) remains unaffected. It indicates that the system with the proposed converter topology is stable and has a good dynamic response.

4.1.3. Dynamic Response of the Proposed Parallel Version Converter with the Different AC Reference Voltages. Figure 8 shows the dynamic response of the proposed converter topologies for DC and AC load transients at different AC reference voltages. Figures8(a) and 8(b) show step-up and step-down DC load change in DC network with phase a voltages 140 V and 100 V (peak-peak) of converter units 1 and 2 while the v_{ref} is 70 V, 50 V, and v_{dcref} is 380 V. As the DC load current is changed from 3.8 A to 7.6 A, the DC output voltage slightly decreases and finally, it restores its original position within one cycle and vice versa.

During the DC load, the AC output voltage (v_{AC}) remains unaffected. The 380 V DC output voltage level [37] has been used in DC data centers. Because this is a rather high voltage, particularly effective grounding and protection procedures are required.

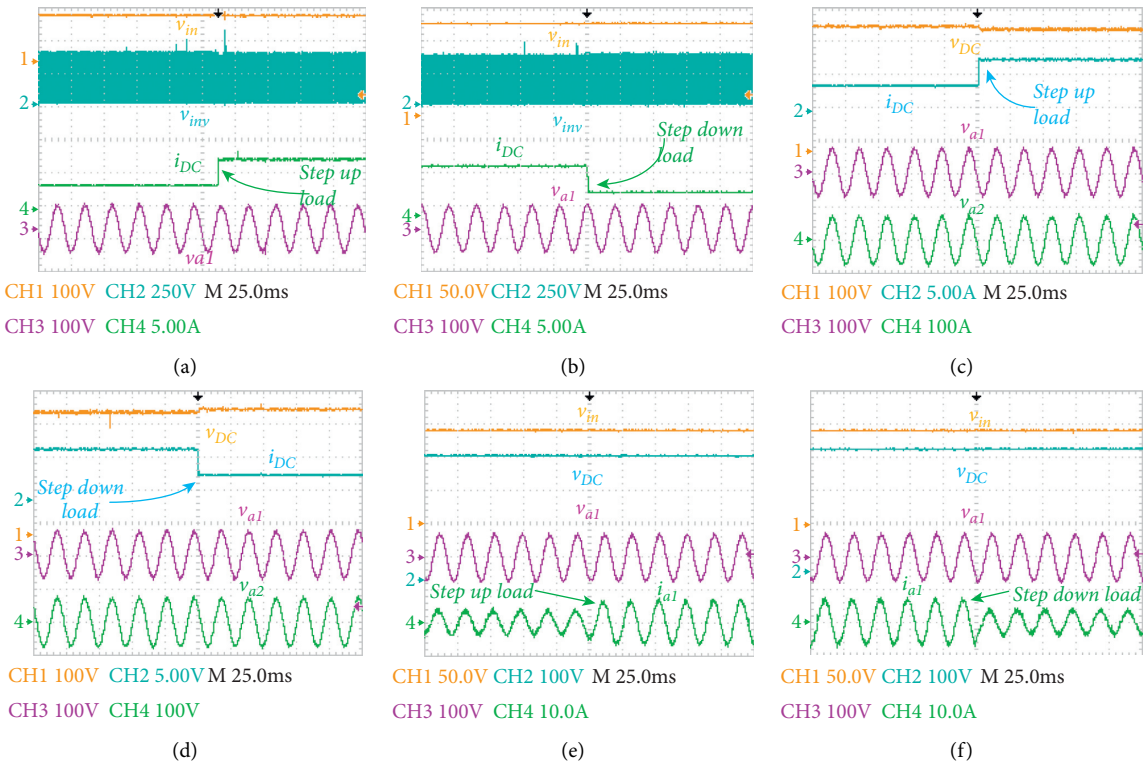


FIGURE 14: Dynamic result of the parallel version topology. (a) Step-up load change with v_{inv} and v_{a1}, (b) step-down load change with v_{inv} and v_{a1}, (c) step-up load change with v_{DC}, v_{a1}, and v_{a2}, (d) step-down load change with v_{DC}, v_{a1}, and v_{a2}, (e) step-up load change with v_{a1} and v_{DC}, and (f) step-down load change with v_{a1} and v_{DC} with $v_{\text{dcref}} = 380$ and $v_{\text{ref}} = 70$ V.

4.2. Validation of Proposed Series Version (Regulated Dual AC and Single DC Outputs). The proposed series version is verified for 2.02 kW with DC power $P_{DC} = 1056$ W and AC power $P_{ac} = 960$ W power output.

4.2.1. Steady-State Response of the Proposed Topologies in the Series Version. Figures 15 and 16 show the steady-state simulation and hardware result of the proposed series version, respectively. The DC and AC reference voltages for both the inverter units are 325 V and 80 V.

Figures 15 shows the simulation result for the steady-state response of the series version of the proposed topology for AC and DC voltage reference $v_{\text{ref}} = 80$ V (peak AC for both units) and $v_{\text{dcref}} = 325$ V, respectively. With the input voltage $v_{\text{in}} = 140$ V, the DC load resistance is 100 Ω and the AC load resistance for both inverter units is 20 Ω.

Figure 15(a) shows the input voltage ($v_{\text{in}} = 140$ V), capacitors voltages ($v_{Ca} = 97$ V and $v_{Cb} = 228$ V), and inductor (L_{a}) current ($i_{\text{La}} = 15.5$ A). Figure 15(b) shows inductor (L_{b}) current ($i_{\text{Lb}} = 15.5$ A), dc-link voltage ($v_{inv} = 325$ V), and diode voltages ($v_{Dx} = 325$ V and $v_{Dy} = 325$ V). Figure 15(c) shows DC output current and voltage ($i_{\text{DC}} = 3.25$ A and vDC = 325 V and) along with three-phase voltages (160 V peak-peak) of unit 1. Figure 15(d) shows three-phase currents (8 A peak-peak) of unit 1, three-phase voltages (160 V peak-peak) of unit 2, and currents (8 A peak-peak) of unit 2. All the values are equal to the respective theoretical values.

It is important to mention that if one unit becomes unbalanced, the other unit will continue to supply power without any interference from unit 1 and vice versa in the case of the parallel version of the proposed topologies. However, in the case of the series version of the proposed topologies, with an unbalanced load, the output voltages and currents of units 1 and 2 will become unbalanced.

Figure 16(a) shows the hardware results with the input voltage $v_{\text{in}} = 140$ V, dc-link voltage $v_{inv} = 325$ V, and inductor currents $i_{\text{La}} = i_{\text{Lb}} = 16.1$ A which is also input current (i_{in}). Since $i_{\text{La}} = i_{\text{Lb}}$, charging discharging nature of both inductor currents is the same. Figure 16(b) shows $v_{\text{in}} = 140$ V, capacitor voltages $v_{\text{Ca}} = 97$ V and $v_{\text{Cb}} = 228$ V, and diode switching voltage $v_{\text{Dx}} = 325$ V. Figure 16(c) gives input voltage v_{in}, DC output current $i_{\text{DC}} = 3.25$ A, DC output voltage $v_{\text{DC}} = 325$ V, and dc-link voltage $v_{inv} = 325$ V. Here v_{inv} is equally divided between both units 1 and 2. Figure 16(d) shows the dc-link voltage ($v_{inv} = 325$ V) and diode voltages ($v_{\text{Dx}} = v_{\text{Dy}} = 325$ V) along with input voltage ($v_{\text{in}} = 140$ V). It is noticed that diodes are reverse biased during ST state and forward biased during NST state. During ST state, $v_{inv} = 0$ V and the diodes D_x and D_y are reverse biased; consequently the voltages across the diodes are negative ($v_{\text{Dx}} = v_{\text{Dy}} = -325$ V).

Further, during the NST state, the diodes are forward biased ($v_{\text{Dx}} = v_{\text{Dy}} = 0$ V) and $v_{inv} = 325$ V. Figures 16(e) and 16(f) show three-phase voltages (v_{a1}, v_{b1}, v_{c1}) and (v_{a2}, v_{b2}, v_{c2}) of the inverter units 1 and 2 with v_{DC} and phase c currents i_{c2}. All the phases of inverter units 1 and 2 have the

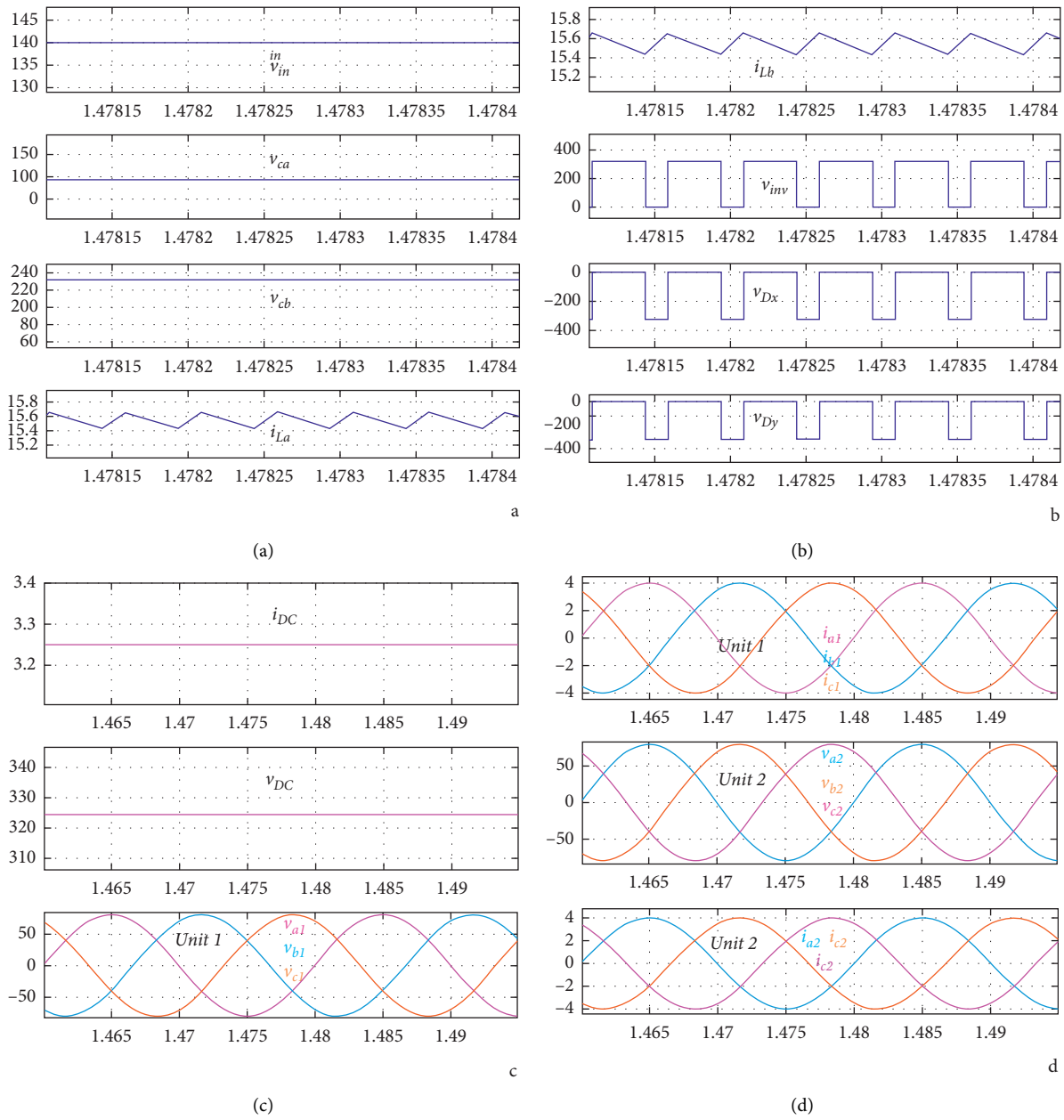


FIGURE 15: Steady-state simulation result of the proposed series version topology. (a) Input voltage, capacitor voltages, inductor current i_{La}, (b) inductor current i_{Lb}, dc-link voltage v_{inv}, and diode voltages, (c) output DC current and voltage along with three-phase voltages of unit 1, and (d) three-phase currents of unit 1 and three-phase voltage and currents of unit 2 with $v_{dcref} = 325$ V and $v_{acref} = 80$ V.

same voltage magnitude, i.e., 160 V (peak-peak) when the v_{acref} is 80 V. All the three-phase voltages are 120° phase apart from each other and balanced.

4.3. Efficiency Analysis and Power Loss Distribution of the Proposed Topologies. Figures 17 and 18 show the experimental efficiency of both the parallel and series version topologies. Figure 17(a) shows the efficiency versus total power output curve during parallel version when AC power is constant and DC power variable. In Figure 17(b), AC power is variable and DC power is constant. From Figures 17(a) and 17(b), it can be observed that the measured efficiency of the proposed parallel version topology is 90.01% at 2.18 kW load power.

Similarly, Figure 18(a) shows the efficiency versus total power output curve during the series version when AC power is constant and DC power variable. In Figure 18(b) AC power is variable and DC power is constant. It can be seen from Figures 18(a) and 18(b) that the efficiency of the proposed series version topology is 89.95% at a load power of 2.02 kW. It is necessary to mention that the efficiency of the proposed topologies can be further improved by optimizing the passive components, printed circuit boards, and semiconductor devices.

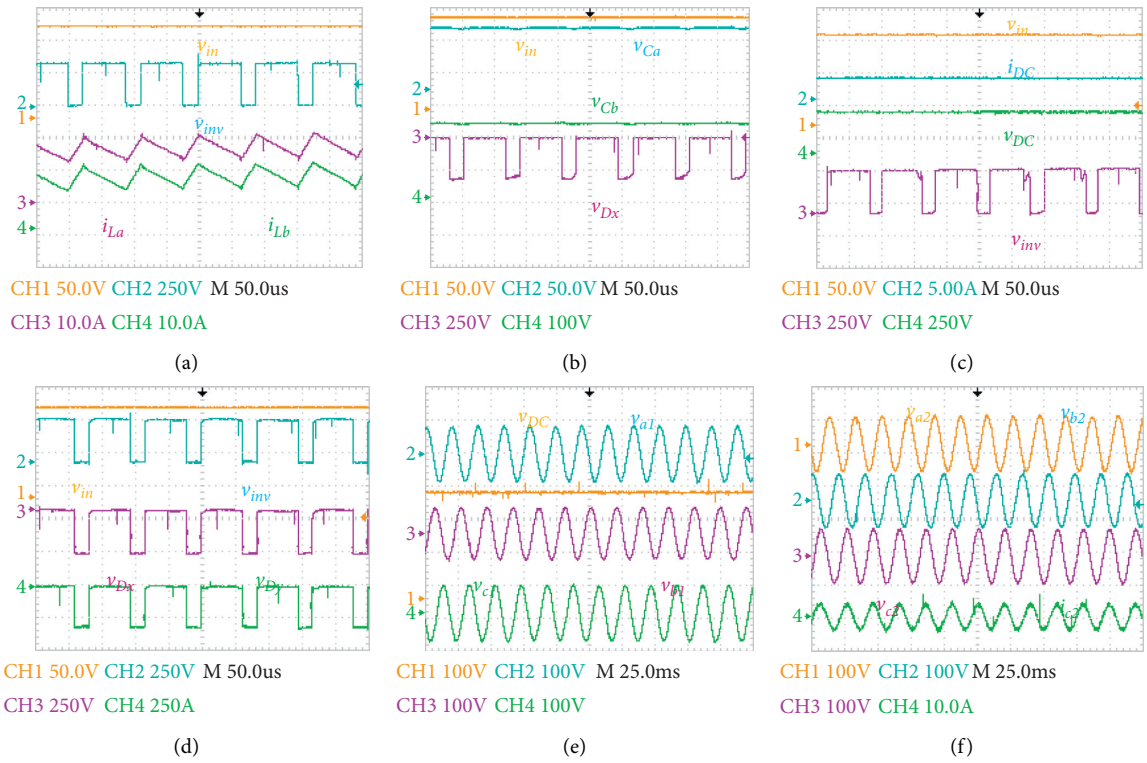


Figure 16: Steady-state result of the proposed series version topology. (a) Inductor currents with v_{inv}, (b) capacitor voltages with diode voltage (v_{Dy}), (c) dc output voltage (v_{DC}) and current (i_{DC}) with v_{inv}, (d) diode voltages (v_{Dx} and v_{Dy}) with v_{inv}, (e) three-phase voltages of unit 1 with v_{DC}, and (f) three-phase voltages of unit 2 with phase c current i_{c2}.

The power loss distribution of elements of the proposed parallel and series version is shown in Figures 19(a) and 19(b) and calculated as discussed in [38]. This is achieved by calculating the nonidealities, voltages, and currents of the elements of the proposed topologies. Power losses in the proposed topologies are contributed by conduction and switching states of semiconductor devices, as well as losses in passive components [39, 40].

For calculating the power losses, the following assumptions are taken:

(1) The switches are modeled by an ideal switch having a forward resistance (r_S) and a collector to emitter saturation voltage ($v_{CE(on)}$)

(2) The diodes are modeled by an ideal switch having a forward series resistance (r_D) and a forward voltage drop (v_{FD})

(3) The winding dc resistance (DCR) of inductors (r_L) and equivalent series resistance (ESR) of capacitors (r_C) are considered

(4) The collector to emitter current of switches (i_{CE}), anode to cathode current of diodes (i_D), the current through inductors (i_L), and the current through capacitors (i_C) are considered

(5) The inductor current ripples are ignored

4.4. Losses in Switches (IGBTs). The conduction loss of switches in the inverter bridge is calculated as

$$P_{Con\,d\_S} = \frac{1}{T_s}\int_0^{T_s}\left(v_{CE(on)}i_{C(avg)} + r_S i_{C(rms)}^2\right)\mathrm{d}t. \tag{22}$$

The switching loss is calculated as

$$P_{Switch\_S}^{on,off} = \frac{1}{T_s}\int_0^{t_{on}+t_{off}} v_{CE}(t)i_C(t)\mathrm{d}t. \tag{23}$$

Total power losses of the inverter switches are calculated as

$$P_{Total\_S} = 12\left(P_{Con\,d\_S} + P_{Switch\_S}^{on,off}\right). \tag{24}$$

4.5. Losses in Diodes. The conduction losses of diodes are calculated as

$$P_{Con\,d\_D} = \frac{1}{T_s}\int_0^{T_s}\left(v_{FD}i_{D(avg)} + r_D i_{D(rms)}^2\right)\mathrm{d}t. \tag{25}$$

Generally, turn-on switching losses of diodes are negligible. The turn-off switching losses of diodes are calculated as

$$P_{Swicth\_D}^{off} = \frac{2}{T_s}\int_0^{t_{off}} v_D(t)i_D(t)\mathrm{d}t. \tag{26}$$

4.6. Losses in Inductors. The power losses of inductors include core losses and winding losses. Generally, the core

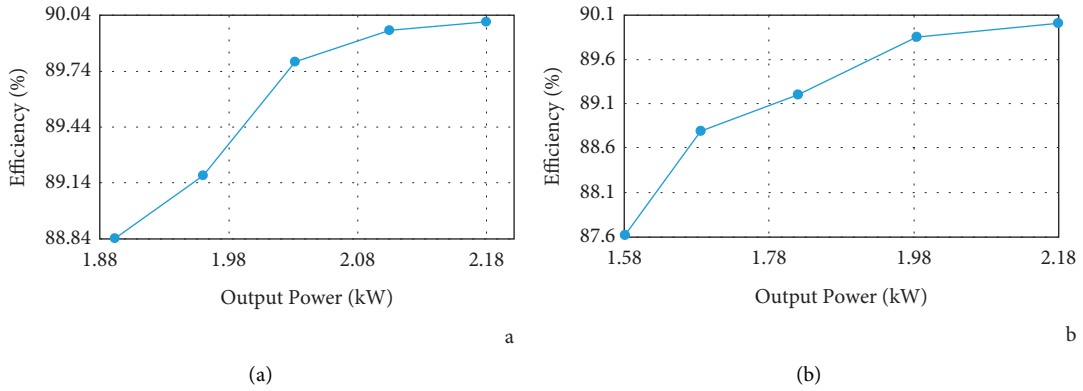


Figure 17: Measured efficiency versus total output power curve for parallel version. (a) Variable DC and constant AC power and (b) variable AC and constant DC power.

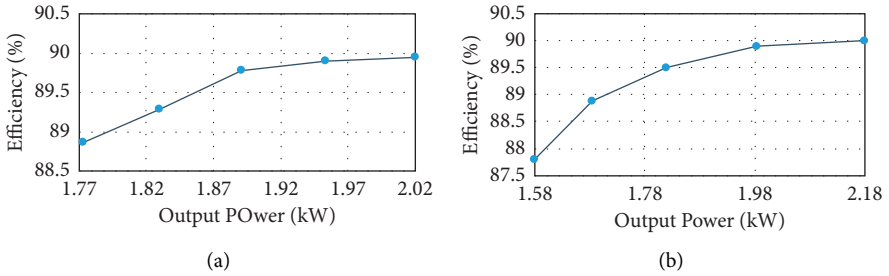


Figure 18: Measured efficiency versus total output power curve for series version. (a) Variable DC and constant AC power and (b) variable AC and constant DC power.

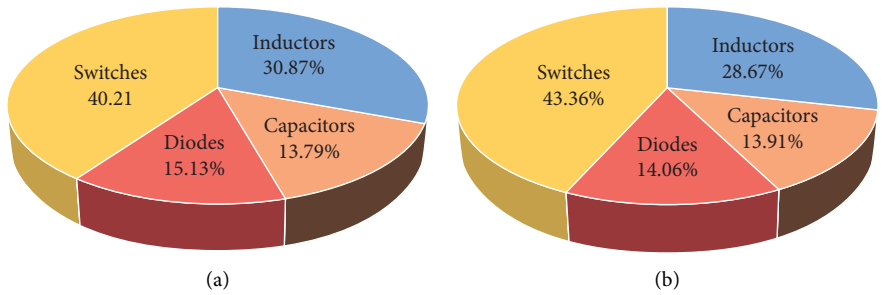


Figure 19: Power loss distribution for (a) parallel and (b) series version topologies.

losses are negligible for pulse width modulated converters. The winding losses depend on the resistances of the windings (r_L) of inductors and are calculated as

$$P_{win\ d\_L} = r_L i^2_{L(rms)}. \tag{27}$$

4.7. Losses in Capacitors. The power losses of the capacitors depend on the equivalent series resistances (r_C) and are calculated as

$$P_{rC} = \frac{1}{T_s} \int_0^{T_s} r_C i_C^2 dt. \tag{28}$$

The overall loss is theoretically calculated by the addition of the above breakup of losses.

To compare the efficiencies of the proposed topologies with other topologies, a comparison table (Table 6) between the proposed topologies and closely related similar hybrid converter topologies is prepared. It is found that the efficiency of the proposed topologies is quite comparable with others. Table 6 shows that the efficiencies of BDHC [35], CFSI [29], and hybrid buck-boost converter [34] are less than that of the proposed topologies. Two converters IHC [32] and minimum phase dual output converter [33] show higher efficiency than that of the proposed topologies. However, there are some advantages of the proposed topologies over these converters. The converters of [32, 33]

Table 6: Efficiencies of the various hybrid converters.

Hybrid converter	Maximum efficiency (%)
BDHC [31]	88.1
CFSI [29]	82.45
Hybrid buck-boost converter [34]	88.5
IHC [32]	91.32
Minimum phase dual output converter [33]	91.4
Proposed parallel topology	90.01
Proposed series topology	89.95

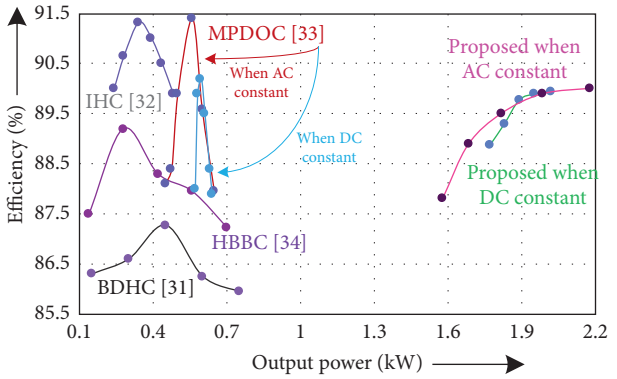


Figure 20: Efficiency comparison curve of the different converters.

have only one DC and one single-phase AC output, whereas the proposed topologies are capable of providing simultaneous multiple series or parallel three-phase AC along with one DC output.

Figure 20 shows the efficiency comparison curve of the proposed parallel version topology with the other topologies [31–34].

5. Conclusion

This paper presents two versions of diode-assisted switched LC series-parallel topologies with n number of AC outputs and one boost DC output simultaneously. The proposed parallel version topology is capable of giving n number of three-phase AC including one boost DC output with constant voltage and variable load current. Likewise, the series version gives n number of three-phase AC including one boost DC output with constant load current and variable voltage. All the outputs of the proposed topologies are independently regulated and can be fed directly to microgrids and multiple loads simultaneously without using an extra local adapter/regulator. The proposed topologies are operated with a hybrid pulse width modulation technique. Detailed mathematical modeling, steady-state, and efficiency analysis are carried out for the proposed topologies in the paper. Finally, 2.18 kW and 2.02 kW prototypes for parallel and series versions topology are developed, respectively, to validate the performance for two AC outputs and one DC output. The measured efficiency of the parallel and series version of the proposed topology is 90.01% and 89.95% respectively.

Abbreviations

D_x and D_y: Diodes
L_a and L_b: Inductors
DSP: Digital signal processor
PI: Proportional integral
SPWM: Sinusoidal pulse width modulation
HMGS: Hybrid microgrid systems
MOCs: Multioutput converters
qZSI: Quasi Z source inverter
ST: Shoot-through
NST: Non-shoot-through
R_{DC}: DC load resistance
C_{dc}: Filter capacitor
v_{inv}: dc-link voltage
v_{in}: Input voltage
KVL: Kirchhoff's voltage law
KCL: Kirchhoff's current law
D_s: Duty cycle
T_s: Switching period
v_C: Capacitor voltage
v_D: Diode voltage
v_{DC}: DC voltage
i_L: Inductor current
i_D: Diode current
B: Boost factor; peak AC voltage
m_a: Modulation index
G: Gain
3d: Three-dimensional
v_{AC}: AC voltage
R_{AC}: AC load resistance
v_{ref}: AC reference voltage
$P_{3-\varnothing}$: Three-phase AC power
P_{DC}: DC power
v_{dcref}: DC reference voltage
LC: Low pass filter
Y: Star connection
Z: Impedance.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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