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Research Article

Design of New Nonisolated High Gain Converter for Higher Power Density

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A high gain nonisolated DC-DC converter using a single power semiconductor switch is proposed in this article. The operation of the proposed converter is explained under continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM). The mathematical expressions for steady-state voltage gain, voltage stress, and current stress of diodes and switch are provided. Also, the design of inductors and capacitors in the CCM mode is explained with appropriate mathematical equations. The proposed topology is tested with a 200 W prototype at 50 kHz and a 60% duty cycle. The dynamic behavior of the proposed converter is examined by changing the duty cycle value and also load values. The proposed converter is verified with experimental results to prove the effectiveness of its operation. The proposed converter provides higher steady-state voltage gain as compared with recently developed topologies. The efficiency and power density of the proposed converter is 90% and 1.16 kW/L, respectively.

1. Introduction

The increase in carbon emission and depletion of natural resources due to nonrenewable power generation affects the environment largely. This downside makes a gaining reputation in incorporating the renewable energy sources (RES). The development of RES like photovoltaic (PV) and wind are evolving around the globe in recent years. As per the International Energy Agency report [1], RES will be the largest source of electricity generation globally in 2025. The increase in PV installation capacity motivates the researchers to focus more on the DC-DC power conversion topologies for effective utilization of RES power [2]. The development of DC-DC power conversion topologies mainly depends on few significant parameters such as high efficiency, high conversion ratio, transformerless configuration, control techniques, low size, and less cost.

The DC-DC converter can be classified broadly into two types such as isolated and nonisolated topologies [3]. The isolated topologies utilize a high-frequency transformer that acts as galvanic isolation between the source and the output as well as it increases the voltage gain of the converter by adjusting its turns ratio [4]. But it has certain drawbacks such as the higher volume and cost and saturation of the transformer. Considering RES application, the DC-DC converter plays vital role to provide good efficiency, high voltage gain, and low cost. Therefore, the development of new nonisolated topology for RES application is considered to be the right choice. But the nonisolated DC-DC converter topology should provide high voltage gain at low duty cycle which is the key challenge for designing a new topology. Though several changes have been incorporated on the traditional nonisolated converters to improve the voltage gain [5], but still there is the necessity to develop a new converter with high voltage gain at a low duty cycle with reduced stress.

A voltage lift technique based on the high step-up DC-DC converter has developed in [6] for providing high voltage gain, but it utilizes two switches that may lead to increase in power loss of the converter. In [7], the buck-boost converter based on the ZETA converter has been designed with the single power semiconductor switch for automobile electronics. It has focused on both step-up and step-down conversion. The hybrid

converter has been developed [8] by combining the cuk and boost converter that provides low output ripple and high voltage gain. It supports the hybridizing two input power sources such as photovoltaic cells, fuel cells, and battery. But the power loss is high due to multiple switches thereby reducing the efficiency [8]. The quadratic boost converter topology has been developed [9] such that it provides high voltage gain as compared with a conventional boost converter. But the topology has utilized two switches for achieving high voltage gain thereby increasing the overall loss of the converter and reducing the efficiency [9]. Many transformerless hybrid converter topologies have been developed with the help of voltage multiplier cells, switched capacitor, and switched inductor combinations for providing high voltage gain [10]. An improved hybrid topology has been developed [11] by combining the switched inductor and switched capacitor cells. The topology provides reasonable voltage gain at less duty cycle, but it utilizes three switches [11]. Voltage multiplier cells (VMC) are one of the best methods to increase the converter's voltage gain. The development of high step-up converters with different multiplier cells continuously evolves yearly to improve their power density, efficiency, and fast dynamic response for different advantages and applications. Therefore, in this article, a new voltage multiplier cell is proposed with two inductors, two diodes, and four capacitors to provide the maximum voltage gain and reduced voltage stress across the main switch.

The advantages of the proposed converter are given below:

(i) The proposed converter utilizes single switch with less voltage stress (0.59 times of output voltage) which produces higher voltage gain ($G = 10.75$) at 60% duty cycle

(ii) The power density and efficiency of the proposed converter are 1.16 kW/L and 90%, respectively

(iii) The dynamic behavior of proposed converter is examined under varying duty cycles and load conditions

Furthermore, the operation of the proposed converter is examined through the laboratory-based experimental prototype with 200 W.

2. Operation of the Proposed High Gain DC-DC Converter

The proposed high gain DC-DC converter topology is developed by combining the modified quadratic boost converter (MQDBC) with the unique voltage multiplier cell (VMC). The proposed high gain DC-DC converter topology is shown in Figure 1, which consists of single switch (S_1), five inductors (L_1, L_2, L_3, L_4 and L_5), seven capacitors ($C_1, C_2, C_3, C_4, C_5, C_6$, and C_o), six diodes (D_1, D_2, D_3, D_4, D_5 and D_6), and load R_0. It has two modes of operation such as mode-I and mode-II in CCM. The topology consists of multiple components, but it operates at less duty cycle to provide higher voltage gain with reduced voltage and current stress which is the significant aspect of the proposed topology.

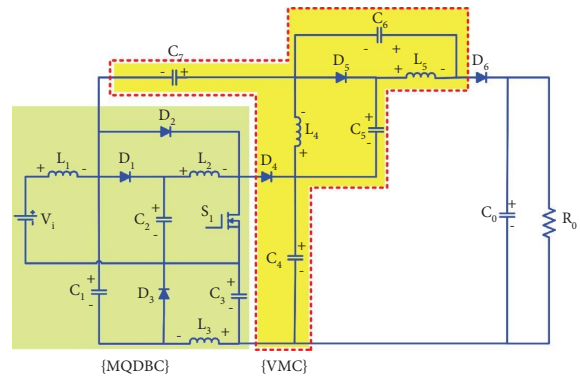

Figure 1: Proposed high gain DC-DC converter.

2.1. Continuous Conduction Mode

2.1.1. Mode-I. The operation of mode-I is explained when the switch is closed. The current path is shown in Figure 2, where the energy from the DC input charges the inductor L_1, and the capacitor C_2 charges the inductor L_2. The capacitor C_4 charges the inductor L_4 and C_5 charges inductor L_5. The combined charge of the capacitors C_4 and C_5 supports for charging the capacitors C_3, C_6, and C_7. The capacitor C_1 supports to charge the capacitor C_3 and inductor L_3. The capacitor C_0 discharges the stored charge to the load:

$$\left\{\begin{array}{c} V_{L1} = V_i; V_{L2} = V_{C2}; V_{L3} = V_{C1} - V_{C3} \\ V_{L4} = V_{C4} - V_{C3} - V_{C7}; \\ V_{L5} = V_{C4} + V_{C5} - V_{C6} - V_{C3} - V_{C7} \end{array}\right\}. \quad (1)$$

2.1.2. Mode II. The operation of mode-II is explained with two stages of operation when the switch is opened. The current path of the first stage of operation is shown in Figure 3. Here, the energy stored in inductor L_1 and the energy from DC source charges the capacitor C_1 through D_3. The stored energy in the inductor L_2 & L_3 and the capacitors C_2 & C_3 discharge through D_3 and D_4 to the capacitor C_4. It should be noted that the capacitor C_2 makes the D_1 to be in reverse biased condition due to $V_{C2} > V_{C1}$. The inductor L_4 charges the capacitor C_5 through D_5. The stored energy in the capacitor C_7, C_6, and inductor L_5 discharges through D_6 to charge the capacitor C_0 and supply the energy to the load.

In the second stage of operation, $V_{C2} < V_{C1}$ makes the diode D_1 in forward-biased condition. Therefore, the energy from the DC source charges the capacitor C_2 through D_1. The changes in current flow of the capacitor C_3, C_4, and inductor L_3 occurs, which is predicted as shown in Figure 4:

$$\left\{\begin{array}{c} V_{L1} = V_i - V_{C2} = V_i - V_{C1} \\ V_{L2} = V_{C2} + V_{C3} - V_{C4} \\ V_{L3} = -V_{C3}; V_{L4} = -V_{C5} \\ V_{L5} = -V_{C6} \\ V_0 = V_i - V_{L1} + V_{C7} + V_{C6} + V_{C3} \end{array}\right\}. \quad (2)$$

The analytical waveform of the proposed converter under CCM is illustrated in Figure 5. Applying the volt-sec

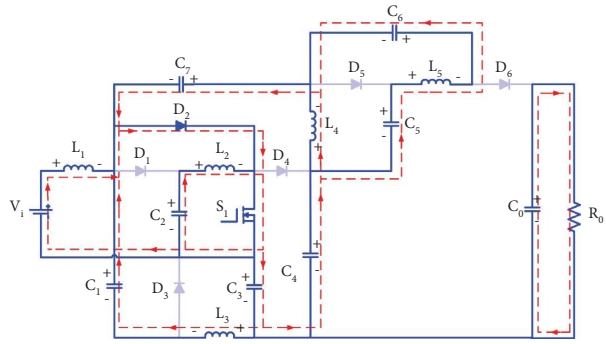

Figure 2: Equivalent circuit of proposed in mode-I.

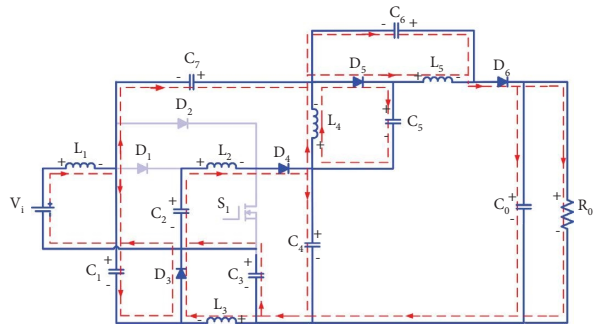

Figure 3: Equivalent circuit of proposed converter in mode II (first stage).

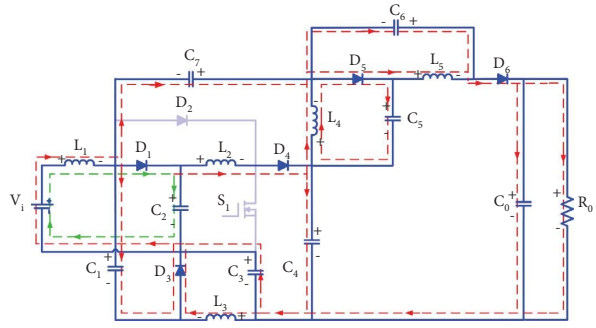

Figure 4: Equivalent circuit of the proposed converter in mode II (second stage).

balance principle on the inductors (L_1toL_5), the following expressions can be obtained:

$$\left\{\begin{array}{l} V_{C1} = V_{C2} = \dfrac{V_i}{1-D}; V_{C3} = V_{C5} = V_{C6} = \dfrac{DV_i}{1-D} \\ V_{C4} = \left[\dfrac{1+D-D^2}{(1-D)^2}\right]V_i; V_{C7} = \left[\dfrac{\left(2\ D-D^2\right)}{(1-D)^2}\right]V_i \end{array}\right\}, \quad (3)$$

$$V_i - V_{L1} + V_{C7} + V_{C6} + V_{C3} = V_0. \quad (4)$$

The proposed converter steady-state voltage gain (M) is derived by solving the equations (3) in (4) as

$$\left\{M = \frac{V_0}{V_i} = \frac{1+3\ D-3D^2}{(1-D)^2}\right\}. \quad (5)$$

2.2. Discontinuous Conduction Mode. The operation of the proposed converter in DCM is divided into three instants. At the first instant ($t_0 < t < t_1$), the switch S_1 is closed. It is similar to the mode-I operation in CCM. At the second instant ($t_1 < t < t_2$), the switch S_1 is opened and the inductor starts to decay. It is also similar to mode-II operation in CCM. At the third instant ($t_2 < t < t_3$), the switch S_1 is still opened and the inductor currents decays to zero. The equivalent circuit of DCM mode for this instant is shown in

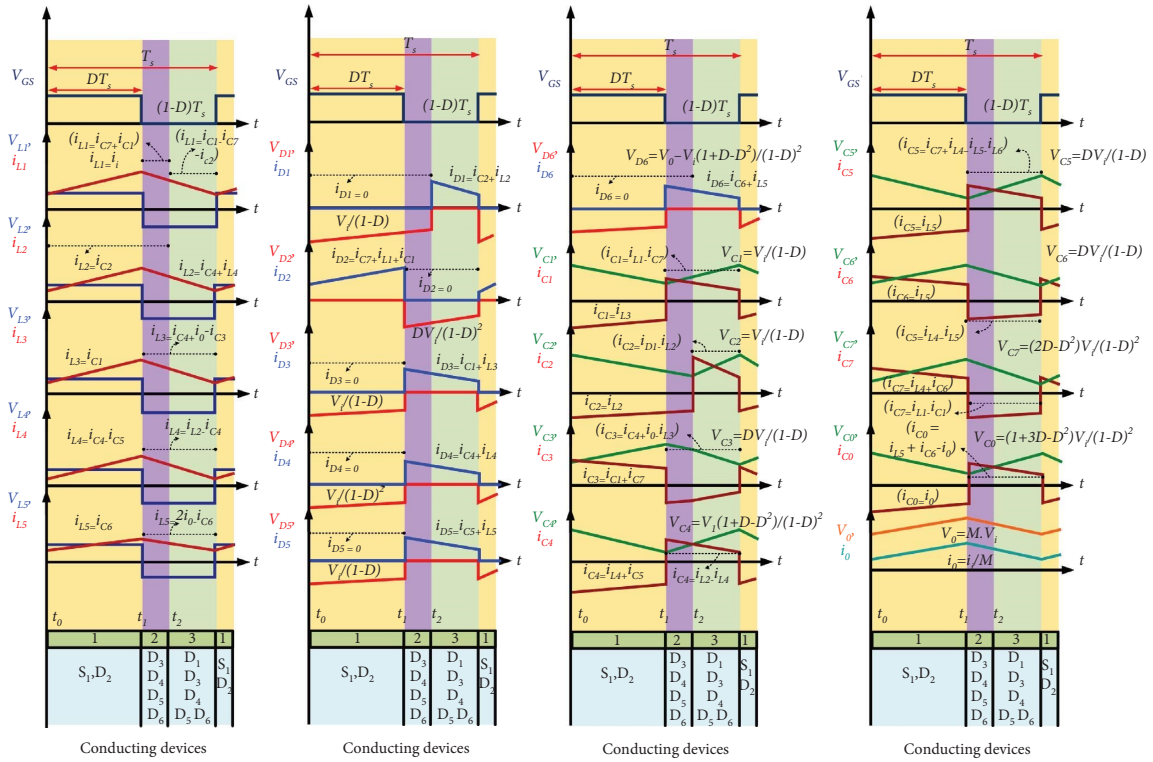

Figure 5: Analytical waveform of the proposed converter under CCM operation for one switching cycle.

Figure 6. It is noted that all the diodes are in reverse biased condition, and the stored energy in capacitor C_6 is discharged to the load R_0.

Applying the volt-sec balance principle across the inductors L_1, L_2, L_3, L_4, and L_5 under DCM operation, the voltage gain and duty cycle can be obtained as follows:

$$G_{\mathrm{DCM}} = \frac{V_0}{V_i} = 1 + \frac{5\ D}{D_{m2}} + \frac{D^2}{D_{m2}^2}, \tag{6}$$

$$D_{m2} = \frac{D}{1.5}. \tag{7}$$

From the analytical waveform of the DCM operation, as shown in Figure 7(a), the average current of diode D_6 is derived, and it is expressed as given below:

$$i_{D6\_\mathrm{avg}} = \frac{1}{2} D_{m2} \frac{V_i D}{L_{eq} f_s}. \tag{8}$$

The duty cycle of "D_{m2}" is calculated as follows:

$$D_{m2} = \frac{K_L G_{\mathrm{DCM}}}{D}. \tag{9}$$

The voltage transfer gain (G_{DCM}) can be obtained by equating (7) and (9)as

$$G_{\mathrm{DCM}} = \frac{D^2}{1.5 K_L}, \tag{10}$$

where K_L is the normalized inductor time constant, which is given as

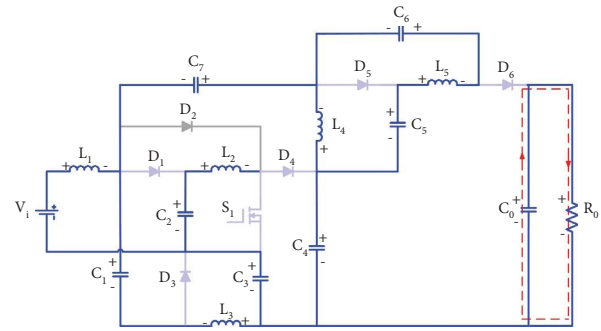

Figure 6: Equivalent circuit of the proposed converter in DCM.

$$K_L = \frac{L_{eq} f_s}{R}. \tag{11}$$

Figure 7(b) shows the plot between voltage gain versus duty cycle under CCM and DCM operation.

2.3. Boundary Conduction Mode. When the proposed converter is operated at the boundary of CCM and DCM, then the voltage gain of CCM and DCM is equal. Therefore, the normalized boundary inductor time constant "K_B" is found by equating (5) and (10) as

$$K_b = \frac{D^2 (1 - D)^2}{\left(1 + 3\ D - 3D^2\right)}. \tag{12}$$

From Figure 7(c), it is evident that if the "K_b" is larger than "K_L," then the converter operates in DCM else in CCM.

2.4. Design Considerations. The accurate design of proposed converter components is necessary to obtain the desired outcome. The voltage ripple and current ripple equations can be determined by applying amp-sec balance and volt-sec balance on the proposed converter capacitors and inductors, respectively:

$$\left\{\begin{array}{c} i_{L5}=2i_0(1-D);\, i_{C5}=2i_0;\, i_{C6}=\dfrac{i_0[2(D-1)]}{(1-D)} \\ i_{L4}=2i_0\left[(1-D)+(1-D)^2\right]-i_0\left[\dfrac{(2\,D-1)^2}{(1-D)}\right] \\ i_{L2}=\dfrac{i_{L4}+(2\,D-1)i_{C5}}{(1-D)};\, i_{C4}=2i_0D-i_{L4}+i_{L2} \\ i_{L3}=i_0(D-1)+i_{C4}(2\,D-1);\, i_{C2}=\dfrac{i_{L2}D}{(1-D)} \\ i_{C7}=\dfrac{(2i_0-i_{L5})(1-D)}{D}+i_{L4};\, i_{L1}=\dfrac{i_{L3}D}{1-D}+i_{C7}+i_{C2} \end{array}\right\}. \tag{13}$$

Here, f_s is the switching frequency of the switch S_1:

$$\left\{\begin{array}{c} \Delta i_{L1}=\dfrac{V_iD}{L_1f_s};\, \Delta i_{L2}=\dfrac{V_iD}{(1-D)L_2f_s};\, \Delta i_{L3}=\dfrac{V_iD}{L_3f_s} \\ \Delta i_{L4}=\dfrac{V_iD}{L_4f_s};\, \Delta i_{L5}=\dfrac{V_iD^2}{(1-D)L_5f_s} \end{array}\right\}. \tag{14}$$

The capacitor ripple voltage are as follows:

$$\left\{\begin{array}{c} \Delta V_{C1}=\dfrac{i_{C1}(1-D)}{C_1f_s} \\ \Delta V_{C2}=\dfrac{(i_{L1}-i_{C1}-i_{L5}+i_{C6}-i_{L2})(1-D)}{C_2f_s} \\ \Delta V_{C3}=\dfrac{(i_{C1}+i_{L4}+i_{C6})D}{C_3f_s};\, \Delta V_{C4}=\dfrac{i_{L2}(1-D)}{C_4f_s} \\ \Delta V_{C5}=\dfrac{i_{L4}(1-D)}{C_5f_s};\, \Delta V_{C6}=\dfrac{i_{C6}D}{C_6f_s} \\ \Delta V_{C7}=\dfrac{(i_{L4}+i_{C6})D}{C_7f_s};\, \Delta V_{C0}=\dfrac{(i_{L5}+i_{C6})(1-D)}{C_0f_s} \end{array}\right\}. \tag{15}$$

2.5. Voltage and Current Stress Analysis. From the mode-I, the voltage stress of the diodes $D_{1,3,4,5,6}$ and current stress of the switch S_1 and diode D_2 can be determined as

$$\left\{\begin{array}{c} V_{D1}=V_{D3}=V_{D5}=\dfrac{V_i}{1-D} \\ V_{D4}=\dfrac{V_i}{(1-D)^2};\, V_{D6}=V_0-V_i\left[\dfrac{1+D-D^2}{(1-D)^2}\right] \end{array}\right\}, \tag{16}$$

$$\{i_{D2}=(i_{L1}+i_{C7})D;\, i_{S1}=(i_{L1}+i_{C7}+i_{L2})D\}.$$

From the mode-II, the voltage stress of diode D_2, switch S_1, and current stress of the diodes $D_{1,3,4,5,6}$ can be calculated as

$$\left\{V_{D2}=\frac{DV_i}{(1-D)^2};\, V_{S1}=\frac{V_i}{(1-D)^2}\right\},$$

$$\left\{\begin{array}{c} i_{D1}=(i_{C2}+i_{L2})(1-D);\, i_{D3}=(i_{C1}+i_{L3})(1-D) \\ i_{D4}=i_{L2}(1-D);\, i_{D5}=(i_{C5}+i_{L5})(1-D) \\ i_{D6}=(i_{C6}+i_{L5})(1-D) \end{array}\right\}. \tag{17}$$

3. Comparison with Recently Developed Quadratic Topologies

This section presents the comparison of proposed high gain DC converter with recently developed nonisolated topologies. Figure 8(a) illustrates the comparison of voltage gain with various duty cycles. It is worth mentioning that the proposed converter provides higher voltage gain when compared to the topologies developed in [12–23]. Figure 8(b) clearly depicts the total semiconductor switch utilization and operating duty cycle of the proposed converter with other recently developed topologies. From Figure 8(b), it is clearly understood that the proposed converter utilizes a single semiconductor switch as compared with the topologies developed in [12–18, 22, 23]. Increase of semiconductor switch may increase the size of the converter and decrease the power density of the converter. The converters developed in [13–16, 18, 22, 23] were operated at higher duty cycle to obtain reasonable voltage gain which shall increase the conduction loss of the converter. The ratio of voltage gain (M) to Total Component Count (TCC) is measured to find the component utilization factor of the converter. The proposed converter is operated at a duty cycle of 60% which provides a voltage gain of 10.75. Figure 8(c) shows the comparison of M/TCC ratio of the proposed converter with recently developed topologies at duty cycle of 60%. It is noted that the proposed converter developed converter in [17, 22] has a same ratio (0.55), but those topologies utilizes more than a single semiconductor switch. Also, the component utilization factor is performed for a higher duty cycle of 0.8 for all converters, as shown in Figure 8(d). It is noted that the proposed converter has a higher M/TCC ratio as compared with other developed converters in [13, 15–23].

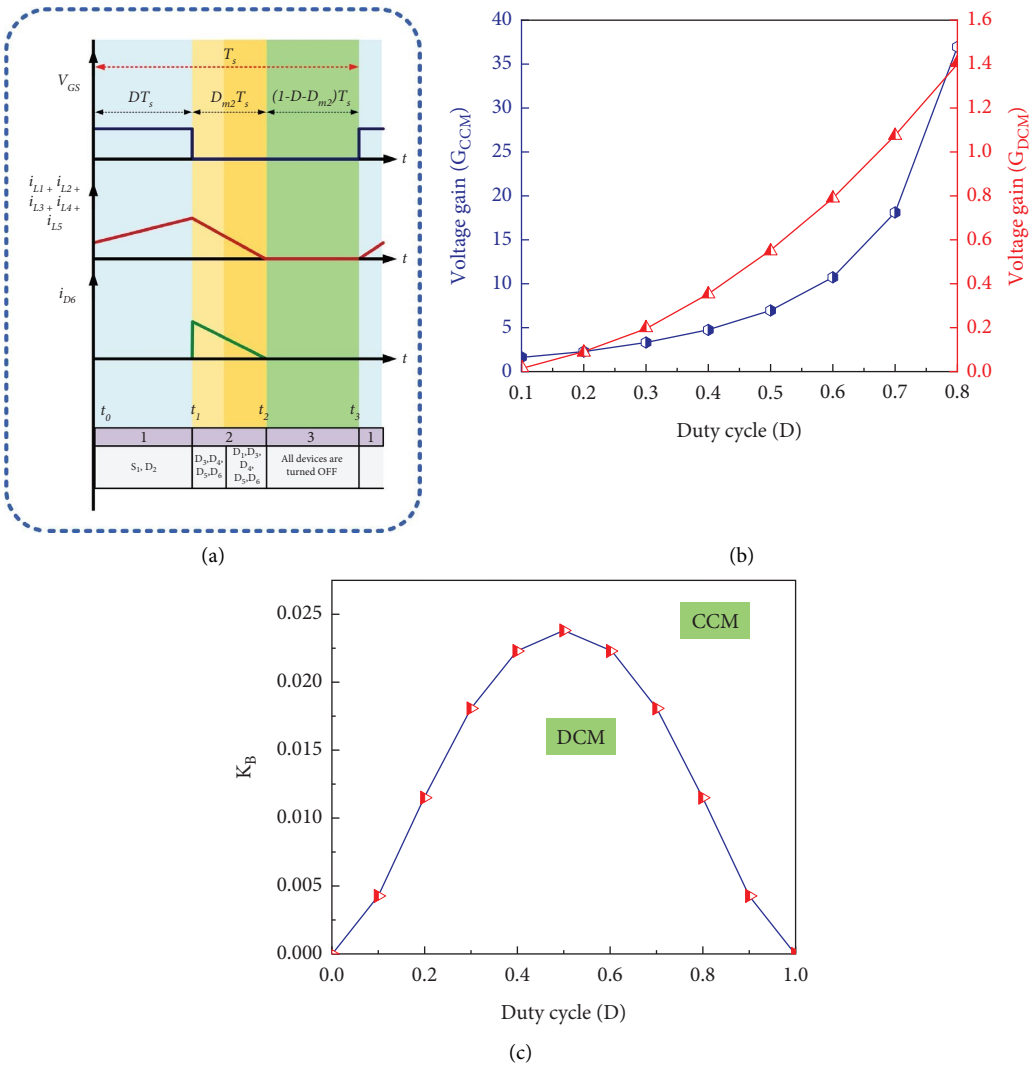

FIGURE 7: (a) Analytical waveform under DCM operation. (b) Voltage gain of CCM and DCM versus duty cycle. (c) (K_b) vs duty cycle.

4. Experimental Results

In order to validate the functionality of the proposed converter in CCM operation, a laboratory-based 200 W prototype is developed. The proposed converter is operated at 50 kHz for an input voltage of 20 V with 60% duty ratio. The parameter of the proposed converter are listed in Table 1.

The maximum height of the prototype is 1.65 inch, and the total area is 6.35 inch^2. Therefore, the power density of the proposed converter is 1.16 kW/L. Figure 9(a) shows the input and output voltage waveform of the proposed converter where the output waveform is maximized in Figure 9(a) to show the magnitude of ripple voltage. It is 1.7% of the output voltage which is similar to the designed value. The obtained experimental result of output voltage is found to be 204 V which is 5% lower than the theoretical value. Figure 9(b) shows the input and output current waveform. The maximum value of input (I_{in}) and output current (I_0) obtained from the experimental result are 11 A and 0.88 A, respectively. The experimental results confirm that the output current is found to be continuous at 60% duty cycle. Therefore, the proposed topology is more suitable for renewable energy applications. Figure 9(c) represents the voltage and current stress of the switch. The maximum voltage across the switch during OFF-state is 121 V. During the ON-state, the maximum current flowing through the switch is 16.9 A. Figures 9(d)–9(f) show the voltage across the diodes. It is observed that the average voltage of diode D_4 blocks the maximum voltage as compared with other diodes.

The reverse peak voltage of the diodes is $V_{R\,D1,3,5\_peak}$ = 44 V, $V_{R\,D2\_peak}$ = 79 V, $V_{R\,D4\_peak}$ = 121 V, and $V_{R\,D6\_peak}$ = 46 V. The maximum voltage across the capacitor is shown in Figures 9(g)–9(j). The maximum value of the individual capacitor voltage is V_{C1} = 48 V, V_{C2} = 49 V, V_{C3} = 29.1 V, V_{C4} = 151.4 V, V_{C5} = 27 V, V_{C6} = 26.9 V, V_{C7} = 102.2 V, and V_{C0} = 204 V. These values are closely matched with the designed values. The dynamic behavior of the proposed converter is examined by changing the duty ratio and load values. Figure 9(k) shows the output voltage and output current for change in load. The values of the

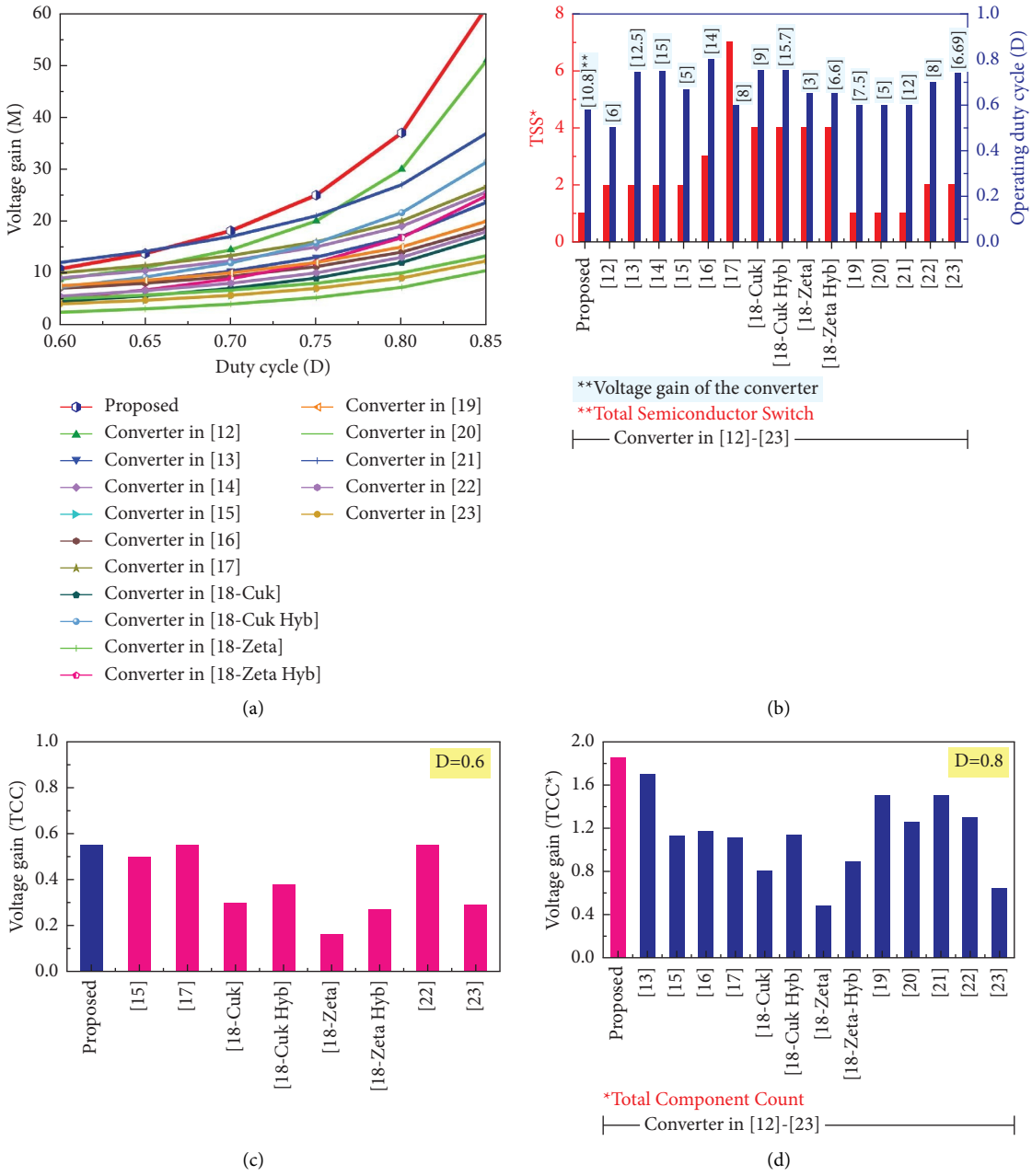

FIGURE 8: Comparison of the proposed converter with recently developed converters found in [12–23]. (a) Voltage gain vs duty cycle. (b) TSS vs duty cycle. (c) Voltage gain/TCC for $D = 0.6$. (d) Voltage gain/TCC for $D = 0.8$.

resistive load is adjusted (i.e., R = 308Ω, R = 230Ω, and R = 230Ω) at 60% duty cycle. It is observed that the output voltage is maintained constant, and the output current varies with the load. Figure 9(l) shows the variation in output voltage for the various duty cycles. The proposed converter is tested by varying the duty cycle (i.e., $D = 0.4$, 0.5, and 0.6) for a constant load of R = 185Ω.

The power loss and efficiency of the proposed converter are analyzed to show the effectiveness of the proposed converter. The expression for the total power loss is

$$\left\{P_{\text{Loss}} = P_{\text{ind}} + P_{\text{cap}} + P_{\text{switch}} + P_{\text{diode}}\right\}, \tag{18}$$

where P_{ind} and P_{cap} are the total power loss of the inductors and capacitors, respectively. P_{switch} and P_{diode} are the total

Table 1: Specifications of the proposed converter.

Component	Values	Dimension
Inductors	$L_1 = 1.2$ mH, $L_2 = 3$ mH, $L_3 = L_4 = 1$ mH, $L_5 = 1.4$ mH	1.5 inch $(L) \times 1.15$ inch $(B) \times 1.08$ inch (H)
Capacitors	$C_1 = C_2 = 12\,\mu$F(ESY156M063AC3), $C_4 = C_7 = 10\,\mu$F (ESK106M160AH1), $C_3 = C_5 = 33\,\mu$F (ESY336M050AG1), $C_6 = 6.8\,\mu$F (ESY685M050AC2) and $C_0 = 5.6\,\mu$F (ESK685M250AG3)	0.43 inch $(L) \times 0.19$ inch (D), 0.47 inch $(L) \times 0.39$ inch (D), 0.28 inch $(L) \times 0.31$ inch (D), 0.28 inch $(L) \times 0.19$ inch (D), 0.43 inch $(L) \times 0.31$ inch (D)
Diodes	$D_1 = D_3 = D_5 = D_6 =$ MUR1610CTG, $D_2 =$ MUR1615CTG $D_4 =$ STTH2002)	0.42 inch $(L) \times 0.19$ inch $(B) \times 1.18$ inch (H) 0.41 inch $(L) \times 0.18$ inch $(B) \times 1.17$ inch (H)
MOSFET	IXFH120N30X3	0.62 inch $(L) \times 0.19$ inch $(B) \times 1.65$ inch (H)

L-length, B-breadth, H-height, D-diameter.

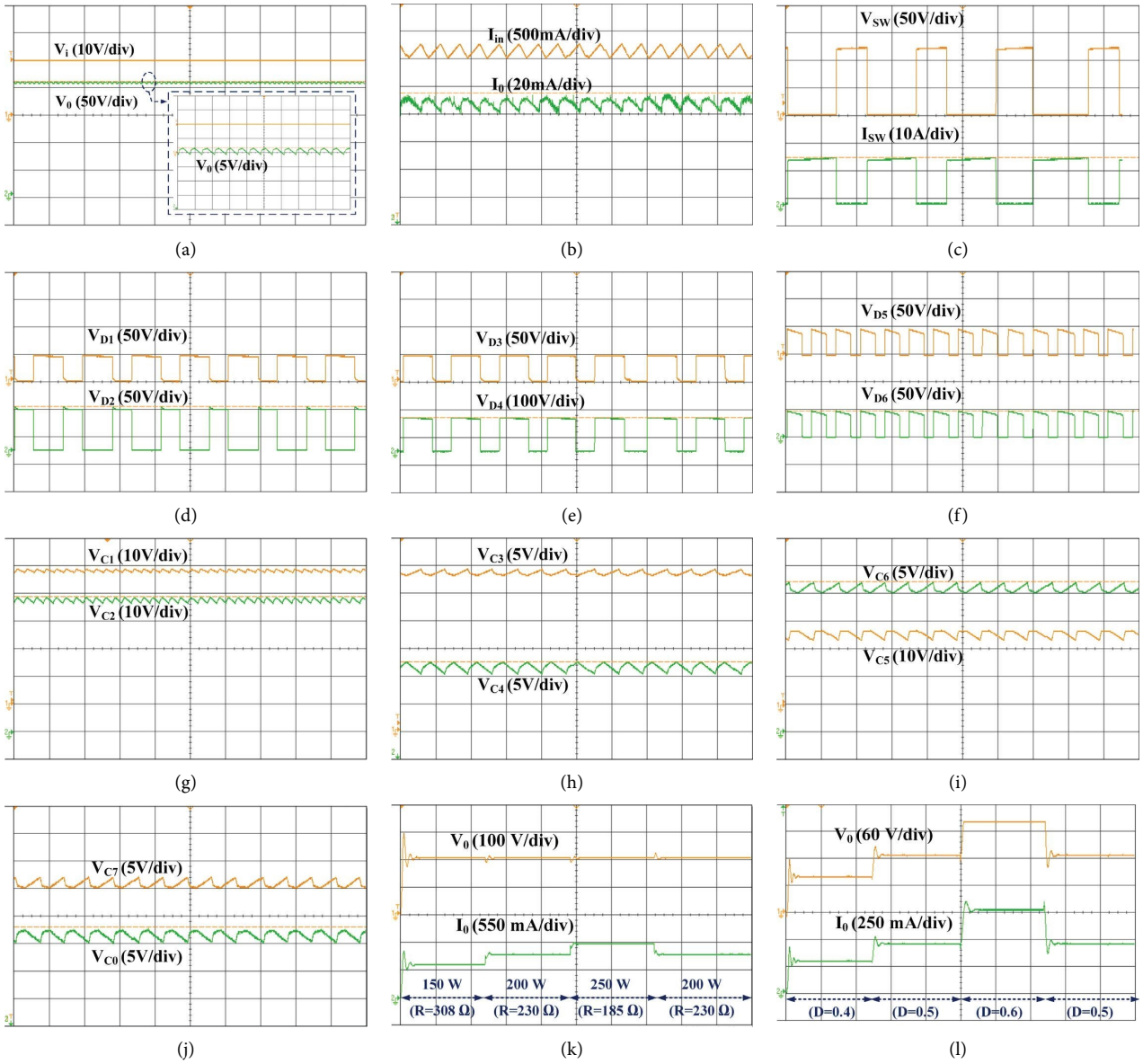

Figure 9: (a) Input and output voltage, (b) input and output current, (c) voltage and current stress on switch, voltage across diodes, (d)D_1 and D_2, (e)D_3 and D_4, (f)D_5 and D_6, (g) voltage across capacitors C_1 and C_2, (h)C_3 and C_4, (i)C_5 and C_6, (j)C_7 and C_0, (k) output voltage and output current for the varying load, and (l) output voltage for the varying duty cycle.

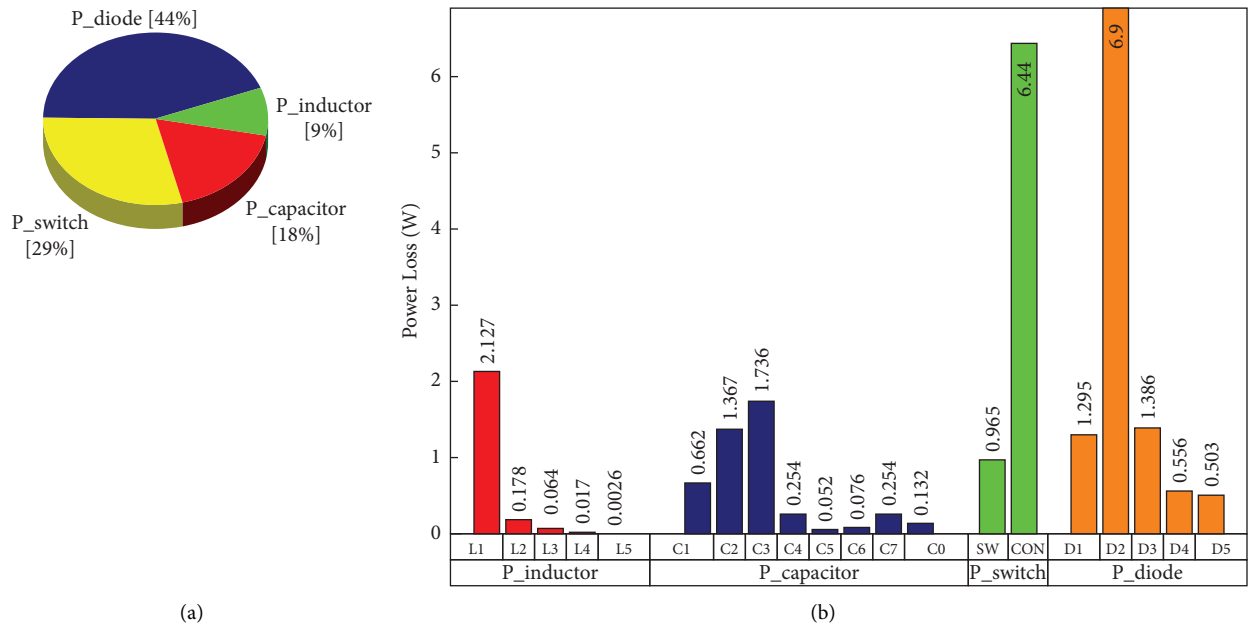

Figure 10: (a) Cumulative losses. (b) Loss breakdown analysis.

power loss of switch and diodes, respectively. The conduction loss and switching loss are considered for calculating the P_{switch}.

The power loss expression for individual components are given below:

$$\left\{\begin{array}{l} P_{\text{ind}} = \sum_{n=1}^{5} r_{Ln}.i_{Ln}^2;\ P_{\text{cap}} = \sum_{n=1}^{7} r_{Cn}.i_{Cn}^2 \\ P_{\text{diode}} = \left(\sum_{n=1,\ n\neq 2}^{6} r_{F\,Dn}.(1-D)i_{Dn}^2 + V_{F\,Dn}.(1-D)i_{Dn} \right) \\ \quad + \left(r_{F\,D2}.Di_{D2}^2 + V_{F\,D2}.Di_{D2} \right) \\ P_{\text{cond.loss}} = r_{DS}D\left(i_{S1}\right)^2 \\ P_{\text{switching.loss}} = f.C_s.\left(\dfrac{V_i}{(1-D)^2}\right)^2 \end{array}\right\}, \quad (19)$$

where r_{DS} is the ON-state resistance of the MOSFET; r_L and r_C are the equivalent series resistance of inductor and capacitor, respectively; and r_{FD} and V_{FD} are the forward resistance and threshold voltages of the diode, respectively. Figures 10(a) and 10(b) show the cumulative loss of the proposed converter components and breakdown loss of the individual components in the proposed converter, respectively. The loss analysis for individual components will help to evaluate the efficiency of the converter. This proposed converter delivers an efficiency of 90% for an input voltage of 20 V with a 60% duty cycle for a switching frequency of 50 kHz. From the loss breakdown analysis, it is confirmed that the loss of diode D_2 and conduction loss of the switch is higher than the other components.

5. Conclusion

A high gain DC-DC converter has been proposed and examined under CCM, DCM, and BCM in this article. The steady-state voltage gain has been derived along with the voltage stress and current stress of the components. The mathematical expression for designing the inductors and capacitors has been provided. The proposed topology has been tested with 200 W in the laboratory-based prototype, and the results have been obtained effectively. The proposed topology has tested with dynamic condition by changing the duty cycle and load value to check the feasibility of the topology. The efficiency and power density of the proposed converter is 90% and 1.16 kW/L, respectively. The proposed converter utilizes a single switch for achieving higher voltage gain so that it could be useful for RES applications.

Data Availability

Not applicable for this research work.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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