Research Article

A Single DC Source Generalized Switched Capacitors Multilevel Inverter with Minimal Component Count

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Received 11 March 2023; Revised 9 May 2023; Accepted 23 May 2023; Published 3 June 2023

Academic Editor: Mahdiyeh Eslami

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This paper presents a new single-source switched capacitor- (SC-) based multilevel inverter (MLI) design with a boosting potential of three times the supply voltage. To produce a waveform with seven output voltage levels, the suggested switching capacitor inverter consists of eight switches, single diode, and two capacitors. Because capacitors are inherently balanced, there is no need for a balancing circuit or sensor. The structure can be expanded using the provided generalized equations. In addition, the technique for switching control and loss analysis is explored. A fair comparison with the most recent SCMLI topologies has been conducted to demonstrate the merits of the proposed work. Furthermore, the proposed topology is evaluated using the MATLAB/SIMULINK tool, and experiments under both transient and steady-state situations are performed to demonstrate its feasibility. At dynamic-loaded situations, the performance of the proposed SCMLI with dynamic modulation index and switching frequency is tested.

1. Introduction

The multilevel inverter is becoming more popular in industrial and academic applications because of its enhanced power quality, efficiency, low losses, and total harmonic distortion (THD). The use of MLIs provides significant benefits in the fields of medium- and high-voltage applications [1, 2]. In comparison to conventional inverters, it has a better power handling capacity and a higher degree of modularity, and it requires a relatively smaller amount of filtering. Because of its flexible design, MLI can be used in many different fields of electrical engineering. Generally, there are three types of conventional MLIs such as flying capacitor (FC) MLI, diode-clamped (DC) MLI, and Cascaded H-bridge (CHB) MLI. They enclose some disadvantages in terms of voltage stress, the number of active-passive components, a capacitor’s voltage maintaining its own self-balancing voltage, and voltage gain.

For example, DC MLI and FC MLIs have difficulties with capacitor voltage balancing and need multiple switching components for a multilevel voltage generation. The cascaded H-bridge MLI is one such device that receives extensive use in renewable energy integration system (REIS). The CHB MLI is one of the most popular topologies in the literature because of its simple and extensible design [3].

Numerous isolated sources (DC) are used in the MLI topologies proposed in [4–6]. As a result, it preserves to be used in either as asymmetrical or a symmetrical configuration. All of these MLI topologies feature a modular design, making it simple to add more basic cells or subcells to increase the output voltage. But each of these topologies requires a much higher amount of isolated DC sources at input and power components, which fallout in an increase in size. This, in turn, causes the circuit to be cumbersome and expensive. The problem is caused by the fact that there are several DC sources available. However, these are excellent
for locations that have access to a variety of input sources, such as renewable forms of energy. The output voltages are generated by a novel MLI topology in which voltage sources are connected in a series-parallel configuration. H-bridge makes it simple to combine numerous DC sources into a renewable energy system [7, 8].

The switched capacitor SC topologies in recent years have a great interest in the research field because of some excellent features such as (i) boosting the ability of the input voltage, (ii) multiple DC voltage sources can be replaced by capacitors, and (iii) inherent self-balancing property of capacitors. These factors reduced the weight, size, and costs. The series-parallel combination of the DC source and capacitor of the multilevel inverter has good modular structure features and capacitor voltage balancing without any external balancing circuit presented in [9–11]. Multiple sources advocated in [12, 13] have back-end H-bridge. Due to the fact that it comprises various sources, it becomes complicated and expensive. The authors in references [13–19] further describe an active NPC capacitor inverter in the midst of a similar principle with a voltage-boosting capability of 1.5V_{DC}. The topology described in [20, 21] has a modular SC structure with a minimum number of switching components. Another generalized structure of the SC technique reduces the total standing voltage for generating seven voltage levels, but switching components is increased [22–26]. The topology proposed in [22] reduced the blocking voltage, i.e., the voltage stress is within the supply voltage but larger numbers of passive and active components are used. A cross-switched triple gain SC topology is presented in [27–29]. However, this topology suffers several drawbacks, such as it includes a larger number of switching components and higher discharging time compared to the charging time of capacitors. The preceding paragraphs inspire the development of a novel generalized SC-based topology with less active and passive components, boosting capability, and self-balancing capability.

In light of these concerns, this study proposes a unique compact SC inverter with the following noteworthy characteristics:

(a) The capacitors are self-balancing.
(b) Power supply voltage-boosting capabilities (i.e., three times the supply voltage).
(c) Less than 50% of switches operate for any level of voltage.
(d) Each fundamental cycle has an identical number of repetitions for both charging and discharging.
(e) The smallest possible number of switching components.
(f) The switching components are subjected to less voltage stress.
(g) The generalized structure of SCMLI is easily achievable.

The enduring sections of the article are structured as follows: Section 2 includes a description of the suggested topology, the operational principle of different states, the finding of the most optimal capacitance values, the inherent-balancing capability of capacitors, and the modulation scheme. Loss analysis of the SCMLI topology is presented in Section 3. Section 4 discusses the generalized structure. Section 5 discusses the simulation process as well as the interpretation of experimental results. The relative analysis is introduced in Section 6 to confirm the significance of the structural design. Discussion on findings and applicability are also presented. Finally, Section 7 concludes with the highlights of the suggested topology.

2. Proposed Seven-Level SC-MLI Topology

Figure 1 illustrates the suggested seven-level SC MLI topology’s structural design. It is composed of two floating capacitors C_2 and C_1, a power diode D, and a direct current source V_{DC}. Two distinct types of eight-power semiconductor switch S_{i} (x = 1, 2, ..., 8) are described, as depicted in Figure 1. (a) IGBTs by antiparallel diode and (b) IGBTs not including antiparallel diode are considered. A threefold voltage-boosting capability is provided by the proposed topology (0, ±V_{DC}, ±2V_{DC}, ±3V_{DC}). The capacitors, C_1 and C_2, are inherently self-balanced. It has four pairs of complementary switches (i.e., S_1S_2S_3S_4, S_5S_6S_7S_8) to evade the short circuit. The charging path of the capacitors and load is indicated by dotted red and black lines. Table 1 explains the conceptual topology’s valid switching states. The “OFF” and “ON” states of the switches are represented by “0” and “1.” Table 2 summarizes the stresses on the switches.

2.1. Working Principle. The operating concept of the suggested MLI is demonstrated with the help of the following states listed in Table 1 and the analogous circuit design illustrated in Figure 2.

(i) State-1 (output voltage v_0 = 0): This voltage level can be achieved in two ways, i.e., the switches S_1, S_4, and S_7 (or S_2S_3S_6) are ON. In both ways, capacitors C_1 are brought in parallel with the DC source and charged up to a voltage equivalent to 1V_{DC}. The equivalent circuit representations intended for zero voltage level are displayed in Figures 2(a) and 2(b).

(ii) State-2 (output voltage v_0 = 1V_{DC}): In this state of operation, the switches S_1S_2S_3S_4, and S_7 are activated simultaneously to achieve the output voltage v_0 = 1V_{DC}. During this state, the capacitors C_1 are charged to 1V_{DC}. Figure 2(c) depicts the equivalent state of V_{DC} voltage level.

(iii) State-3 (output voltage v_0 = 2V_{DC}): In this state of operation, the switches S_2S_3S_6S_7, and S_7 are activated simultaneously to achieve this voltage v_0 = 2V_{DC} level at the output. During this state, capacitor C_3 charges to 2V_{DC}. The corresponding circuit of this state is presented in Figure 2(d).

(iv) State-4 (output voltage v_0 = 3V_{DC}): To obtain this output voltage level v_0 = 3V_{DC}, the switches S_2S_5S_8, are switched on simultaneously. During
International Transactions on Electrical Energy Systems

2.2. Design of Optimum Values of the Capacitor. The capacitors get charged while they are connected in shunt fashion by way of an isolated DC voltage source ($V_{DC}$) and discharge their deposited energies to the output when connected with the supply source. The discharging values of capacitance are expressed as

$$\Delta Q_{c,j} = \int_{\theta_1}^{\theta_2} I_p \sin(\omega t - \varnothing)dt,$$

where $\theta_1$ and $\theta_2$ are the longest releasing time span, $I_p$ is the maximum load current values, and $\varnothing$ is the power factor angle.

The values of $\theta_1$ and $\theta_2$ can be measured as follows [26] from Figure 3(b):

$$\theta_1 = \frac{\sin^{-1}1/3}{2\pi f},$$

$$\theta_2 = \frac{\sin^{-1}1/3}{2\pi f}.$$

The optimal capacitance values are determined by the subsequent factors: (i) peak load current values, (ii) highest discharging period, and (iii) lowest voltage ripple ($AV$) [17, 18]. As a result, the best possible capacitance values can be mentioned as

$$C_i \geq \frac{\Delta Q_{c,j}}{\Delta V_{c,j}}.$$

The maximum voltage spikes may be computed for pure resistive load

$$\Delta V_{c,1} = \frac{1}{\omega R_1} \int_{\theta_1}^{\theta_2} V_{DC}dt + \frac{1}{\omega R_1} \int_{\theta_1}^{\pi - \theta_2} 2V_{DC}dt,$$

$$\Delta V_{c,2} = \frac{V_{DC}}{\omega R_2} [2\pi - \theta_1 - 2\theta_2],$$

$$\Delta V_{c,3} = \frac{1}{\omega R_2} \int_{\theta_1}^{\pi - \theta_2} 2V_{DC}dt,$$

$$\Delta V_{c,4} = \frac{V_{DC}}{\omega R_2} [2\pi - 4\theta_2].$$

The details of self-balancing based on the parallel/series procedure of the switched capacitors as shown in Figure 2 make the capacitors self-balanced automatically [22].

2.3. Modulation Strategy. The suggested inverter is switched using a technique called phase disposition pulse with modulation (PDPWM). In this technique, a 50 Hz sine wave (u) is compared with eight constant signals (0+, 1/3, 2/3, 1, 0−, −1/3, −2/3, and −1), and the results are fed into a “AND” gate and a “Ex-OR” gate to yield the desired outputs.
In the second step, the sine wave is compared with six 1/3-height carrier signals $e_1, e_2, e_3, e_4, e_5,$ and $e_6$ to produce the corresponding output signals $j_1, j_2, j_3, j_{11}, j_{22},$ and $j_{33},$ as shown in Figure 3(b) and graphically in Figure 3(c). Each of the signals $P_1, P_2, P_3, P_4, P_{11}, P_{22}, P_{33},$ and $P_{44},$ as well as their inverted counterparts, are fed into separate “AND” gates in the auxiliary circuit 2 of Figure 3(b), which in turn generate the corresponding outputs $x_1, y_1, x_2, y_2, x_{11}, y_{11}, x_{22}, y_{22}$ and $y_3.$ Driving pulses for switches $S_1 − S_8$ can be generated.
from the outputs of the auxiliary circuit 2 in Figure 3(b) using "OR" gates and the equations (8)–(14).

\[
S_1 = x_{11} + y_{22} + x_{22} + y_{33} + x_{33}, \quad (8)
\]

\[
S_2 = y_{11} + x_{1} + y_{2} + x_{2} + y_{3} + x_{3}, \quad (9)
\]

\[
S_3 = x_{2} + y_{3} + y_{33} + x_{22} + y_{3}, \quad (10)
\]

\[
S_4 = y_{1} + y_{11} + x_{1} + y_{2} + y_{22} + x_{11}, \quad (11)
\]

\[
S_5 = x_{3} + x_{33}, \quad (12)
\]

\[
S_6 = x_{2} + y_{33} + x_{22} + y_{33}, \quad (13)
\]

\[
S_7 = y_{11} + y_{1} + x_{1} + x_{2} + y_{2} + x_{3}, \quad (14)
\]

**Figure 3**: Control scheme: (a, b) simple logic-based switching scheme; (c) output voltage.
\[ S_8 = y_1 + y_1 + x_{11} + x_{22} + y_{22} + x_{33}. \]

### 3. Power Loss Analysis

This suggested topology has three sorts of losses. These losses are (a) conduction losses, (b) switching losses, and (c) ripple losses.

#### 3.1. Switching Losses \( (P_{sw}) \)

While switches are bowed ON and OFF, switching losses occur. The power losses in favour of every distinctive switch during ON and OFF are shown in Figure 4 [13].

Turn-ON power losses are

\[ P_{on,sw} = \frac{1}{6} f_0 (VI_{on} t_{on}). \]  

Turn-OFF power losses are

\[ P_{off,sw} = \frac{1}{6} f_0 (VI_{off} t_{off}), \]

where \( V \) is the voltage across the switches before and after activation. \( I_{on} \) and \( I_{off} \) are the current flowing through the switches once they are turned on. \( t_{on} \) and \( t_{off} \) are the switch’s OFF and ON times. Thus, the proposed topology’s total losses associated with switching \( (P_{sw}) \) is stated in

\[ P_{sw} = \sum_{n=1}^{8} (P_{on,sw,n} + P_{off,sw,m}), \]  

where \( n \) represents level count and \( m \) represents switch count.

#### 3.2. Conduction Losses \( (P_{con}) \)

As a result of turning on the power switch, conduction losses are incurred. During the ON-state, the internal resistance of the power switch \( (R_s) \) and diode \( (R_d) \) wasted power.

In general, conduction losses are now the sum of the all switches and diodes power losses.

\[ P_{con} = V_{s,on} I_{s,avg} + I_{d,avg}^2 R_{d,avg} + V_{d,on} I_{d,avg} + I_{d,avg}^2 R_{d,on}, \]  

where \( V_{s,on} \) and \( V_{d,on} \) are the ON-state voltage drop of the switch and diode, respectively.

\( I_{d,avg} \) and \( I_{d,avg} \) be the RMS and average current of the diode and switch, respectively.

So, the proposed SC-MLI’s overall power losses associated with conduction are given by

\[ P_{con} = \sum_{i=1}^{k} \left( \sum_{j=1}^{n} (P_{con}) \right), \]

where \( n \) and \( k \) represent switch count and conduction paths, respectively.

#### 3.3. Ripple Losses \( (P_R) \)

The capacitor charges when a parallel connection is made between it and the power source. The capacitor’s charging current creates ripple losses. So, the voltage ripple can be illustrated [25] from equations (5) and (7) as

\[ \text{Ripple loss } (P_R) = f_0 \sum_{i=1}^{2} (C_i \Delta V_i^2). \]

Therefore, the total power losses \( (P_T) \) are

\[ P_T = P_{sw} + P_c + P_R. \]

### 4. Generalized Structure

Figure 1 shows a simple architecture that can easily be expanded to create a higher output voltage via simply adding SC cells or connecting them in series. By using a SC-based multilevel inverter, increasing the number of SC units increases the output voltage. Capacitors determine the maximum output voltage and serve as virtual sources. The 9-level output voltage is made achievable by including an additional SC unit in the suggested design. The generalised configuration of the proposed SCMLI topology for the expansion is depicted in Figures 5(a) and 5(b). The generalised arrangement of MLI with a SC unit is shown in Figure 5(a), and the generalised structure with a cascade tie is shown in Figure 5(b).

SCMLI’s broad equation can be stated in terms of SCs. As a result, Table 3 lists the recommended SCMLI inverter switches, diode, and output level.

### 5. Comparative Assessment

The suggested SCMLI topology is compared to the seven-level SC topologies provided in Table 4 to assess its benefits. Among other criteria, the proposed architecture was assessed in provisions of maximum blocking voltage (MBV), gain, switch count per level, TSV, and cost function. The proposed and chosen topologies share...
a single-source and seven-level SC topologies. Furthermore, two parameters are evaluated to measure the cost-effectiveness of the structural design: component count per level and cost function. Switch count per voltage level \( F_{CL} \) is defined as follows:

\[
F_{CL} = \left( N_S + N_{SW} + N_C + N_D \right) / N_L
\]  

(23)

Cost function is defined as

\[
CF = \left( N_{SW} + N_C + N_D + \alpha * TSV_{pu} \right) \times N_S / N_L
\]  

(24)

The weight factor \( \alpha \) will be near to unity and it completely depends on switching components’ significance or the maximum load voltage. In the proposed architecture, this factor (\( \alpha \)) is “1”, i.e., both switching components and TSV\(_{pu} \) are equally important. As the name implies, TSV\(_{pu} \) is the sum of all each switch voltage stresses divided by the maximum load voltage. These two factors \( F_{CL}, CF \) decide the cost, size, and weight of the inverter. The proposed architecture is comprised of only 8 switches, one diode, and two capacitors in order to provide a 7-level output. It is noticed that the value of \( F_{CL} \) and CF of the anticipated topology is not as much as the recently proposed SCMLI topologies mentioned in Table 4 except the ones in \([31, 32, 35]\). However, the gain in \([30–35]\) are less than the proposed one. This shows the said topology is associated with a smaller number of the driver unit, heat sinks, protection units, etc. Henceforth, the proposed converter’s overall system cost, weight, and size are low among the state-of-the-art topologies. These features make the suggested topology more attractive and advanced. However, the topologies advocated in \([16, 18, 22, 30–34]\) have a higher number of capacitor unit which means their stress and inrush current are very high, which degrades their reliability.

### 6. Results and Discussions

#### 6.1. Simulation Results

A MATLAB/Simulink model of a seven-level SC inverter is constructed to test the viability of the proposed MLI. Table 5 displays the simulation parameters used in the analyses. The suggested inverter steady-state performance has been simulated under an R-L load (30 and 80 mH). Figure 6(a) depicts current and voltage waveforms.
Each step’s voltage is 50 V, and the highest output is 150 V. Due to the input source of 50 V, an increase gain of 3 is realized, which agrees with the theoretical notion.

The finding that the 2 capacitors are inherent-balancing with diminish voltage ripples supports the investigation of balancing the capacitor voltage. The consequences of the rapid shift in load are shown in Figure 6(b). The findings show the inverter’s ability to work across an extensive choice of loads, with a peak voltage of 3Vdc at a 7-level.

The proposed inverter can respond to variations in carrier wave frequency accurately. Figure 6 shows the voltage and current output vs. frequency (c). In all instances, it was discovered that the inverter exhibits a quick transient reaction (200 Hz to 2 kHz). The output voltage varies when the modulation index (M) amplitude varies, as seen in Figure 6(d). When M lowers from 0.9 to 0.75 and subsequently to 0.2, the output voltage steps down from seven levels to five levels and then three levels, as shown in Figure 6(d). The speedily completion of the transient operations conveys the high transient performance of the proposed inverter. To investigate power losses, the proposed model was simulated using PLECS-based software, and the IGBTs datasheet was imported. The THD analysis of voltage and current is shown in Figures 6(e) and 6(f). Figure 6(g) depicts the power loss distribution for a purely resistive load. Overall, the proposed topology has an efficiency of around 96.2%.

6.2. Experimental Results. Experimentation with a research laboratory model is given here to authenticate the theoretical conclusions and reveal the viability of the suggested topology in both steady-state and dynamic circumstances.

Table 4: Comparative analysis with other seven-level existing SCMLI in literature.

<table>
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Each step’s voltage is 50 V, and the highest output is 150 V. Due to the input source of 50 V, an increase gain of 3 is realized, which agrees with the theoretical notion.

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Table 5: Simulations and experimental parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<td>Output frequency (f)</td>
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<td>Switching frequency (fS)</td>
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<tr>
<td>Driver</td>
<td>TLP250</td>
</tr>
</tbody>
</table>

The suggested inverter steady-state operation has been tested using an R-L load model (30 and 80 mH). Figure 7 depicts a voltage and current waveform (a). The maximum output is 150 V, with 50 V increments. With a 50 V input voltage, a boost gain of 3 is obtained, which is reliable through the theoretical expectation.

Figure 7 depicts the experimental waveform of the step change load’s load voltage vL, load current iL, and voltage across the capacitors (b). When there is a sudden shift in load, the load voltage level remains constant. The waveform shows that when a step change in load is introduced, the voltage across the two capacitors is inherently balanced. Figure 7(c) also depicts experimental results for scenarios with a variable switching frequency (in this, i.e., 100 Hz and 5 kHz). It is vital to note that the output voltage level remains constant under these situations.

As seen in Figure 7(d), the output voltage varies as the modulation index amplitude changes. Furthermore, as seen in Figure 7(d), as M falls from 0.9 to 0.5, then to 0.2, the quantity of output voltage steps lowers from seven to five, then to three. The maximum efficiency obtained from the experimental setup by the use of a power quality analyzer (Fluke 43B) is 97.16%. Finally, experimental results reveal that the proposed design performs adequately in both dynamic and steady-state circumstances.

6.3. Discussions on Findings and Applicability. The suggested design generates a seven-level waveform with three times the voltage gain, as shown by modelling and experimental results. It has been shown that the proposed topology reduces power loss in the switches. Based on a survey of the existing literature on SCMLIs, the following use cases have been identified for the proposed topology:

6.3.1. High-Frequency AC Distribution. Due to the significant reduction in the number of power conversion stages, the size of the transformer, and the size of the filter, a high-frequency alternating current (HFAC) power distribution system (PDS) has gained popularity in high-power density applications such as telecommunication [36, 37], spacecraft, and computer systems [38]. Another emerging field for HFAC PDS is its use in localised networks, such as...
Figure 6: Simulation results: (a) wave of steady state, (b) step-in-load waveforms, (c) step-in-switching frequency waveforms, (d) waveform for modulation index steps of 0.95 to 0.5 and 0.5 to 0.2, (e, f) THD analysis of voltage and current, and (g) graphics of losses.
microgrids, buildings, and electric vehicles [39]. The use of magnetic circuits or dc–dc boost converters can be avoided in low voltage regions when SCMLI topologies are implemented.

6.3.2. Photovoltaic- (PV-) Based Power Generation Systems and Electric Vehicle (EV) Traction System. Renewable sources of energy, such as solar systems, have low power outputs. Cascading PV modules, a dc–dc boost inverter, or

FIGURE 7: Laboratory results: (a) photograph of prototype, (b) steady-state profiles, (c) step-in-load waveforms, (d) step-in-switching frequency waveforms, and (e) waveform for modulation index steps of 0.95 to 0.5 and 0.5 to 0.2.
a step-up transformer can all be used to increase the voltage. These methods raise the bar in terms of complexity, expense, footprint, and energy waste [40]. However, SCMLIs offer grid compatibility, a high-resolution waveform, reduced filtering needs, and increased voltage gain [41, 42]. Cascading the cells in EV systems is one way to get a high dc-link voltage, although charge balancing is a problem [43–45]. To circumvent these limitations of conventional EV drives, SCMLIs are being developed as a practical interface for converting low-voltage dc to high-voltage ac [45, 46].

7. Conclusion

This article describes a revolutionary SC-based boost-type seven-level inverter. The proposed SC-MLI topology's primary objective is to minimize switching components in order to achieve a high gain and with eight switching components and single isolated DC source seven levels are obtained in the output voltage profile. Additionally, the proposed converter output voltage is 3 times that of an input supply voltage, and capacitors are naturally self-balanced. The mathematical modelling of proposed topology is presented and validated with simulated results. Efficiency and loss investigation of the proposed MLI topology are presented and compared the same through the recent literature available on SC-MLI topologies. A brief comparative study has been carried out to check the superiority of other SC topologies in component count per level, MBV, and gain of the converter. This analytical comparison makes the proposed work more competitive and prominent. In the end, the experimental and simulated results for linear and nonlinear loads empower the findings of the study and reveal the practicality of the suggested design topology. Proposed SC-MLI topology performance was good at dynamic linear and nonlinear loads and with dynamic modulation index.

Data Availability

No underlying data were used to support the findings of this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

This work was supported by International Research: SA/China Joint Research Programme 2021, with Reference no. BCSA210303588702 and Unique Grant no. 148770.

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