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Research Article

Design and Implementation of Nonisolated High Step-Up DC-DC Converter

Mehdi Zamani,[1] **Amir Aghaie**,[2] **Ali Zamani**,[3] **Rana Tari**,[4] **Mostafa Abarzadeh**,[5] **and Seyed Hossein Hosseini**[2]

[1]*Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran*
[2]*Faculty of Electrical and Computer Engineering, University of Tabriz, 29th Bahman Blvd, Tabriz, Iran*
[3]*Faculty of Electrical and Computer Engineering, University of Hormozgan, Bandar-e-Abbas, Iran*
[4]*Electrical Engineering Department, Seraj Higher Education Institute, Tabriz, Iran*
[5]*R&D Department, SmartD Technologies, Montreal, Canada*

Correspondence should be addressed to Mehdi Zamani; mehdi.zamani67@gmail.com

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This article presents a novel structure for a high step-up DC-DC converter. The proposed converter offers several advantages, including a simple structure, high voltage gain, high efficiency, reduced voltage stress on the semiconductors, and fewer components. A two-winding coupled inductor has been employed to enhance the output voltage level in this topology. The suggested structure has only one power switch with low ON-state resistance ($R_{DS\text{-}ON}$), reducing power losses. Moreover, the zero-voltage switching (ZVS) and zero-current switching (ZCS) features of the diodes of the proposed converter result have improved overall efficiency. To evaluate and ascertain the enhanced performance of this configuration, the study of different modes of operation, steady-state investigation, and a comparative study between the proposed and other relevant topologies are presented. A laboratory prototype is designed and implemented with an input voltage of 12 V, an output voltage of 150 V, and a 200 W rated power level under a 50 kHz switching frequency. The maximum efficiency of the recommended topology is measured at the rated output power, equal to 96.98%. Also, for an output power range from 50 W to 350 W, the efficiency is obtained higher than 95%.

1. Introduction

Recently, the usage of DC-DC converters has risen in electric vehicle (EV) applications, renewable energy, LED drivers, and uninterruptible power supplies system (UPS) [1, 2]. The use of high voltage gain and high-efficiency DC-DC converters is recommended to increase voltage levels and efficiency in renewable energy sources [3]. When designing these converters, it is essential to consider factors such as efficiency, voltage gain, input current ripple, and converter volume. Conventional boost converters are not ideal for high voltage gain due to losses caused by various components [4–6]. Increasing the duty ratio can also lead to issues with the output diode. This can limit the switching frequency and system size while reducing efficiency and causing electromagnetic interference (EMI). To address these issues, nonisolated high voltage gain DC-DC converters have been developed through research [7–10].

In isolated converters, extensive and costly transformers are used [11–13]. So, isolated converters have a higher implementation cost than nonisolated converters [14]. Because numerous applications do not need electrical isolation in a nonisolated DC-DC structure, the usage of coupled inductors equips a valuable voltage-lift technique in these topologies to achieve high step-up voltage gain [15]. Also, by adopting a coupled inductor, two coils can be implemented through one core [16]. Hence, the volume of the structure can be diminished. In [17], a closer investigation of the isolated converter has been presented. Converters employing transformers are regarded as different categories of the dual active bridge (DAB). The main disadvantages of these converters are high dv/dt stresses on AC link

insulation, high conduction losses, a higher number of components, an imbalance in the DC-link capacitor's voltage, and complicated voltage balancing control.

Recently, many studies have been presented in the nonisolated DC-DC converters' area. In [18], an interleaved high step-up topology is introduced for renewable energy systems using the voltage multiplier. This topology has a continuous input current. Nevertheless, the number of components that are used is high. The introduced converters in [19–21] use a voltage multiplier circuit and coupled inductor in their structures. These converters suffer from a high component count and input current ripple. Another nonisolated structure is reported in [22], which has bidirectional and soft switching features. Besides, this converter utilizes a coupled inductor to attain high voltage gain. But, the number of employed power switches is high, which has a negative effect on efficiency.

In [23], several structures are proposed by using one coupled inductor and two power switches. However, they have similar characteristics, such as soft switching, and provide more choices for practical application. In [24], a coupled inductor-based boost DC-DC converter is rendered that is adequate for distributed generation applications. This converter benefits from soft switching and has high efficiency. However, the number of power utilized is high, and the voltage stress over the output diode increases by turns ratio enhancement. In [25], a nonisolated interleaved structure assisted with a coupled inductor is introduced. This structure has a higher number of elements in comparison to other analogous topologies. A coupled inductor-based bidirectional converter is reported in [26], which has high efficiency. Nevertheless, the voltage gain of this converter is lower than other related topologies. Some nonisolated structures are reported in [27, 28]. Although these kinds of topologies provide high voltage gain, they experience some problems, such as low efficiency, hard switching, and a high number of used components. An interleaved transformerless high step-up DC-DC converter without auxiliary switches and low input current ripple is presented in [29] for PV-based power generation systems. This topology benefits from the soft switching of semiconductors, where all power switches and didoes operate under soft-switching conditions. Therefore, higher power efficiency is obtained. In [30], a series LC switch capacitor multistage high voltage gain boost converter is proposed for electric vehicle (EV) usages. The main advantages of this converter are the low number of components and the VMC stages are extendable. Thus, the voltage gain can be adjusted, resulting in reduced voltage and current stress of semiconductors. In [31], a coupled inductor-based interleaved soft-switched high step-up converter is suggested for renewable energy applications. The voltage lift capacitors and coupled inductors are used to increase the output voltage without further increasing the duty cycle of the power switches. Due to the interleaved structure, a low ripple input current is obtained. Also, the voltage stress over power switches is reduced.

This article introduced a new structure of a high step-up DC-DC converter with soft switching capability on the output diode. Comprehensively, the proposed converter offers several advantages, including a high voltage conversion ratio, a simple and compact structure, easy controllability, a low component count, and high efficiency.

In this converter, a two-winding coupled inductor is employed to enhance gain of the voltage. The recommended structure has just one low ON-state resistance ($R_{\text{DS-ON}}$) power switch that reduces the conduction power losses. Also, a noticeable benefit of this suggested topology is the ZVS and ZCS of diodes that can increase efficiency. The rest of the article presents the principle of the modes of operation, analysis of the steady-state and efficiency, design procedure, and comparison between the proposed and other similar configurations. Consequently, an experimental prototype with 12 V/150 V and a 200 W power level under a 50 kHz switching frequency is developed to verify the proposed topology's analysis and truthfulness. The structure of this document is as follows: Section 2 presents the proposed DC-DC converter and its operating modes. The investigation of the suggested structure in steady-state is discussed in Section 3, while Section 4 explains the efficiency interpretation. Design considerations are outlined in Section 5, and comparisons with other topologies are made in Section 6. The experimental results are presented in Section 7, followed by the conclusions in Section 8. Finally, an appendix is included in Section 9.

2. Proposed DC-DC Converter and Its Operating Modes

The proposed high step-up DC-DC converter's power circuit and the primary time waveforms of this structure are demonstrated in Figures 1 and 2, respectively. As demonstrated in Figure 1, the components of the presented topology are one coupled inductor, one power switch (S), four diodes (D_1, D_2, D_3, and D_o), and four capacitors (C_1, C_2, C_3, and C_o). Capacitors C_2 and C_3 act as passive clamps and diminish the voltage stress over the power switch.

Based on the following considerations, it can simplify the steady-state and the operation principle investigations of the proposed structure.

(1) All components of the proposed converter are ideal

(2) Due to the large value of the capacitors, the ripple of the capacitor's voltage can be ignored throughout the period (T_s)

(3) The term of the transitory modes is shorter than the main operation modes' duration

(4) The coupled inductor is assumed as an ideal transformer with a turns ratio equal to $N = n_2/n_1$, leakage (L_k), and magnetizing (L_m) inductances

In the rest of this section, the operation principle of the proposed high step-up topology is analyzed. According to Figure 2, each T_s has one transient mode (mode 1). These transient modes have a small-time duration. The other modes (2, 3, and 4) are the main operation modes.

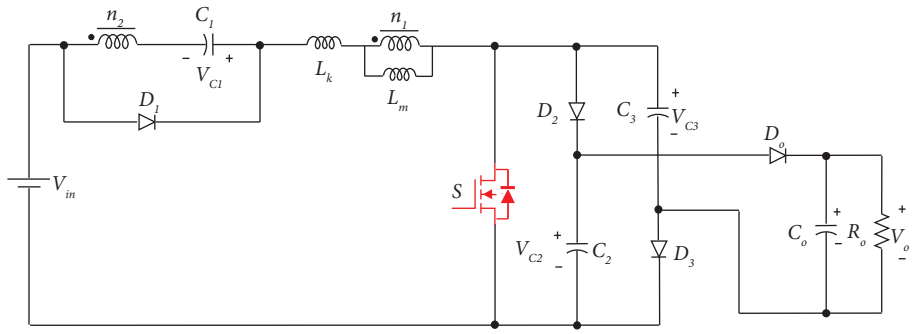


Figure 1: Schematic diagram of the proposed converter.

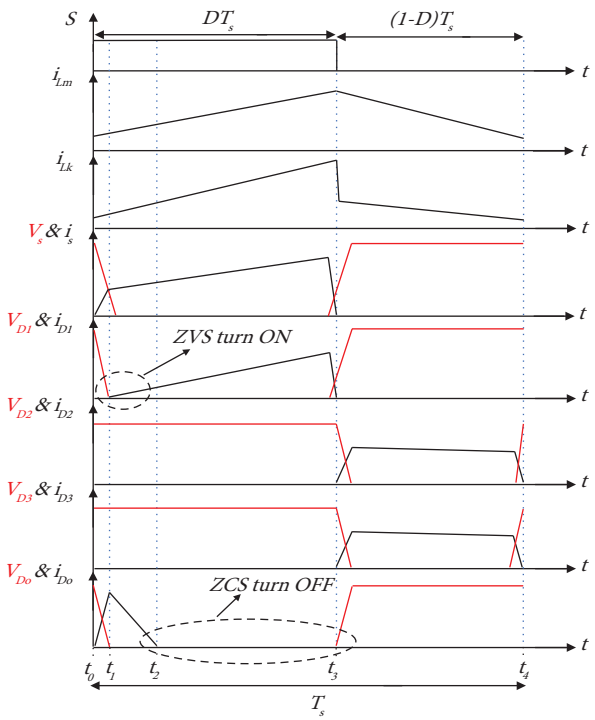


Figure 2: Time waveforms of the suggested structure.

2.1. Mode 1 ($t_0 < t < t_1$). In this transient mode, power switch S is turned ON. Diodes D_1, D_2, and D_3 are reverse biased, and diode D_o is conducted. Also, capacitors C_1, C_2, and C_3 are discharged. One can state that the magnetic current (I_{L_m}) begins to charge linearly by utilizing the energy stored in capacitor C_2. The equivalent circuit is presented in Figure 3(a). Equations (1)–(4) in this mode are

$$k = \frac{L_m}{L_m + L_k}, \tag{1}$$

$$V_{L_m} = k\left(V_{in} + V_{C_1} - V_{n_2}\right), \tag{2}$$

$$V_{n_2} = NV_{L_m}, \tag{3}$$

$$V_{L_m} = \frac{k}{1 + kN}\left(V_{in} + V_{C_1}\right). \tag{4}$$

2.2. Mode 2 ($t_1 < t < t_2$). During this time interval, diode D_1 is turned On at ZVS state. Diode D_o and power switch S are still turned ON. Because of the forward bias of D_1, the voltage of capacitor C_1 is identical to the secondary side of the coupled inductor voltage. In this mode, the currents of L_m and L_k increase linearly. Capacitor C_1 is charged, and C_2 and C_3 are discharged. The equivalent circuit of this mode is displayed in Figure 3(b). Based on this figure, the energy of capacitor C_2 is moved to the load by diode D_o. The equations of this interval are

$$V_{L_m} = kV_{\text{in}}, \tag{5}$$

$$V_{C_1} = V_{n_2} = \text{NV}_{L_m} = \text{kNV}_{\text{in}}, \tag{6}$$

$$V_o = V_{C_2} + V_{C_3}, \tag{7}$$

$$i_{D_1} = i_{C_1} + i_{\text{in}}, \tag{8}$$

$$i_{\text{in}} = i_{L_k}, \tag{9}$$

$$i_S = i_{\text{in}} + i_{C_3}, \tag{10}$$

$$i_{C_3} = i_{C_2} = i_{D_o} = i_{C_o} + i_o. \tag{11}$$

2.3. Mode 3 ($t_2 < t < t_3$). In mode 3, power switch S and diode D_1 are still turned ON. Furthermore, diodes D_2 and D_3 are turned OFF. When t is equal to t_2, at the state of ZCS, diode D_o is turned OFF. Thus, its reverse recovery loss is alleviated. The passing current of capacitors C_2 and C_3 are zero, and C_o is discharged to the load. Magnetic current (I_{L_m}) reaches to the maximum point. The equivalent circuit of this status is shown in Figure 3(c). Moreover, the equations of this stage are achieved by

$$\begin{aligned} i_{C_o} &= -i_o, \\ i_{in} &= i_{L_k} = i_S. \end{aligned} \tag{12}$$

2.4. Mode 4 ($t_3 < t < t_4$). When t is equal to t_3, switch S and diode D_1 are turned OFF. The voltage of capacitors C_2 and C_3 are equal. Moreover, diodes D_2 and D_3 are forward-biased.

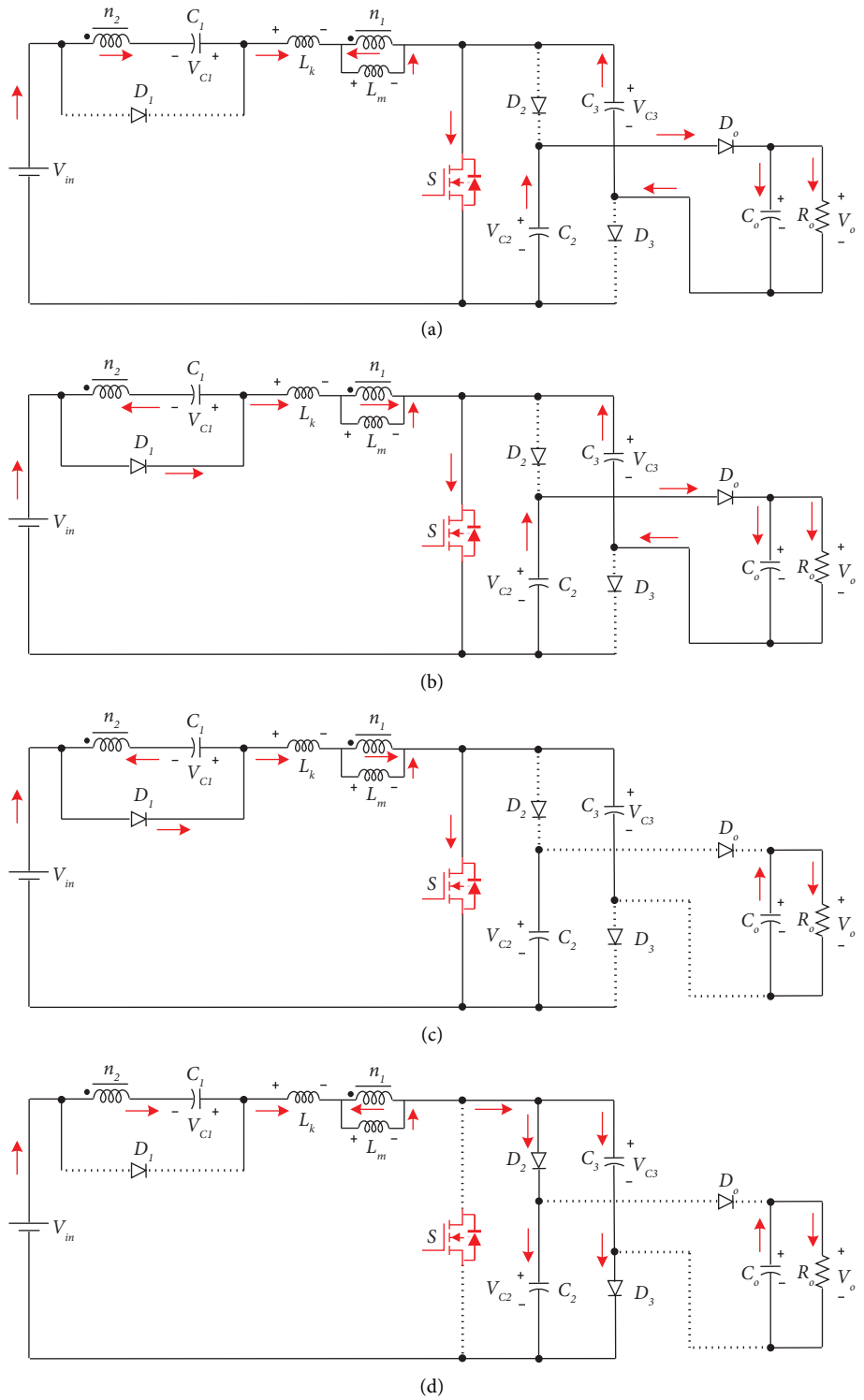


Figure 3: Equivalent power circuits of the proposed structure in the operation modes: (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

These capacitors are charged through D_2 and D_3, and their currents are equal to half of the input current. Furthermore, the currents L_m and L_k decrease in this condition. The equivalent circuit is depicted in Figure 3(d). The equations of this mode are

$$V_{L_m} = \frac{k}{1+kN}\left(V_{in} + V_{C_1} - V_{C_2}\right), \quad V_{C_2} = V_{C_3}, \tag{13}$$

$$i_{\text{in}} = -i_{C_1} = i_{L_k} = i_{D_2} + i_{D_3}, \quad i_{C_2} = i_{C_3} = i_{D_2} = i_{D_3} = \frac{1}{2} i_{\text{in}}. \tag{14}$$

3. Investigation of the Suggested Structure in Steady State

This section presents the voltage gain, voltage stresses of the power switches and diodes, and current equations for the proposed converter based on the assumptions made in the previous section.

3.1. Voltage Gain. In accordance with the principle of volt-second balance upon magnetizing inductor L_m, equations (15) and (16) can be written in the step-up mode:

$$\langle V_{L_m} \rangle_{T_s} = 0, \tag{15}$$

$$D\left(kV_{in}\right) + (1-D)\left(\frac{k}{1+kN}\left(V_{in} + V_{C_1} - V_{C_2}\right)\right) = 0. \tag{16}$$

In equation (6), the voltage of the capacitors C_2 and C_3 is

$$V_{C_2} = V_{C_3} = \frac{V_{in}(1+k+k(N-1)D)}{1-D}. \tag{17}$$

Finally, the output voltage is twice the voltage of capacitors C_2 or C_3

$$V_o = 2V_{C_2} = \frac{2V_{in}(1+k+k(N-1)D)}{1-D}. \tag{18}$$

Ignoring the leakage inductance L_k effect on the output voltage (for $k=1$), the voltage gain equation is

$$M = \frac{V_o}{V_{in}} = \frac{2(1+1+(N-1)D)}{1-D} = \frac{4+2(N-1)D}{1-D}. \tag{19}$$

Figure 4 displays the voltage gain variations versus the turns ratio of the coupled inductor and duty cycle. It is evident that by raising D and N, the voltage gain is enhanced.

3.2. Voltage Stress. As displayed in Figure 3(d), the related equation in mode 4 is

$$V_S = V_{C_2} = V_{C_3} = \frac{2+(N-1)D}{1-D} V_{\text{in}} = \frac{2+(N-1)D}{4+2(N-1)D} V_o. \tag{20}$$

Thus, the voltage stress all over the power switch can be written as

$$V_S = \frac{V_o}{2}. \tag{21}$$

The following equation is written in mode 4

$$V_{D_1} = V_{C_1} - V_{n_2} = V_{C_1} - \text{N}V_{L_m}. \tag{22}$$

Consequently, the voltage stress of the diode D_1 is obtained as

$$V_{D_1} = \text{N}V_{\text{in}} - \frac{N}{N+1}\left(V_{in} + \text{N}V_{\text{in}} - \frac{2+(N-1)D}{1-D} V_{\text{in}}\right). \tag{23}$$

In equations (19) and (23), V_{D1} can be rewritten as a function of the output voltage

$$V_{D_1} = \frac{N(2+(N-1)D)}{4(N+1)+2\left(N^2-1\right)D} V_o. \tag{24}$$

Furthermore, the voltage stress throughout the didoes D_2, D_3, and D_o are archived as follows

$$V_{D_2} = V_{D_3} = V_{C_2} = V_{C_3} = \frac{2+(N-1)D}{1-D} V_{in} = \frac{V_o}{2}, \tag{25}$$

$$V_{D_o} = V_o - V_{C_2} = \frac{2+(N-1)D}{1-D} V_{in} = \frac{V_o}{2}. \tag{26}$$

The voltage stress on power switch S and didoes D_2, D_3, and D_o are the same. Figure 5 depicts the variations of the normalized voltage stresses against D and N. According to Figure 5, the voltage stress across semiconductors is constant with duty cycle variations.

3.3. Calculation of the Current. In this part, the peaks, root mean square (RMS), and average values of the currents are determined. The peak currents of the semiconductors are calculated as follows:

$$i_{D_1} = \frac{(N-1)+2\left(N^2-1\right)D}{1-D} I_o, \tag{27}$$

$$i_{D_2} = i_{D_3} = \frac{1}{1-D} I_o, \quad i_{D_o} = \frac{1+2(N-1)D}{(1-D)} I_o, \quad i_S = \frac{3+2(N-1)D}{D(1-D)} I_o. \tag{28}$$

It is evident that the peak currents of diodes D_2 and D_3 are equal. Also, the peak current of diode D_1 is the maximum peak current of the proposed structure. The average currents of the used semiconductor elements are given by

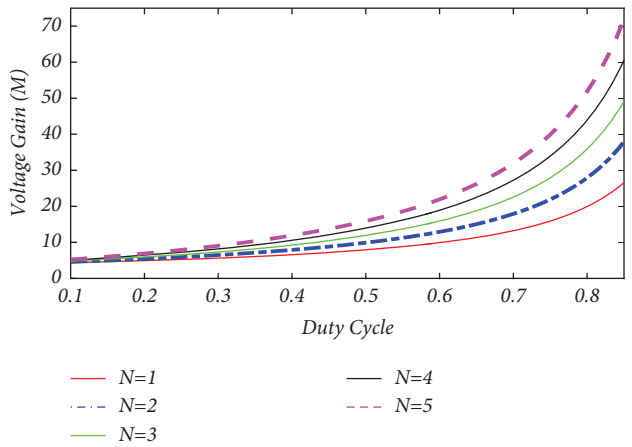


Figure 4: The suggested converter's voltage gain variations versus D and N.

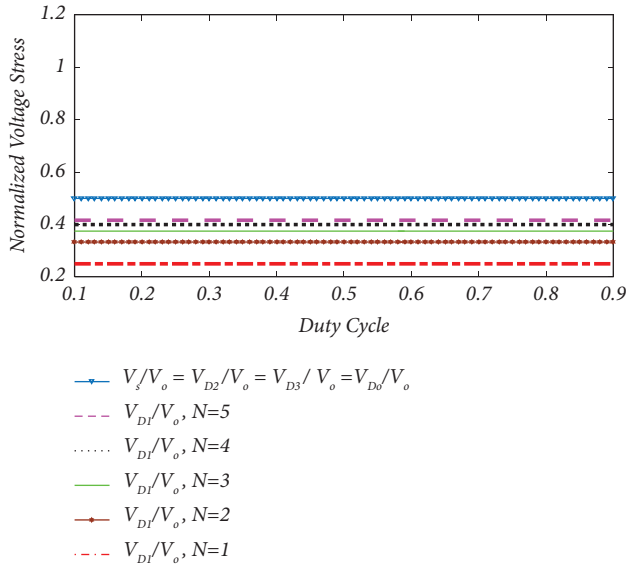


Figure 5: The voltage stress variations over semiconductors versus D and N.

$$I_{D_1} = \frac{(N-1)D + 2\left(N^2-1\right)D^2}{1-D} I_o, \tag{29}$$

$$I_{D_2} = I_{D_3} = I_{D_o} = I_o, \tag{30}$$

$$I_S = I_{in} - I_{D_2} = \frac{3 + 2(N-1)D}{1-D} I_o. \tag{31}$$

According to (30), the average currents are equal for diodes D_2, D_3, and D_o. The RMS currents are essential for efficiency analysis. By (32)–(35), the RMS currents of the power switch and the diodes obtain the following:

$$I_{D_1}^{rms} = \frac{\sqrt{D}\left((N-1) + 2\left(N^2-1\right)D\right)}{1-D} I_o, \tag{32}$$

$$I_{D_2}^{rms} = I_{D3}^{rms} = \frac{1}{\sqrt{1-D}} I_o, \tag{33}$$

$$I_{D_o}^{rms} = i_{D_o} = \frac{\sqrt{D}(1 + 2(N-1)D)}{1-D} I_o, \tag{34}$$

$$I_S^{rms} = \frac{3 + 2(N-1)D}{\sqrt{D}(1-D)} I_o. \tag{35}$$

The capacitors and coupled inductor RMS currents are

$$I_{C_1}^{rms} = I_{n_2}^{rms} = \sqrt{\frac{(3 + 2(N-1)D)^2 + 4N^2D(1-D)}{N^2D(1-D)^2}} I_o,$$

$$I_{C_2}^{rms} = I_{C_3}^{rms} = \sqrt{\frac{1}{1-D}} I_o,$$

$$I_{C_o}^{rms} = \sqrt{\frac{1-D}{D}} I_o,$$

$$I_{n_1}^{rms} = \sqrt{\frac{(3 + 2(N-1)D)^2 + 4D(1-D)}{D(1-D)^2}} I_o. \tag{36}$$

4. Efficiency Interpretation

Considering the parasitic resistances below, the efficiency of this proposed converter can be easily specified.

(1) $R_{\text{DS-ON}}$: the resistance of the MOSFET in a turn-on state

(2) $R_{(\text{Ln1,Ln2})}$: the equivalent series resistor (ESR) of the winding coupled inductors

(3) R_C: the ESR value of the C_1, C_2, C_3, and C_o

(4) R_D: the diodes' resistance in forwarding state

The efficiency of the recommended structure can be calculated by using (37) and (38)

$$\eta = \frac{P_o}{P_o + \Delta P} \times 100\%, \tag{37}$$

$$\Delta P = P_S + P_D + P_{CL} + P_C. \tag{38}$$

In (38), P_S indicates the power loss of the switch S, which can be given by

$$P_S = P_{\text{Cond}} + P_{\text{Switching}}, \tag{39}$$

where P_{Cond} is the conduction losses, and $P_{\text{Switching}}$ is the switching losses of the switch S

$$P_{\text{Cond}} = R_{\text{DS-ON}}\left(I_S^{rms}\right)^2,$$
$$P_{\text{Switching}} = \frac{1}{2} f_s\left(t_{rs} + t_{fs}\right) I_S V_S. \tag{40}$$

P_D shows the losses of the diodes:

$$P_D = P_{\text{Cond\_D}} + P_{\text{Forward\_Voltage}}, \tag{41}$$

where $P_{\text{cond\_D}}$ and $P_{\text{Forward\_Volatge}}$ are the conduction and forward voltage losses of the used diodes, in order

$$P_{\text{Cond\_D}} = \sum_{j=1}^{\text{Number of Diodes}} R_{D_j}\left(I_{D_j}{}^{rms}\right)^2,$$
$$P_{\text{Forward\_Voltage}} = \sum_{j=1}^{\text{Number of Diodes}} V_{D_j} I_{D_j}{}^{avg}. \tag{42}$$

The conduction power loss of the coupled inductor is

$$P_{CL} = R_{L_{n1}}\left(I_{n_1}^{rms}\right)^2 + R_{L_{n_2}}\left(I_{n_2}^{rms}\right)^2. \tag{43}$$

Besides, P_C shows the power loss of all capacitors, which is

$$P_C = \sum_{j=1}^{\text{Number of Diodes}} R_{C_j}\left(I_{C_j}{}^{rms}\right)^2. \tag{44}$$

5. Design Considerations

This section discusses the design of different circuit components. The value of the magnetizing inductor is important in determining the characteristics of the coupled inductor. The turns ratio of the coupled inductor is also crucial as it affects switch voltage stress and duty cycle. Capacitor values are determined based on voltage ripple magnitudes. Finally, the dynamic performance subsection demonstrates the recommended structure's frequency response and control loop.

5.1. Magnetizing Inductance L_m. L_m can be written as

$$L_m = \frac{V_{L_m} D}{\Delta i_{L_m} f_s}. \tag{45}$$

In order to achieve CCM state, the magnetizing inductance current ripple can be presumed as

$$\Delta i_{L_m} \le \frac{I_{L_m}}{2}. \tag{46}$$

Therefore, the value of L_m can be written as a function of the input voltage, average of output current, duty cycle, and switching frequency.

$$L_m \ge \frac{2D(1-D)V_{in}}{(4 + 2(N-1)D) I_o f_s}. \tag{47}$$

5.2. Turns Ratio (N). Using (19), the turns ratio can be derived as follows:

$$N = \frac{M(1-D) - 4}{2D} + 1 = \frac{\left(V_o/V_i\right)(1-D) - 4}{2D} + 1. \tag{48}$$

According to (48), the value of D influences N.

5.3. Capacitors. The value of all used capacitance is

$$C = \frac{i_c D}{\Delta V_c f_s}, \tag{49}$$

that is, the voltage ripple of the capacitors are considered as follows:

$$\Delta V_C = 2\% V_C. \tag{50}$$

Using (50), it can be mentioned that the capacitor's voltage ripple is negligible. Thus, the values of the used capacitors are

$$C_1 \ge \frac{D(3 + 2(N-1)D) I_o}{2\%(1-D) N^2 V_{in} f_s},$$
$$C_2 = C_3 \ge \frac{(1-D) I_o}{2\%(2 + (N-1)D) V_{in} f_s}. \tag{51}$$

5.4. Dynamic Performance. The dynamic performance of the proposed structure is studied using the state-space average method. The system equations are provided.

The following presumptions are investigated in order to have a state equation,

(1) All components are considered ideal

(2) The input current is continuous

The dynamic analysis of the proposed converter based on the open loop transfer function has been performed by using the Bode diagram. The frequency response of the suggested structure, which is named G_{vd} (control-to-output) can be obtained as follows:

$$G_{vd} = \frac{\widehat{v}_o}{\widehat{d}} = \frac{1.01 \times 10^7 s^4 - 8.9 \times 10^{-6} s^3 + 2.14 \times 10^{17} s^2 - 314000 s + 6.22 \times 10^{24}}{s^6 + 99.12 s^5 + 8.88 \times 10^8 s^4 + 9.01 \times 10^{10} s^3 + 3.34 \times 10^{16} s^2 + 5.66 \times 10^{20} s + 7.21 \times 10^{22}}. \tag{52}$$

The equation (52) is obtained by considering the experimental result value and element values. The Bode diagram, which is defined as a control to output transfer function (the magnitude dB and phase frequency response) in the Laplace domain, has been depicted in Figure 6(a). In order to control the output voltage, the closed loop scheme

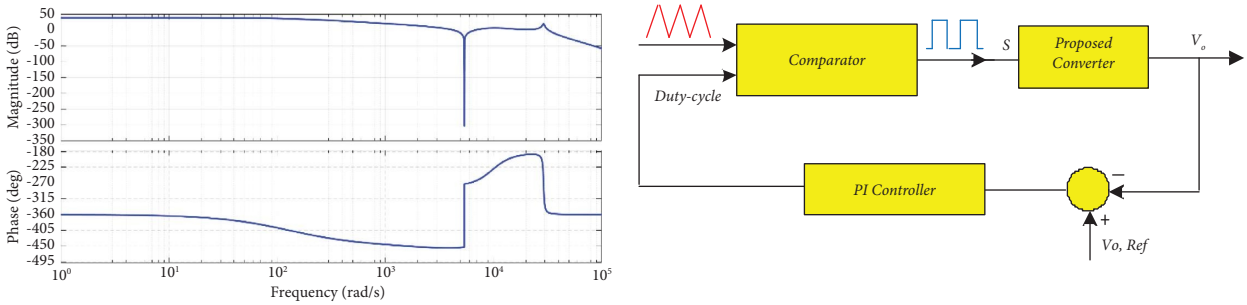


Figure 6: (a) Frequency response of the recommended structure and (b) control loop of the suggested structure.

with a PI controller is suggested, which is indicated in Figure 6(b). As seen in Figure 6(b), the suitable value of the output voltage ($V_{o,\mathrm{Ref}}$) is compared with V_o. The differences between V_o and $V_{o,\mathrm{Ref}}$ is transferred to the PI controller to provide the appropriate duty cycle. Finally, the produced duty cycle via the PI controller is compared with a carrier wave to produce the proper interpolated. It is noticed that the values of PI controller variables, which include a gain and time constant, are achieved by a trade-off.

6. Comparison with Other Topologies

In this part, a comparative study between the proposed coupled inductor-based high step-up DC-DC converter and other converters are provided. In this approach, voltage gain, number of utilized elements, voltage stress all over the diodes and power switches, common ground, input current ripple, continuous input current, and efficiency are regarded. The comparison is presented in Table 1.

According to this Table, the voltage gain of the proposed converter is equal to 13 in $D = 0.6$ and $N = 2$, which is higher than the other introduced converters. Therefore, the proposed structure has a smaller duty cycle, and the coupled inductor turns ratio for the same voltage gain. Figure 7 shows the voltage gain comparison among the presented topologies in Table 1.

The voltage stress of the power switch of the proposed structure is equal to 0.5 for any range of D and N, which is higher than the converters in [1, 3, 6, 10, 12–14] and [16]. However, all of these converters have higher voltage stress across the diodes in comparison to the proposed structure.

Accordingly, the proposed structure has the advantages of high voltage gain, lower voltage stress on the semiconductors, and high efficiency with sufficient elements over the previous topology in the field of coupled inductor-based DC-DC. Thus, it has to be noticed that the presented high step-up converter can be employed in high voltage applications.

The proposed high step-up and high-efficiency DC-DC converter can be used in some of the abovementioned applications, such as renewable energy systems like photovoltaic (PV) and lighting systems. The presented converter can boost the low voltage of the battery (~12 V) to the high voltage level needed in automotive lighting devices that drive high intensity discharge (HID) lamps and LED floodlights. Also, standalone PV-based street lighting systems are another LED technology in which the suggested DC-DC converter can be used to increase the PV panel's low voltage (<20 V) to the needed high voltage level for lighting.

7. Experimental Results

This section evaluates and verifies the operation principle, the steady state, and the efficiency analysis of the proposed structure. The experimental prototype has experimented with 200 W, 12 V input to 150 V output voltage, and 50 kHz switching frequency.

In the Appendix section, the list of the prototype circuit components and the specification of the experimental prototype of the presented topology are given in Tables 2 and 3, respectively. As illustrated in Figure 8, the input, output, and capacitors' (C_1, C_2, and C_3) voltages are measured. In this figure, mathematical analysis related to the voltage of the capacitors is verified. According to Figure 8(a), the voltage of capacitor C_1 is almost 19 V, which verifies equation (6). The voltages of C_2 and C_3 are illustrated in Figures 8(b) and 8(c), which are equal to 75 V. Therefore, these results confirm the accuracy of equation (17). The input and output voltages are shown in Figure 8(d). Because of the turns ratio of the coupled inductor, the high output voltage of 150 V is obtained for the low value of the duty cycle ($D = 0.6$). Figure 9 illustrates the voltage across the power switch S, which is about 77 V and confirms the equation (20). This value is much less than the converter's output voltage. Consequently, in the presented structure, a power switch with a low $R_{DS\text{-}ON}$ can be used, which decreases the conduction loss and improves the efficiency of the converter. The voltage and current measurements of diodes D_1, D_2, D_3, and D_o are depicted in Figures 10(a)–10(d). According to Figure 10(a), the value of the voltage of diode D_1 is almost 51 V, which verifies equation (24). Besides, diode D_1 is turned ON at the ZVS state. The voltage measurement of diode D_2 is shown in Figure 10(b), which is about 77 V.

Figure 10(c) indicates the voltage of diode D_2 is almost 77 V. Finally, the voltage and current measurements of diode D_o are represented in Figure 10(d). The value of the voltage throughout diode D_o is about 77 V, which verifies (26). According to this figure, diode D_o is turned OFF at the ZCS state.

Table 1: Comparison of the high step-up DC-DC converter and similar structures.

Converter	Number of components				Voltage gain	V_s/V_o	V_D/V_o	Eff (%) at 200 W	Common ground	Input current ripple	Continuous input current
	Mag*	S^*	D^*	C^*							
[1]	1	2	5	3	$(N(2-D))/(1-D)=7$	$1/(2N(2-D))=0.17$	$1/(2-D)=0.71$	94.55	No	High	No
[3]	1	1	3	3	$(N+1)/(1-D)=7.5$	$1/(N+1)=0.3$	1	95.5	No	Low	Yes
[5]	2	2	2	3	$N/(1-D)=5$	$1/N=0.5$	1	95.5	Yes	Low	Yes
[6]	2	1	4	5	$(N+1)/(1-D)=7.5$	$1/(N+1)=0.3$	$1/(N+1)=0.66$	96.2	No	High	No
[7]	2	1	2	2	$N/(1-D)=5$	$1/N=0.5$	1	95.9	No	Low	No
[10]	2	1	2	2	$(2+N-D)/(1-D)=8.5$	$1/(2+N-D)=0.29$	$(1+ND)/(2+N-D)=0.65$	94.4	Yes	High	Yes
[12]	2	1	3	3	$(N+1)/(1-D)=7.5$	$1/(N+1)=0.33$	$1/(N+1)=0.66$	—	No	Low	Yes
[13]	2	1	4	3	$(1+ND)/(1-D)=5.5$	$1/(1+ND)=0.45$	$1/(1+ND)=0.9$	93.8	No	High	No
[14]	2	1	3	4	$(N+1)/(1-D)=7.5$	$1/(N+1)=0.33$	$1/(N+1)=0.66$	94.6	Yes	Low	No
[16]	2	4	5	5	$(N+1)/(1-d)=7.5$	$1/(N+1)=0.33$	1	95	Yes	High	No
Proposed	1	1	4	4	$(4+2(N-1)D)/(1-D)=13$	0.5	0.5	96.98	No	High	Yes

$N=2$ and $D=0.6$.

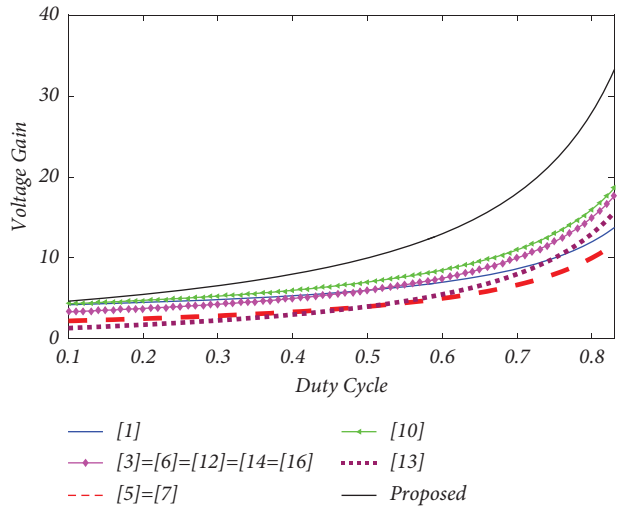


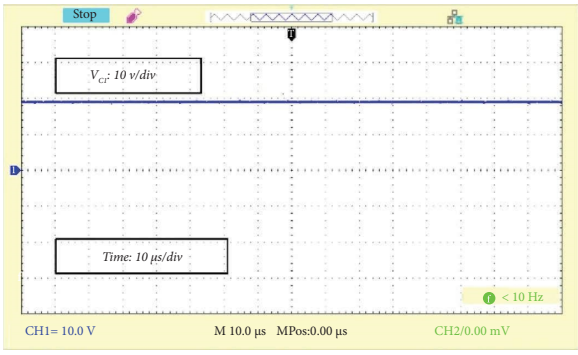
Figure 7: Comparison of the voltage gain between the recommended topology and the other introduced structures.

Table 2: System parameters used in the prototype.

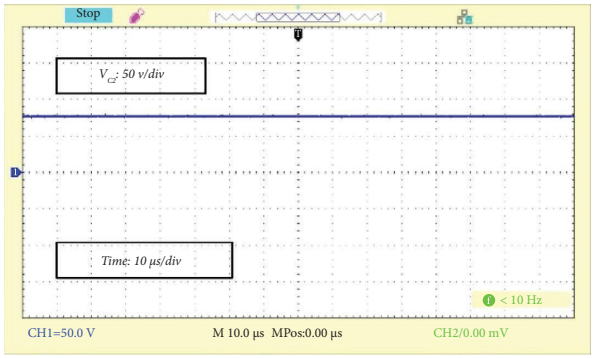
Element	Specification
switch	IRF260 N (200 V/50 A), $R_{DS\ (ON)} = 0.04\ \Omega$
Diodes	MUR2060 (600 V/20 A)
C_1	50 V/47 μF
C_2 and C_3	200 V/220 μF
C_o	450 V/470 μF
Coupled inductor	Ferrite EE core and L_m=200 μH

Table 3: Hardware parameters of the proposed structure.

Parameters	Value
Power rating	200 W
Input voltage	12 V
Output voltage	150 V
Turns ratio	2
Switching frequency (f_s)	50 kHz
Duty-cycle (D)	0.6

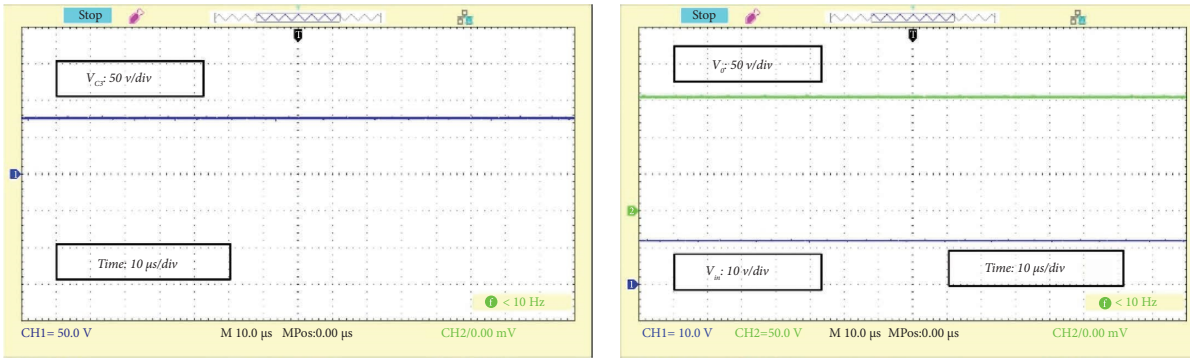


(a)



(b)

Figure 8: Continued.



(c) (d)

FIGURE 8: Voltage measurements: (a) V_{C1}, (b) V_{C2}, (c) V_{C3}, and (d) V_{in} and V_{o}.

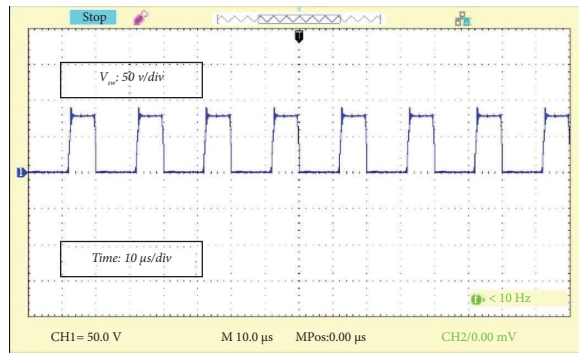
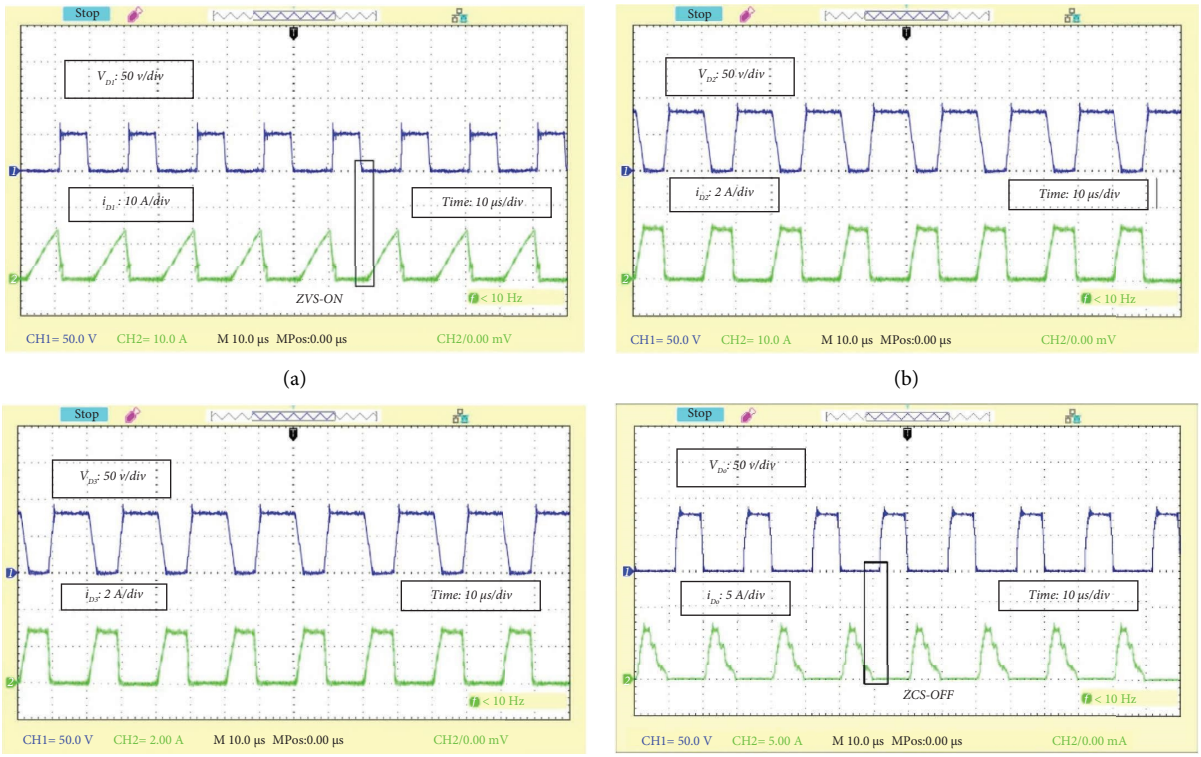


FIGURE 9: The measured voltage of the power switch voltage (V_s).



(a) (b)

(c) (d)

FIGURE 10: Voltage and current measurements: (a) V_{D1} and i_{D1}, (b) V_{D2} and i_{D2}, (c) V_{D3} and i_{D3}, and (d) V_{Do} and i_{Do}.

Table 4: Comparison of calculated and measured voltages at 200 W output power.

Parameters	Calculated (V)	Experimental (V)	Error (%)
V_{C1}	22.8	19	20
V_{C2}	75.6	75	0.8
V_{C3}	75.6	75	0.8
V_{D1}	51.66	51	1.3
V_{D2}	77.5	77	0.65
V_{D3}	77.5	77	0.65
V_{Do}	77.5	77	0.65
V_{sw}	77.5	77	0.65
V_{out}	151.2	150	0.8

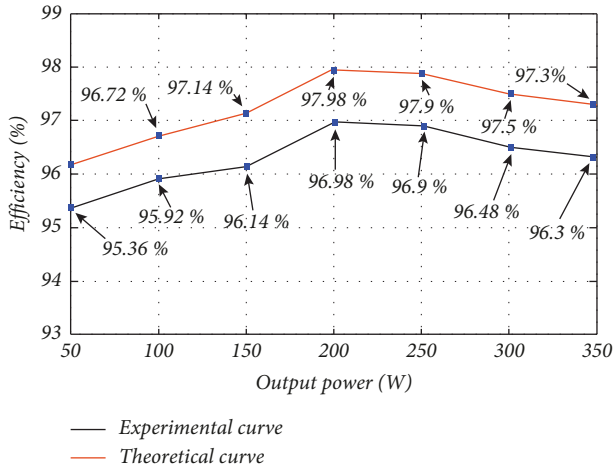


Figure 11: The efficiency curve of the proposed converter.

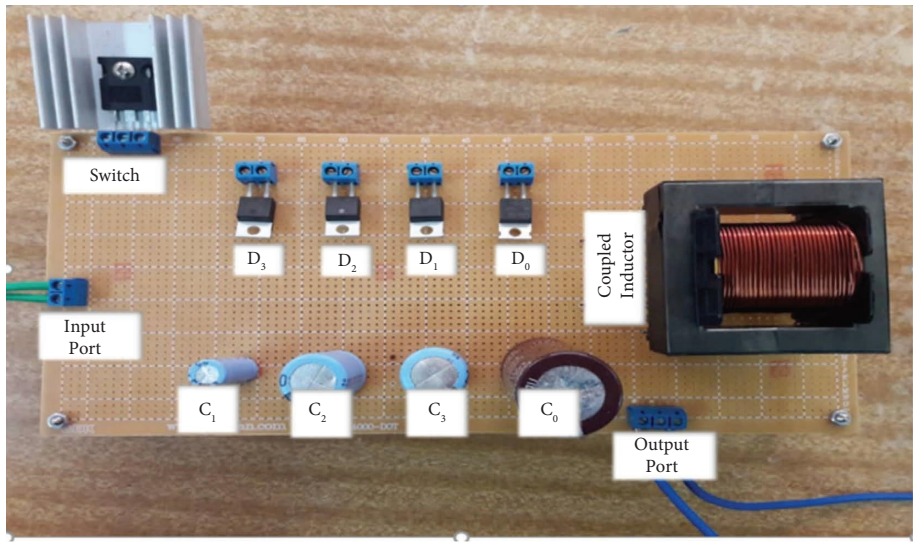


Figure 12: Experimental prototype of the proposed structure.

A comparison between the calculated and measured voltages at 200 W output power is presented in Table 4.

The efficiency curve of the presented nonisolated high step-up DC-DC converter is indicated in Figure 11. From this figure, the maximum efficiency of the proposed topology occurs at the rated output power (200 W), which is equal to 96.98%. Also, the proposed converter efficiency is high using a low ON-state resistance power switch.

Technical investigation and experimental analysis outcomes verify that the recommended converter is an appropriate option for renewable energy applications like PV systems due to the high voltage gain. Also, because of the low peak voltage through the elements, the less number of the power switch and diodes, and the high output voltage, the proposed topology can be utilized for different power rates, Figure 12. The implemented prototype of the proposed structure has been denoted.

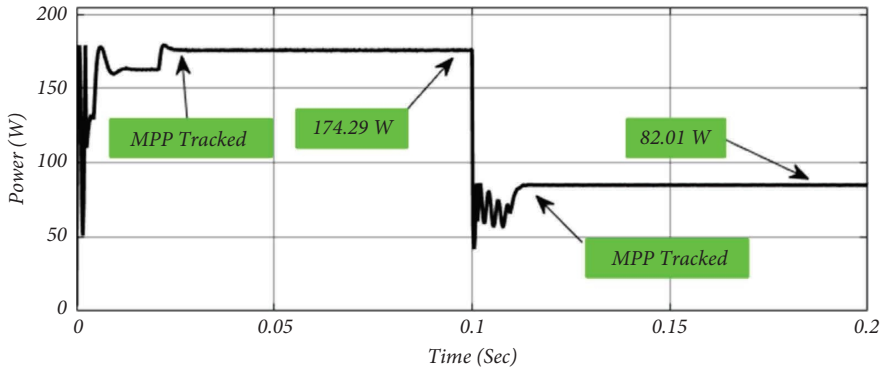


Figure 13: MPPT results.

Furthermore, the proposed converter is connected to a PV array, including three series 60 W PV panels that can produce 180 W in ideal irradiation ($G = 1000\ \mathrm{W/m^2}$). Also, between the PV array and the proposed converter, a low-pass filter (LC) is added to reduce the input current ripple. MPPT result is depicted in Figure 13. Using the P&O MPPT algorithm, the maximum power point of the PV array is tracked for two different irradiations. Before $t = 0.1$ sec, the irradiation of PV panels is $1000\ \mathrm{W/m^2}$, and the available MPP is 180 W. The tracked MPP using the proposed converter is obtained at 174.29 W. After $t = 0.1$ sec, the irradiation of PV panels became $500\ \mathrm{W/m^2}$, and the available MPP is 87 W. In this condition, the tracked MPP using the proposed converter is obtained at 82.01 W.

8. Conclusion

This article proposed a novel high step-up DC-DC converter based on the coupled inductor technique. The proposed structure advantages can be classified as (1) high voltage conversion ratio with high efficiency, (2) simple structure, (3) lower peak voltage across the semiconductor elements, and (4) less number of components. This converter employs a two-winding coupled inductor to enhance the output voltage. This topology has just one power switch with lower ON-state resistance, reducing the switch losses. Besides, the zero-voltage switching (ZVS) and zero-current switching (ZCS) of diodes are the other advantages of the proposed structure, which can increase the overall efficiency. The principle of the operation modes analysis of the steady-state and efficiency, design procedure, and comparison with other introduced similar structures are presented to verify the performance of the proposed topology. The match between the presented experimental results and analytical analysis verifies the performance and viability of the proposed converter and its applicability for various applications.

Appendix

In this section, Table 2 provides a list of the circuit components used in the prototype, while Table 3 presents the specifications of the experimental prototype for the topology discussed.

Data Availability

The data used to support the findings of this study are available from the corresponding author on request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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