Hindawi
International Transactions on Electrical Energy Systems
Volume 2023, Article ID 4057091, 17 pages
https://doi.org/10.1155/2023/4057091

Research Article

The Design of 2S2L-Based Buck-Boost Converter with a Wide Conversion Range

B. Nagi Reddy,[1] **B. Srikanth Goud**,[2] **Ch. Naga Sai Kalyan**,[3] **Praveen Kumar Balachandran**,[4] **Belqasem Aljafari**,[5] **and K. Sangeetha**[6]

[1]*Department of Electrical and Electronics Engineering, Vignana Bharathi Institute of Technology, Hyderabad, India*
[2]*Department of Electrical and Electronics Engineering, Anurag University, Hyderabad 500088, India*
[3]*Department of Electrical and Electronics Engineering, Vasireddy Venkatadri Institute of Technology, Guntur, India*
[4]*Department of Electrical and Electronics Engineering, Vardhaman College of Engineering, Hyderabad, India*
[5]*Department of Electrical Engineering, College of Engineering, Najran University, Najran 11001, Saudi Arabia*
[6]*Department of CSE, Kebri Dehar University, Kebri Dehar, Ethiopia*

Correspondence should be addressed to K. Sangeetha; sangeethak@kdu.edu.et

Received 20 August 2022; Revised 4 October 2022; Accepted 11 October 2022; Published 14 April 2023

Academic Editor: Bamidele Victor Ayodele

This manuscript proposes a novel nonisolated negative output buck-boost converter topology for wide voltage conversion applications. To design this converter, a typical buck-boost converter configuration is used. In conventional buck-boost converter, the active switches designed are replaced by two switches-two inductors (2S2L) cells. The proposed converter operates in the continuous conduction mode (CCM) operation under steady-state conditions. This converter has a lower component count and low voltage stress on the switches and diodes. Moreover, the major advantage of this buck-boost converter topology is that a wide range of step-down and step-up voltage conversions can be achieved. The performance of the proposed system is designed in MATLAB/SIMULINK. A few other comparisons are also presented to demonstrate the competitiveness of the proposed buck-boost converter.

1. Introduction

Negative output DC-DC converters are now available with a significant contribution within the industrial domain, such as regenerative braking systems (RBS), data transfer interfaces, signal generators, power electronics systems with neutral point clamping, and generation of solar power [1–4]. The buck-boost converter and the Cuk converter, two well-known negative output converters, have a similar conversion ratio. These two converters are designed to provide an output voltage that is either higher or lower than the input voltage.

At the duty cycle where D is close to 0 or 1, both converters can generate exceptionally good step-down or step-up DC output voltage, which cannot be observed in reality due to the limitations of active switches and diodes unless a transformer (such as a flyback converter) is used to acquire a wider conversion ratio. Unfortunately, using a transformer might result in switching voltage overshoot and EMI difficulties, lowering efficiency [5–7]. Transformer-less converters have been thoroughly researched over the years to achieve high efficiency. There are two types of transformer-less converters, namely, nonconnected inductor converters and coupled inductor converters. Many coupled inductor-based high step-up converters have been developed; similar to isolated converters, a high voltage gain can be achieved by increasing the coupled inductor's turns ratio, and voltage stresses can be reduced using a variety of voltage-clamp strategies, including active and passive circuits.

To achieve high voltage, the magnetic components of noncoupled inductor-type converters are reduced [7]. In recent decades, many negative output converters have been introduced, such as the voltage conversion ratio ($-D$)

indicated in [8] for the negative output KY buck converter, which has a quick dynamic response and smooth switching operation. Reference [9] presents a KY buck-boost topology with the inverted output and a voltage conversion ratio of ($-2D$) but no inverse features. The inverted load voltage-based KY boost converter was described in [10], and it was built by adding a capacitor with an extra diode to boost the converter which has a voltage gain of ($-1/(1-D)$).

The voltage lift methodology is used in the N/O self-lift Luo converter [1], the enhanced N/O self-lift Cuk converter [2], the N/O super-lift converter [11], and the voltage-lift-type Cuk converters [12]. However, all of the converters presented have an obvious error: a significant current spike running through the energy-transferring capacitor due to an abrupt change in voltage across it. Basic power loss and EMI are created by the current spike induced by this capacitor, which is essentially constrained by the dependent parameters [13].

There are a few atypical switched-capacitor converter topologies that use resonant operation rather than forced charging and discharging and are more efficient than standard switched-capacitor converters [14]. There have been several quadratic PWM converters with negative output switching proposed. They are a modified cascade of buck and buck-boost converters that just need a single switch and three diodes to work. Despite having different configurations, they have the same voltage conversion ratio ($-D^2/(1-\mathrm{D})$).

Conventional buck-boost converters have a reduced conversion ratio and a smaller step-down capacity [15]. In [16, 17], switched networks are used in the Cuk converter to make negative output hybrid Cuk converters as well as in the buck-boost converter to make hybrid buck-boost converters. A switched-capacitor (SC) structure is used in one inverted output hybrid buck-boost configuration, whereas a switched-inductor (SL) structure is used in another inverted output hybrid buck-boost configuration.

The addition of switched networks necessitates the use of extra diodes, capacitors, or inductors in the network design to increase the conversion rate, leading to even more sophisticated circuits, higher power losses, and lower efficiency. The voltage ratio ($-1/(1-\mathrm{D})$) for a single-stage switched-capacitor-inductor inverted output boost converter was published in [18]. However, to decrease the current spike caused by the power transferal capacitor, an auxiliary resonant inductor must be added, adding circuit convolution and reducing efficiency.

Power is supplied to today's integrated circuits (ICs) by a power supply that is less than 5 volts. To reduce the power loss of modern high-power consumption CPUs, future microprocessor supply voltages are expected to drop from 3.5 to 1 V, or even lower. As a result, power sources that can reduce the conventional 12 V (or 48 V) voltages to around 1 V are needed. Internet services require a 48 V DC battery that can be increased to a 380 V intermediate DC level, whereas high-intensity discharge lights (HID) used in vehicle headlamps require a voltage spike from the battery's 12 V to more than 100 V during start-up.

It was necessary to get such a high voltage-to-conversion ratio. Step-down converters would have to run at less than 0.1 duty cycle, while step-up converters would have to run at more than 0.9 duty cycle. The peak duty cycle of this magnitude lowers efficiency and impairs transient responsiveness [19]. A new negative output buck-boost converter topology is proposed in this paper. It modifies the buck-boost converter design somewhat and uses a high conversion ratio to generate a reversed output voltage. The power-transferring capacitor is used to store the power in this new converter, and there is no quick voltage shift on it.

The main contribution of the proposed work is as follows:

(i) For wide voltage conversion applications, a novel nonisolated negative output buck-boost converter topology is proposed.

(ii) In a conventional buck-boost converter, the active switch is replaced by two switches-two inductors (2S2L) cells.

(iii) The operation of this converter configuration's continuous conduction mode (CCM) under steady-state conditions is briefly discussed.

(iv) The proposed converter can produce wide voltage conversion ratio in both ways (step-down and step-up) with continuous input current. These are most promising and necessary features for any DC-DC converters used for renewable and EV applications. So for the applications such as PV and fuel cell inputs, the generated voltage is limited considering the size, hence the proposed converter can be most suitable.

The proposed converter is designed and simulated using MATLAB/Simulink. The structure of the paper is summarized as follows: In Section 2, the working principle and steady-state analysis of the planned converter are described, and in Section 3, simulation findings are presented to verify the preliminary theoretical study. Finally, in Section 4, some findings are offered.

2. Steady-State Analyses

We consider the circuit in Figure 1 for steady-state analysis. It is a new voltage negative output converter with a V_{DC} input voltage. Passive components include inductors L_A and L_B, capacitors C_A and C_B, and a resistive load R_L. Power switches S_A and S_B, as well as diodes D_A and D_B, govern the circuit's operation. The continuous conduction mode is used by this converter circuit (CCM). We assume that all of the circuit's components are in excellent condition.

2.1. Operating Principle. The circuit has two stages of operation. The power switches S_A S_B, which regulate the operation of a circuit, are turned on in the first step, as shown in Figure 2(a). Currents begin to flow via the inductors L_A L_B, which are represented by the characters i_{LA} and i_{LB} in the circuit. As illustrated in the diagram, V_{CA} this is the voltage across the capacitor C_A and V_{CB} is the output voltage. In the second stage, both the active switches S_A S_B are switched off,

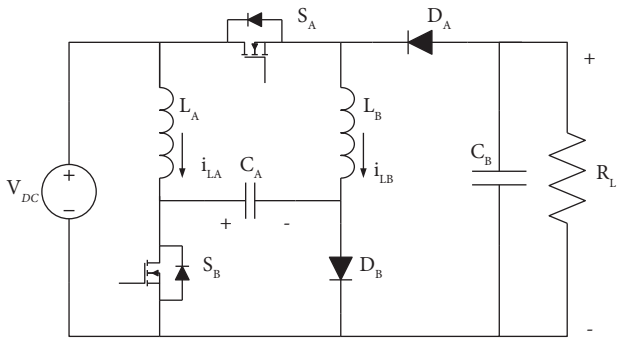

Figure 1: The suggested inverted output buck-boost configuration.

as presented in Figure 2(b). By turning on and off the active switches synchronously, the circuit is operated in two steps.

2.1.1. Mode 1. During stage 1 operation, active switches S_A S_B are switched on, as previously mentioned. The time interval during which these switches are turned on is (NT, NT + DT). Reverse voltage flows across diodes D_A and D_B since the active switches are in the ON state, which make them open switches. V_{DC}, the circuit's input voltage supply, delivers power to the inductor L_A and capacitor C_A. Diodes D_A D_B are subjected to voltage stresses. The voltage produced at the capacitor C_A is viewed by the diode-applied voltage. The input voltage V_{DC}, as well as the energy dissipated by a capacitor C_A, energy, is supplied to any of the other inductors L_B. The voltage stress across the diode D_B is described as the variation between the input voltage V_{DC} and the output voltage V_0.

$$\begin{aligned} L_A\frac{di_{L_A}}{dt} &= V_{DC},\\ L_B\frac{di_{L_B}}{dt} &= V_{DC} + V_{C_A},\\ C_A\left(\frac{dV_{C_A}}{dt}\right) &= -iL_B,\\ C_B\left(\frac{dV_B}{dt}\right) &= -\frac{V_B}{R_L}. \end{aligned} \tag{1}$$

2.1.2. Mode 2. As previously indicated, the power switches S_A S_B are switched off throughout the next time interval (NT + DT, NT + T) in the second stage. In this operation, the diodes D_A D_B come into the picture as closed switches. Power is delivered to the capacitor C_A via the diode D_A from the input voltage V_{DC} and inductor L_A. Because the diodes are conducting in this circumstance, the output capacitor C_B receives energy from the inductor L_B through these diodes. Voltage stresses develop across the power switches S_A S_B. The voltage stress S_A is equal to the voltage along the capacitor C_A. Just like in the first stage, the voltage stress induced across S_B is equal to the difference between the input voltage V_{DC} and the output voltage V_0.

$$\begin{aligned} L_A\left(\frac{di_{L_A}}{dt}\right) &= V_{DC} - V_{C_A},\\ L_B\left(\frac{di_{L_B}}{dt}\right) &= V_B,\\ C_A\left(\frac{dv_{C_A}}{dt}\right) &= i_{L_A},\\ C_B\left(\frac{dv_B}{dt}\right) &= -i_{L_B} - \frac{V_B}{R}. \end{aligned} \tag{2}$$

2.2. Voltage Conversion Ratio M (D). V_{DC}, V_{C_A}, by i_{L_A} by i_{L_B}, I_0, and V_0 are considered to be the DC values. Inductors L_A L_B fulfil the volt-second balance if the designed converter is in steady-state, with net volt-seconds within each period equal to zero. Thus,

$$\begin{aligned} DV_{DC} + (1-D)\left(V_{DC} - \mathrm{V_{C_A}}\right) &= 0,\\ D\left(V_{DC} + V_{C_A}\right) + (1-D)V_B &= 0. \end{aligned} \tag{3}$$

As a result, (3) can be used to calculate V_{CA} and V_0, with the following results:

$$V_{C_A} = \frac{1}{1-D}V_{DC}, \tag{4}$$

$$V_0 = \frac{\mathrm{D}\ (2-\mathrm{D})}{(1-\mathrm{D})^2}V_{DC}. \tag{5}$$

As a result, the proposed converter's voltage conversion ratio may be inferred from (5), and its expression is

$$\begin{aligned} M &= \frac{V_B}{V_{DC}}\\ &= -\frac{D(2-D)}{(1-D)^2}. \end{aligned} \tag{6}$$

The designed converter operates in step-down mode if the duty cycle is less than 0.29 and the voltage conversion ratio M is even less than 1. The rest of the time, it 'is in step-up mode.

2.3. Voltage Stresses of Switch and Diode. The diodes voltage stresses can be calculated using mode 1.

$$\begin{aligned} V_{D_A} &= \frac{V_{DC}}{1-\mathrm{D}},\\ V_{D_B} &= \frac{V_{DC}}{(1-D)^2}. \end{aligned} \tag{7}$$

The power switches' voltage stresses can be calculated using mode 2.

$$\begin{aligned} V_{S_A} &= \frac{V_{DC}}{1-\mathrm{D}},\\ V_{S_B} &= \frac{V_{DC}}{(1-D)^2}. \end{aligned} \tag{8}$$

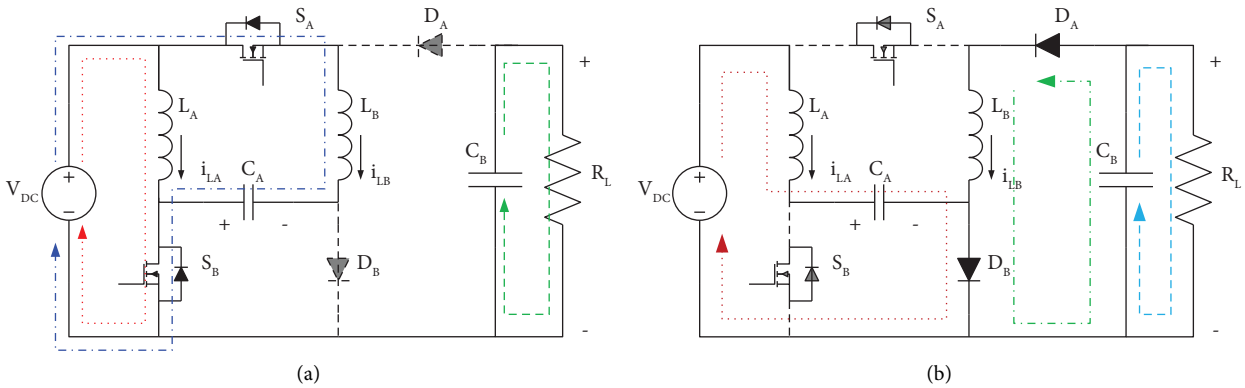

Figure 2: Steady state operating modes of the converter; (a) mode 1 and (b) mode 2.

2.4. Switch and Diode Current Stresses. C_A and C_B capacitors meet the charge balancing principle when the proposed converter reaches a steady state. As a result, the following i_{L_A} i_{L_B} expressions can be derived:

$$i_{L_A} = \left(\frac{\mathrm{D}}{(1-D)^2}\right) I_0,$$
$$i_{L_B} = \left(\frac{1}{1-\mathrm{D}}\right) I_0. \tag{9}$$

The current through the power switch S_A is, according to the operating principle,

$$i_{S_A}(t) = \begin{cases} i_{L_A}(t) + i_{L_B}(t), \\ 0, \end{cases} \tag{10}$$

As a result, the DC value i_{S_A} can be calculated as follows:

$$i_{S_A} = \left(\frac{\mathrm{D}}{(1-D)^2}\right) I_0. \tag{11}$$

Similarly, the current across the power switch S_B has a DC value of

$$i_{S_B} = \left(\frac{\mathrm{D}}{1-\mathrm{D}}\right) I_0. \tag{12}$$

The current that flows through the diode D_A is generated by operating modes, where

$$i_{D_A}(t) = \begin{cases} 0, \\ i_{L_A}(t) + i_{L_B}(t). \end{cases} \tag{13}$$

As a result, it may get the DC value of i_{D_B} by

$$i_{D_B} = \left(\frac{1}{1-\mathrm{D}}\right) I_0. \tag{14}$$

The DC value of the current passing through the diode D_B can be computed using the same approach

$$i_{D_B} = I_0. \tag{15}$$

2.5. Current and Voltage Variation Ratio. The inductor current i_{L_A} rises during the first subinterval and dips during the second subinterval, which has been shown in the traditional time-domain waveforms in Figure 3. As a result, the current ripple and current deviation from the peak value can be calculated as follows:

$$\Delta i_{L_A} = \frac{V_{DC} DT}{L_A}, \tag{16}$$

$$\delta_1 = \frac{\left(\Delta i_{L_A}/2\right)}{i_{L_A}} = \frac{(1-D)^2 \mathrm{T} R_L}{2|\mathrm{M}| L_A}. \tag{17}$$

Moreover, the current ripple from peak to peak and i_{L_B} deviation is determined as follows:

$$\Delta i_{L_B} = \frac{D(2-D) V_{DC} T}{(1-D) L_B}, \tag{18}$$

$$\delta_2 = \frac{\left(\Delta i_{L_B}/2\right)}{i_{L_B}} = \frac{(1-D)^2 \mathrm{T} R_L}{2 L_B}. \tag{19}$$

The following equations can be used to determine the maximum average voltage ripple and also the change in voltages V_{CA} and V_0

$$\Delta V_C = \left(\frac{D^2(2-\mathrm{D})}{(1-D)^3}\right)\left(\frac{V_{DC}\mathrm{T}}{R_L C_A}\right), \tag{20}$$

$$\varepsilon_{C_A} = \frac{\left(\Delta V_{C_A}/2\right)}{V_{C_A}} = \frac{D|M|T}{R_L C_A}, \tag{21}$$

$$\Delta V_B = \left(\frac{D^2(2-\mathrm{D})}{(1-D)^2}\right)\frac{V_{DC}\mathrm{T}}{R_L C_B}, \tag{22}$$

$$\varepsilon_{C_B} = \frac{(\Delta V_0/2)}{V_B} = \frac{DT}{2R_L C_B}. \tag{23}$$

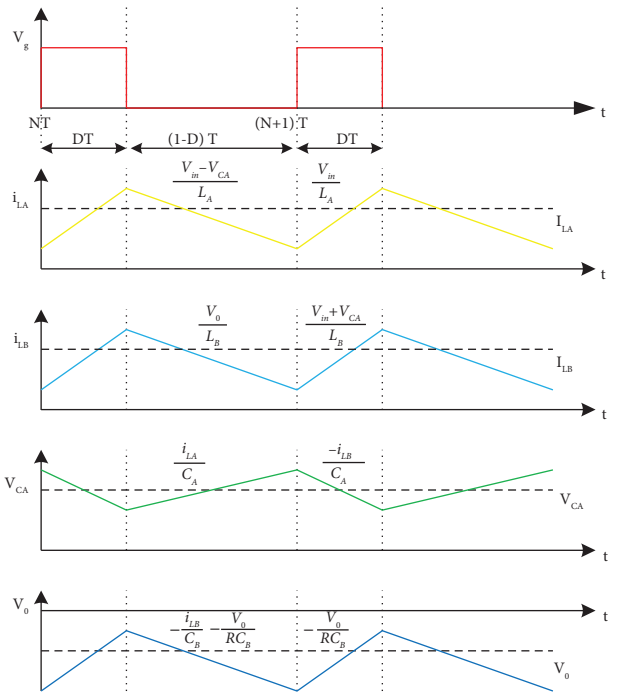

FIGURE 3: The proposed converter's time-domain waveforms under steady-state conditions.

2.6. Inductor and Capacitor Design. The equation is used to compute the ripple current of the inductors L_A, L_B. The inductor voltage V_L, ripple current (Δi_{L_A}) switching frequency (f_s), and duty cycle (D) are used to select the inductor. In mode 1, the incoming inductances L_A L_B contain voltages similar to V_{DC}. As a result, L_A L_B inductance values are determined by employing (24) and (25), respectively.

$$L_A = \frac{V_{DC}DT}{\Delta i_{L_A}}, \tag{24}$$

$$L_B = \frac{D(2-D)V_{DC}T}{(1-D)\Delta i_{L_B}L_B}. \tag{25}$$

For $D = 0.673$, $V_{DC} = 12\,\text{V}$, $f_s = 40\,\text{kHz}$, $\Delta i_{L_A} = 0.5\,\text{A}$, and $\Delta i_{L_B} = 0.8\text{A}$. The value of L_A and L_B is given by $L_A = 403.8\,\mu\text{H}$ and $L_B = 1024.16\,\mu\text{H}$, respectively.

The capacitor charge variance can be used to determine the value of the capacitors C_A and C_B both of which contain voltage ripple. As a result, C_A and C_B can be determined by using relation (26) and (27).

$$C_A = \left(\frac{D^2(2-D)}{(1-D)^3}\right)\left(\frac{V_{DC}T}{R_L\Delta V_{CA}}\right), \tag{26}$$

$$C_B = \left(\frac{D^2(2-D)}{(1-D)^2}\right)\left(\frac{V_{DC}T}{R_L\Delta V_{CB}}\right). \tag{27}$$

For $D = 0.673$, $I_0 = 0.5\,\text{A}$, $f_s = 40\,\text{kHz}$, $\Delta V_{CA} = 2\text{V}$, and $\Delta V_{CB} = 1\,V$. The value of C_A and C_B is given by $C_A = 12.9\,\mu\text{F}$ and $C_B = 8.45\,\mu\text{F}$

2.7. Comparisons with Various Negative Output Topologies. The proposed converter topology is compared to several different switched-inductor converters, including the N/O hybrid buck-boost configuration, N/O self-lift Luo configuration, and basic buck-boost converter. The change of voltage conversion ratios of these converters concerning the duty cycle is depicted graphically in Figure 4. As indicated in Table 1, none of these converters uses inductors, capacitors, diodes, or switches. The abrupt voltage shifts in these converters are also depicted. The converter is meant to have a larger voltage conversion ratio than other N/O converters, such as the topology of the self-lift Luo converter, which can only give higher output voltage. For the step-down voltage conversion ratio, a N/O buck-boost converter is evaluated to the proposed converter. Because it does not have any abrupt voltage changes and has an additional power switch. The proposed converter is chosen over the hybrid buck-boost converter since it has no abrupt voltage changes and has an additional power switch. The presence of abruptly changing voltage in the self-lift Luo converter causes a change in current, causing the capacitor to be shut off. In addition, the number of diodes employed in these N/O converters varies from the specified converter.

From Figure 4(a), we can conclude that the converter which is designed has the maximum value of ideal step-up voltage conversion ratio, i.e., about 45 at duty cycle $D = 0.8$ compared with the other N/O converters, which have a much lesser value of this ratio.

From Figures 4(b) and 4(c), we can conclude that the converter which is designed has the less switch and diode voltage stresses compared with the other N/O converters, which have higher voltage stresses on the switches and diodes.

3. Simulated Results

Initially, a DC-DC converter is simulated in the step-up mode of operation using PSIM simulation to validate the theoretical review. The components used, such as inductors and capacitors, are arranged in detail using (17) and (19), and their properties are listed in Table 2. Because the inductor resists current changes and the capacitor resists voltage changes, the current tolerance value for the inductor is set to 0.5, the voltage across capacitor C is set to 2%, and the voltage across capacitor Co is set to 1%. Time-domain waveforms of step-up and step-down modes are obtained after the simulations. All the simulation waveforms from Figure 5 are in the step-up mode only. The proposed DC-DC converter is considered to be operating in the continuous conduction mode (CCM).

In the MATLAB/Simulink environment, a 2S-2L-based buck-boost converter (see Figure 1) is designed. For the steady-state analysis., the inductors L_A L_B in the proposed converter are assumed to be working in CCM. The values of the inductors and capacitors are calculated using the theoretical analysis described in section II and the equations (16), (18), (20), and (22) stated in Table 2. The inductors $L_A(\Delta i_{L_A})$ and $L_B(\Delta i_{L_B})$ current ripples are 0.5 and 0.8 amps, respectively. Similarly, the capacitors $C_A(\Delta V_{C_A})$ $C_B(\Delta V_{C_B})$ have voltage ripples of 2 V and 1 V, respectively.

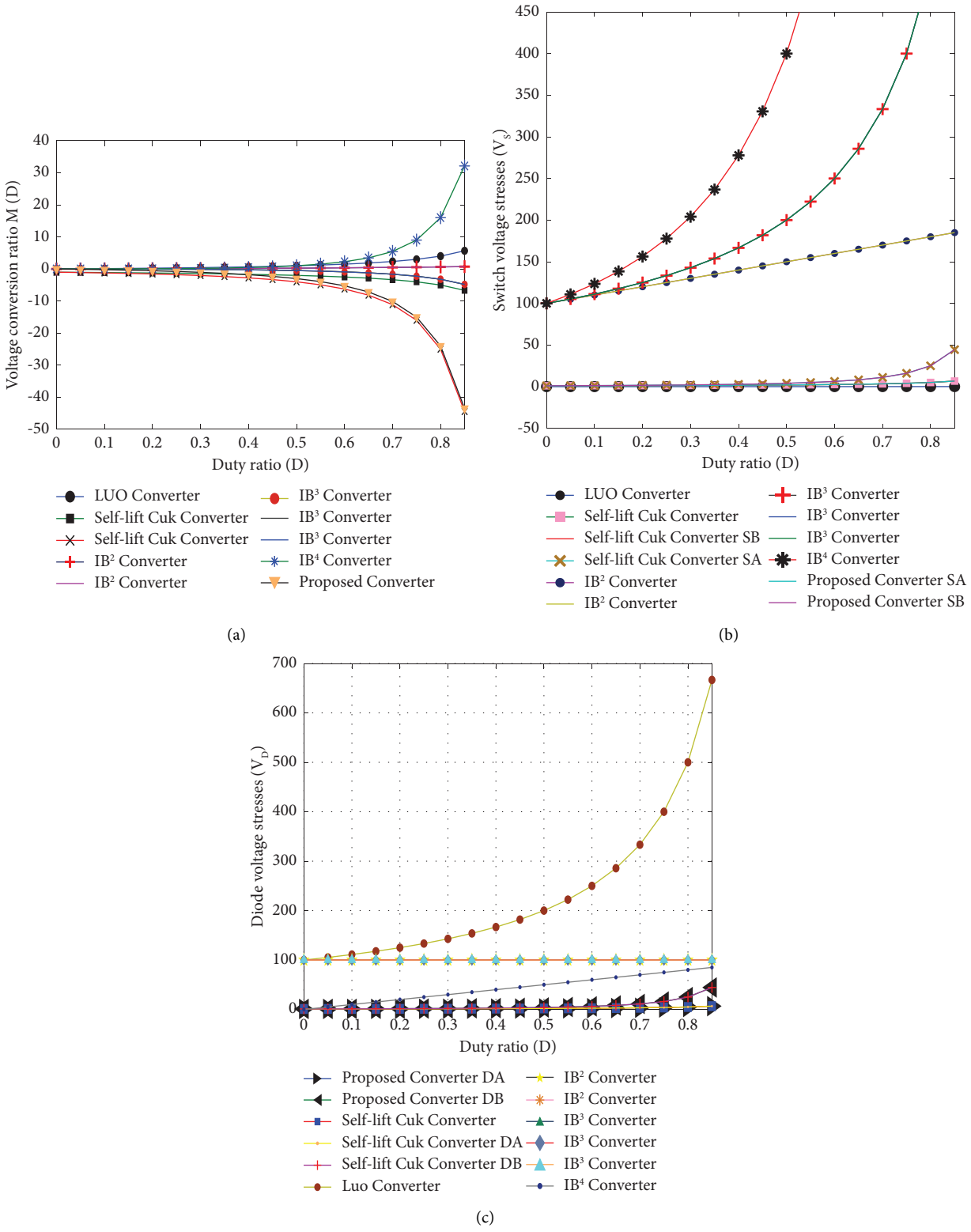

Figure 4: (a) D and $M(D)$: voltage conversion ratio $M(D)$ values for various duty ratio (D). (b) D and $V(D)$: switch voltage stresses for various duty ratios. (c) D and $V(D)$: diode voltage stresses for various duty ratios.

Table 1: Comparisons with Various Negative Output Topologies.

References	Parameters				
	No. of switches	No. of diodes	No. of inductors	No. of capacitors	$M(D)$
[4]	1	1	2	2	$D/1-D$
Converter–1 [12]	1	2	2	3	$-1/1-D$
Converter–2 [12]	2	3	3	3	$-1/(1-D)^2$
Converter–1 [15]	1	3	2	2	D^2
Converter–2 [15]	1	3	2	2	D^2
Converter–3 [15]	1	3	2	2	$-D^2/1-D$
Converter–4 [15]	1	3	2	2	$-D^2/1-D$
[16]	1	3	2	2	$-\mathrm{D}^2/1-D$
[18]	1	3	2	2	$D^2/(1-D)^2$
Proposed converter	2	2	2	2	$-D(2-D)/(1-D)^2$

Table 2: Parameters of main components.

Components	Step-up mode
Input voltage V_{in}	12 V
Output voltage V_{out}	100 V
Switching frequency f	40 kHz
Output load R	200 ohms
Duty cycle D	0.673
Inductor $L_A = V_{\mathrm{in}}\mathrm{DT}/\Delta i_{L_A}$	403.8 μH
Inductor $L_B = D(2-D)V_{\mathrm{in}}T/(1-D)\Delta i_{L_B}$	1024.16 μH
Capacitor $C_A = D^2(2-D)V_{\mathrm{in}}T/(1-D)^3R\,\Delta V_{C_A}$	12.89 μF
Capacitor $C_B = D^2(2-D)V_{\mathrm{in}}T/(1-D)^2R\Delta V_{C_B}$	8.43 μF
Δi_{L_A}	0.5 A
Δi_{L_B}	0.8 A
ΔV_{C_A}	2 V
ΔV_{C_B}	1 V
$\mathrm{M}(D) = -\mathrm{D}(2-D)/(1-D)^2$	8.33

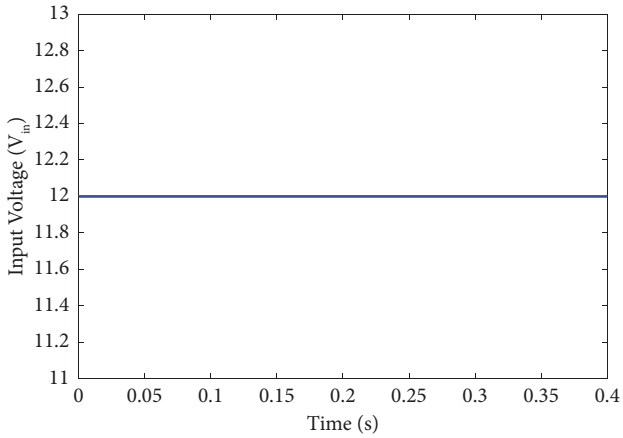

Figure 5: MATLAB simulated input voltage 12 V (V_{in}) waveform of the proposed configuration.

Figure 5 depicts a simulated waveform of input voltage (12 V) obtained from a DC voltage source. The simulated input current waveforms for the few switching cycles are displayed in Figure 6. The simulated waveform of the input current does not hit the zero level, as discussed in the theoretical analysis. As a result, the proposed converter

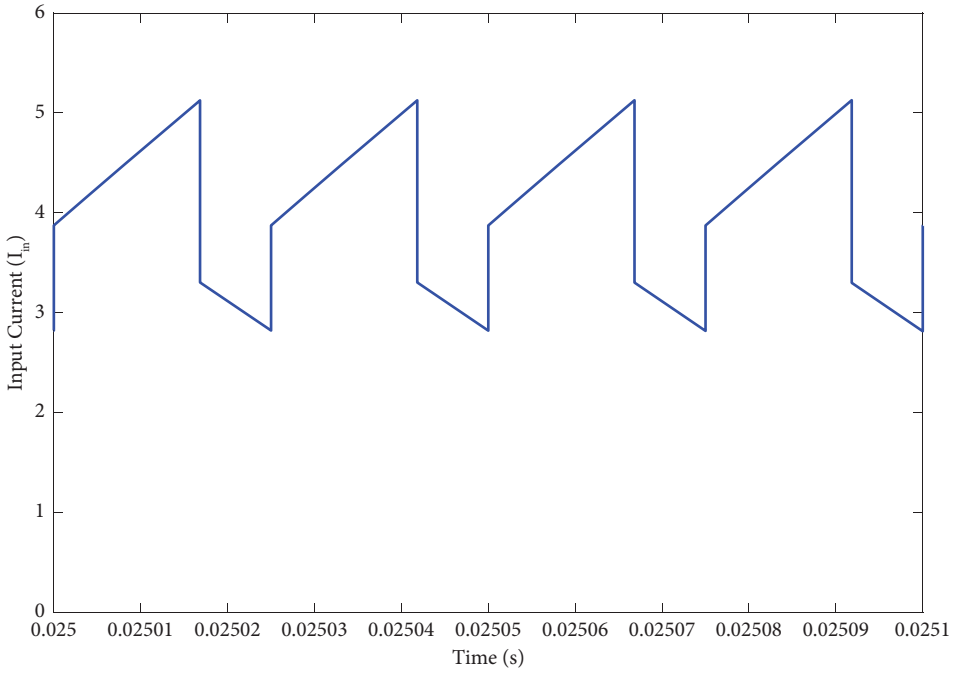

FIGURE 6: Simulation waveform of input current (I_{in}) showing the continuous operation.

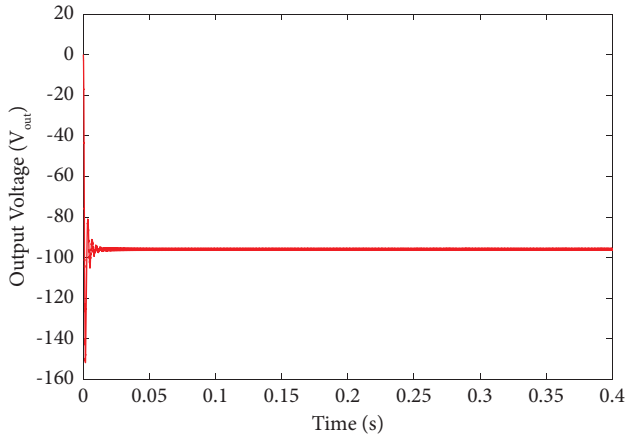

FIGURE 7: The simulation result of output voltage with a ripple of 0.94%.

generates a continuous input current, which is important in renewable energy systems.

Figure 7 depicts the simulated output DC voltage waveform. In the theoretical study, the output voltage is considered to be 100 V, while the simulation result shows an average of 95.95 V. The ripple in the output voltage is approximately 0.94%, which is well within the universal limitations (2%). The magnified version of the DC output current with a small ripple is shown in Figure 8. For a 100 V output voltage, the output load current is 0.5 A, according to theoretical calculations. The average value of the simulated waveform is 0.48 A.

The simulated waveforms of active switching elements are shown in Figures 9–12. Figures 9 and 10 illustrate the voltage and current waveforms of the active switch S_A. The waveforms of the voltages and currents of the active switch S_B are shown in Figures 11 and 12.

The simulated waveforms of passive switching elements are shown in Figures 13–16 (diodes). The voltage and current waveforms of the diode D_A are shown in Figures 13 and 14,

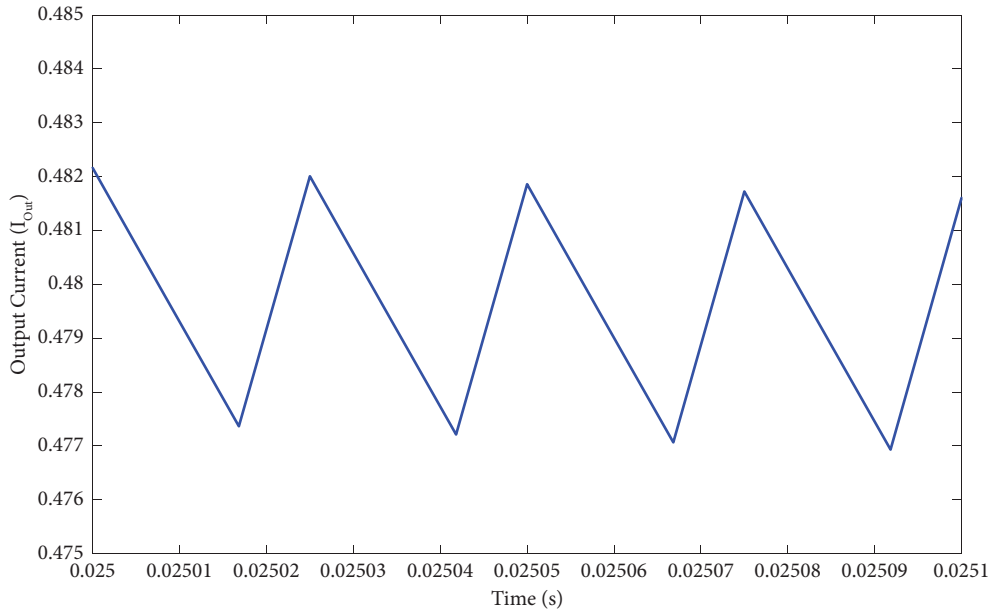

Figure 8: The simulation result of output current with an average value of 0.48 A.

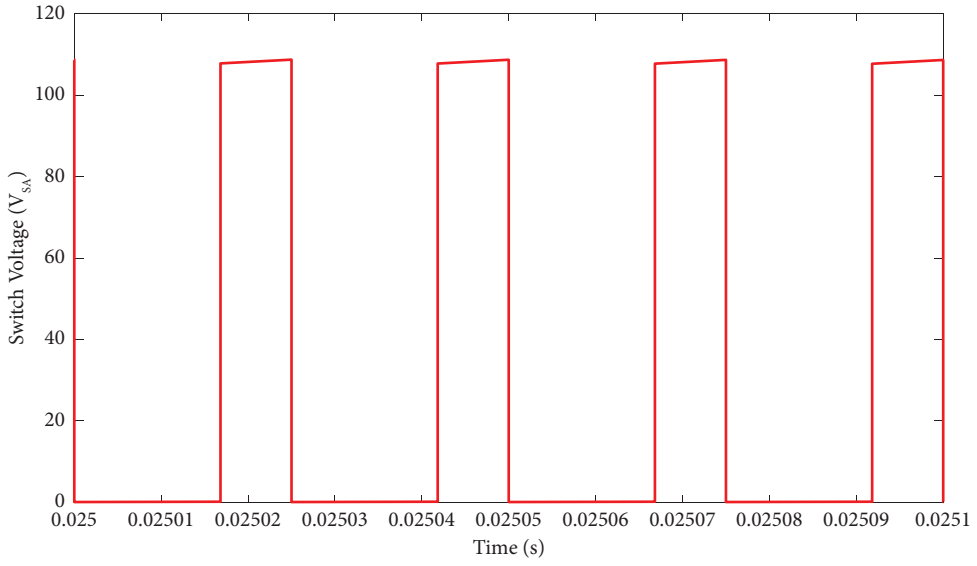

Figure 9: The switch S_A simulated voltage waveform.

whereas the voltage and current waveforms of the diode D_B are shown in Figures 15 and 16.

Both inductors' working modes are set to CCM with a permissible ripple, as indicated in the theoretical analysis. Equations (24) and (25) are used to compute the inductor L_A and L_B values for ripple currents of 0.5 and 0.8 amps. The computed current waveforms of inductors L_A L_B are shown in Figures 17 and 18. The ripple currents (Δi_{L_A}) (Δi_{L_B}) are the same as the theoretical values, as seen in these figures.

Using formulas (26) and (27), the capacitors are designed with a ripple voltage of 2 V and 1 V, respectively. Figures 19 and 20 illustrate the simulated voltage waveforms

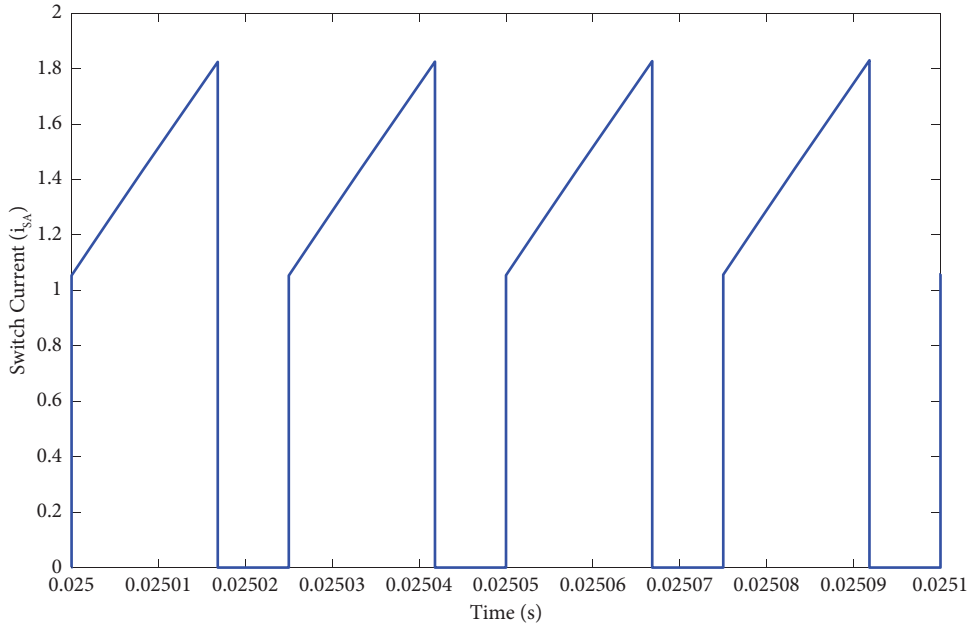

FIGURE 10: The switch S_A simulated current waveform.

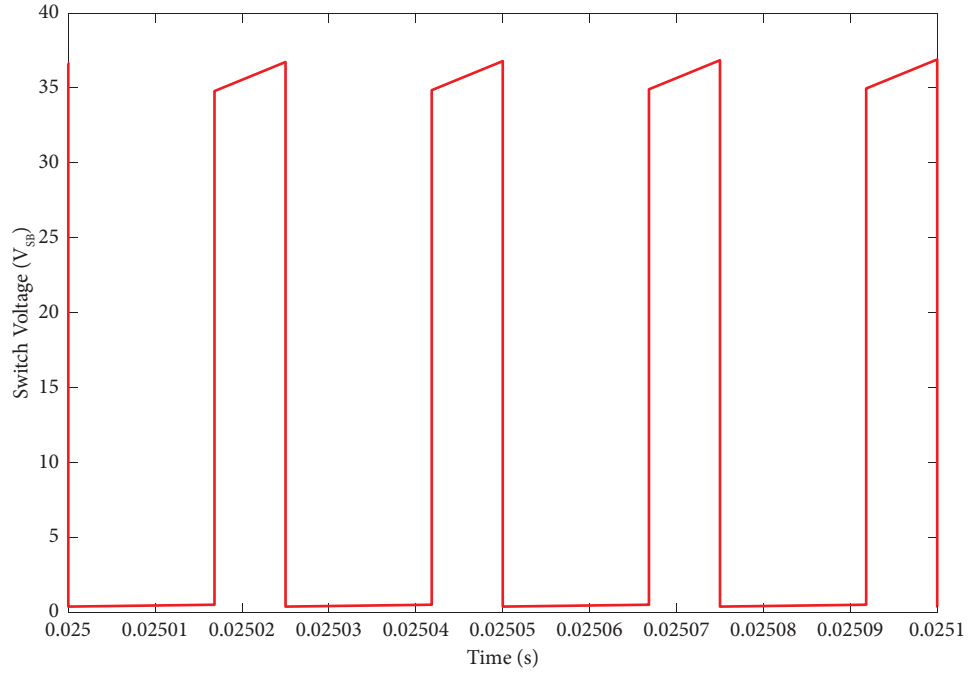

FIGURE 11: The switch S_B simulated voltage waveform.

of capacitors C_A C_B. The ripple voltages (ΔV_{CA}) and (ΔV_{CB}) are the same as the theoretical values, as shown in these figures.

Table 3 shows the performance of the proposed 2S2L-based buck-boost converter for various duty ratios. For duty ratios of 0.2 to 0.7, the proposed converter has an efficiency better than 90%, with high efficiency of 96.67% for duty ratios of 0.55 or 55%. With an efficiency of over 84%, the proposed converter has also demonstrated better performance at very low duty ratios. It is also worth noting that the

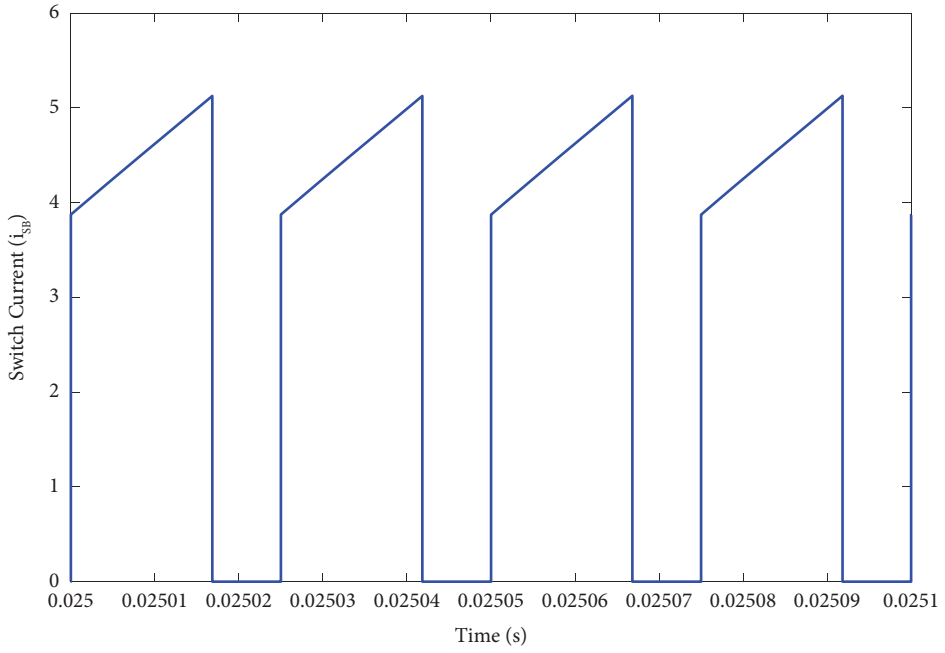

Figure 12: The switch S_B simulated current waveform.

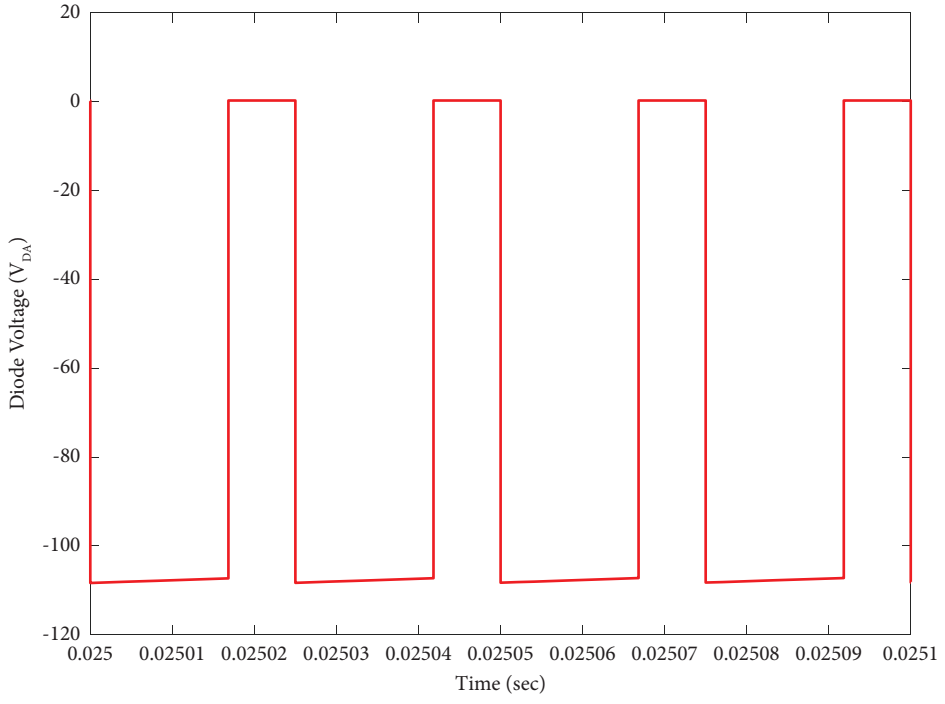

Figure 13: The diode D_A simulated voltage waveform.

proposed converter's ripple percentage is less than 2%, which is highly acceptable (universal acceptable range). The simulated values of the switching voltage stresses are displayed in Table 4 (both active and passive). Table 4 displays that the voltage stresses on the active switch S_A and the diode D_A are closer to the converter's output voltage.

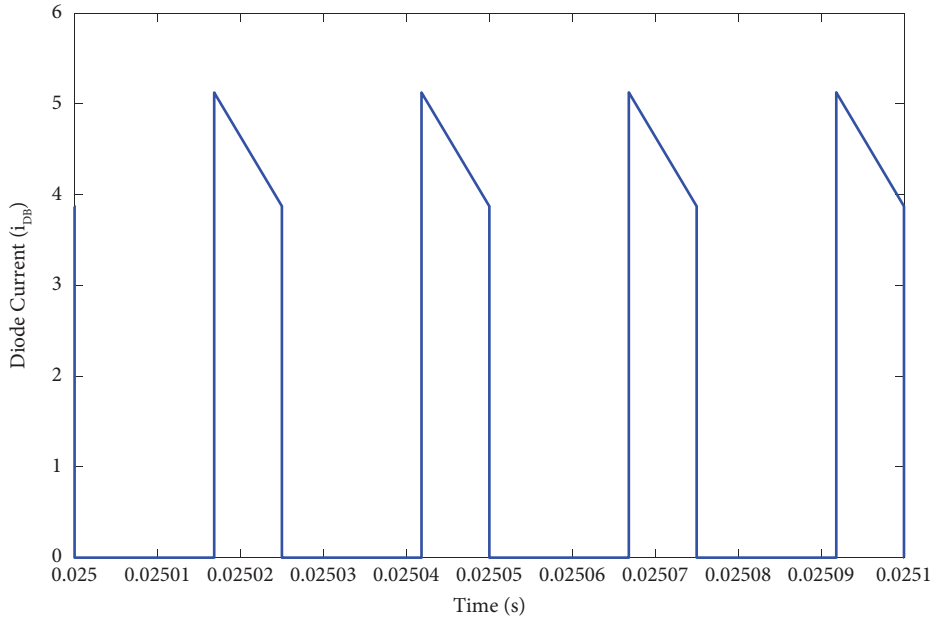

Figure 14: The diode D_A simulated current waveform.

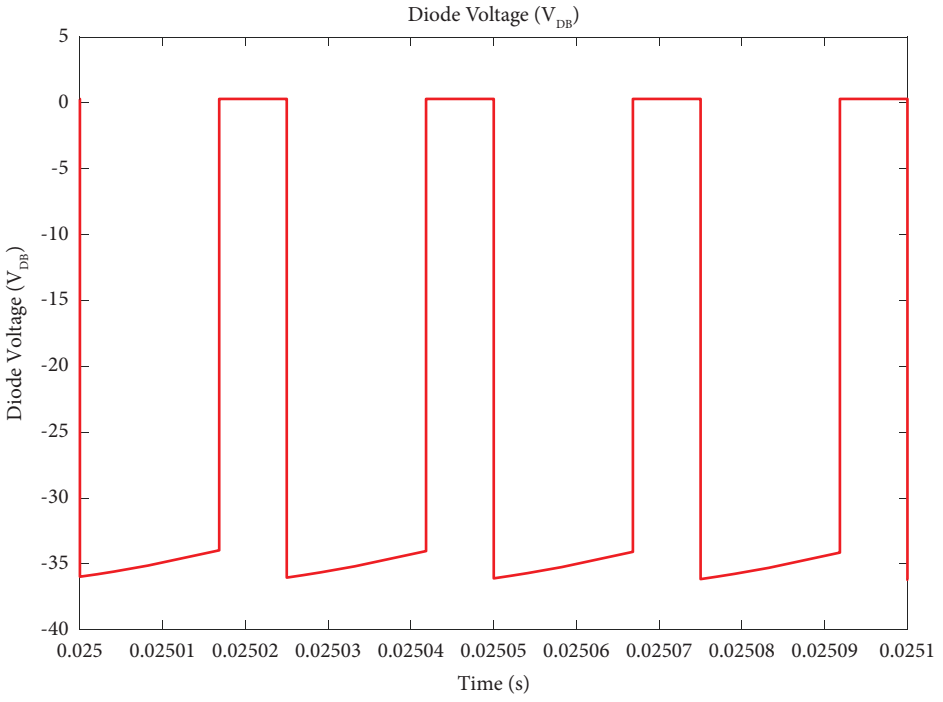

Figure 15: The diode D_B simulated voltage waveform.

When compared to the converter output, the voltage strains on the active switch S_B and the diode D_B are also quite low.

Figure 21 shows the performance curve of simulated output voltage (V_{out}) for different duty ratios (D). Figure 22 demonstrates the designed converter's efficiency curve in terms of duty ratio (D), and Figure 23 represents the plot of output ripple voltage (%) for various duty ratios (D).

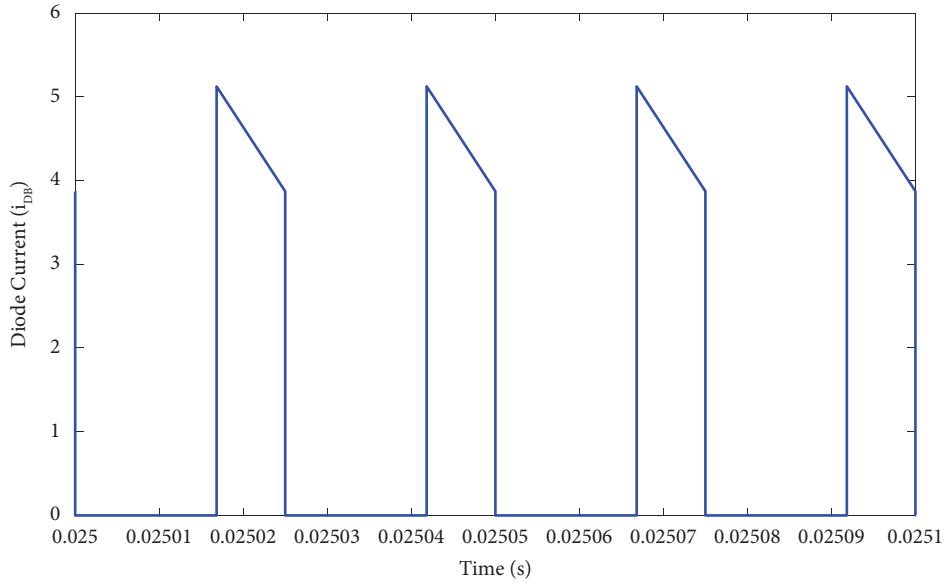

FIGURE 16: The diode D_B simulated current waveform.

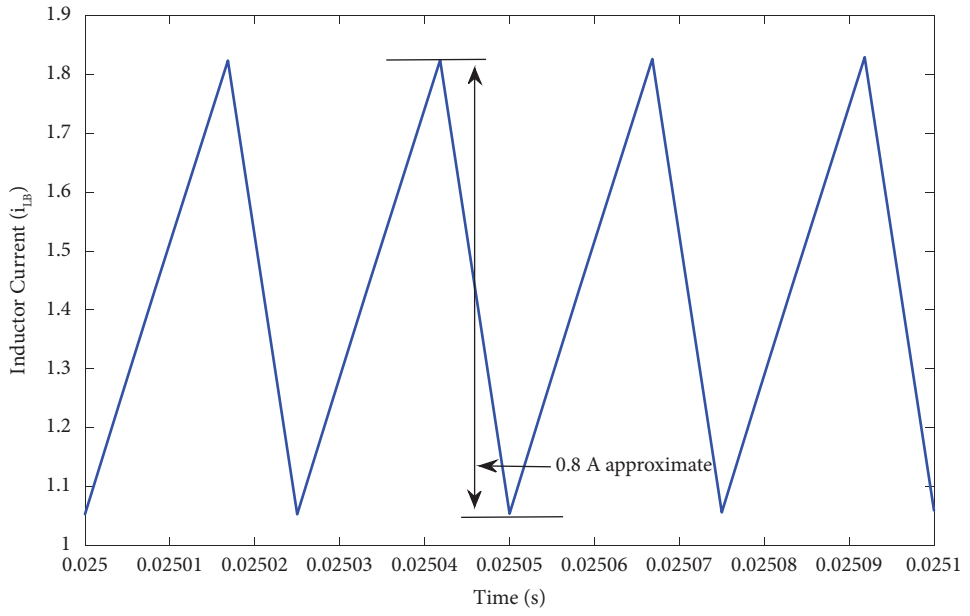

FIGURE 17: The inductor L_A simulated current waveform.

In Table 5, the proposed 2S2L circuit performance is presented for the designed duty ratio under light load conditions (below 50%). The load current as well as the output power of the configuration is varied as the load is changing. For a very light load (10%), the 2S2L converter performance is not up to the mark as it is designed for a full load (100%). However, as the load increases, the performance of the converter improves, which is recorded in Table 5. Figure 24 shows the performance of the 2S2L converter under light load conditions.

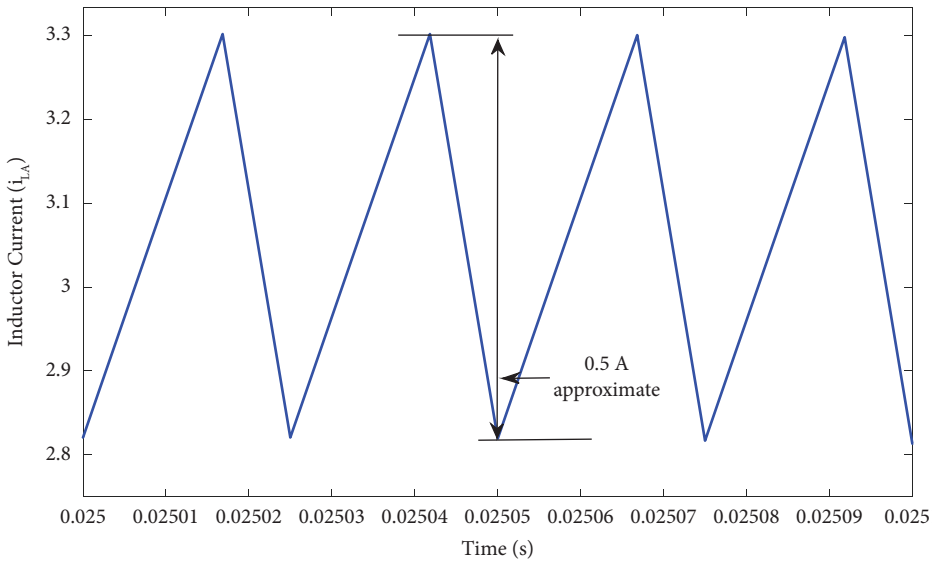

Figure 18: The inductor L_B simulated current waveform.

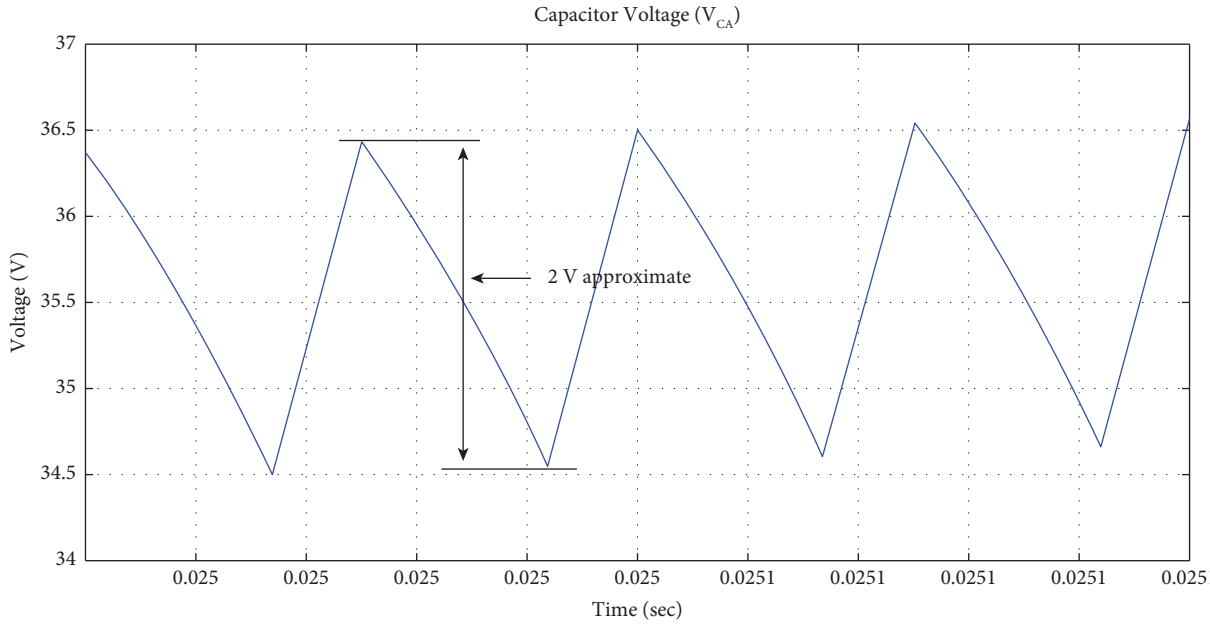

Figure 19: The capacitor C_A simulated voltage waveform.

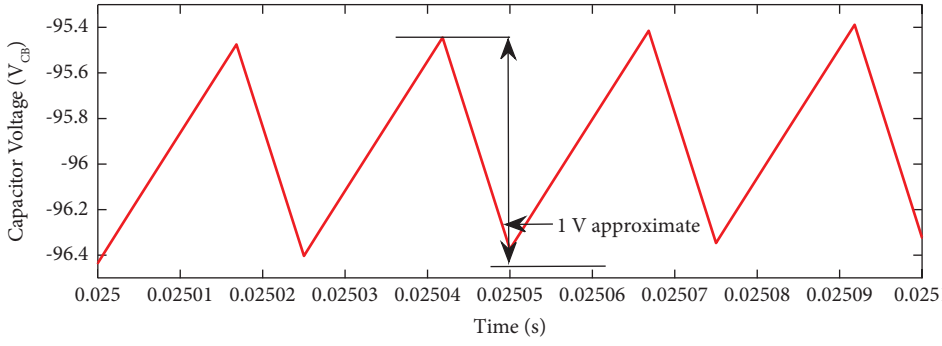

Figure 20: Simulated voltage waveform of capacitor C_B.

Table 3: Performance analysis for various duty ratios.

S.no	Duty ratio (D)	Output voltage (V_0)	% ripple	P_{in} (Watts)	P_0 (Watts)	% efficiency
1	0.1	4.761	0.5250	0.1341	0.1133	84.48
2	0.15	7.401	0.5404	0.3058	0.2738	89.53
3	0.2	10.09	0.4955	0.5544	0.5090	91.81
4	0.25	12.82	0.5460	0.8796	0.8217	93.41
5	0.3	15.56	0.5784	1.2852	1.2105	94.18
6	0.35	18.32	0.5458	1.7688	1.6781	94.87
7	0.4	21.06	0.6172	2.3268	2.2176	95.30
8	0.45	26.72	0.6736	3.7176	3.5697	96.02
9	0.5	34.91	0.5729	6.3168	6.0935	96.46
10	0.55	45.92	0.7621	10.9056	10.5432	96.67
11	0.6	61.14	0.8177	19.344	18.6904	96.62
12	0.65	82.84	0.8450	35.736	34.3123	96.01
13	0.673	95.95	0.9379	48.252	46.0272	95.38
14	0.7	114.7	0.8718	69.84	65.7804	94.18
15	0.75	162.1	0.9870	146.4	131.3820	89.74
16	0.8	227.3	1.0998	328.44	258.3264	78.65

Table 4: Active and passive switching voltage stresses.

S.no	Duty ratio (D)	Output voltage (V_0)	V_{S_A} Simulated	V_{S_B} Simulated	V_{D_A} Simulated	V_{D_B} Simulated
1	0.1	4.761	17.07	15.66	−16.75	−15.35
2	0.15	7.401	19.71	17.06	−19.39	−16.74
3	0.2	10.09	22.41	18.23	−22.08	−17.91
4	0.25	12.82	23.14	19.16	−24.81	−18.85
5	0.3	15.56	27.89	19.84	−27.57	−19.53
6	0.35	18.32	30.66	20.25	−30.33	−19.94
7	0.4	21.06	33.43	20.38	−33.10	−20.08
8	0.45	26.72	39.10	21.86	−38.78	−21.55
9	0.5	34.91	47.34	24.08	−47.02	−23.75
10	0.55	45.92	58.41	26.78	−58.08	−26.41
11	0.6	61.14	73.7	30.14	−73.36	−29.07
12	0.65	82.84	95.5	34.4	−95	−33.8
13	0.673	95.95	108.7	36.72	−108.32	−36.02
14	0.7	114.7	127.6	40	−127.15	−39
15	0.75	162.1	175	46.45	−175	−44.91
16	0.8	227.3	240.9	53	−240	−50

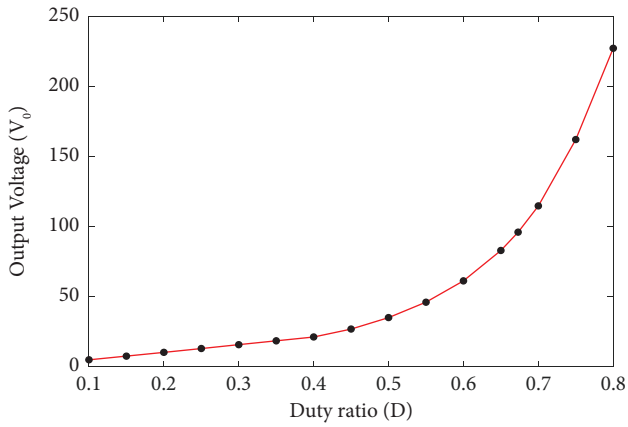

Figure 21: Performance curve of simulated output voltage (V_{out}) versus duty ratio (D).

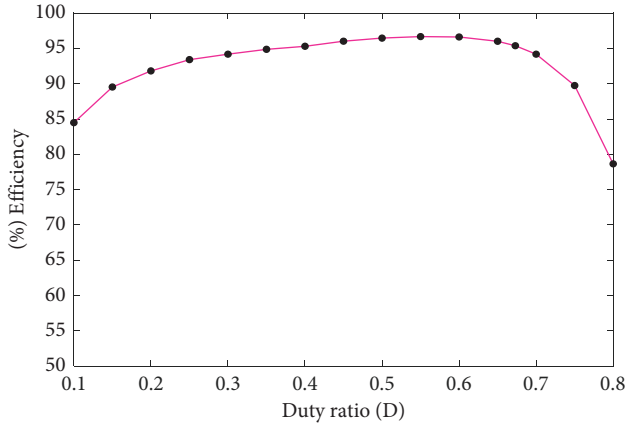

Figure 22: The designed converter's efficiency curve in terms of duty ratio (D).

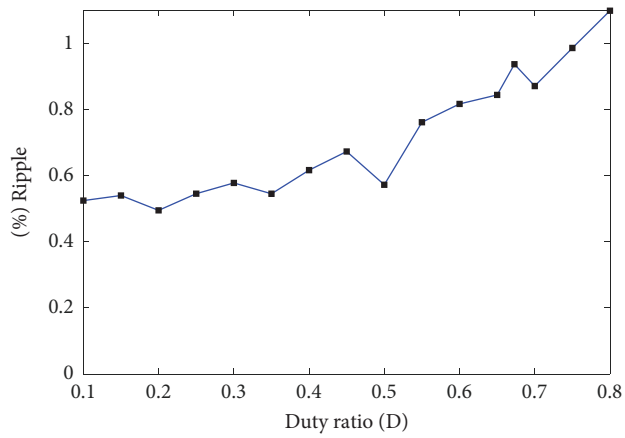

Figure 23: Plot of output ripple voltage (%) for various duty ratios (D).

Table 5: Performance of the converter under light load conditions.

S. no.	Load (%)	Output voltage (V)	Output current (A)	Output power (W)	Efficiency (%)
1	10	82.5	4.12	340	68
2	30	105.3	1.75	185	86
3	50	117.8	1.18	139	90
4	100	95.95	0.48	46	95.4

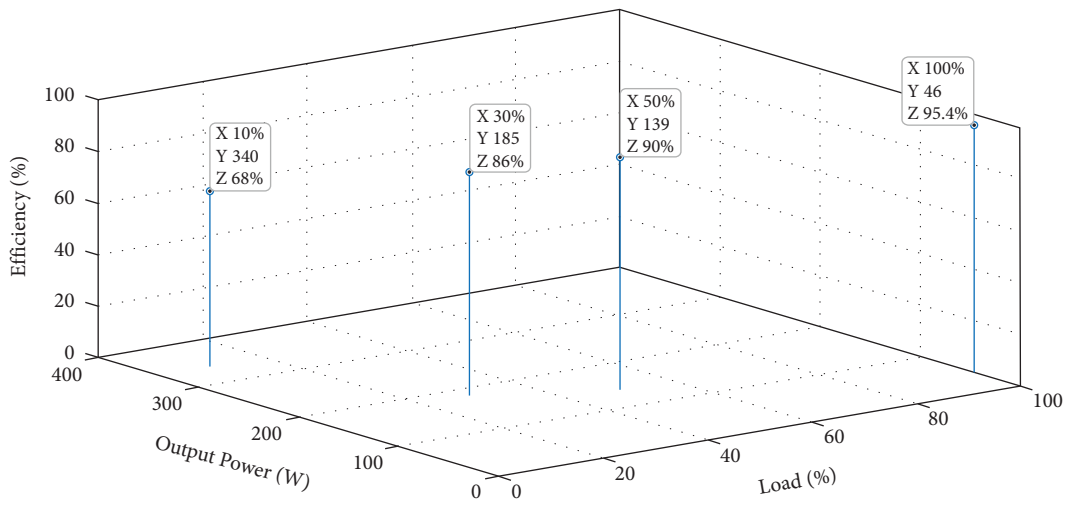

Figure 24: Performance of the proposed converter under light load conditions.

4. Conclusions

This proposed converter includes deep step-down and step-up voltages, as well as a percentage ripple of less than 2%, which is acceptable because it lowers the capacitor filter's output value. It can be observed that the proposed converter has an efficiency greater than 90% for duty ratios ranging from 0.2 to 0.7, with the highest efficiency of 96.67% at 55% or a 0.55 duty ratio. At duty ratios less than 0.2 or 20%, several other conventional converters have an efficiency less than 70%. The proposed converter, on the other hand, has an efficiency of 84% at such low duty ratios. The diode and switching stresses in the proposed converter are both low, which decreases losses. The proposed converter has several advantages, including being simple to modify by adding only four components to a traditional buck-boost converter, having a constant input current, a high voltage conversion ratio, and a simple control system. To achieve the step-up or step-down voltage, no transformers or coupled inductors are used. Furthermore, the proposed converter is low-cost and lightweight, and it can handle a wide range of duty ratios. Furthermore, the suggested converter has a lower rate of voltage stress on the switches as compared to the output voltage. According to the results, the designed converter has

a higher output voltage than the other topologies. The proposed converter is used in energy renewable systems, regenerative braking systems, and other industrial applications.

Data Availability

No data were used to support the findings of this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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