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Research Article

A Switched-Capacitor-Based 7-Level Self-Balancing High-Gain Inverter Employing a Single DC Source

Yatindra Gopal,[1] **Kaibalya Prasad Panda**,[2] **Akanksha Kumari**,[3] **and Julio C. Rosas-Caro**[4]

[1]*Department of Electrical and Electronics Engineering, Sri Venkateswara College of Engineering and Technology, Chittoor, Andhra Pradesh 517127, India*
[2]*Department of Electrical Engineering, School of Technology, Pandit Deendayal Energy University (PDEU), Raisan PDPU Rd, Gandhinagar, Gujarat 382007, India*
[3]*Department of Electronics and Communication Engineering, Sreenivasa Institute of Technology and Management Studies, Chittoor, Andhra Pradesh, India*
[4]*Facultad de Ingenieria, Universidad Panamericana, Alvaro del Portillo 49, Zapopan 45010, Mexico*

Correspondence should be addressed to Yatindra Gopal; ygopal.phd@rtu.ac.in and Julio C. Rosas-Caro; crosas@up.edu.mx

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This paper discloses a novel switched capacitor (SC)-based 7-level inverter with a single DC source. The proposed inverter has the ability to self-balancing the voltage of the capacitor without using a closed-loop voltage balancing circuit. Two capacitors are equally charged by the input source owing to the series-parallel charging and discharging continuously in a full cycle. The proposed 7-level SC inverter requires less number of switches, driver diodes, and capacitors and a lower number of semiconductor switches than most recently developed topologies. Furthermore, four out of the eight switches operate at the fundamental frequency, which simplifies the control scheme. A fundamental frequency switching scheme is used to control the output of the inverter. The self-balancing and voltage-boosting features of the proposed structure are validated on MATLAB/software platform and verified experimentally.

1. Introduction

Now a days, switched capacitor-based multilevel inverters (SC MLI) play an important role in the conversion of DC-AC power due to their excellent performance [1]. The configuration of SC MLI augments with renewable energy (RE) and electric vehicles with better performance [1, 2]. For the generation of staircase waveform of output voltage with less distortion multilevel inverters (MLI), the structure is more appropriate for enhancing the power quality. Numerous types of MLIs are designed by the researchers in which three classical configurations of MLIs are diode clamped MLIs (DC MLIs), flying capacitor MLIs (FC MLIs), and cascaded H-bridge inverters (CHB MLIs). These conventional MLIs have various advantages over the 2-level inverters. On the other hand, 3-level MLIs suffer from related as well as different limitations. These conventional MLIs use full for different industrial work for producing specific voltage output up to five levels. When producing a higher-level voltage waveform, they require a large number of devices. DC MLIs require a large number of diodes and DC link capacitors, FC MLIs require more capacitors, and CHB MLIs require more number of DC power supply. Hence, few demerits present in conventional MLIs like more DC sources and switches are required with an increase in the volume, size, and cost of inverters [3]. In the current year, various researchers focused on topological development in MLIs configuration to solve the unbalance problem of capacitor voltage. Numerous reduced device count structures of MLIs have been proposed in recent years [4, 5]. However,

these configurations do not have the ability to self-boosting due to complex support algorithms and thus circuits as in [5] have been proposed to mitigate the unbalance problem in capacitor voltage. With the advantage of the switched-capacitor MLI (SC MLI)-based approach, a 7-level topology is also presented in [6]. At the same time, the number of switches is reduced in [7] by only using ten switches for producing 7-level voltage output. Later on, several SC MLIs have been disclosed in the literature. Some of them have requirement of a higher switch count, more number of capacitors, more voltage stress, or low voltage gain. This has motivated the development of a new compact module structure.

In this paper, a novel 7-level SC MLI is designed using only 8 switches and a single DC source. This configuration can generate a 3-time boosted staircase output by the use of only one DC source. Various switching techniques are evolved recently for the control of MLIs [8, 9]. Different techniques such as the sinusoidal switching pulse technique with multitriangular carriers in [9], multivector space technique in [9, 10], and selective harmonic elimination pulse-width modulation (SHE PWM) in [10] are widely used. In overall, the SHE PWM control technique is superior, low switching frequency-based, and easy to control and eliminates the harmonics from output voltage [10]. In this paper, the SHE PWM control technique is used to control the switching angles of the inverter and to obtain the output voltage. The proposed inverter is suitable for renewable and sustainable energy applications, where the low-input-side DC voltages require stepping-up. The operation of the proposed topology is tested by MATLAB/software simulation and verified experimentally.

2. Principle of Proposed 7-L SC MLI

The proposed 7-L SC MLI topology consists of 8 switches S_1 to S_8, 3 diodes D_1, D_2, and D_3, and two capacitors C_1 and C_2. The input voltage source V_{in} is used as the input of the inverter and *Vo* is the output voltage. Figure 1 represents the 1-phase 7-L switched-capacitor-based multilevel inverter (7-L SC MLI) with a single DC source.

2.1. Operation of 7-L SC MLI. Two capacitors and 8 switches are employed to produce 7-L staircase waveform output voltage. The 7 levels are six bipolar levels and a zero level at the output voltage waveform. Using input voltage source V_{in}, the structure produces $\pm V_{in}$, $\pm 2V_{in}$, $\pm 3V_{in}$, and 0. All the switches are consisting of antiparallel diodes, and taking into account inductive load, the operational analysis is presented.

The different modes of operation to generate the output levels of SC MLI are as follows:

Mode I (V_{dc}). The output level $+V_{dc}$ is obtained when switches S_1, S_2, S_3, S_7, and S_8 are OFF and S_4, S_5, and S_6 are in conducting mode. Diode D_3 is in forward conduction and the capacitor C_2 is charged.

Mode II ($+2V_{dc}$). In this mode, switches S_1, S_4, S_7, and S_8 are OFF and the remaining switches S_2, S_3, S_5, and S_6 are in conduction mode. Due to this, the capacitor C_2, which is earlier charged to the input voltage magnitude now discharged and the capacitor C_1 gets charged at the same time.

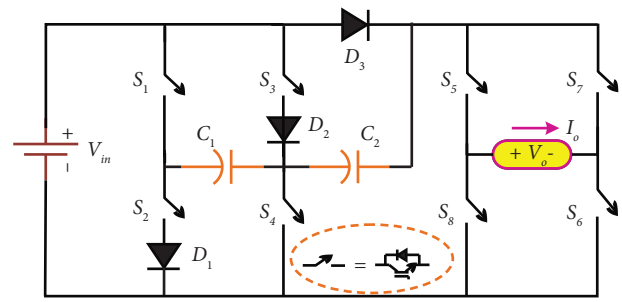

FIGURE 1: 7-L switched-capacitor-based multilevel inverter (7-L SC MLI).

Mode III ($+3V_{dc}$). In this mode, switches S_2, S_3, S_4, S_7, and S_8 are OFF and the remaining switches S_1, S_5, and S_6 are in conduction mode. Both the capacitors discharge in series with the DC source to produce the maximum voltage output in this mode.

Mode IV ($-3V_{dc}$). In this mode, switches S_2, S_3, S_4, S_5, and S_6 are OFF and the remaining switches S_1, S_7, and S_8 are in conduction mode. The operation of capacitors is similar to the maximum positive level in this mode. Both capacitors discharge simultaneously with the DC source.

Mode V ($-2V_{dc}$). In this mode, switches S_1, S_4, S_5, and S_6 are OFF and the remaining switches S_2, S_3, S_7, and S_8 are in conduction mode. Due to this, the capacitor C_2 discharges in series with the input source to produce the second negative level output.

Mode VI ($-V_{dc}$). In this mode, switches S_1, S_2, S_3, S_5, and S_6 are OFF and the remaining switches S_4, S_7, and S_8 are in conduction mode. Only the DC source is accountable to generate the output $-V_{dc}$ in this mode. The capacitor C_2 is charged at the same time and C_1 is in idle condition.

Mode VII ($0V_{dc}$). In this mode, switches S_1, S_2, S_3, S_4, S_5, and S_7 are OFF and the remaining switches S_6 and S_8 are in conduction mode. Two upper switches from the bridge circuit or two lower switches can be triggered to generate the zero level output.

The switching scheme of the 7-L SC MLI with seven different voltage levels ($+V_{dc}$, $+2V_{dc}$, $+3V_{dc}$, and $0V_{dc}$) and the charging and discharging period of capacitors are shown in Table 1.

2.2. Self-Voltage Balancing Analysis. From the operation analysis discussed in Section 2.1, it is clear that the capacitor C_1 is charged during $2V_{dc}$ and $-2V_{dc}$. On the other hand, the capacitor C_2 is charged during V_{dc} and $-V_{dc}$. In addition to this, the capacitor C_1 is discharged during $3V_{dc}$ and $-3V_{dc}$, whereas the capacitor C_2 is discharged during $2V_{dc}$, $3V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. Therefore, symmetrical charging and discharging operation is attained. Also, the capacitors are

Table 1: Switching states of the 7-L SC MLI with capacitor charging (↑) and capacitor discharging (↓) period.

Voltage level	Conducting devices	Capacitor $(C_1)\uparrow$	Capacitor $(C_2)\downarrow$
0	S_5, S_7	—	—
V_{dc}	S_4, S_5, S_6	—	↑
$2V_{dc}$	S_2, S_3, S_5, S_6	↑	↓
$3V_{dc}$	S_1, S_5, S_6	↓	↓
$-3V_{dc}$	S_1, S_7, S_8	↓	↓
$-2V_{dc}$	S_2, S_3, S_7, S_8	↑	↓
$-V_{dc}$	S_4, S_7, S_8	—	↑

charged in parallel connection with the DC source and discharged in series connection with the source to the load. It is also noteworthy that the parasitic resistance is kept low and each capacitor gets sufficient time to charge and discharge within one fundamental cycle. Owing to this, the voltage across the capacitor is naturally maintained at input DC source magnitude throughout the circuit operation. This validates the self-balancing nature and appropriate capacitance is chosen taking into account the maximum time to discharge, while allowing least voltage ripple as follows:

$$C_n \geq \frac{\Delta Q_c}{\Delta V_c} = \frac{2I_{op}\cos\theta_n \cos\varnothing}{k\omega V_{dc}}, \quad (1)$$

where ΔQ_c is the amount of capacitor discharging rate, ΔV_c and k (7-8%) are the ripple voltage and percentage ripple of the capacitor C_n, I_{op} is the maximum value of load current that flows through the capacitors, θ_n is the stating instant of discharging of a capacitor, Φ is the load power factor angle, and ω is the frequency $(2\pi f)$.

2.3. Modulation Technique. The objective of MLIs with low switching frequencies is to produce staircase voltage waveforms. The sequence of each switching function can be chosen to minimize the total harmonic distortion (THD). This is called selective harmonic elimination (SHE) pulse width modulation (PWM). There are also high-frequency modulation techniques, which produce a lower THD with the compromise of having more switching losses. Some examples of high-frequency modulation techniques are sinusoidal pulse width modulation (SPWM) with triangular carriers [11, 12] and space vector modulation. The advantage of SHE PWM [13–16] is its reduced switching frequency. The SHE PWM is commonly used in large power inverters in which switching losses may be very large; if the switching frequency increases, an optimal selection of switching functions eliminates selected harmonics from the output voltage SHE PWM technique pilot to inverter operation at lower switching frequency waveform. Newton–Raphson method and the resultant theory technique are also used for calculating the transcendental equations to find out the switching angles [16]. The former approach requires a good initial guess and gives only a few sets of solutions. In this article, the SHE PWM technique is used to generate the optimal value of switching angles for 7-L SC MLI. The synthesized voltage waveform of 7-L SC MLI is shown in Figure 2. This method utilizes multiple switching for each output voltage step with an enhanced quality of voltage waveform of output, and hence, it is appropriate for high-power converters. The multiple set of solutions for the nonlinear transcendental equations is stored in the form of the look-up table.

3. Comparative Estimation

In order to evaluate the advantage of the proposed SC MLI compared to the recently developed MLIs [17–27], Table 2 presents the different performance parameters, i.e., the required number of switches (No_{sw}), number of diodes (No_d), number of capacitors (No_c), boosting performance, and capability of handling an inductive load.

The MLIs in [17, 23] require a smaller number of switches, but the first one has no boosting ability and the second one is unsuitable for low power factor loading. MLIs introduced in [18, 19] both generate the 7-L output voltage with an equal number of switches, but boosting gain (G) is only 1.5 times of input. In [20], the circuit is capable of boosting voltage 3 times but still requires more switches. In [21, 22], the boosting gain is of 3 times, while generating a 7-L output, but the requirement of switches is more. In [24–27], the number of switch requirement is more for producing 7-L output compared to the proposed structure. The MLI in [25] has the voltage gain limited to 1.5 with number of switches and capacitors required more. In [26], diodes are not required, whereas the structure in [27] has the requirement of high voltage rating switches. The proposed 7-L SC MLI topology exhibits boosting of voltage to $3V_{in}$ and no sensors are required for balancing of the capacitor. In every fundamental cycle, symmetrical charging and discharging are achieved and the number of components with active switches is less. It is noteworthy that the voltage stress in the proposed structure is considerably increased, while maintaining high-gain output. However, as recently there is a lot of development in power electronics components, switches with high voltage rating are readily available, which can be utilized for the proposed circuit design. In fact, a trade-off is essential between the voltage rating (stress) and voltage gain of the MLI. The performance comparison justifies the optimality and compactness for the developed SC MLI in terms of the number of components, while attaining high-gain output. Therefore, the proposed 7-L single-input MLI is highly suitable in single-phase renewable energy applications.

4. Simulation and Experimental Results

The 7-L SC MLI consists of IGBT switches, capacitors, and diodes as shown in Figure 1 and are simulated in the MATLAB/Simulink platform and also verified experimentally. A single DC source of 65 V is considered for validation. The output frequency of the inverter is 50 Hz, and the loads used during the test are an R-load (90 Ω) and RL-load (90 Ω-120 mH and 180 Ω-200 mH). The 2200 μF rating of the capacitor is selected based on the longest discharging period. The SHE PWM technique discussed in Section 2.2 is applied

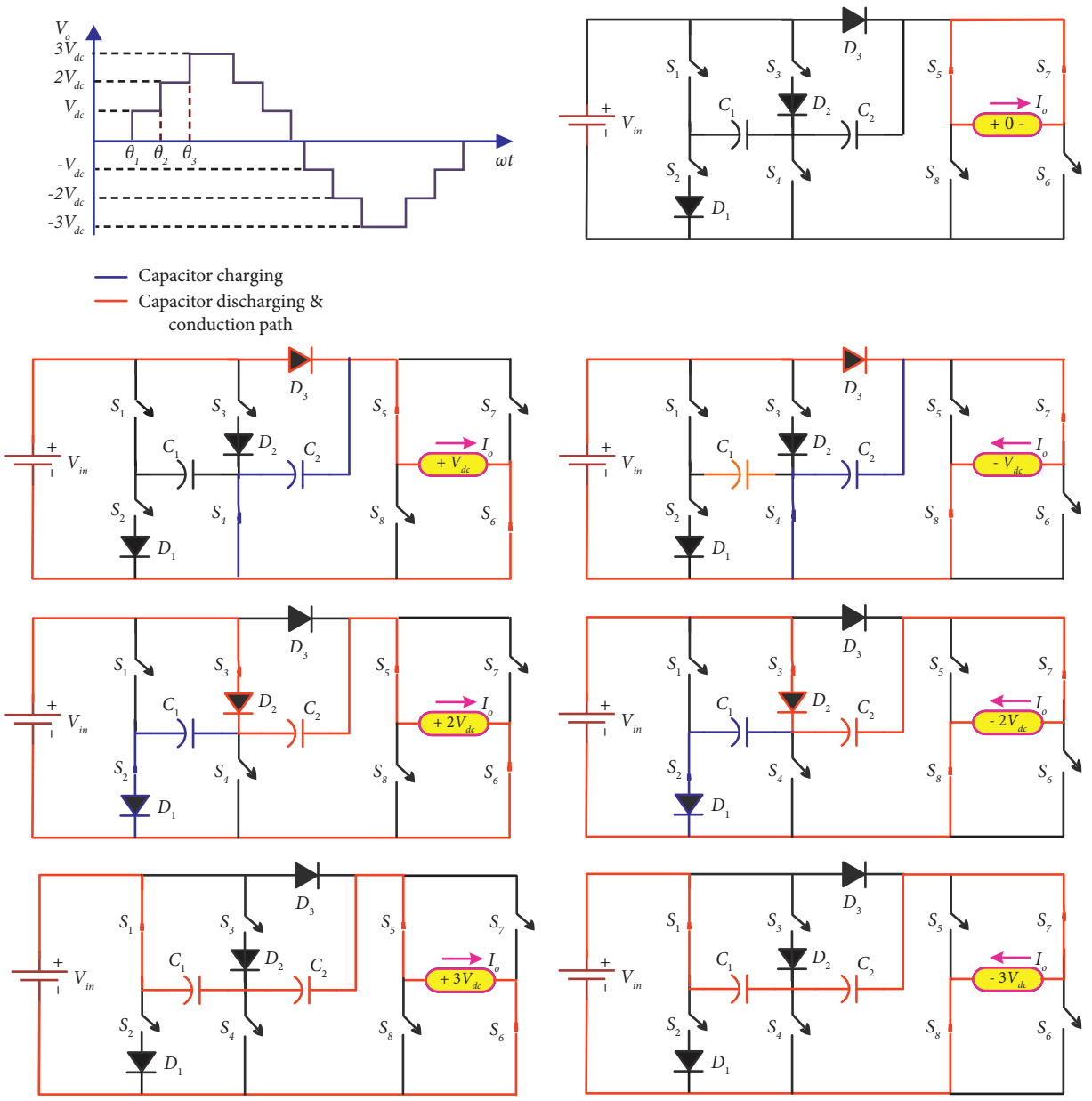

Figure 2: Device operation of proposed 7-L SC MLI.

Table 2: 7-L SC MLI topologies comparison with a single input.

Parameters	N_{osw}	N_{od}	N_{oc}	TVS	Gain (G)	Can feed inductive load
17 [2015]	7	2	3	5	1	Yes
18 [2020]	8	2	2	7	1.5	Yes
19 [2019]	10	0	3	8	1.5	Yes
22 [2016]	16	0	3	14	3	Yes
21 [2019]	13	4	3	13	3	Yes
20 [2020]	9	1	2	15	3	Yes
23 [2014]	7	4	2	15	3	No
24 [2021]	11	0	3	18	3	Yes
25 [2020]	10	0	3	16	1.5	Yes
26 [2019]	12	0	2	16	3	Yes
27 [2020]	12	2	3	26	3	Yes
Proposed MLI	8	3	2	18	3	Yes

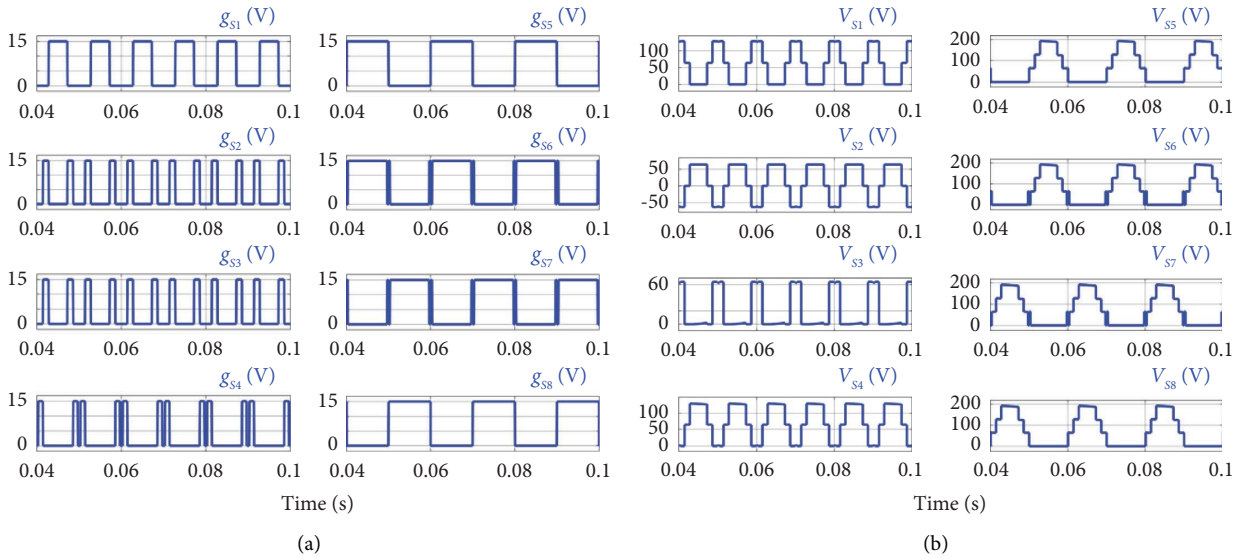

Figure 3: (a) Gate pulses at Mi = 0.9 and (b) standing voltage across the switches.

to find the optimal value of firing angles while keeping the THD minimum. Three nonlinear equations (corresponding to the SHE) are solved, and the switching angles are calculated offline which are used to control the switches. The angles are determined with the objective of eliminating the 5^{th} and 7^{th} orders of harmonics from the output. At a *modulation index* (Mi) = 0.9, the program generates optimum THD, and to validate the change in THD with a change in Mi, angles corresponding to other Mi values of 0.1 are also selected in the simulation and experimental analysis.

4.1. Simulation Analysis. Figure 3(a) shows the PWM pulse across the switches at Mi = 0.9, and the standing voltage across each of the switches is illustrated in Figure 3(b) in which switches block only positive voltage (they are unidirectional). Figure 4 shows the results of the 7-L SC MLI with voltage THD under different Mi conditions. At a lower Mi value, the output is almost a 5-level output, and at a higher Mi, a clear 7-level output is synthesized. Both the capacitor voltages are maintained as desired, and the output current follows the output voltage due to a purely resistive load. It is clearly observed from the results that SHE is the best optimal value for minimum THD at a lower frequency. The THD (%) is reduced as the lower order harmonics (5^{th} and 7^{th}) are removed at a higher Mi. The proposed configuration of MLI is thus suitable to be used with a low-size filter and in applications such as solar, wind, and hybrid energy sources.

Figure 5 shows the dynamic operational ability of the proposed MLI. Under a sudden change in load, Figure 5(a) shows that the load current smoothly changes from purely resistive to sinusoidal-like under inductive loading. The capacitor voltage ripples are also very less as can be verified from the results. Figure 5(b) depicts the smooth change in capacitor voltages and output voltage as a result of the sudden change in input voltage. The capacitor voltages are balanced at the desired value under all operating conditions.

A major inevitable issue in SC circuits is the high current spikes (inrush current) during the capacitor charging process. All the SC MLIs published to date have the same concern. Nevertheless, a recently developed structure in [24] employs a quasiresonant cell in the input side that addresses the issue with capacitor current. By selecting suitable value of small inductor and capacitor (L_{in} and C_{in}), the quasi resonant cell limits the capacitor inrush current during charging. The proposed topology, as presented in the manuscript though, cannot completely eliminate the current spikes; it can be reduced by connecting the quasiresonant cell as in [24]. The resonant cell inductance is chosen considering equivalent series resistance (R_{eq}) in the charging loop with equivalent capacitance (C_{eq}) as follows:

$$L_{in} \geq \frac{R_{eq}^2 C_{eq}}{4}. \tag{2}$$

Figures 5(c) and 5(d) show the capacitor currents along with output voltage without and with employing the quasiresonant cell, respectively. It is clear that charging currents are quite high (≈50 times) in normal operation of the SC type MLIs even when considering the parasitic resistance in the charging path. Taking into account the resonant cell, the capacitor current is drastically reduced without affecting the 7-L operation of the MLI. In the future, much effort needs to be attempted to address the issues with SC current spikes.

4.2. Experimental Analysis. The operation of the proposed structure is further verified experimentally on a low-scale 0.3 kW prototype. MOSFETs (IRF840) and diodes (MUR460) are used to build the prototype. An Arduino-based controller is used to control the switches, and switching pulses are processed through the TLP250-based driver circuit. The driver amplifies the pulses from the

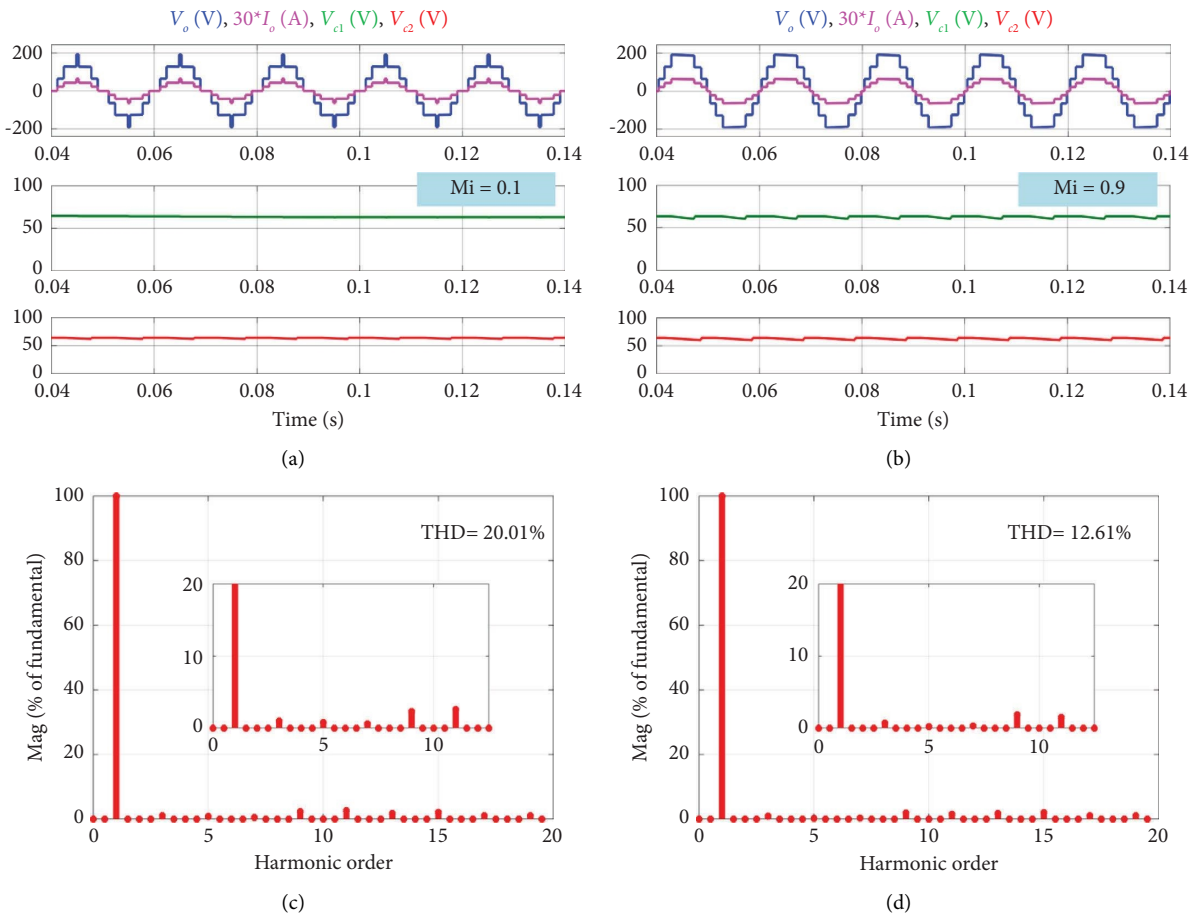

Figure 4: (a) Result under Mi = 0.1, (b) result under Mi = 0.9, (c) harmonic spectra at Mi = 0.1, and (d) harmonic spectra at Mi = 0.9.

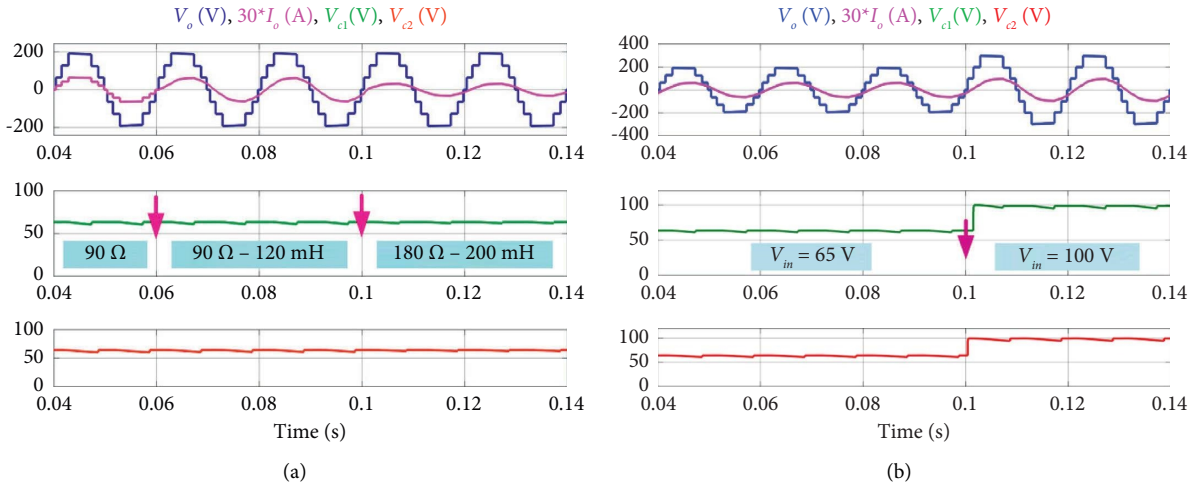

Figure 5: Continued.

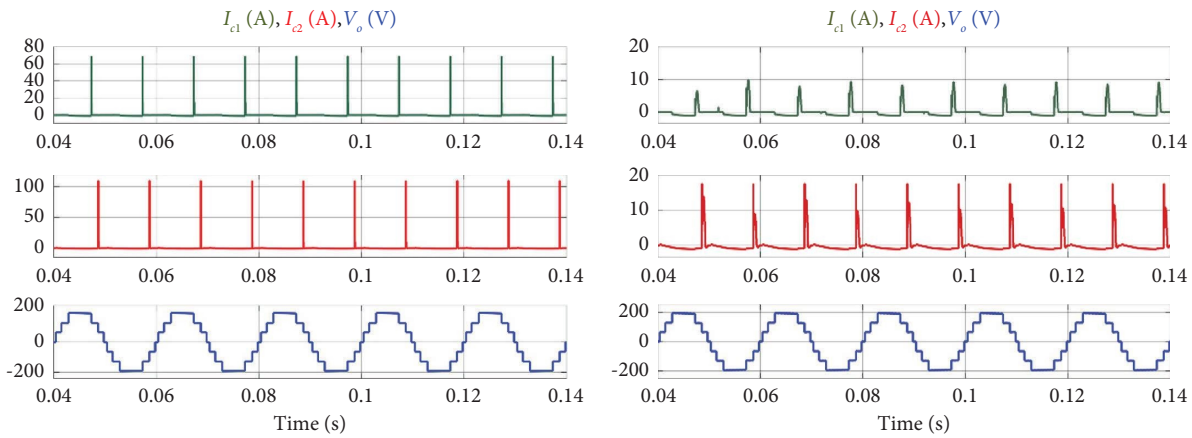

FIGURE 5: Dynamic operation of the proposed MLI: (a) result under sudden variation in loading, (b) result under sudden variation in input voltage, (c) capacitor currents without the resonant cell, and (d) capacitor currents employing the resonant cell.

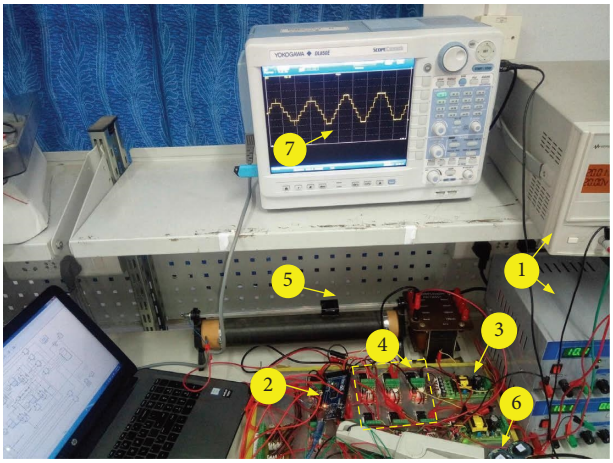

FIGURE 6: Experimental test bench for the proposed topology consisting of (1) isolated DC source, (2) controller, (3) isolated input to driver circuit, (4) switches with drivers, (5) load combination, (6) capacitors, and (7) output on oscilloscope.

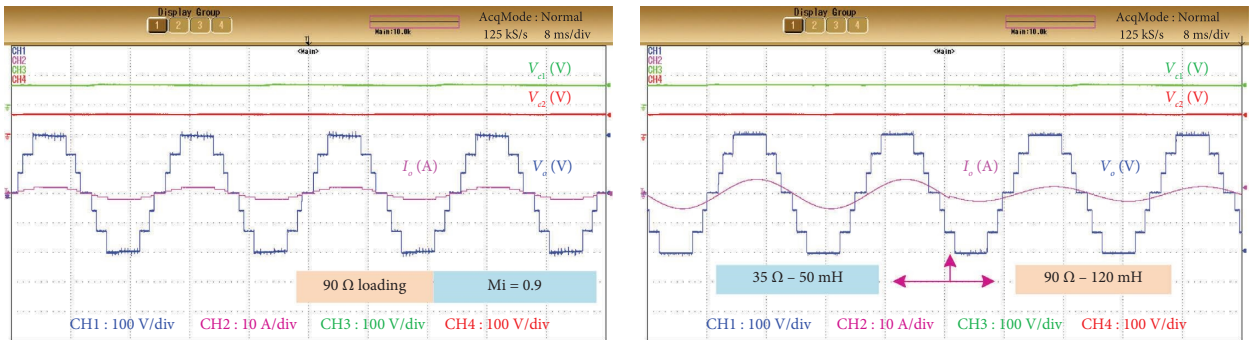

FIGURE 7: Continued.

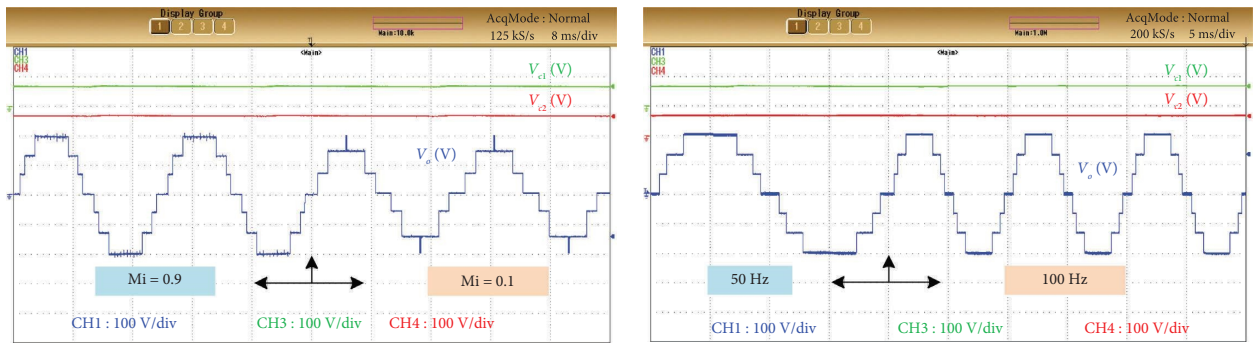

FIGURE 7: Experimental result of the proposed MLI (a) under pure resistive loading, (b) under sudden load variation, (c) under change in switching angles (Mi change), and (d) under change in operating frequency.

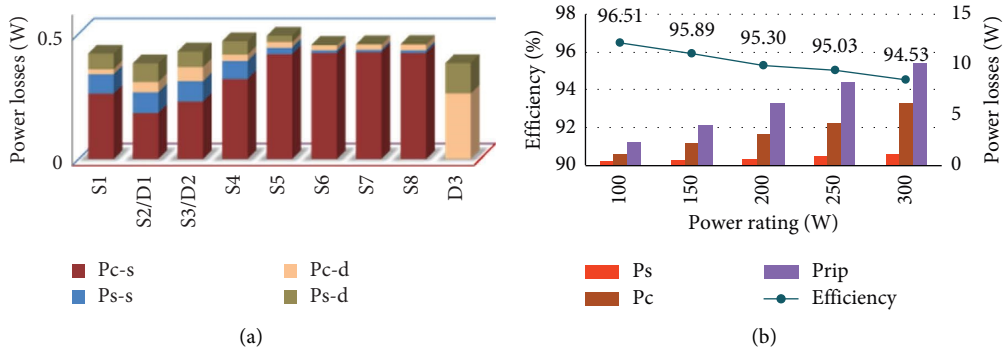

FIGURE 8: (a) Power loss analysis on individual device and (b) efficiency and overall power loss evaluation.

control and also isolates the control circuit from the power board. Different loads such as resistive type and inductive type loadings are taken into account to verify the operation of the proposed MLI. Figure 6 shows the test setup of the proposed 7-L circuit.

Figure 7(a) shows the output under 90 Ω loading and Figure 7(b) depicts a clearly matching output as in the simulation under dynamic, varying inductive loading. Under change in load, the load voltage is stable and only the load current varies. Figure 7(c) depicts the switching angle changes with the change in modulation index output voltage pattern changes. It is noteworthy that the fundamental 7-L output is still achievable under very low modulation index. The maximum positive voltage level is still obtainable. Furthermore, under the variation in frequency of operation, the 7-L output is obtained in Figure 7(d). The capacitor voltage ripple changes smoothly under frequency doubling. The results verify the smooth operation of the proposed circuit, capacitor voltage self-balancing, and low ripple under severe dynamic operating conditions.

Furthermore, the power loss of the proposed circuit is evaluated for individual components considering 90 Ω–120 mH loading. The conduction loss and switching losses of the switches (Pc-s, Ps-s) and diodes (Pc-d, Ps-d) are illustrated in Figure 8(a). In general, three major power loss components in the proposed SC MLI are the switching loss (Ps), conduction loss (Pc), and the ripple power loss (Prip). The overall losses under different rating of the MLI are depicted in Figure 8(b). Power rating is varied by changing the loading. The total power loss is about 9.8 W for 0.2 kW output and 17.4 W for 0.3 kW power rating. The maximum efficiency evaluated is 96.51%, which may further vary considering different rating devices.

5. Conclusion

In this paper, the 7-L SC MLI structure is designed based on switched capacitor concept. The proposed 7-L SC MLI structure requires only one DC source and a smaller number of switches. The capacitors are self-balanced and generate an output voltage with three times the input voltage amplitude. The size of capacitors can be optimized for a high-frequency operation. A comparison is carried out with several MLI from the literature in view of the number of devices, TSV and boosting capacity, and capability of different loads which verifies the optimality and advancement of the proposed structure. The switching operation is based on the SHE PWM technique which justifies very less loss operation at the fundamental frequency. Simulation and experimental results validate the suitability of producing high-gain 7-level output under different operational modes. The proposed structure is highly applicable for low- and medium-power energy conversion applications.

Data Availability

The data used in this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Authors' Contributions

Yatindra Gopal conceptualised the study, developed methodology, wrote the original draft, and validated the study. Kaibalya Prasad Panda performed the experimental validation and wrote the manuscript. Akanksha Kumari wrote the original draft, performed formal analysis, and validated the study. Julio C. Rosas-Caro supervised the study, performed formal analysis, and reviewed, and edited the manuscript.

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