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Research Article

Dynamic Behavior and Stability Analysis of Automatic Voltage Regulator with Parameter Uncertainty

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This research article describes a novel optimization technique called simulink design optimization (SDO) to compute the optimal PID coefficients for an automatic voltage regulator (AVR). The time-domain performance of the proposed controller was analyzed using MATLAB/Simulation, and its performance was compared with that of water cycle algorithm, genetic algorithm, and local unimodal sampling algorithm-based PID controllers. The robustness of the proposed controller was verified by applying the disturbances to the generator field voltage and the amplifier parameter uncertainty. The studies presented in literature were discussed the AVR loop stability using the Bode plot which will not give the minimum stability margins. This study proposes a novel stability analysis called disk-based stability analysis to authenticate the stability of the AVR loop which is obtained by the classical analysis. This stability was compared with the proposed stability analysis. The MATLAB results reveal that the SDO-PID controller regulates the terminal voltage of the generator precisely, is more robust to parameter uncertainty, and is more stable than the other controllers. The maximum allowable parameter uncertainty of the amplifier model was identified as 102% of its nominal parameters. The stability margins are recognized as DGM = 10.40 dB and DPM = 56.50° for the AVR stability.

1. Introduction

Maintaining the power-grid voltage profile is a significant challenge for power engineers. When the grid terminal voltage profile deviates from its idle characteristics, it leads to large variations in the power grid dynamics, and the electrical apparatus, which depends on the power grid, may drop rapidly [1, 2]. In addition, the reactive power consumed by the load was greater than the active power consumption. This can be mitigated by incorporating an AVR into the power grid. The key role of the AVR is to keep the grid terminal voltage as constant, but the AVR does not perform this task alone and requires a PI/PID controller for effective control of the grid terminal voltage [3, 4].

Tuning the PID coefficients is a significant challenge for plant engineers and researchers. Although different control

techniques have been proposed and implemented for the AVR loop, the PID controller remains the best choice for AVR. The control strategies used for tuning PID controller coefficients are classified into three categories: classical [5], intelligent [6–10], and heuristic methods [11–14]. In [15], a novel time-domain objective function was minimized by applying particle swarm optimization (PSO). [2] proposed a local unimodal sample (LUS) algorithm for optimal PID coefficients and proved that the dynamic performance with the proposed algorithm is more superior than the PSO and GA-based PID controllers. Teaching-learning-based optimization (TLBO) in [16] proved that TLBO-PID is more efficient than the controllers presented in the literature. In [17], a streamlined ant-colony-optimization with a novel restrained NelderMead technique was proposed. This novel controller gives a finer transient response compared to GA, PSO, TLBO, and ABC. The AVR not only controls the voltage of the generator terminal but also maintains power system stability and security. A novel optimization technique for tuning PID parameters based on the mother nature-inspired algorithm named as water-cycle-algorithm (WCA) was proposed, and its performance was compared with that of other controllers in [8]. An optimal PID controller was modeled in [18] using the tree-seed algorithm (TSA), and the performance of AVR with TSA-PID was correlated with various metaheuristic methods presented in the literature. A dynamic PID controller was developed for an AVR system considering the field-voltage limitation effect using a hybrid equilibrium optimizer (HEO) in [19]. In [1], a quick and robust PID controller was developed using artificial-ecosystem based optimization (AEO). In addition, the strength of the AEO was studied by applying excitation voltage and generator voltage disturbances. Many optimizing liaisons (MOL) method is an abridged form of the PSO algorithm. The robustness of the AVR system is analyzed by considering the changes in time constants of AVR components in the range of ±50% [20].

Simulink Design Optimization (SDO) is a powerful toolbox for minimizing the cost function using optimization algorithms such as gradient search or pattern search algorithms. The advantages of this design optimization method over other optimization methods are that it is easy to implement efficiently, takes less time to converge, and finds the optimum response with fewer trials. In this study, the SDO technique was used to optimize the controller coefficients to satisfy the required rise time and overshoot constraints.

In control systems, many techniques are available to test the dynamic system stability. Among these techniques, owing to its simplicity, a pole-zero map is used commonly [21]. In the frequency domain, plant stability is analyzed by computing the classical stability margins, gain-margin (GM) and phase-margin (PM), from the Bode diagram [22]. The greater the margins, the greater the plant stability. The main drawback of classical GM and PM from the Bode plot is that they do not provide the minimum phase and gain margins to analyze plant stability. This article introduces a novel approach to study the AVR loop stability called disk-based stability margin analysis [23–25]. The disk-based stability approach gives a stronger assurance of system stability over the classical margin analysis. The key contributions of this analysis are as follows:

(i) The AVR is modeled by considering the parameter uncertainty.

(ii) A novel tuning approach called simulink design optimization was proposed.

(iii) The stability of the AVR with different controllers was analyzed using a pole-zero map, bode plot, and disk-based stability margin analysis, its performance was compared.

(iv) The performance of AVR under the parameter uncertainty was analyzed.

The remainder of this manuscript is arranged as follows. In Section-2, the AVR mathematical analysis is demonstrated. The PID coefficients are tuned in Section-3 using simulink design optimization. In Section-4, the proposed controller performance is discussed and compared with other optimization methods. The article is ended with the conclusions.

2. Automatic Voltage Regulator-Mathematical Model

AVR is an electronic device which automatically maintains the AC generator voltage at a set point. The prime duty of the AVR is to suppress the variations in voltage of the generator to supply a constant and reliable power to the consumer or the load. It is part of the generator excitation system and is normally placed in the AC generator main control box, in the terminal box, or located under the alternator rear cover. The AVR operation is influenced by various parts of the AC generator. Figure 1 shows a schematic of the AVR loop.

The AVR on the generator performs several functions such as regulating, controlling, and monitoring the generator terminal voltage based on the feedback principle. Initially, the voltage error signal (e) is generated by sensing and differentiating the AC generator voltage (V_t) and the setpoint voltage (V_{ref}); then, the voltage error is used to modify the field current by lowering or increasing the current flow to the exciter stator. This leads to a lower or higher voltage at the AC generator terminal; that is, if there is any change in the generator voltage, the output of the generator is automatically stabilized by the AVR.

2.1. Amplifier Model. The amplifier output voltage $V_R(S)$ depends on the error voltage e (s); therefore, ($\Delta V_R(s) = K_{AMP}\Delta es$). Where K_{Amp} is the amplifier gain constant and τ_{Amp} be the amplifier time constant. The amplifier transfer function is given as follows:

$$G_{Amp}(s) = \frac{\Delta VR(s)}{\Delta e(s)}$$
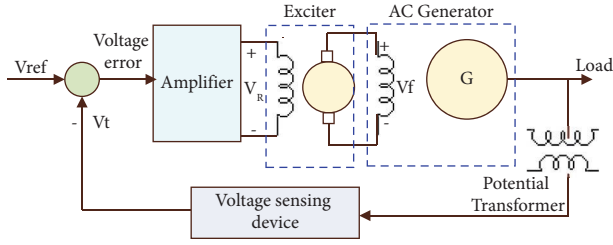$$= \frac{K_{Amp}}{1 + s\tau_{Amp}}. \tag{1}$$

FIGURE 1: Simplified model of the AVR loop.

2.2. Field Exciter Model.

The field exciter provides a suitable control signal for the control of alternator terminal voltage. Let R_{ex} and L_{ex} be the exciter field resistance and inductance, respectively; then we get the following equation:

$$\Delta V_R = R_{ex}\Delta i_e + L_{ex}\frac{d}{dt}\Delta i_e,$$

$$\Delta V_R(s) = R_{ex}\Delta I_e(s) + SL_e(s).$$

(2)

The change in the exciter field current Δi_e produces a suitable field voltage ΔV_f. The change in the field voltage depends on the change in the field current. Hence

$$\Delta V_R(S) = K_{Ex} * \Delta i_e(S).$$

(3)

From (2) and (3), $\Delta V_f(S) = K_{Ex}/(1 + S\tau_{ex}\Delta V_R(S))$, where K_{ex} = Field exciter gain constant and T_{ex} = Field exciter time constant = (L_{ex}/R_{ex}).

$$G_{ex}(s) = \frac{\Delta V_f(s)}{\Delta V_R(s)}$$

$$= \frac{K_{ex}}{1 + s\tau_{ex}}.$$

(4)

2.3. AC Generator Model.

Generally, the generator field was excited by the field voltage V_f. Let R_f and L_f denotes the generator field resistance and reactance, respectively. At no load, the generator terminal voltage, V_t, is proportional to the field current I_f. Hence

$$G_{gen}(s) = \frac{\Delta V_t(s)}{\Delta I_f(s)},$$

$$= \frac{K_{gen}}{1 + s\tau_{gf}},$$

(5)

where K_{gen} = AC generator gain constant and τ_{gf} = generator time constant = L_f/R_f.

2.4. Terminal Voltage Sensor Model.

The AC generator voltage is measured by the voltage sensing device, passed through the rectifier and filter circuit, and then differentiated with the set-point voltage V_{ref} to generate a voltage error signal. The main advantage of using a voltage sensor is that it has a quick response to the generator terminal voltage.

$$G_{vs}(s) = \frac{K_{vs}}{1 + s\tau_{vs}},$$

(6)

where K_{vs} = Voltage sensor gain constant and, τ_{vs} = Voltage sensor time constant. Using equations (1), (4), (5) and (6), AVR schematic diagram can be redrawn as a transfer function model, as shown in Figure 2.

Sometimes, the generator may lose its excitation when the AVR fails. This causes a sudden decrease in the terminal voltage at the generator side, and the generator should shut down when an under-voltage fault occurs. If the generator does not have any under-voltage protection, it may run, but there is a severe damage at the load or consumer side. This can be mitigated by adding a suitable PI/PID controller to the AVR. Table 1 lists the standard range and the proposed nominal values of the AVR loop.

After considering the aforementioned proposed values, the equation (7) represents the CLTF of the AVR loop.

$$G_{AVR}(s) = \frac{V_t(s)}{V_{ref}(s)}$$

$$= \frac{0.1s + 10}{0.0004s^4 + 0.0454s^3 + 0.555s^2 + 1.51s + 11}.$$

(7)

The closed-loop plant represented by equation (7) is stable because the real and complex poles of the AVR loop lie on the left half of the s-plane. The response (closed-loop) of the AVR loop without the controller has more oscillations, as shown in Figure 3, with a first-peak magnitude of 1.5056 pu (%Mp = 65.31) and a steady-state error of 0.0909 pu. This transient behavior influences the power plant stability and security.

3. PID Controller Design

The controller is mechanism that mitigates the deviation between the process variable and set point. The important function of the controller includes (i) It decreases the steady-state error by improving the steady-state accuracy, (ii) Plant stability improves, (iii) It will speed up the response of the over-damped plant, and (iv) Reduces the noise signals produced by the plant. Generally, PI or PID controllers are used for plant control. The PI controller produces an actuating (control) signal depending on the proportional plus integral of error signal. The PI controller can be mathematically represented as follows:

$$\text{Control signal } u(t) = K_p e(t) + K_i \int e(t)dt.$$

(8)

The PID controller generates the actuating (control) signal depending on the proportional and integral and derivative of error signal. The PID controller can be mathematically represented as follows:

$$\text{Control signal } u(t) = K_p e(t) + K_i \int e(t)dt + K_d\frac{d}{dt}e(t).$$
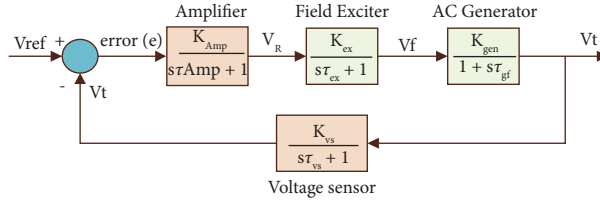
(9)

FIGURE 2: Transfer function model of AVR loop.

TABLE 1: Standard range and proposed nominal values of AVR.

Component	Standard range	Proposed value
Amplifier	$K_{Amp} = 10$ to 40 $\tau_{Amp} = 0.02$ to 0.1 sec	$K_{Amp} = 10$ $\tau_{Amp} = 0.1$ sec
Field exciter	$K_{ex} = 1$ to 10 $\tau_{ex} = 0.4$ to 1 sec	$K_{ex} = 1$ $\tau_{ex} = 0.4$ sec
AC generator	$K_{gen} = 0.7$ to 1 $\tau_{gf} = 1$ to 2 sec	$K_{gen} = 1$ $\tau_{gf} = 1$ sec
Terminal voltage sensor	$K_{vs} = 1$ $\tau_{vs} = 0.01$ to 0.06 sec	$K_{vs} = 1$ $\tau_{vs} = 0.01$ sec

Result:
1st peak amplitude =1.5056pu (%Mp = 65.31)
Rise time = 0.4377sec
Steady state error = 0.0909pu

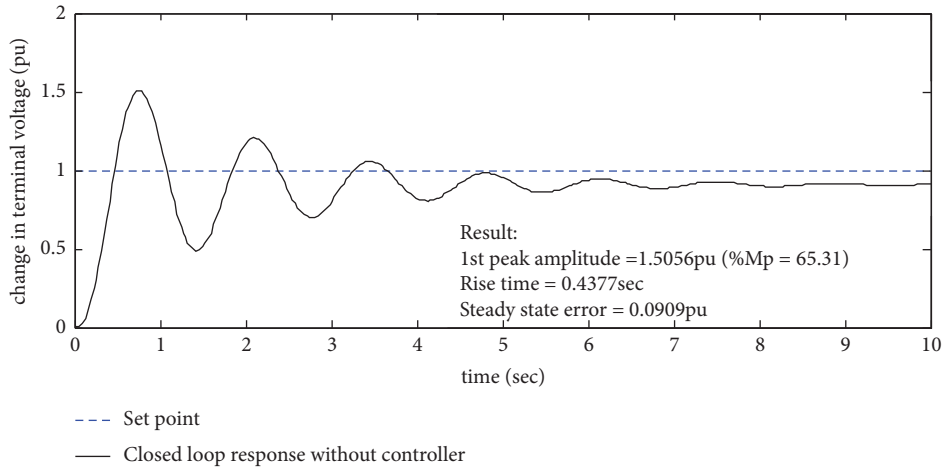--- Set point

—— Closed loop response without controller

FIGURE 3: Closed loop response of AVR-no controller.

The derivative (D) term in PID controller will lead to performance improvement by quick damping of transients. Figure 4 provides the process/plant with the PID controller.

3.1. Water Cycle Algorithm (WSA).

The WCA is a meta-heuristic algorithm inspired by real-life water cycle process. It was first introduced by [26] to solve various engineering design problems. Figure 5 shows the WCA flow diagram for the AVR loop. The main benefit of WCA over other control methods is that it is a direct and computationally difficult free method.

The WCA is developed depending on constant water movement in the nature. In this algorithm, raindrops collection is streams though different water cycle stages. The basic concepts and schemes which underlie the WCA are motivated by nature and based on an inspection of the
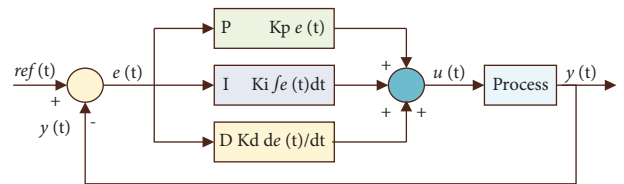

FIGURE 4: Structure of PID controller with process/plant.

water-cycle process and how rivers and streams flow to the sea in the natural world. Like other optimization methods, the WCA starts with the primary population N_{pop}, also called as the fitness function solution. The following steps were used in the WCA optimization process [8, 26].

Step-1: Initialize the parameters: N_{pop} (population number), Max.Itr (maximum iterations), d (distance
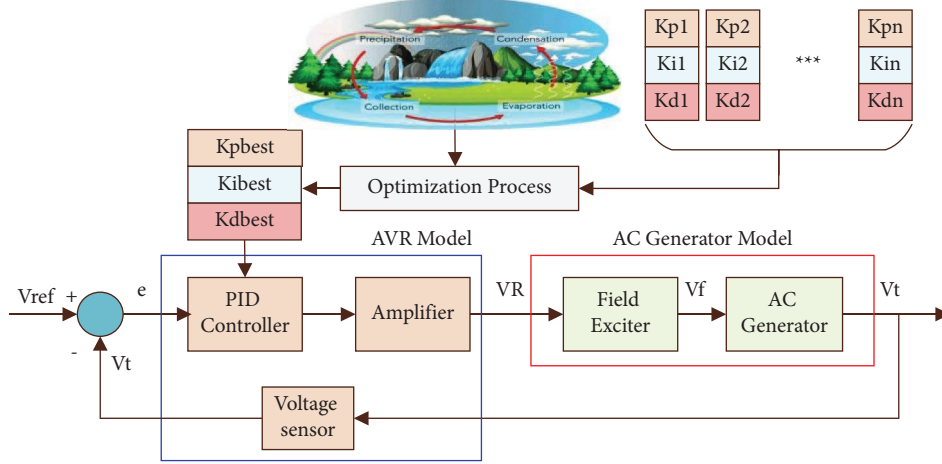
FIGURE 5: WCA flow diagram for AVR loop.

between the stream and river), and N_{sr} (sum of the number of rivers).

Step-2: Generate the initial population randomly. In addition, initial streams, rivers, and the sea are formed.

Step-3: Evaluate the fitness value/cost function ($Cost_n$) for each raindrop.

Step-4: Add raindrops to the rivers and sea using

$$NS_n = \text{round} \left\{ \left| \frac{Cos\, t_n}{\sum_{i=1}^{Nsr} Cos\, t_i} \right| \right\} * N_{pop} - N_{sr}, \tag{10}$$

$$n = 1, 2, \ldots, N_{sr}.$$

Step-5: Update the locations of rivers and streams using the following equations:

$$X_{river}^{i+1} = X_{river}^i + \text{rand} * C * \left(X_{sea}^i - X_{river}^i \right),$$
$$X_{stream}^{i+1} = X_{river}^i + \text{rand} * C * \left(X_{river}^i - X_{Stream}^i \right), \tag{11}$$

where rand = random number in [0, 1] space, C is a constant between 1 and 2.

Step-6: If the river provides the best solution, the position of the river is exchanged with the sea. Similarly, if the stream finds a solution superior to that of the river, the stream and river positions are exchanged.

Step-7: Check the evaporation condition, that is,

$$\left| X_{sea}^i - X_{river}^i \right| < d_{max}; \quad i = 1, 2, \ldots, d_{max} - 1. \tag{12}$$

If the evaporation condition is satisfied, the rain process starts and a new stream location is

$$X_{stream}^{new} = L_b + \text{rand} * (U_b - L_b), \tag{13}$$

where L_b and U_b be the lower and upper bounds, respectively.

Step-8: Reduce the present distance between the stream and river, $d_{max}^{i+1} - d_{max}^i - (d\left(_{max}^i\right)/(\text{Max} \cdot \text{Itr}))$. If $d < d_{max}$, it shows that the river reached the sea.

Step-9: Check the convergence criteria, that is, maximum iterations reached. If the stopping criterion is satisfied, print the optimum values of K_p, K_i, and K_d. Otherwise repeat from Step 5.

3.2. Simulink Design Optimization (Proposed Method). Simulink design optimization (SDO) provides blocks, functions, and interactive tools for analyzing and tuning plant parameters using numerical optimization. This technique helps in the enhancement of model accuracy by using the test data to regulate the physical parameters. Using this design optimization technique, it is possible to find out the sensitivity of the plant and fit the model to test data also. The overall performance of the plant can be enhanced by combinedly optimize the physical plant parameters and controller gains using this technique. This technique is regularly used for dynamic system control. The following steps were used to obtain the optimized controller coefficients.

Step-1: Take any model and connect it in MATLAB/ Simulink with the help of the required block per problem, including PID controller.

Step-2: To specify the step-response requirements, add a check step response characteristics (CSRC) block to the model. To obtain this block, click the library browser on the simulation tab and select the signal constraints in the simulink design optimization list (see Figure 6).

Step-3: Drag and drop the CSRC block into the model window and connect it to the plant output. The block is connected to a signal for which the design requirements are specified, as shown in Figure 7.

Step-4: Double-click the CSRC block to open the block parameters dialog and specify the bounds of the rise time, settle time, % overshoot, initial, and final values. To open the Response Optimizer in the CSRC block parameter dialog, click on Response Optimization. The region bounded by the line segments shows the step-response requirements specified in the CSRC block.
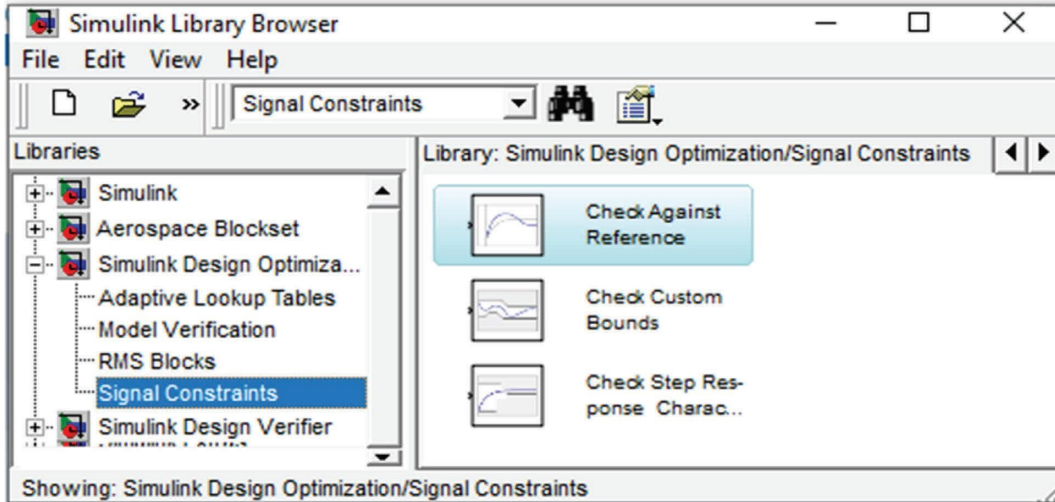
FIGURE 6: Identification process of the check response characteristics block.
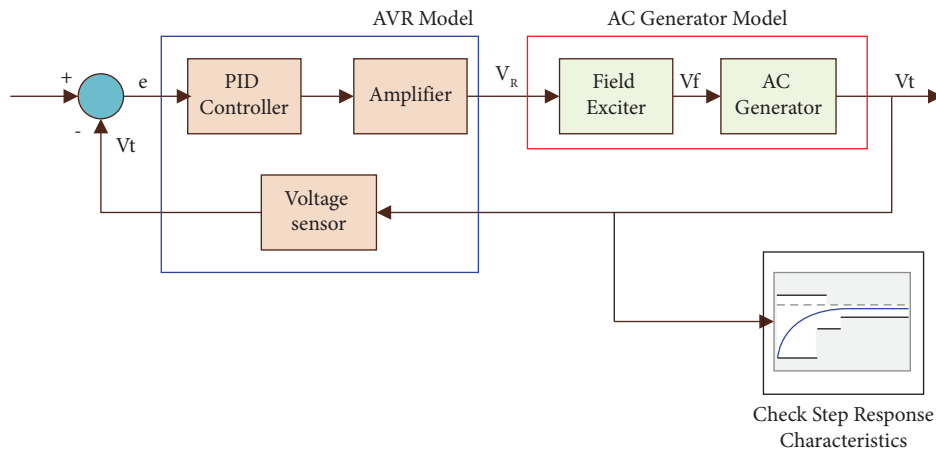

FIGURE 7: AVR loop with CSRC block.

Step-5: Now, select New from the design variable set list to create a set of desired variables (see Figure 8). K_i, K_p, and K_d are then selected to add parameters to the desired variable set and press ←.

Step-6: Click Optimize to optimize the model response. The modified design variables were obtained using the gradient descent method at each iteration. After the completion of optimization, the message optimization converged will appear in the optimization progress report. This indicates that the optimization solver finds a solution that reaches the desired requirements within the tolerance and parameter bounds.

Step-7: Finally, verify that the model output satisfies the optimized response. The optimized response lies in the region formed by the desired requirement line segments. To check the optimized controller parameters, click DesignVars in the model workspace.

The optimal PID coefficients attained by the proposed technique are $K_p = 0.815$, $K_i = 0.563$, and $K_d = 0.284$.

4. Simulation Results and Discussion

4.1. Time-Domain Performance Comparison with Other Controllers. The proposed controller is studied with respect to its performance and compared with other controllers in the literature by drawing time-domain plots. Figure 9 shows the variations in the generator terminal voltage for a given set-point signal. According to Figure 9, the rise time, peak overshoot and settling time of the AVR loop controlled by the proposed controller are low, whereas the AVR loop controlled by the LUS-PID has a longer rise time, even though its overshoot and settling time (t_s) is small.

Table 2 shows a comparison of the set-point tracking performances of the various controllers. According to Table 2, the AVR loop controlled by the SDO-PID exhibits superior performance compared to the WCA-PID, GA-PID, and LUS-PID.

Figures 10 and 11 show the variations in the field voltage and manipulated control signal applied to the amplifier for further control of the generator field voltage, respectively.
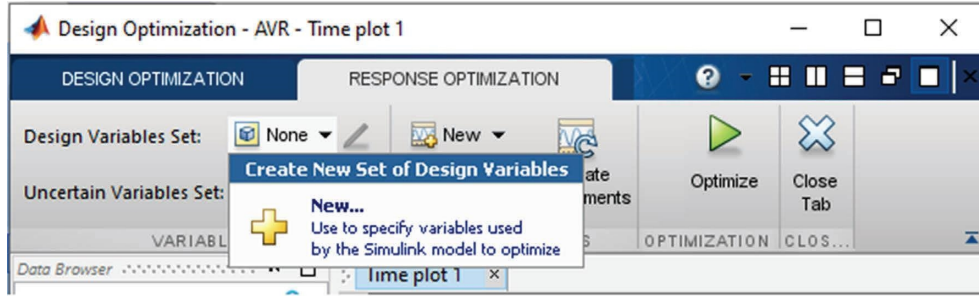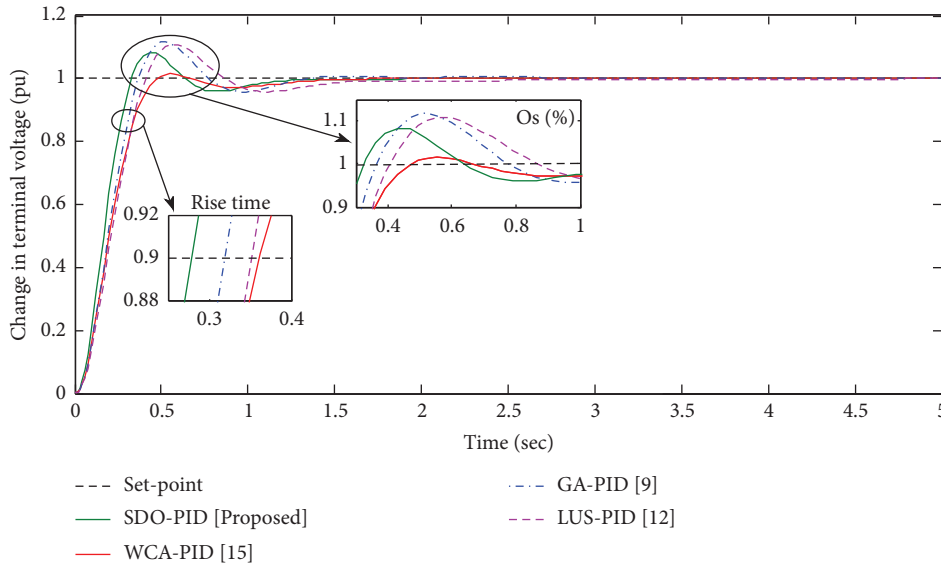
Figure 8: Create new set of design variable.

Figure 9: Comparison of time-domain performance of SDO-PID with other controllers.

Table 2: Comparison of SDO-PID performance with other controllers.

Controller	Rise-time, t_r (sec)	%Overshoot	Settling-time, t_s (sec)
SDO-PID (proposed)	0.278	8.39	0.95
WCA-PID [8]	0.362	2.42	0.45
GA-PID [11]	0.319	10.62	1.12
LUS-PID [2]	0.352	9.91	1.29

4.2. Verification of Controller Robustness. Any controller designed for any plant should be robust and stabilize the closed-loop plant. One way to check the robustness of the controller is to apply of an external disturbance to the field voltage. Figure 12 shows the change in the terminal voltage owing to disturbances in the field excitation.

As shown in Figure 12, the robustness of the SDO-PID is greater because its performance is closer to that of the external disturbance. The WCA-PID and LUS-PID possess low robustness to the external disturbances in field voltage.

Another way to check the robustness of the controller is parametric uncertainty. Practically, the amplifier in the AVR loop is a nonlinear element, as it consists of a power-electronics-based control circuit. We considered the uncertainty of the amplifier parameters (K_{Amp} and τ_{Amp}). The

uncertainty of the amplifier is modeled such that the amplifier parameters vary up to the maximum allowable value from their nominal value. Figure 13(a) shows the performance of the SDO-PID-controlled AVR under parametric uncertainty. As shown in Figure 13(a), the maximum allowable parametric uncertainty is 102% of the nominal value. Beyond this value, the AVR loop was unstable.

Similarly, Figures 13(b) and 13(c) illustrate the performance of the AVR loop with WCA-PID/GA-PID and LUS-PID, respectively, under parameter uncertainty. The maximum allowable variations in the amplifier parameters with the WCA-PID/GA-PID, and LUS-PID were 83% and 86% of the nominal value, respectively. Beyond these values, the AVR loop was unstable. According to the analysis, the SDO-PID was more robust than the other controllers.
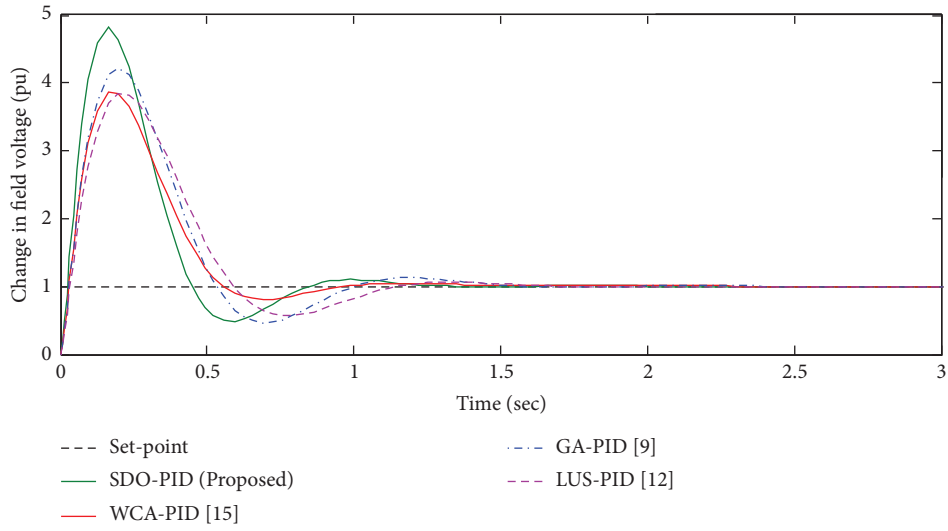
FIGURE 10: Variations in field voltage with SDO-PID and comparison with other controllers.
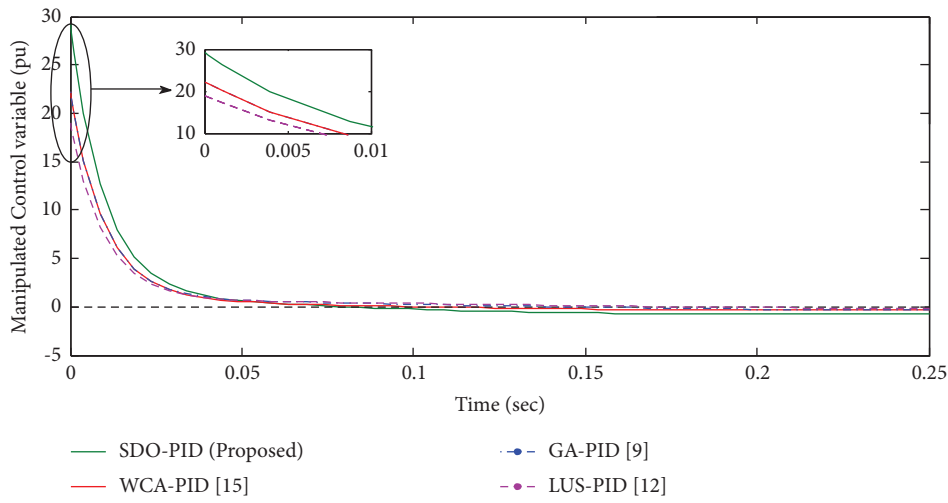

FIGURE 11: Comparison of manipulated control signal and comparison with other controllers.
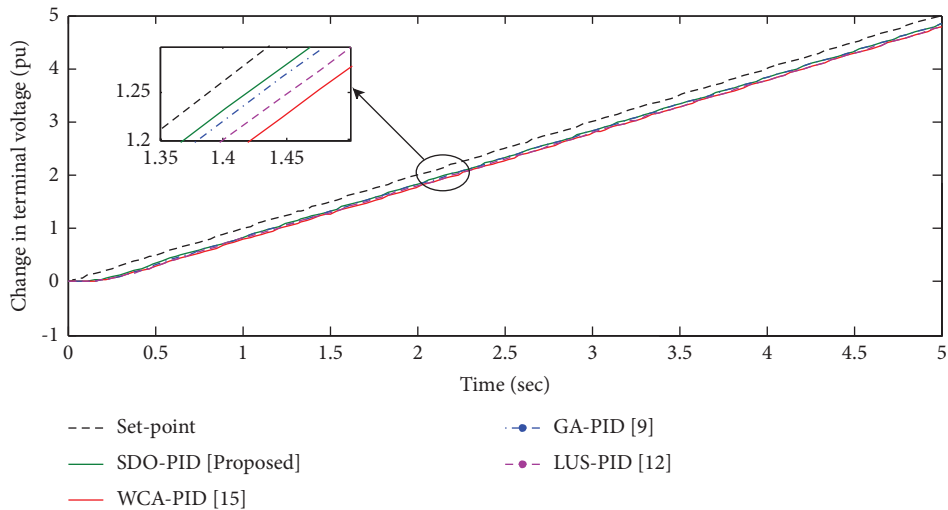

FIGURE 12: Performance comparison of various controllers for disturbances in field voltage.
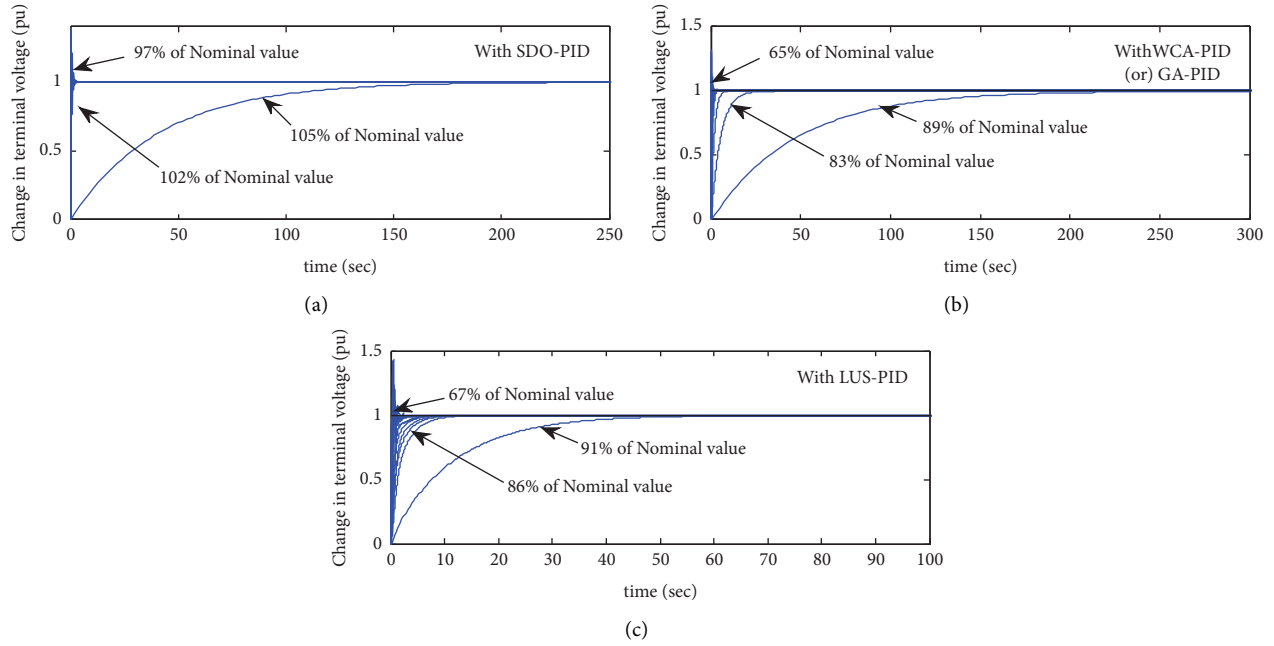
FIGURE 13: Performances of AVR loop with various controllers under amplifier parameter uncertainty. (a) With SDO-PID. (b) With WCA-PID or GA-PID. (c) With LUS-PID.

4.3. Verification of AVR Loop Stability.

4.3. Verification of AVR Loop Stability. The closed-loop stability of the AVR with the controller is verified by drawing a pole-zero plot, computing the stability margins from the bode diagram, and also by computing the minimum stability margins using disk-based stability analysis.

4.3.1. Pole-Zero Plot Analysis. The pole-zero plot is used to discuss the stability of the dynamic system by locating the poles on the left side of the s-plane. Figure 14 shows the location of poles and zeros on the s-plane.

Table 3 gives the poles and zeros of the AVR loop with different controllers. In accordance with pole-zero plot logic, the AVR system controlled by the four controllers is stable. However, if examined in depth, the AVR loop with the SDO-PID is more stable than the other PID controllers. The AVR loop with WCA-PID, GA-PID, and LUS-PID has a slow response and increased rise time owing to its dominant poles that are nearer to the origin/imaginary axis compared to SDO-PID. The major limitation of the pole-zero plot is that it indicates whether the plant is stable or not but does not give the stability margin limits.

4.3.2. Bode Analysis. It is easy to draw and verify the stability of the dynamic system using the Bode diagram. The requirements for any stable system are GM and PM, that is, if the margin is greater, the plant is more stable. The comparison of the Bode diagrams of the controlled AVR loop is shown in Figure 15.

The classical margins (GM and PM) of the studied controllers are listed in Table 4. According to Table 4, the AVR loop controlled by the SDO-PID is more stable because it provides more GM and PM than the other controllers.

However, the AVR loop with WCA-PID has lower stability margin values, that is, the AVR loop with WCA-PID is the least stable when compared to the SDO-PID, GA-PID, and LUS-PID controllers. The limitation of Bode analysis is that it cannot provide the minimum stability margin to check plant stability.

4.3.3. Disk-Based Stability Analysis. Similar to classical margins (GM and PM), disk margins quantify closed-loop stability against changes in gain or phase in an open-loop response. The disk-based margin approach gives a stronger assurance of system stability than the classical margin analysis because it considers all frequencies and loop interactions. Figure 16 shows the variations in gain or phase margins with four controllers, which indicate that the AVR can tolerate the perturbations without becoming unstable. The region inside the gain margin or phase margin plot indicates the AVR loop stability. Table 5 lists disk margins (DGM and DPM) for various controllers.

According to Table 5, the gain and phase margins (using SDO-PID) occurs at 8.10 rad/s. At this frequency, the AVR loop can tolerate variations in the open-loop gain of ±10.4 dB or phase of ±56.50°. Also, at 7.47 rad/s, the AVR loop with WCA-PID can tolerate the open-loop gain variations of ±9.20 dB or a phase of ±51.80°. From the comparison of disk margins with various controllers, it is clear that the AVR loop with the SDO-PID provides more stability than the other controllers.

Figures 17 and 18 depict the disk-based stability margins of the AVR model (open-loop) with SDO-PID and LUS-PID, respectively, for amplifier uncertainty (i.e., 102% of nominal values). The AVR with the SDO-PID offers the least stability for the modeled uncertainty of the amplifier. This
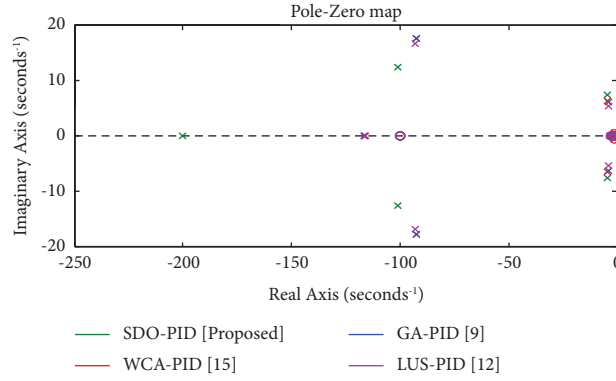
Figure 14: Location of pole-zeros on the S-plane.

Table 3: Poles and zeros of AVR loop with controllers.

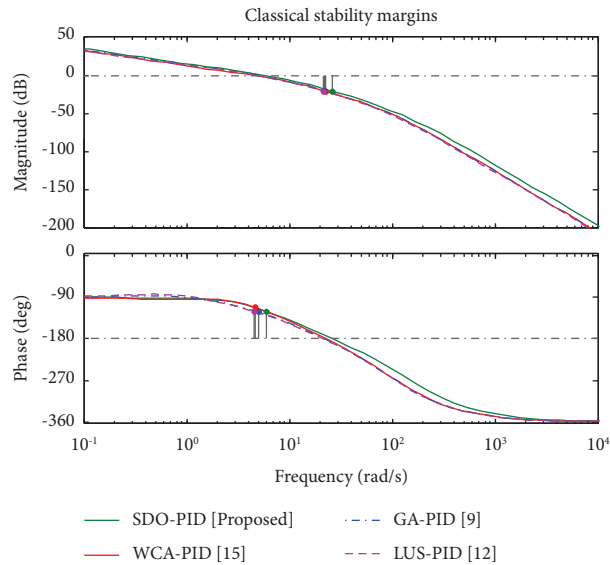| Controller	Poles	Zeros
SDO-PID (proposed)	$-99.97, -10.49, -0.5 \pm 4.662i$	-100
WCA-PID [8]	$-100, -1.165, -0.927 \pm 0.177i, -0.046 \pm 0.064i, -0.012 \pm 0.0055i$	$-100, -1, -0.013 \pm 0.0047i$
GA-PID [11]	$-100, -1.165, -0.0272, -0.0074, -0.927 \pm 0.177i, -0.04 \pm 0.062i$	$-100, -2.66, -0.768$
LUS-PID [2]	$-100, -1.157, -0.036, -0.006, -0.93 \pm 0.167i, -0.038 \pm 0.0537i$	$-100, -3.173, -0.62$

Figure 15: Comparison of Bode plots of AVR with controller.

Table 4: Classical margins comparison.

Controller	Gain margin (GM)	Phase margin (PM)
SDO-PID (proposed)	24.4 dB (at 32.7 rad/s)	67.9° (at 5.88 rad/s)
WCA-PID [8]	20.6 dB (at 22.7 rad/s)	66.3° (at 4.7 rad/s)
GA-PID [11]	20.62 dB (at 22.7 rad/s)	66.1° (at 4.68 rad/s)
LUS-PID [2]	21.5 dB (at 22.2 rad/s)	66.6° (at 4.26 rad/s)

can be stated by observing the stability margins of all the sampled models (see Figure 17). According to Figure 17, the stability margins of some sampled models lie below the stability margin of the nominal model; hence, the AVR with SDO-PID is the least stable. But, for the same amplifier
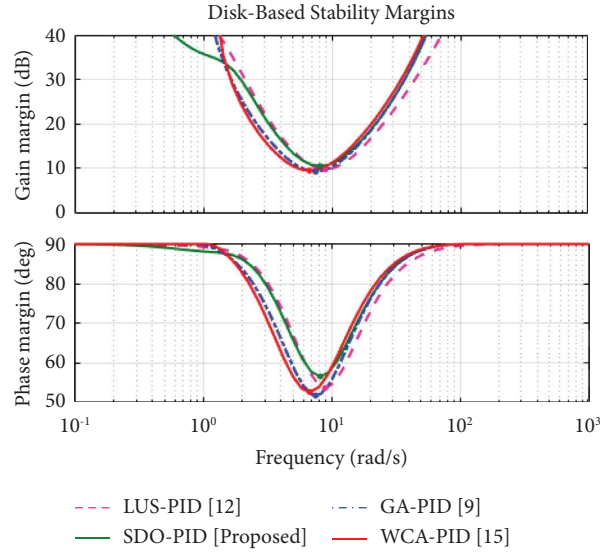
Figure 16: Disk-based stability margins of nominal AVR open-loop model with controller.

Table 5: Classical margins comparison.

Controller	Disk gain margin (DGM)	Disk phase margin (DPM)
SDO-PID (proposed)	10.40 dB (at 8.10 rad/s)	56.50° (at 8.10 rad/s)
WCA-PID [8]	9.20 dB (at 7.47 rad/s)	51.80° (at 7.47 rad/s)
GA-PID [11]	9.41 dB (at 6.70 rad/s)	52.60° (at 6.70 rad/s)
LUS-PID [2]	9.67 dB (at 8.88 rad/s)	53.60° (at 8.88 rad/s)

Figure 17: Disk margins of the maximum uncertain AVR loop with SDO-PID.
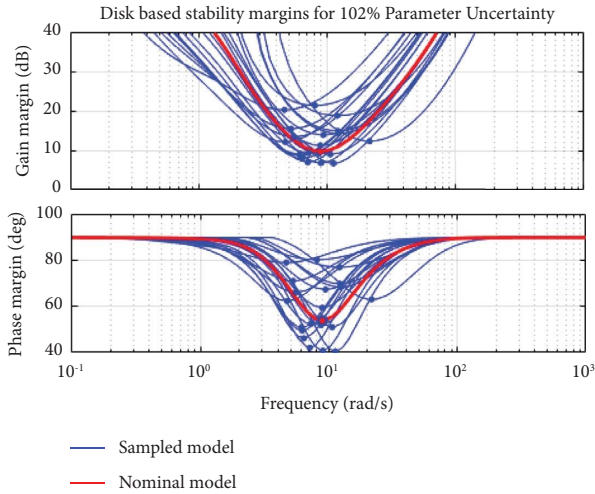

Figure 18: Disk margins of the maximum uncertain AVR loop with LUS-PID.

uncertainty, the AVR with the LUS-PID is unstable according to Figure 18.

5. Conclusion

This article introduced a novel optimization technique called Simulink Design Optimization (SDO) to determine the optimal PID coefficients (K_i, K_p, and K_d) for the AVR loop. The obtained SDO-PID coefficients were adopted to check the AVR loop performance for the unit step change in the terminal voltage. The time-domain performance of the SDO-PID is correlated with WCA, GA, and LUS-PID controllers. The results show that the SDO-PID provides good time-domain performance with regard to rise-time and

overshoot. The robustness of the proposed and other optimized controllers was verified for field-voltage disturbances and parameter uncertainty in the amplifier model (K_{Amp}, τ_{Amp}). In comparison, it was demonstrated that the SDO-PID is more robust against parameter uncertainty and identified the maximum allowable parameter uncertainty of the amplifier model as 102% of its nominal parameters. Although the stability of the AVR loop with various controllers has been presented well in the referenced papers, the effects of parameter uncertainty in the amplifier and perturbation in the feedback loop have not yet been discussed well. In this study, a novel stability analysis called disk-based stability analysis is introduced to discuss the AVR loop stability in addition to the classical stability analysis. It is identified that the AVR loop controlled by the SDO-PID offers the disk-based margins as DGM = 10.40 dB (@ 8.18 rad/s) and DPM = 56.50° (@ 8.18 rad/s). Finally, from the MATLAB results, it is clear that the SDO-PID is not only robust and corrects the terminal voltage efficiently, but also enhances the AVR loop stability.

Data Availability

No Supplementary data are available. If anything needed, please contact Dr.Asadi Srinivasulu, head.openlabs@ bluecrest.edu.lr.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Authors' Contributions

Pasala Gopi performed conceptualization, data curation, formal analysis, methodology, software, and writing-original draft. P Srinivasa Varma performed supervision, investigation, formal analysis, visualization. Ch Naga Sai Kalyan performed plagiarism check and removal of the document. Dr. Ravikumar CV was responsible for visualization, investigation, formal analysis, and software. Dr. Asadi Srinivasulu performed supervision, writing–review & editing. Bhimsingh Bohara performed project administration, visualization. Rajesh A was responsible for visualization, investigation, formal analysis. Mohd Nadhir bin Ab Wahab performed supervision, investigation, formal analysis, and visualization. Sathish K performed formal analysis, software, plagiarism checking and writing.

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