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Research Article

THD Reduction of Improved Single Source MLI Using Upgraded Black Widow Optimization Algorithm

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An upgraded Black Widow Optimization algorithm for obtaining the ideal switching angles of a reduced structure multilevel inverter is proposed in this paper with minimum voltage THD. The conventional BWO algorithm has been modified and proposed to solve the THD minimization problem with faster convergence rate, lesser tuning variables, and lesser number of equations than the other existing nature inspired algorithms. The reduced structure MLI is designed with three asymmetrical DC voltage sources of ratio 1 : 2 : 4 to generate 15-level output voltage which requires reduced number of switching devices in comparison with the existing topologies of equivalent voltage level. The asymmetrical DC voltage sources to the MLI are derived from a single DC voltage source using a multisecondary winding DC-DC converter in order to provide the isolation between the load side and source side. The proposed modified BWO algorithm reduces the complexity of solving the nonlinear equations to achieve the best result by avoiding the local optima. To verify the effectiveness of the upgraded BWO algorithm, the optimization problem for three phase fifteen level MLI has been solved using the genetic algorithm, BFO algorithm, and PSO algorithm. The results for the above three applied algorithms are compared with the upgraded BWO and presented. The proposed algorithm has minimized the output voltage THD to 1.83% at 0.88 modulation index. The developed scheme has been corroborated with the help of MATLAB simulation and the results have been verified through a hardware model developed in laboratory.

1. Introduction

In the present era, power converters are mostly used in power sectors for different applications such as low voltage to high voltage conversion, for sustainable energy conversion and power quality improvement. Power converters for high voltage and high power application are enlightened by multilevel converters. Cascaded inverters have drawn the focus of researchers due to their modularity, less dv/dt stress on device, less use of component, and minimum electromagnetic interference that is discussed in [1]. Cascade H-bridge multilevel inverter (CHBMLI) has been used in different literature studies for high power AC load and grid integration. CHBMLI has been implemented for PV-grid integration with maximum power point tracking presented in [2, 3] as it can provide low ripple content output voltage and current with minimum switching frequency in comparison to conventional two level converter. In order to improve the power quality through MLI, the steps of output voltage waveform are increased which avoids the application of filter circuit and make the system cost effective. But to obtain higher output voltage level, CHBMLI requires

a greater number of switching devices and DC voltage sources. To generate the desired output voltage level with the minimum number of switching devices, reduced MLI with H-bridge structure are proposed in [4, 5]. In the above literature studies, it has been observed that the use of reduced switch MLI has overcome the voltage stress on device at each level and reduces the number of driver circuits which leads to minimum installation area and cost.

In comparison with symmetrical voltage sources-based MLI, the MLIs that are designed with unequal voltage sources require less voltage sources and smaller number of switching devices to develop high level output voltage. Several structures of MLIs with asymmetrical voltage sources of favorable ratios are presented to achieve higher level output voltage with better efficiency [6–9]. In order to obtain more steps across MLI output voltage, number of DC sources is needed to increase. This drawback has been resolved in some developed models [10–15] by connecting series capacitors across a single voltage source. But there is a major concern regarding balancing of DC-link capacitor voltage when the number of series capacitors or storage devices are connected across a single DC source. But in these articles, the rated voltage across the capacitors is maintained without any additional circuits and achieved the higher voltage level across MLI. The MLI fed with single DC source has been developed in addition with isolation through transformer to achieve extensive output voltage level [16,17]. MLI structure is adopted in different research studies to improve power quality or to minimize the distortion due to harmonics content, for which proper switching scheme is needed to develop. Pulse width modulation (PWM) technique is the most commonly used switching technique to operate the MLI in order to reduce the distortion at a desired level. The level-shifted SPWM technique has been employed for determining the specific switching angles to operate the MLI with reduced THD [18]. An advanced PWM scheme for a reduced MLI topology has also been proposed in [19] which has achieved lower output voltage THD than the traditional SPWM technique. But these PWM techniques impose high frequency switching operation of MLI that leads to high switching loss and reduces the overall efficiency. To eliminate the harmonics from the output of a cascaded H-bridge MLI with lower frequency, a selective harmonic current mitigation PWM technique is proposed in [20]. But, to operate the MLI with fundamental frequency, nearest level control (NLC) [21] switching technique is proposed to minimize the distortion of output voltage.

Despite of all the above methods, selective harmonic elimination (SHE) problem through different design of MLI has been solved using evolutionary computing methods such as the genetic algorithm (GA), particle swarm optimization (PSO), modified PSO algorithm, grey wolf optimization (GWO), firefly algorithm [22], and modified firefly algorithm [23]. These search-based algorithms have followed the biological behavior of different organisms to find out the global optima. These algorithms have been implemented in different fields to solve the engineering problems or to optimize the cost function. Rather than increasing the complexity of computing the nonlinear transcendental equations, the SHE problem has been solved by using PSO for CHBMLI, and reduced voltage THD has been achieved in a simpler manner as per [24, 25]. In order to solve the SHE problem with large number of switching angles, a modified species-based PSO algorithm has been proposed in [26]. For achieving the optimum result with a faster convergence rate, the conventional PSO has been modified and presented in [27]. In the presented literature, the author has minimized the output voltage THD to 11.81% by eliminating the lower order harmonics through a proposed 7-level MLI. Similarly, another bio-inspired metaheuristic algorithm known as grey wolf optimization (GWO) is presented in a modified form to determine the optimum switching angles for a hybrid cascaded MLI [28]. In this research, it has been demonstrated that the modified GWO has provided improved result in contrast to the conventional one. Apart from this, modified GA and modified PSO algorithm are employed in [29, 30], respectively, to determine the optimum switching angles of different MLI topology. But PSO algorithm requires more than one variable to solve the optimization problem, and in case of GWO, a greater number of tuning parameters are required to achieve the convergence. The SHE problem of MLI for different modulation indices has also been solved by differential harmony search algorithm [31] and improved immune algorithm [32]. Furthermore, the nature inspired algorithms have proved their potential towards solving the optimal operation of microgrid by employing GA and artificial bee colony together in [33], solving the economic dispatch problem using hybrid firefly and genetic algorithm [34], frequency control of microgrid by optimizing the controller coefficient through PSO in reference [35], selection of optimal path for cluster microgrid through modified Dijkstra algorithm [36], and determining the optimal path to find out electric vehicle charging station with the help of wild horse optimization technique [37].

In this paper, a converter controlled cascaded reduced MLI is presented. This MLI topology has been proposed in [4] with symmetrical voltage sources which require higher power switches to develop higher level output voltage. The major contributions of the paper are presented as follows:

(1) The presented MLI is designed with unequal DC sources to develop higher output voltage level with minimum number of power devices and driver circuits which reduce MLI power loss, installation, and system cost as well.

(2) An isolated DC-DC converter with multiple secondary windings is designed to provide the desired DC voltages for reduced MLI from a single source. This isolated converter operates with high frequency of 10 kHz and uses a single semiconductor device to provide the isolation between source and load.

(3) This topology does not use additional capacitors and diodes than the presented 15-level CSMLI [38].

(4) To minimize the output voltage THD, the preferable switching angles for the developed MLI, upgraded/modified black widow optimization algorithm has been proposed in this paper. In the proposed algorithm, the mutation process that presented in the conventional BWO algorithm [39] has been

eliminated and the optimum result has been achieved by updating the population vector with less time of operation, which has been explained in Section 3. The proposed algorithm has proved its efficiency in solving the THD minimization problem of the reduced MLI.

(5) The effectiveness and performance of the proposed algorithm have been determined by the comparative study and statistical analysis with other existing population-based algorithms such as GA, BFOA, and PSO which have been presented in Section 4.

The converter-based 15-level reduced MLI is simulated, and the results are verified by developing a prototype in laboratory. The simulation and experimental results for the presented design with the modified BWO algorithm are tendered briefly in Sections 4 and 5, respectively.

2. Proposed Scheme

This research paper has focused on generating multilevel AC output voltage from reduced switch count MLI using a single DC source voltage. The use of DC-DC isolated converter with multisecondary winding has provided the proper isolation between AC load and DC source voltage and diminishes the use of larger number of DC voltage sources that leads to minimize the cost of the system. In order to reduce the harmonics content and to obtain the preferable switching angles for reduced MLI, the modified BWO algorithm is presented. The presented MLI is operated under fundamental frequency in order to reduce the switching loss which reduces the requirement of heat sink and makes the system cost effective as per [40]. The developed design for a three-phase reduced MLI is shown in Figure 1.

2.1. Operation of Asymmetrical Reduced Multilevel Inverter. As shown in Figure 1, the presented converter is modified with multiple secondary windings to generate multiple DC sources for asymmetrical reduced MLI from a single input with appropriate isolation. The converter is operated under high frequency, and by setting the proper turns ratio, varying DC voltages of desired value can be obtained across secondary windings. The output voltage of the isolated converter can be expressed as

$$V_o = \mathrm{KDV}_D, \tag{1}$$

where K is the transformation ratio and D is the duty ratio of the converter. Here, D is set to 0.5 and K values for three secondary windings are set to 2 : 4 : 8 in order to obtain the secondary voltage of ratio 1 : 2 : 4. The relation that satisfies the above is described as follows:

$$\frac{N4}{N1} = 2,$$

$$\frac{N3}{N1} = 4, \tag{2}$$

$$\frac{N2}{N1} = 8.$$

Applying the value of K from equation (2), the secondary voltages relation with respect to primary as shown in Figure 1 will be

$$\begin{aligned} Vo1 &= V_{\mathrm{DA}}, \\ Vo2 &= 2 * V_{\mathrm{DA}}, \\ Vo3 &= 4 * V_{\mathrm{DA}}. \end{aligned} \tag{3}$$

The unequal DC voltages are fed to the reduced multilevel inverter for its operation as demonstrated in Figure 1.

In this research, the MLI is powered by unequal DC sources to develop higher output voltage level than the presented topology [4]. This topology of MLI with equal and unequal voltage sources has exhibited a relation of output voltage level (Vnl) with number of DC voltage sources (Sn) given by equations (4) and (5), respectively.

$$V_{\mathrm{nl}} = (2 * S_n) + 1, \tag{4}$$

$$V_{\mathrm{nl}} = 2^{S_n+1} - 1. \tag{5}$$

Here, a 15-level MLI with ten semiconductor switches is utilized for a three phase system with enhanced power quality. The schematic diagram for phase A, phase B, and Phase C has been represented in Figure 1. The structural diagram for the single phase reduced MLI is displayed in Figure 2. Here, in the reduced structure, a single voltage source is accompanied with two power switches which are connected to H-bridge for generating positive and negative cycle voltage. The requirement of semiconductor switches for Sn number of voltage sources can be determined by

$$n_s = (2 * S_n) + 4. \tag{6}$$

To generate the 15-level stair case output voltage waveform shown in Figure 2(b), the switching pattern for each semiconductor device is illustrated by Table 1.

For obtaining each voltage, level 5 switches are operating at a stretch. In order to explain the MLI operation as per Table 1, 7 modes for positive half cycle are manifested in Figure 3.

As discussed in Section 2.1, the three input voltages applied to the reduced MLI are maintained at a ratio of 1 : 2 : 4 (Vo1 : Vo2 : Vo3) to attain 15-level output voltage across load. In mode 1 as shown in Figure 3(a), the MLI has generated voltage Vo1 across the RL load, in mode 2 voltage Vo2, in mode 3 voltage (Vo1 + Vo2), in mode 4 voltage Vo3, in mode 5 voltage (Vo3 + Vo1), in mode 6 voltage (Vo2 + Vo3), and in mode 7 voltage (Vo1 + Vo2 + Vo3), and is appeared across the load. The flow of current in the circuit at each mode is marked with arrow as shown in Figure 3. Likewise, negative half cycle voltage can be developed using the switching pattern shown in Table 1. Expression of quarter wave symmetry output voltage waveform as shown in Figure 3 can be determined by Fourier analysis. In this paper, the reduced MLI is operated with unequal voltage sources, but from the voltage waveform, it can be observed that the voltage value at each step is equal. Thus, the voltage expression for each phase can be determined by

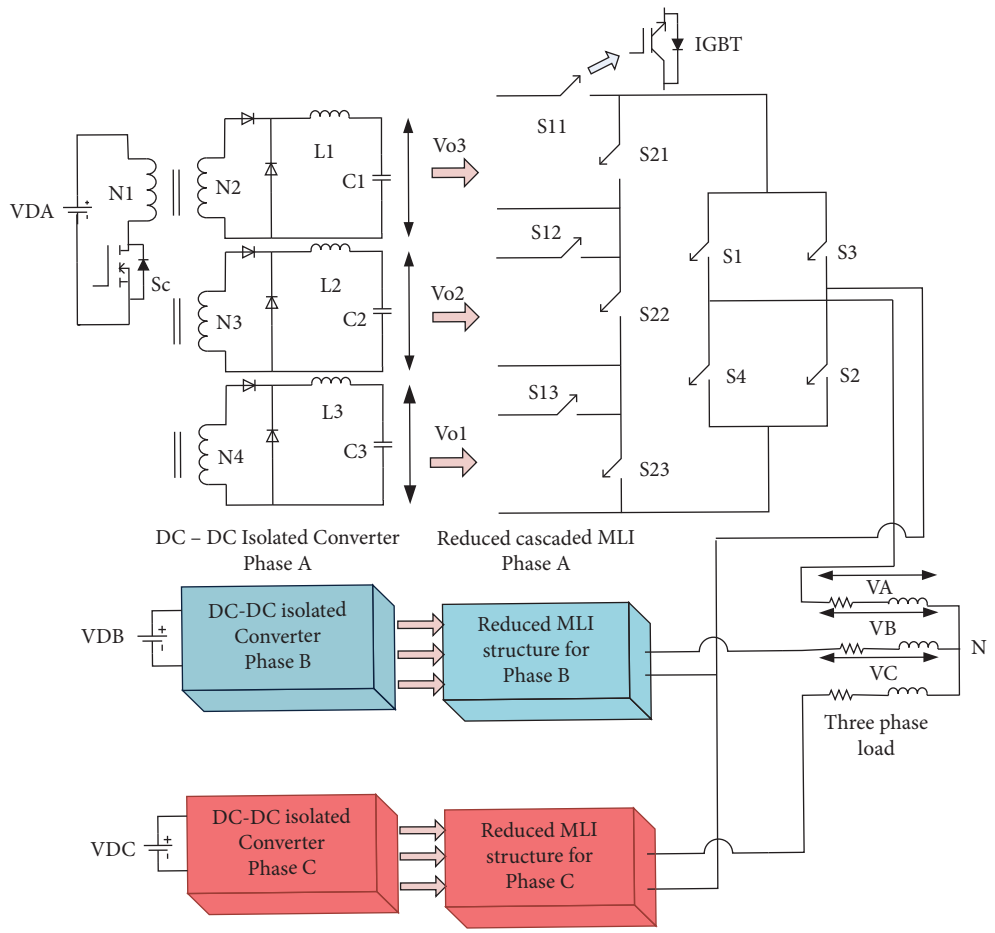


FIGURE 1: Developed converter-based reduced MLI for a three phase system.

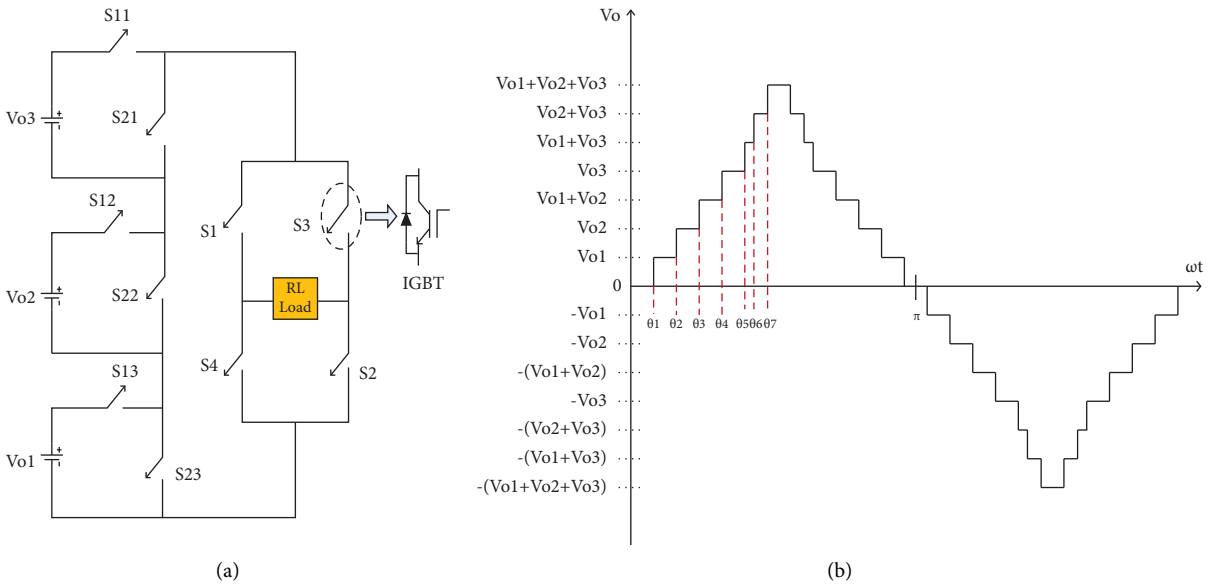


FIGURE 2: (a) Circuit diagram of a single phase 15-level reduced cascaded MLI. (b) Voltage waveform of a 15-level MLI with disparate voltage sources.

Table 1: Switching states of reduced cascaded MLI power devices.

	Switching state for the 15-level reduced MLI													
Switches	Vo1	Vo2	Vo2 + Vo1	Vo3	Vo1 + Vo3	Vo2 + Vo3	Vo1 + Vo2 + Vo3	-Vo1	-Vo2	-(Vo2 + Vo1)	-Vo3	-(Vo1 + Vo3)	-(Vo2 + Vo3)	-(Vo1 + Vo2 + Vo3)
S1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
S2	1	1	1	1	1	1	1	0	0	0	0	0	0	0
S3	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S4	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S11	0	0	0	1	1	1	1	0	0	0	1	1	1	1
S12	0	1	1	0	0	1	1	0	1	1	0	0	1	1
S13	1	0	1	0	1	0	1	1	0	1	0	1	0	1
S21	1	1	1	0	0	0	0	1	1	1	0	0	0	0
S22	1	0	0	1	1	0	0	1	0	0	1	1	0	0
S23	0	1	0	1	0	1	0	0	1	0	1	0	1	0

"0" implies to turn off state and "1" implies to turn on state of a particular switch.

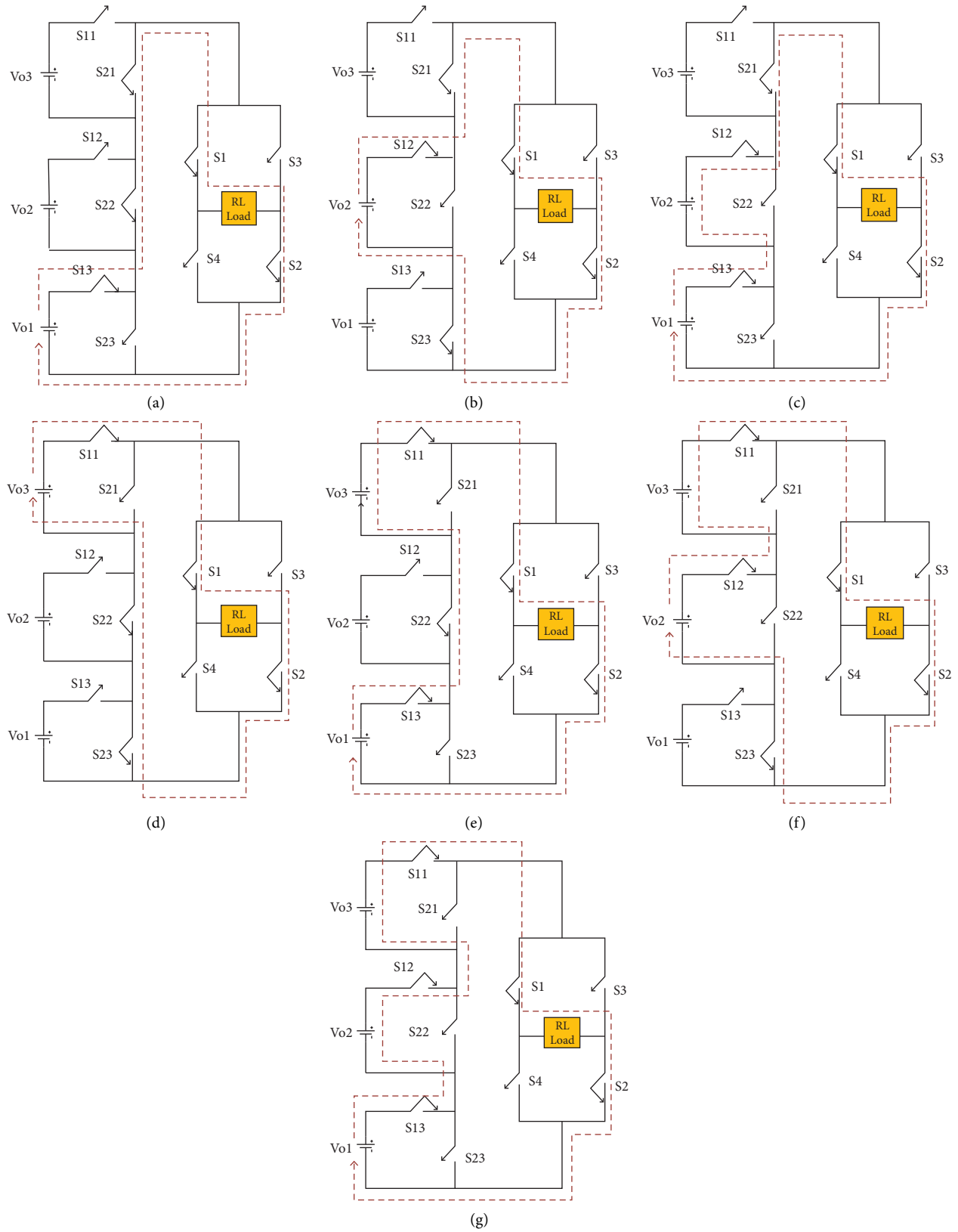


Figure 3: (a) Mode 1 operation, (b) mode 2 operation, (c) mode 3 operation, (d) mode 4 operation, (e) mode 5 operation, (f) mode 6 operation, and (g) mode 7 operation.

$$V(\omega t) = \sum_{\theta=1}^{i} \frac{4V_o}{n\pi} \left(\cos(n\theta_1) + \cos(n\theta_2) + , \ldots , \cos(n\theta_i)\sin(n\omega t)\right). \tag{7}$$

Harmonic content in the output voltage of the above equation is symbolised by "n" and "i" is the number of switching angles of reduced MLI. The above equation describes that the fundamental voltage as well as nth order harmonic voltages are dependent on the switching angles of the reduced MLI. Total harmonic distortion of output voltage that needs to minimize is determined by the following equation:

$$\text{THD} = \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1}. \tag{8}$$

To solve this optimization problem, desirable switching angles for the reduced MLI are obtained using modified BWO algorithm. The switching angles must bear the following relation and lower and upper bounds are set to 00 and 900, respectively.

$$0 < \theta 1 < \theta 2 < \theta 3 < \theta 4 < \theta 5 < \theta 6 < \theta 7 < \frac{\pi}{2}. \tag{9}$$

2.2. Efficiency Analysis of the Asymmetrical Reduced MLI. Efficiency of the multilevel inverter can be determined from the power loss calculation. In this article, the efficiency of asymmetrical reduced MLI has been calculated over different output power and compared with the symmetrical one [4]. The power loss of the converter depends on the switching loss and conduction loss of each switch during its operation. The conduction loss of a power device can be determined by the following:

$$P_{\text{cl}} = \frac{1}{T} \int_{T_{01}}^{T_{02}} \left[V_T + V_D + \alpha I(t)\left(r_T + r_D\right)\right] I(t)\text{d}t, \tag{10}$$

where "T" is the total time period, T01 to T02 is the conduction period of the switch, and "α" is the gain constant of the switch. The conduction loss for a 260 watt single phase reduced MLI is calculated by considering the switching duration of each power device as per Table 1. The instantaneous current is 0.5 A. The total conduction loss of 10 switches is calculated to 5.046 watt.

The switching loss of the power device can be obtained by the following:

$$P_{\text{sl}} = \frac{1}{T}\left[E_N N_N + E_O N_O\right], \tag{11}$$

where the on state and off state energy losses of a switch are denoted by EN and EO, respectively, which can be derived as follows:

$$\begin{aligned} E_N &= \frac{1}{6}\left[V_s I_s T_N\right], \\ E_O &= \frac{1}{6}\left[V_s I_s T_O\right]. \end{aligned} \tag{12}$$

TN and TO represent the number of times a power device is getting turn on and turn off respectively. The voltage across a power device before it is getting on or after it is getting off is given by Vs and the current across the device after switching on or before switching it off is given by Is. From equations (11) and (12), the switching loss of the MLI is calculated to 0.476 watt after putting the different parameter values from the datasheet of the power device.

The total power loss of a switching device is obtained from the summation of conduction loss and switching loss which is 5.516 watt. The efficiency of the MLI is determined by

$$\eta\% = \frac{\text{output power}}{\text{output power} + \text{total power loss of MLI}} * 100. \tag{13}$$

Efficiency of the 260 watt converter is 96.36%. The proposed reduced switch MLI is an improvement on the MLI topology shown in [4]. Thus, to determine the effectiveness of the proposed asymmetrical reduced switch MLI over some existing topologies, the efficiency comparison at different output power level is shown in Figure 4.

3. Modified Black Widow Optimization Algorithm

A new metaheuristic algorithm known as black widow optimization has been proposed by V. Hayyolalam and A. P. Kazem in the year 2020 to solve the real world problem. The mating process of black widow spider and reproduction of their offspring has been mimicked to develop this algorithm. This algorithm has set a benchmark for solving real engineering problem with a greater accuracy as discussed in reference [39].

In order to find out the global optima, the BWO algorithm has proved its efficiency in comparison to other existing population-based algorithms. This algorithm has been initialized by randomly assigning the population of spider or widow. The assigned population is divided into two groups of parents. The reproduction is started by the mating process in between the pair of parents and as per the biological nature of black widow spider; the male spider is consumed by the female spider during mating or after mating. The spider babies are reproduced, where stronger babies are survived and the rest are consumed by the stronger group. The equations are developed for generation of new offspring.

$$\begin{aligned} \text{off}_1 &= A * \text{par}_1 + (1 - A) * \text{par}_2, \\ \text{off}_2 &= A * \text{par}_2 + (1 - A) * \text{par}_1, \end{aligned} \tag{14}$$

where par_1 and par_2 are treated as two groups of parents and "A" is the randomly generated array with the same length of parents. In order to achieve the better convergence, the BWO algorithm is modified with updating the population. After reproduction of new offspring, the stronger offspring group is kept and the rest are discarded. The population is now updated using the following equation:

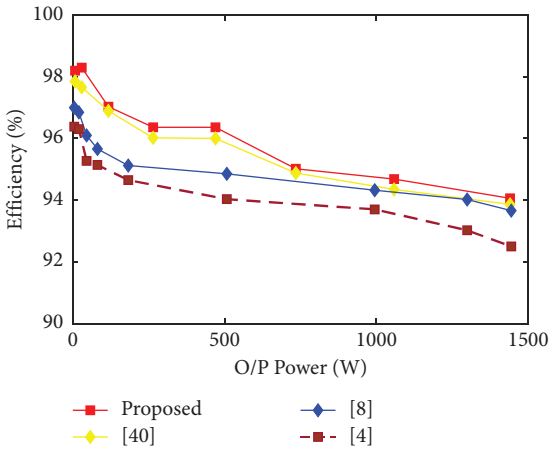


Figure 4: Efficiency comparative study of different topology.

$$BW_{new} = BW_{old} + [\beta(off_{best} - BW_{old}) - off_{worst}], \quad (15)$$

where BW_{new} is the updated population, off_{best} is the strongest population among the offspring, off_{worst} is the weakest child generated from the reproduction, and "β" is the random number between 0 and 1. Here, the mutation process has been dropped to reduce the step size of the algorithm. Developing the new population from the best and worst child is introduced in this research work to solve the optimization problem with faster convergence rate.

3.1. Application of Modified BWO Algorithm in the Presented Scheme. To achieve minimum voltage THD of reduced MLI, the suitable triggering angles for the MLI need to be obtained. Here, the angles are treated as the population or widow that needs to initialize between 0 to $\pi/2$. A population matrix of $[k \times i]$ is generated for the mating and reproduction process as discussed in Section 3. To obtain the best solution and global optima, the following steps are carried out. The flowchart of the proposed algorithm is shown in Figure 5.

Steps:

(a) Initially, maximum iteration number and reproduction rate are assigned.

(b) The population or triggering angle matrix is denoted by "BW" of size $[k \times i]$, where "i" vector is generated randomly from 0 to $\pi/2$.

(c) In this step, the fitness function is calculated for each set of population (triggering angles) using the following equation:

$$f = \min \frac{\sqrt{\sum_{n=3,5\ldots}^{49} V_n^2}}{V_1}. \quad (16)$$

(d) Based on the fitness function values, the stronger population is selected.

(e) The reproduction is started in this step. Two parents' groups are selected from the stronger population and the offspring are generated using equation (14). From the offspring, the stronger offspring group is selected based on their fitness value and rest are destroyed.

(f) Now the population is updated using equation (15).

(g) The best solution from new population is derived and recorded.

(h) Termination condition is checked. If the maximum iteration is occurred, then the entire process is stopped or returns to step 5.

The performance of the modified BWO algorithm for solving THD minimization problem is demonstrated through MATLAB program which has been implemented further in the MATLAB simulation to verify the result. The efficiency of the above algorithm has been substantiated through comparison analysis with the existing bio-inspired algorithms that are shown in Section 4.

4. Simulation Result Analysis with Comparative Study

A converter-based three-phase cascaded reduced MLI is simulated in MATLAB 2016b to verify the productivity of the proposed scheme with the proposed algorithm. A single voltage source of 100 volts is applied to energise the reduced MLI through an isolated converter in each phase. The converter parameter, MLI line voltage, and load current values are given in Table 2. The suitable triggering angles for MLI operation are derived using the proposed modified BWO algorithm to minimize output voltage THD. The MLI is also simulated with the triggering angles which are derived from the GA, BFOA, and PSO in order to determine the output voltage THD and the nth order harmonic contents in it. The triggering angles for each algorithm and the respective voltage THD with the number of tuning variables are cited in Table 3. The performance of MBWO for solving THD optimization problem is compared with the GA, BFOA, and PSO and cited in Table 4.

The converter output voltage waveforms are displayed in Figure 6. The single phase output voltage, line voltage, and load current waveforms at 0.98 power factor are shown in Figure 7.

The FFT analysis has been conducted for different loading conditions to demonstrate the voltage and current THD. The details are described in Figure 8.

From Figure 8, it is observed that the proposed algorithm has reduced the THD of line voltage and load current effectively under varying load conditions.

From the simulation result, nth order harmonic voltages with respect to being fundamental in percentage for the implemented algorithms are demonstrated and cited in Figure 8.

According to Figure 9, modified BWO provides the lowest voltage THD in comparison to other existing algorithms and also diminishes successfully the higher and lower order harmonic voltages from the output. The lowest THD in each algorithm is achieved with a modulation index of 0.86 to 0.88. The variation of THD with respect to

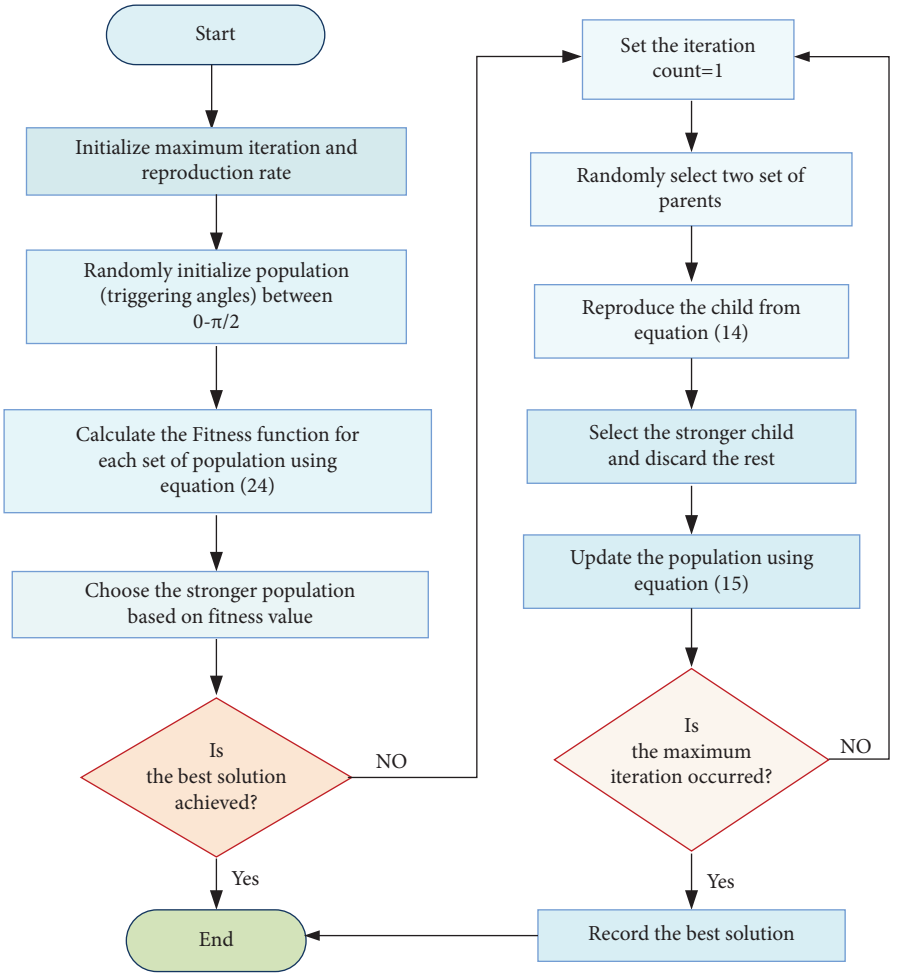


Figure 5: Flowchart diagram of modified BWO algorithm.

Table 2: Simulation parameter and output result.

Simulation parameters		Values
Converter parameter	VDA	100 volts
	Vo1	96 volts
	Vo2	193 volts
	Vo3	387 volts
	L1, L2, L3	5 mH
	C1, C2, C3	1000 μF
MLI parameter	Line voltage (RMS)	906.3 volts
	Load current (RMS)	0.522 A
	RL load (per phase)	1000 Ω, 500 mH

Table 3: Developed switching angles to result in minimum voltage THD for applied algorithms.

Algorithm	THD (%)	Desired switching angles (degree)							Harmonic contents						Required tuning variables
		$\theta 1$	$\theta 2$	$\theta 3$	$\theta 4$	$\theta 5$	$\theta 6$	$\theta 7$	5^{th} order	7^{th} order	11^{th} order	13^{th} order	17^{th} order	19^{th} order	
BFOA	2.86	1.1	8.26	8.9	16.5	17.95	25.6	38.53	1.85%	0.12%	0.68%	0.41%	0.56%	0.6%	3
GA	3.6	1	6.18	8.4	15.33	15.8	32.65	42.98	0.37%	1.4%	1.52%	1.32%	0.74%	1.02%	3
PSO	2.4	1	7.91	11	16.27	26.01	30.63	41.36	0.31%	0.2%	0.9%	0.16%	0.65%	0.34%	4
MBWO	1.83	4.8	9.24	14	21.7	29.77	38.88	58.31	0.3%	0.21%	0.49%	0.07%	0.57%	0.28%	2

Table 4: Performance analysis of MBWO in comparison with GA, BFOA, and PSO.

	GA	BFOA	PSO	MBWO
Output voltage level	15	15	15	15
Computational time	0.74 sec	1.56 sec	0.36 sec	0.32 sec
Computational complexity	High	High	Low	Low
Accuracy	Medium	Medium	High	High
Capability to tackle local minima	Low	Medium	Medium	High
Convergence speed	Low	Low	High	High

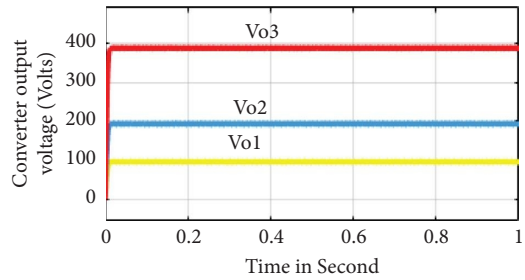


Figure 6: Isolated converter output voltages with respect to time.

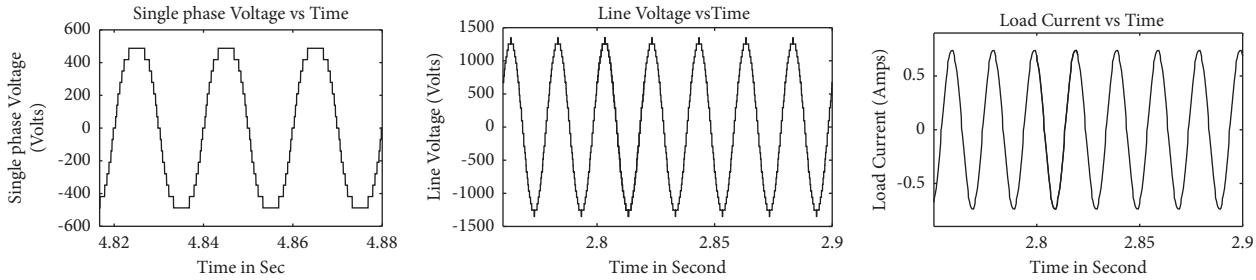


Figure 7: MLI output waveforms: (a) single phase output voltage with respect to time, (b) line voltage with respect to time, and (c) load current with respect to time.

modulation index and comparison analysis of GA, BFOA, and PSO with the modified BWO algorithm in different measures are shown in Figure 10. In addition to this, the THD obtained for the range of the above modulation index by the newly proposed algorithms such as the asynchronous particle swarm optimization-genetic algorithm [41] and opposition-based quantum bat algorithm [42] is 11.47% for 7 level MLI and 4.05% for 17 level MLI, respectively.

Figure 10(a) shows the variation of voltage THD with different modulation indices, and in each modulation index, MBWO has resulted in the lowest voltage THD than other algorithms. The THD at the maximum modulation index of 0.97 has been measured and recorded. At this modulation index, the minimum THD achieved by MBWO is 5.6% and the output voltage THD achieved by PSO, BFOA, and GA is 0.6%, 5.9%, and 6.4%, respectively. Figure 10(b) has shown the nth order harmonic voltages magnitude with respect to fundamental, where it verifies MBWO has suppressed the lower and higher order harmonics prominently in comparison to other three algorithms. Figure 10(c) verifies that MBWO converges faster at each set iteration count than other applied algorithms. Figure 10(d) shows the variation of fitness function with different population size through box plot analysis, which implies that MBWO generates lower value of fitness function with different population size in comparison to the other algorithms. Figure 10(e) shows the range of fitness function value that can vary for different set value of maximum iteration. This proves MBWO generates minimum THD at each iteration which lies below 5%. The productivity of the proposed algorithm using asymmetrical reduced MLI has been determined by the comparative study with the existing switching techniques which are presented in Table 5.

5. Experimental Results

An experimental set up for a 15-level converter-based, cascaded, and reduced MLI is carried out to verify the result obtained from the simulation. The gate pulses for the MLI are generated through ten isolated driver circuits with the help of 18F452 microcontroller and TLP250H optocoupler. The input DC voltages for MLI circuit are developed from a multiwinding isolated converter charged with a 12 volts

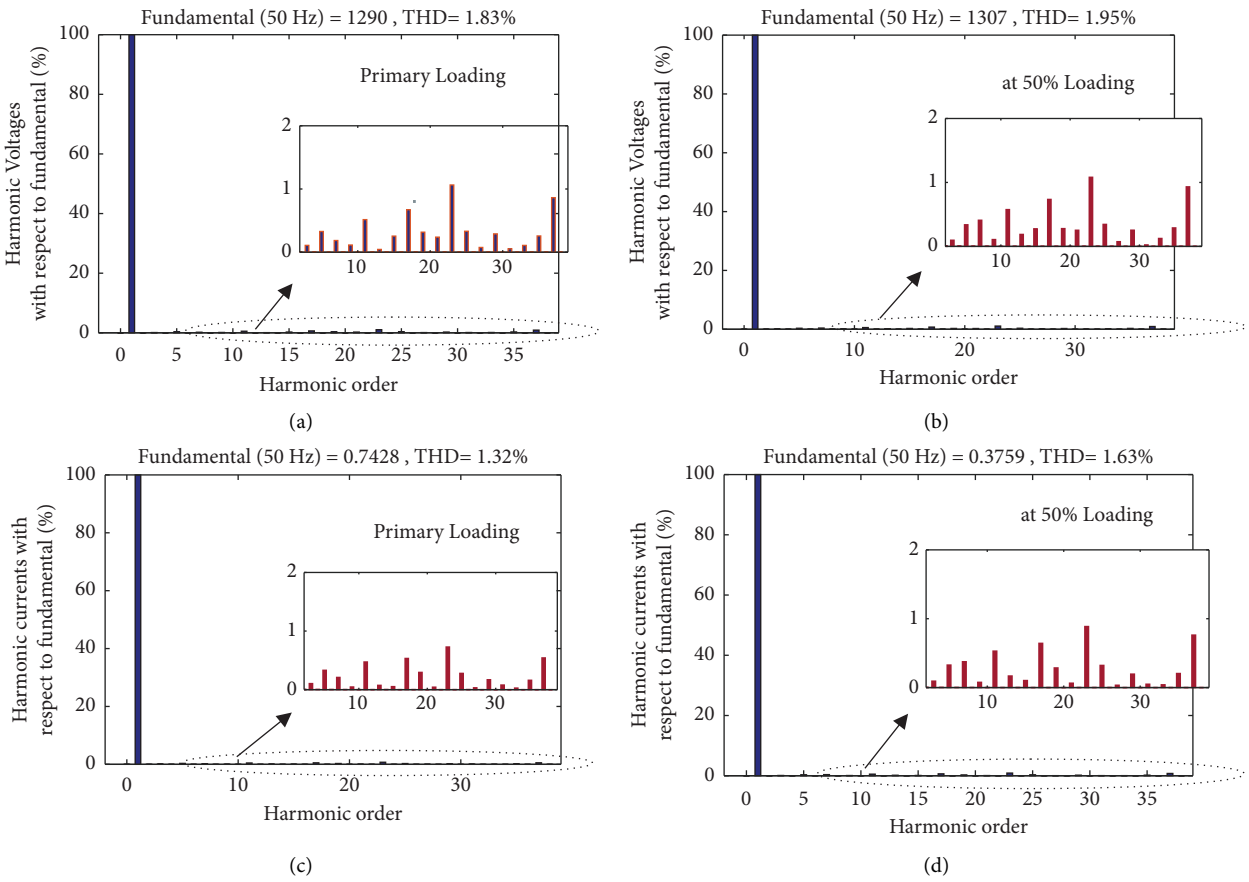


FIGURE 8: (a) FFT analysis graph of line voltage in primary loading. (b) FFT analysis graph of line voltage when loading is doubled. (c) FFT analysis graph of load current in primary loading. (d) FFT analysis graph of load current when loading is doubled.

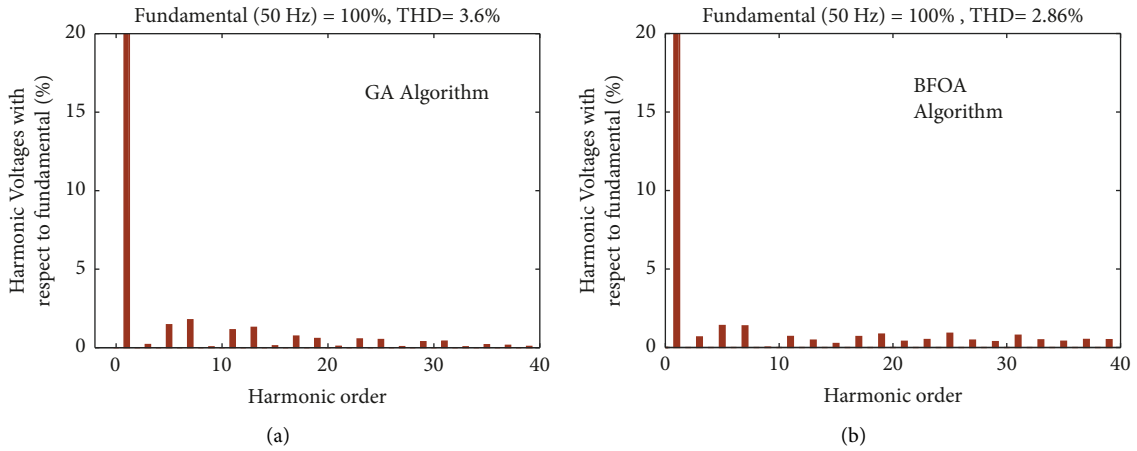


FIGURE 9: Continued.

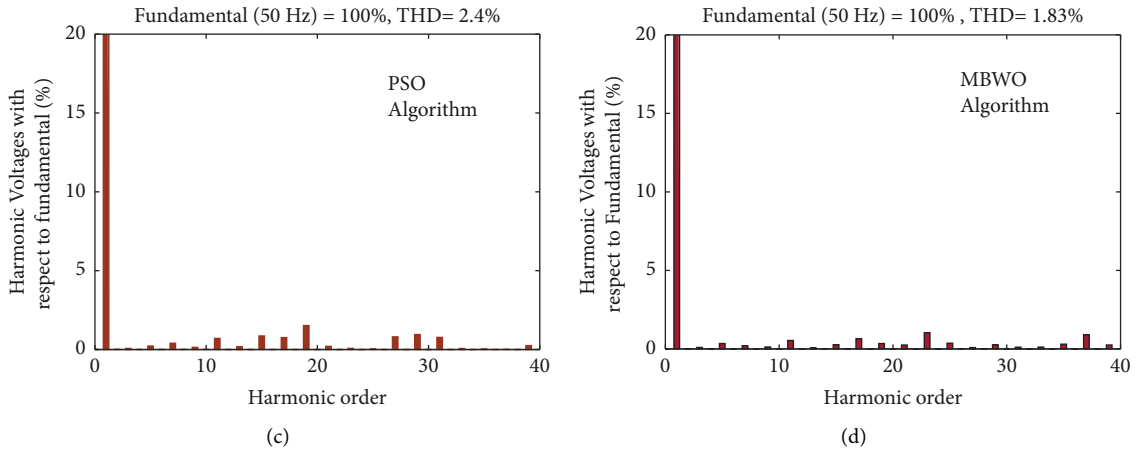


Figure 9: (a) Harmonic content in output voltage for GA algorithm. (b) Harmonic content in output voltage for BFOA. (c) Harmonic content in output voltage for PSO algorithm. (d) Harmonic content in output voltage for modified BWO algorithm.

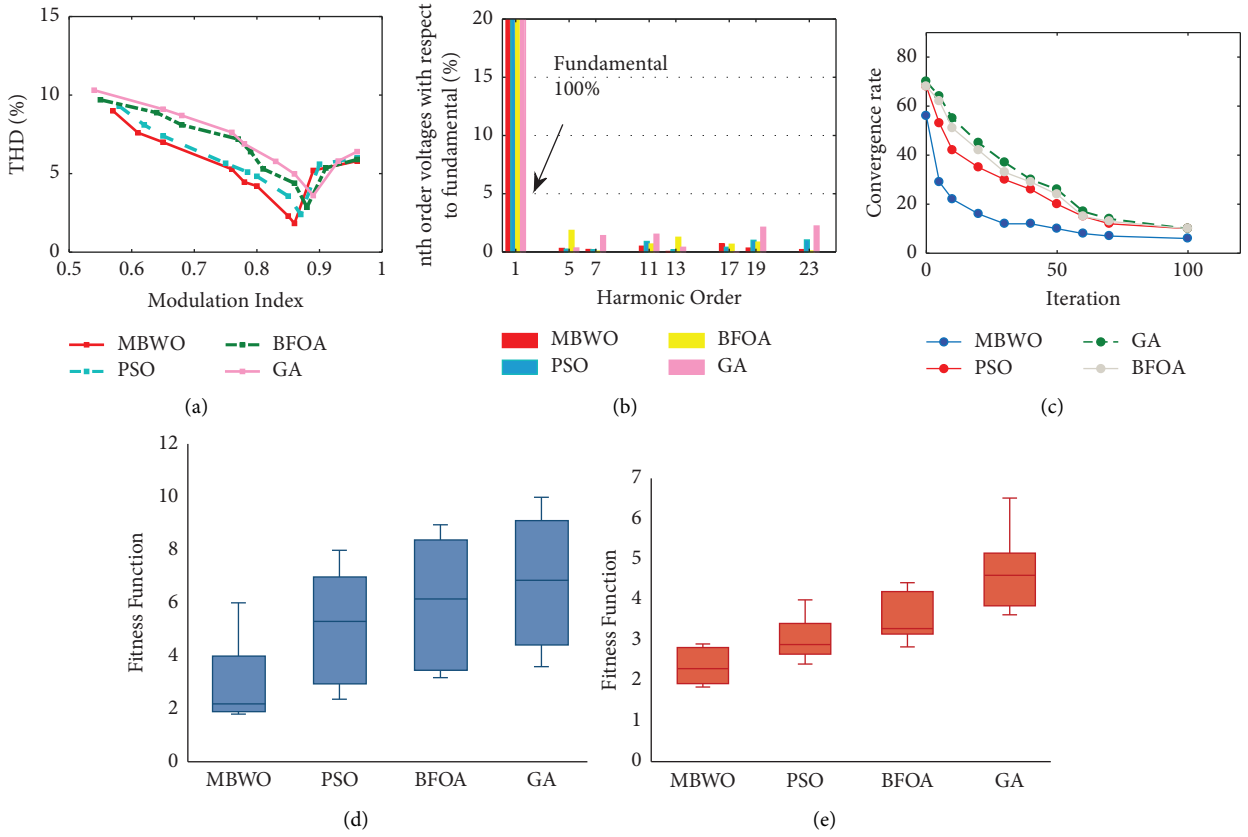


Figure 10: (a) Modulation index vs. THD, (b) harmonic order vs. nth order voltage with respect to fundamental, (c) iteration count vs. convergence rate, (d) box plot of fitness function value based on population size, and (e) box plot of fitness function value based on maximum iteration (for GA, BFOA, PSO, and modified BWO algorithm).

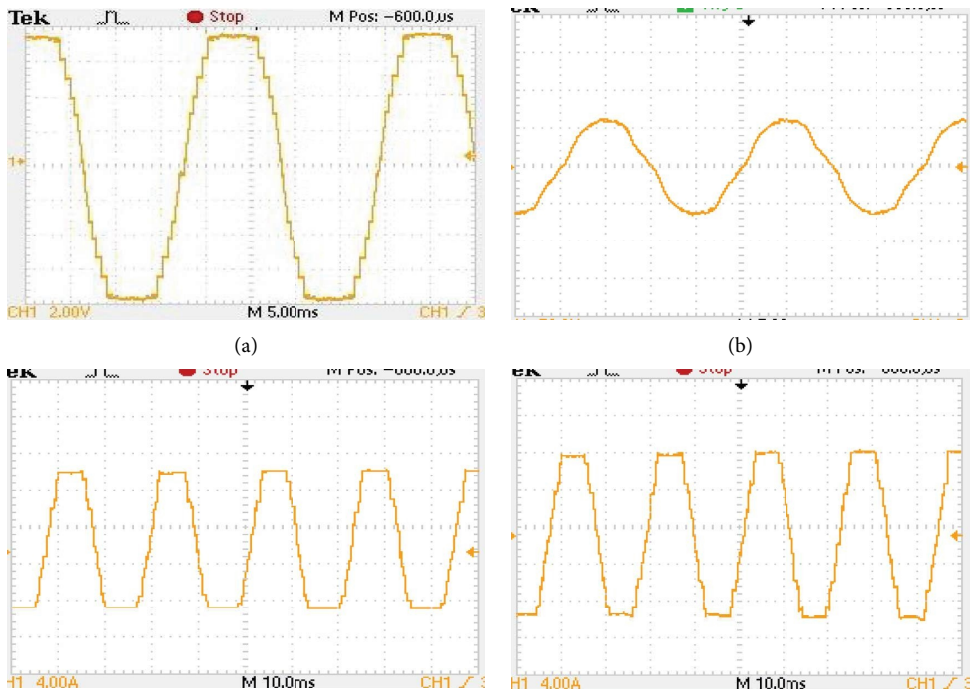
DC supply. The component details are provided in Table 6. MLI output voltage and current with varying load condition are recorded in a DSO of model no. TDS 2022B and are shown in Figure 11. Output voltage and current harmonics spectrum with a modulation index of 0.88 for modified BWO algorithm are also recorded and shown in Figure 12, and the experimental set up is shown in Figure 13.

Table 5: Comparative study of MBWO switching algorithm with existing switching schemes.

References	O/P voltage level	Power switches	Switching techniques	O/P voltage THD (%)
[4]	9	10	Fundamental frequency switching	5.20
[5]	11	11	PWM	9.07
[6]	13	10	Fundamental frequency switching	3.50
[7]	21	10	Fundamental sine quantized switching techniques	3.65
[10]	17	13	NLC modulation	5.15
[12]	15	32	SPWM	7.60
[25]	9	16	PSO	5.44
[27]	7	6 + 2 diodes	Modified PSO	11.81
[28]	11	12	Modified GWO	5.54
[43]	9	8	Honey badger optimization	2.48
[44]	7	12	SHEPWM based on Walsh function	8.84
Proposed	15	10	MBWO	1.83

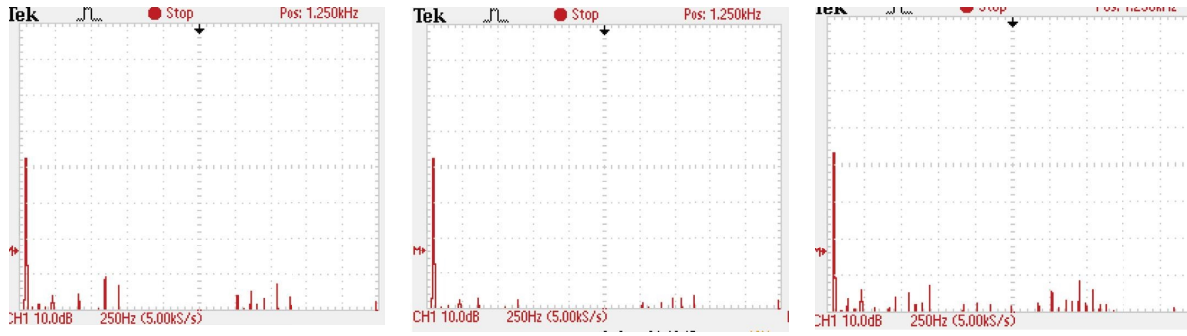
Table 6: Hardware component list.

SI no.	Components	
1	Optocoupler (driver circuit)	TLP250H
2	Microcontroller	PIC18f452
3	IGBT	IE15AB
4	Load	$R = 100\ \Omega$, $L = 35$ mH
5	Isolated converter	Series inductor $L1 = 5$ mH, capacitor = 1000 μF, power MOSFET (IRF740)



(a) (b) (c) (d)

Figure 11: (a) MLI output voltage at a constant load. (b) Load current with RL load. (c) Load current (R load) at a constant load. (d) Load current (R load) at 50% reduction of resistance in load ((scale: for figure (a) channel 1: Y axis = 35.47 V/div), (scale: for figure (b) channel 1: Y axis = 0.56 A/div), (scale: for figure (c, d) channel 1: Y axis = 0.375 A/div)).



(a) (b) (c)

Figure 12: (a) Harmonic spectrum analysis of output voltage, (b) harmonic spectrum analysis of load current (RL load), (c) harmonic spectrum analysis of load current (R load) (scale: for figure (a–c) channel 1: X axis = 250 Hz/div).

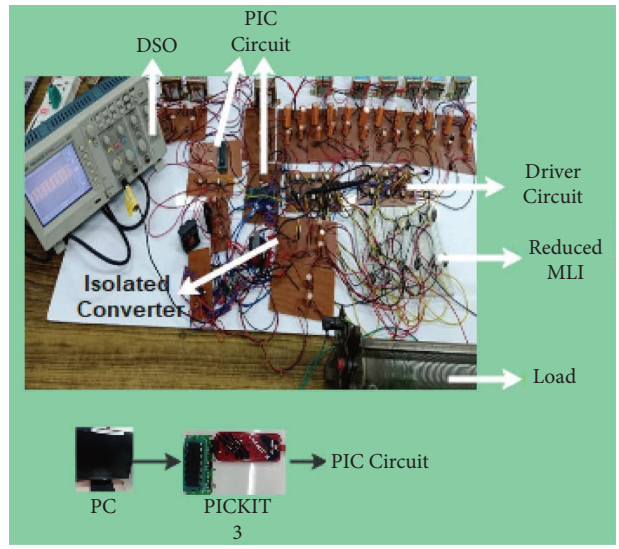


Figure 13: Developed prototype in laboratory.

6. Conclusion

A single DC source-based reduced switch count 15-level MLI is presented with minimum voltage distortion in this paper. The use of isolated converter avoids multiple sources for MLI operation which makes the system frugal. To generate the 15-level output voltage, the reduced MLI is powered with three unequal DC voltage sources of ratio 1 : 2 : 4 generated from three secondary windings of isolated DC-DC converter. The use of unequal DC sources results in higher level output voltage with minimum number of switching devices than the equal one. The MLI operation is carried out with fundamental frequency which has reduced the switching stress and increased the MLI efficiency. The presented scheme is developed for 3 phases with RL load to demonstrate the result and converter efficiency. The harmonic content in the output voltage and load current is minimized much lower from the standard set by IEEE-519 by the proposed modified BWO algorithm. From the FFT analysis graph in different loading conditions, the modified BWO algorithm has proved its potential to solve the optimization problem in a multidimensional searching space. From the comparative study with other nature inspired algorithms, the modified BWO has achieved the minimum THD with better convergence rate and minimum tuning parameters. The best minimized value of voltage THD has been obtained by the modified BWO algorithm because of its dodging characteristics from the local optima. The presented scheme operation with the proposed algorithm is validated through MATLAB simulation and experimental prototype. This MLI scheme with the proposed switching technique can be implemented in different industrial applications of different ratings.

Nomenclature

MLI:	Multilevel inverter
THD:	Total harmonic distortion
BWO:	Black widow optimization
BFO:	Bacterial foraging optimization
PSO:	Particle swarm optimization
GA:	Genetic algorithm

D: Duty ratio of isolated converter
K: Transformation ratio of isolated converter
V_{nL}: Output voltage level of multilevel inverter
S_n: Number of DC voltage sources
n_s: Number of semiconductor switches
n: nth order harmonic content
in: Number of switching angles
V_o: Reference DC voltage
$\theta 1$, $\theta 2$, ... $\theta 7$: Switching angles
f: Fitness function
Pcl: Conduction loss of the switch
V_T: On state voltage drop across transistor
V_D: On state voltage drop across reverse conducting diode
r_T: Resistance of transistor
r_D: Resistance of reverse conducting diode
$I(t)$: Instantaneous current across the power device
η: Efficiency of the MLI.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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