Hindawi
International Transactions on Electrical Energy Systems
Volume 2023, Article ID 8794874, 18 pages
https://doi.org/10.1155/2023/8794874

Research Article

Experimental Implementation of Cascaded H-Bridge Multilevel Inverter with an Improved Reliability for Solar PV Applications

C. Dhanamjayulu and T. Girijaprasanna

School of Electrical Engineering, Vellore Institute of Technology, Vellore, India

Correspondence should be addressed to C. Dhanamjayulu; dhanamjayulu.c@vit.ac.in

Received 18 August 2022; Revised 4 January 2023; Accepted 13 April 2023; Published 28 April 2023

Academic Editor: Murthy Cherukuri

This study presents the boost converter-based cascaded H-bridge (CHB) multilevel inverter with improved reliability for solar PV (photovoltaic) applications. The solar PV is associated with the boost converter to enhance DC link voltage by using the maximum power point tracking-perturb and observe (MPPT-P & O) technique. The proposed configuration is aimed toward the performance analysis of the boost converter-based CHB MLI by reducing the number of components, low total harmonic distortion (THD), reduced power, less cost function, low total standing voltage (TSV), improved reliability, and switching losses for solar PV application. In this study, a CHB multilevel inverter is used to obtain stepped pure sinusoidal AC from the solar PV array. The proposed boost converter extracts maximum power and enhances higher DC link voltage which provides high efficiency. The boost converter is integrated with a 27-level CHB multilevel inverter to generate near-sinusoidal output voltage with lower THD. The inverter is tested with linear and nonlinear loads for robustness, and during dynamic loads, inverter is stable and well suited to grid-connected applications. A detailed comparison is presented on the component count and reliability aspects with existing MLIs and 27-level MLIs. The simulation outcomes of the implemented arrangement are presented with the help of MATLAB/Simulink, an experimental prototype is developed using a dSPACE RTI1104 controller and also tested in the research laboratory for checking the possibility of the implemented arrangement.

1. Introduction

There must be situated worldwide creativities in favor of the elevation of independent renewable energy schemes. This creativity has run for the growth of renewable power-producing systems that remain accomplished in giving self-sufficient power production with the help of additional standalone renewable energy sources (RES) [1, 2]. The further most usually used hybrid RES is the wind in addition to solar power [3, 4]. These two RES remain irregular; consequently, the utilization of ESS (energy storage system) is typical within stand-governing submissions [5, 6]. The hybrid renewable energy schemes are having some controlling methods which offer a resourceful transfer of power. An approach to the energy translation arrangement as well as converters has various demerits at several stages in the system; this is to be implemented with a lot of technical concentration and investigation in this part [7–9]. Henceforth, there is rapid growth in the study of different RES such as solar, tidal, and wind to extract power. Amongst PV, the energy extracted plays an energetic role, and it is direct current (DC) in nature. After getting DC from panels, it is important to convert as AC to meetup with locals as well as industrial power requirements. For this, the inverters play a very important role [1, 9]. The 2-level MLI are operated underneath, a higher switching frequency, resulting in higher dv/dt of voltage production, higher EMI (electromagnetic interferences) [10, 11] as well as increased heat issues in the switches. The MLI can overawe disadvantages related to the 2-level MLI from multiple points of view. With a created number of MLI levels, an almost unadulterated sinusoidal wave structure is accomplished. As the number of MLI levels rises, the THD in the air conditioner yield is diminished. It can minimize the harmonic contents along

with maximizing the power in the AC voltage output side [12, 13]. The tweak game plan serves the purpose of properly turning ON and OFF the force switches. Diode clamped, flying capacitor, and CHB (cascaded H-bridge) MLI are 3 regular MLI topologies [14, 15]. MLIs are usually used in various variable speed drives and renewable energy applications as well as static reactive power compensators [16, 17]. Diode clamped alongside flying capacitor MLI experience issues at higher yield levels such as voltage offsetting alongside unique voltage sharing. Consequently, among the traditional MLI CHB arranging is broadly perceived because of their secluded structure as small as shortcoming open-minded capacity [18–41]. The exchanging heartbeats can be created by utilizing various regulation procedures for MLIs. The boost converter is the standout reasonable converter as it can build the dc voltage as needed, and it is associated with a dc-dc converter among load and sun-based boards to fulfill the necessities [39]. The voltage output from the solar PV feed to the boost converter boosts the output and the output can be changed by changing the parameter of the boost converter.

In this investigation work, a configuration of boost converter-based 27-level cascaded MLI has been presented as an analysis in detail. A brief description of the boost converter is explained in Section 2. Implemented 27-level cascaded MLI is discussed along with simulation results in Section 3. The proposed system losses, efficiency, TSV, cost function, and reliability are presented in Section 4. The comparison of the proposed system with existing topologies is presented in Section 5. The experimental results are described in Section 6. Finally, the conclusion is discussed in Section 7.

2. Proposed Configuration

Figure 1 shows the projected arrangement, and it involves a solar photovoltaic- (PV)-based boost converter with integrated CHB MLI. The maximum possible voltage at the boost converter to survive high variable input currents from radiation through the photovoltaic array is to be maintained. According to the input voltage variations, the boost converter consisting of switches must be given the gate pulses. For constant voltage, the boost control is provided by the MPPT algorithm.

2.1. Modeling of a Boost Converter. The boost converter circuit contains capacitor (C), inductor (L), diode (D), and a load resistor (R_L) alongside the control switch (S). These components are related to the voltage input source (V_{in}) to support the voltage. By the obligation cycle control switch, the output voltage of the lift converter is controlled. The output voltage can be differed by shifting the ON season of the switch, and for the obligation cycle (D), the normal yield voltage can be determined by utilizing the following beneath equation:

$$\frac{V_0}{V_{\text{in}}} = \frac{1}{(1-D)}, \tag{1}$$

where V_{o} = output voltage and V_{in} = input voltage of the converter, respectively, and D = duty cycle.

2.2. Choice of Inductor. The boost converter inductor value is calculated by using following equation:

$$L = \frac{V_{\text{in}}}{F_s * \Delta I_L}, \tag{2}$$

where F_s is the switching frequency (10 kHz) and ΔI_L is the current ripple.

CRF (Current ripple factor) is defined as the ratio between input current ripple and output current. For a respectable estimate of an inductor, the CRF value should be assured within 30%. The inductor current rating is always higher than that of the output maximum current $(\Delta I_L / I_0) = 0.3$.

2.3. Choice of Capacitor. The value of the capacitor can be obtained from

$$C = \frac{I_{\text{out}}}{(F_s * \Delta V_0)D}, \tag{3}$$

where ΔV_0 = voltage output ripple which is typically measured as 5% of voltage output which produces $\Delta V_0 / V_0 = 5\%$.

The boost converter modeling can be calculated by using the above equations and the obtained values are presented in Table 1.

2.4. Solar Photovoltaic Powered Boost Converter. The current and voltage received from the solar photovoltaic array depend on temperature, the number of series-connected strings, and the number of parallel-connected string sand irradiance. So, it is essential to select the type of solar panel intelligently. Here, 1STH-215-P panel, 1Soltech with 2 parallel strings along with 2 series-connected modules per string is designated. The specifications of the selected solar panel are given for 1 series-connected module 1 and parallel string at 25°C temperature and irradiance of 1000 W/m^2 and are described in Table 2. Figure 2 represents the control and operation of a 3-level boost converter 19, which contains two dc-link capacitors C_1 and C_2, boost inductor L, and S_1 and S_2 switches, and Table 1 specifications of the boost converter are tabulated. The 3-level boost converter has 4 modes of operation depending on the switching states. Mode 2 & 3 occurs when either S_1 or S_2 is turned ON. Mode 1 & 4 occurs when S_1 and S_2 are turned OFF or ON, respectively. It is seen that dependent on the estimation of obligation proportion D there are 2 working areas. The converter permits working in Modes 2, 3, and 4 for the obligation cycle ($0 < D < 0.85$), whereas the converter permits working in Modes 1, 2, and 3 for ($0.85 > D < 1$). The connection between the complete dc-interface voltage and PV input source voltage is given by the following expression:

$$V_{dc} = \frac{V_{PV}}{(1-D)}. \tag{4}$$

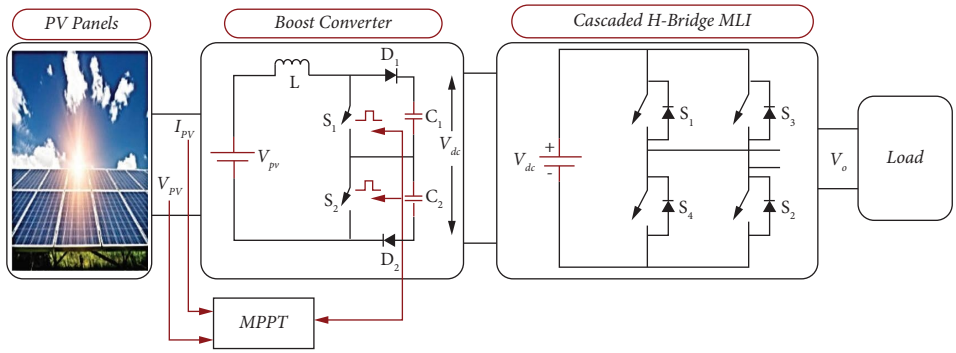

Figure 1: The proposed arrangement.

Table 1: Specifications of a boost converter.

Parameters	Value
Inductance L	15.38 mH
Input DC voltage	~60 V
Capacitance C_1 & C_2	282 μF
Duty cycle	0.85
Resistance (R_2)	10 Ohms

Table 2: Specifications of 215 W PV module.

Parameters	Value
Maximum power	213.15 W
Short circuit current (I_{sc})	7.84 A
Open-circuit voltage (V_{oc})	36.3 V
Current at maximum power point (I_{mpp})	7.35 A
The voltage at maximum power point (V_{mpp})	29 V
Diode ideality factor	0.98117
Diode saturation current (I_o)	$2.9259 * 10^{-10}$A

2.5. MPPT Method. In favor of tracing the maximum power point, it is required to use an algorithm in the P vs. V graph of the solar photovoltaic module. So, many methods are available to track the maximum power point such as incremental conductance, perturbing, and observing the fractional open-circuit voltage, and genetic algorithm. The MPPT algorithm implemented is represented in Figure 3, and the solar PV panel specifications are mentioned in Table 2.

In this paper, perturb and observe algorithm has been used. By varying the perturbation value, the maximum power point willpower speed can be controlled. Figure 3 shows the P&O algorithm flowchart. The algorithm for perturb and observe technique is as follows:

(a) From the solar PV module, read the voltage V_{pv} and current I_{pv} values.

(b) From the measured I_{pv} and V_{pv}, the Power P_{pv} is calculated.

(c) At M^{th} instant, the value of power and voltage is saved.

(d) Repeat step next values at $(M+1)^{th}$ instant are measured.

(e) From M^{th} instant, voltage and power at $(M+1)^{th}$ instant are detracted with the values.

(f) It is inferred that in the correct hand side bend in the force voltage bend of the sun-based PV module where the incline of intensity voltage is negative ($dP/dV < 0$), and the voltage is practically consistent whereas in the left-hand side, the slant is positive ($dP/dV > 0$). In this way, the lower obligation cycle is the correct side of the bend and the higher obligation cycle is the left side bend.

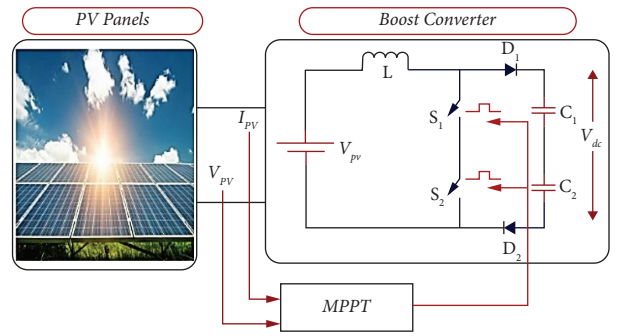

Figure 2: Solar powered 3-level boost converter.

(g) Contingent upon the sign of dV, for example, ($V(M+1) - V(M)$) and dP, for example, ($P(M+1) - P(M)$) regardless of whether to build the obligation cycle or to decrease the obligation cycle chooses after deduction of the calculation. Figure 3 shows the flowchart of perturb and observe algorithm. 1Soltech 1STH-215-P solar PV panel generates 60 V dc voltage with 5 A current, and by using a 3-level DC-DC boost converter, it will boost up the voltage 60 to 403 V dc with 4 A, and the simulation and experimental outcomes are shown in Figures 4 and 5, respectively. The simulation results of PV variation for several irradiances are presented in Figure 6, whereas the experimental results of PV irradiance are presented in Figure 7.

The efficiency of the converter during the irradiation condition is calculated as follows.

Equation (5) represents the output power relation of the PV system during irradiation conditions.

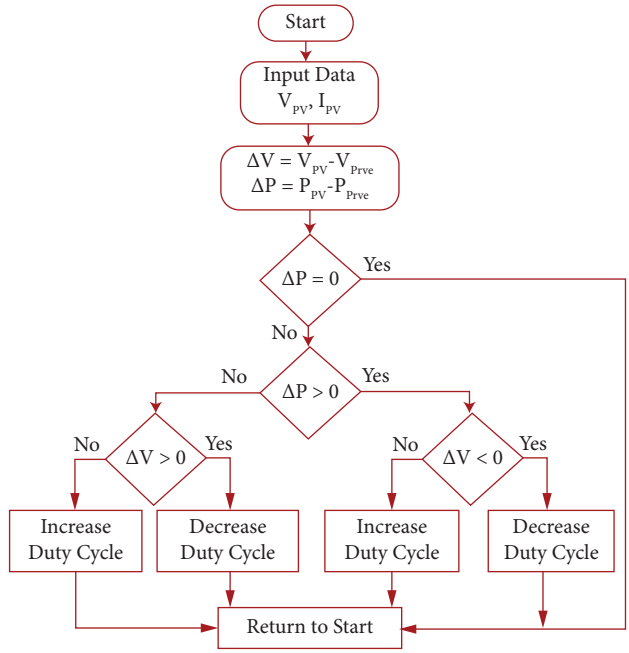

Figure 3: Flowchart of P&O (perturb and observe) algorithm.

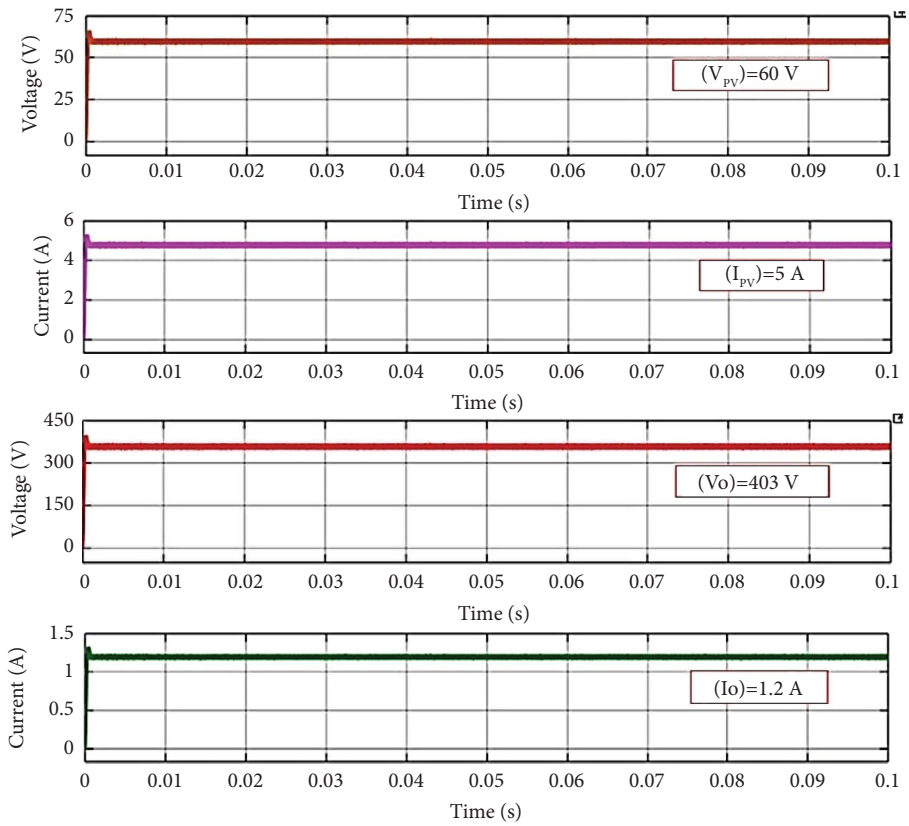

Figure 4: Proposed system simulation waveforms.

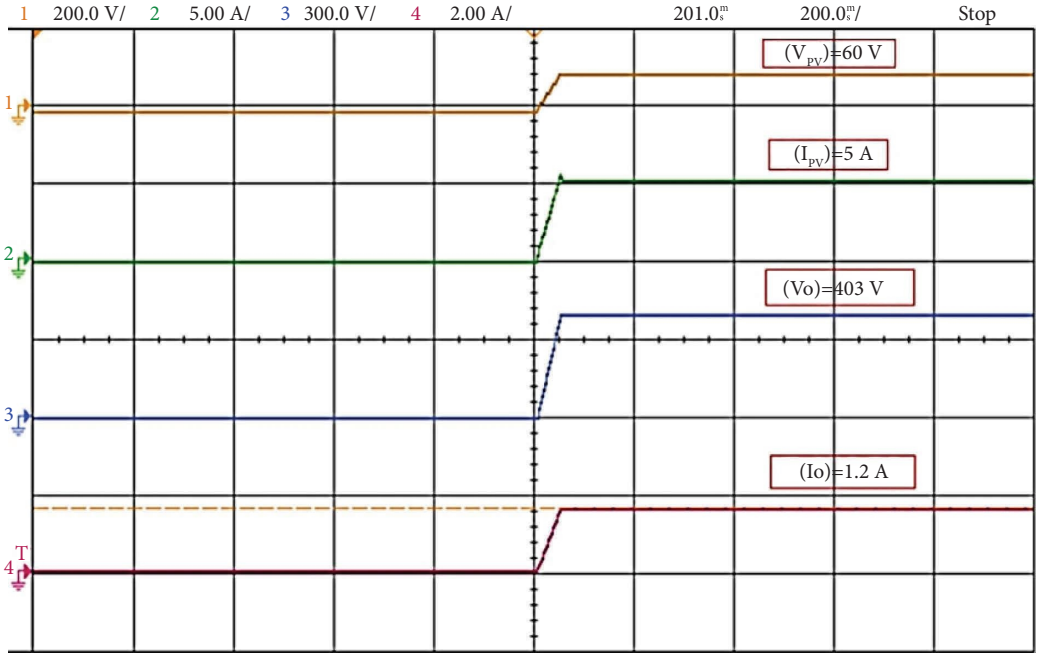

Figure 5: Proposed system experimental waveforms.

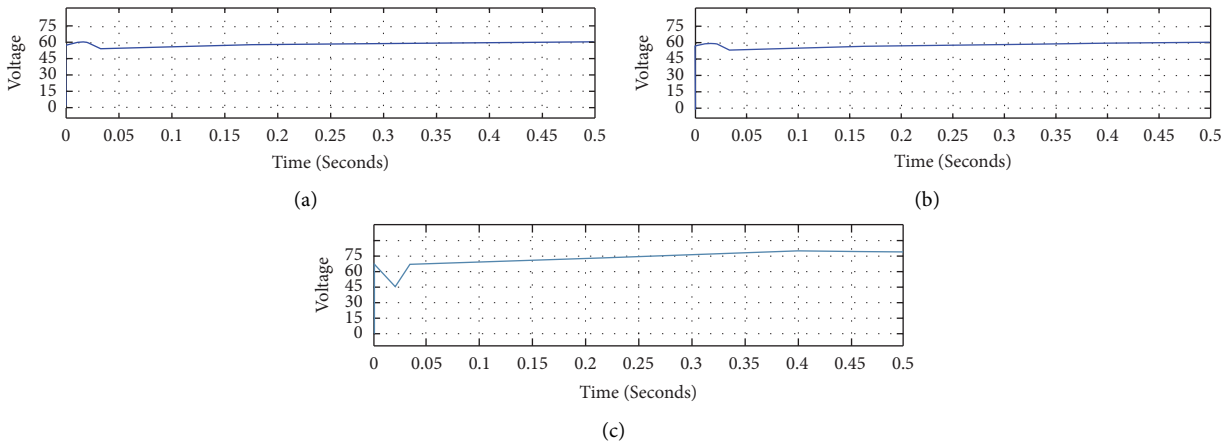

Figure 6: Simulation results of PV irradiance variation. (a) 490 W/m^2. (b) 660 W/m^2. (c) 1000 W/m^2.

$$P_{AC} = I_{rr} A_m \eta_m \eta_i p_{\text{loss}}, \tag{5}$$

where I_{rr} is the irradiance of the PV module (K_{wh}/m^2), A_m is the module (m^2), η_m is the module efficiency = (Output of module/1000 $*$ A_m) $*$ 100, η_i is the efficiency of the inverter = $(P_{\text{out}}/P_{\text{out}} + P_{\text{loss}})$, and P_{loss} is the converter loss = $P_c + P_s$.

Hence, during the irradiation of 1000 W/m^2 to 700 W/m^2, the efficiency is calculated from (5) and found to be 95.68%.

3. Implementation of CBH 27-Level MLI

The inverter is integrated with a boost converter with solar *PV* and electric vehicle applications to produce a pure sinusoidal waveform. The boost converter-based cascaded MLI is shown in Figure 8. The presentation of the cascaded MLI is discussed. The single-phase single bridge inverters are associated in a cascaded fashion giving cascaded MLI. In this analysis situs usually from various DC voltage buses, the desired voltage is appreciated. Considering the DC sources, the fell MLIs are considered into 2 kinds, deviated and symmetric inverters. In a symmetric sort, the voltage of the DC joins is held at a similar level.

The inconvenience of symmetric geography is that the expansion in voltage yield levels builds the number of switches. To overcome the above drawback, the DC buses supplied with unequal voltages are named asymmetric topology. The implemented 27-level MLI uses the asymmetric topology as presented in Figure 8. It contains 3 modules with 3 DC buses and each cell contains 4 switches. It is a mix of 3 single-stage *H*-connect inverters associated with the fell

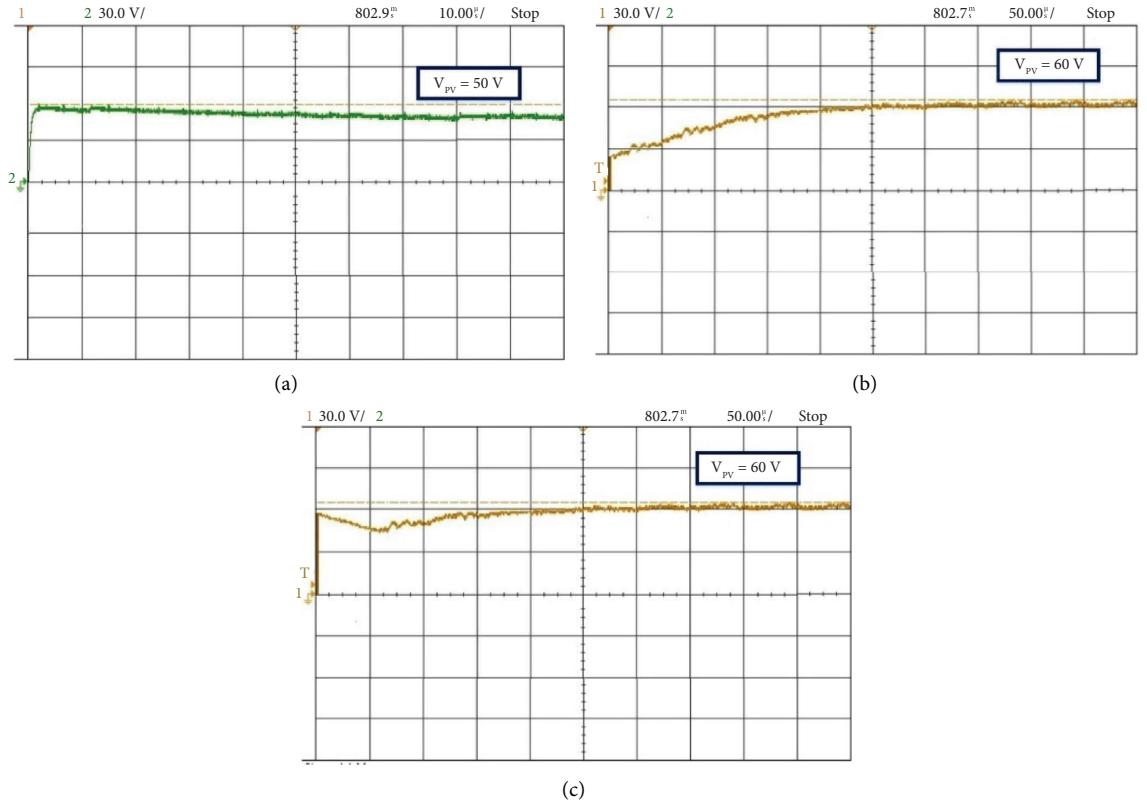

Figure 7: Experimental results of PV irradiance variation. (a) 490 W/m^2. (b) 660 W/m^2. (c) 1000 W/m^2.

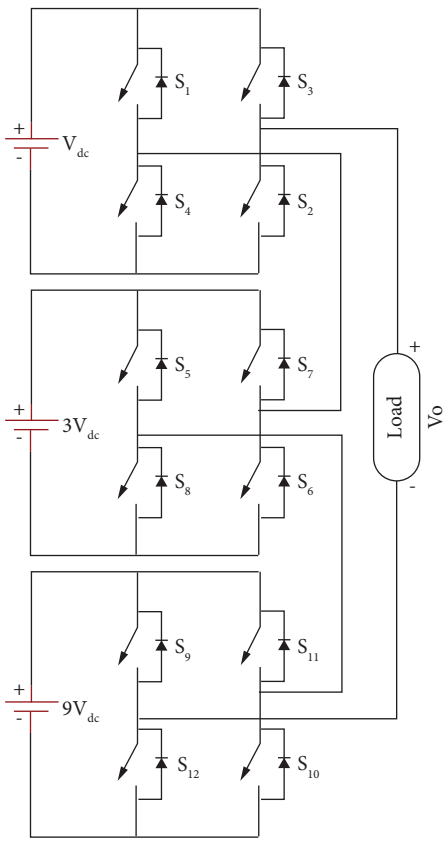

Figure 8: Cascaded H-bridge of 27-level MLI.

mode. The exchange plan for each single inverter cell is comparable to $S_1 = \overline{S_3}$ and $S_2 = \overline{S_4}$ from short-circuiting to avoid the circuit.

The power switches are MOSFETs or IGBTs as shown in Figure 8. The dc voltage is in the proportion of 1 : 3 : 9. A higher no of levels brings about expanded execution with more modest sounds. The benefits of fell staggered inverters are less number of DC sources, exchanging misfortunes, yield exchanging frequencies, decrease in cost, consonant levels, and expanded yield productivity. These wellsprings of DC are connected to a solitary stage H connect inverter, which creates the 3-levels of yield voltages such as follows+V_{dc}, 0, and $-V_{dc}$. The exchanging misfortunes in the framework depend on exchanging recurrence, which thusly is lesser due to the diminished voltage. This examination merges a mix of a few changes to propel the presentation of the inverter. In this technique, the various DC joins are associated with an association of 1 V, 3 V, 9 V... $3S-1$ V. A yield equivalent to $3S$ voltage levels are created by the inverter. A 27-level MLI is to create 27 distinctive voltage levels in the yield. The 27 levels in the yield waveform are ±13, ±12, ±11, ±10, ±9, ±8, ±7, ±6, ±5, ±4, ±3, ±2, ±1, and 0. By using the above equations, the implemented inverter number of switches and number of levels as well as peak PV output voltage can be attained.

3.1. Modes of Operation of 27-Level Cascaded H-Bridge MLI. For +1 V_{dc}, the PV output voltage level is +31 v which is generated by turning on switches S_1, S_2, S_6, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(a). For +2 V_{dc}, the PV output voltage level is +62 V which is generated by turning on switches S_3, S_4, S_5, S_6, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(b). For +3 V_{dc}, the PV output voltage level is +93 V which is generated by turning on switches S_2, S_4, S_5, S_6, S_{10}, and S_{12}, and that can be obtained at the load terminals as shown in Figure 9(c). For −1 V_{dc}, the PV output voltage level is −31 V which is generated by turning on switches S_3, S_4, S_6, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(d). For −2 V_{dc}, the output voltage level is −62 V which is generated by turning on switches S_1, S_2, S_7, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(e). For −3 V_{dc}, the output voltage level is −93 V generated with turning on switches S_2, S_4, S_7, S_8, S_{10}, and S_{12} and that can be obtained at the load terminals as shown in Figure 9(f). Likewise, the remaining levels are followed by using switching (Table 3).

3.2. The Circuit Parameters are Determined for the Proposed 27-Level Topology. The cascaded 27-level inverter parameters such as the number of power switches, sources, voltage levels, and voltage can be estimated as follows.

The number of switches is required as follows:

$$N \text{ swicthes} = 2^m + 4, \tag{6}$$

where m = number of basic unit by considering here m value is 3, then

$$\begin{aligned} \text{swicthes} &= 2^3 + 4 \\ &= 12. \end{aligned} \tag{7}$$

The number of sources is required as follows:

$$N \text{ sources} = m. \tag{8}$$

By considering the m value is 3, then N sources = 3
The number of levels is obtained as follows:

$$N \text{ levels} = 3^m. \tag{9}$$

By considering the m value is 1, then N levels = 3^3 = 27
The output voltage of the 27-level is determined as follows:

$$V0 = \left[2^m + 5\right] * V\text{dc}. \tag{10}$$

By considering the m value is 3 and V_{dc} value is 31, then $V0 = [2^3 + 5] * 31 = 403$V.

The input supplies specified to the circuit are $V_{dc} = 403$ V to accomplish the decided pinnacle voltage of 403 V with the loads ($R = 100\,\Omega$ & 98 mH). The simulation output waveform of the cascaded H-bridge of 27-level MLI is shown in Figure 10. The switching table is shown in Table 3 for the conduction state of switches in 27-level MLI. By using the staircase modulation method, the implemented MLI, gate pulses are created for switches. It is calculated from MATLAB at 10 kHz of switching frequency. The transporter signal is related to a reference sign of 50 Hz. Figure 11 shows the yield voltage just as the current for 27-levels MLI. For the arrangement association, the voltage proportion is 1 : 3 : 9. The information that supplies the predefined voltages to the circuit is $V_{dc} = 31$ V, $V_{1dc} = 93$ V, and $V_{3dc} = 279$ V to accomplish the decided pinnacle voltage of 403 V with the ($R = 100\,\Omega$ & 98 mH) loads. The yield voltage of recreation yields current alongside THD as introduced in Figures 11 and 12.

4. Calculation of Reliability, TSV, Cost Function, Losses, and Efficiency

4.1. Losses and Efficiency. The misfortunes can be estimated by two methods; two significant misfortunes related to switches are exchanging misfortunes and misfortunes of conductions. The conductivity let-down of IGBTs can be overcome [20, 21].

$$Q_{\text{Cl,IGBT}(t)} = \left[V_{\text{IGBT}} + R_{\text{IGBT}} i^{\beta}\right] i(t), \tag{11}$$

where V_{IGBT} is the drop in forwarding voltage of the IGBT, and the drop in forwarding voltage of the diodes is V_d. R_{IGBT} is the equivalent resistance of the IGBTs, and the equivalent resistance of the diodes is R_d, and β is a constant with IGBT specification favors. The normal estimation of the MLIs conductive force misfortune (Q_{cl}) can be given as follows [20, 21] as N_d diodes and N_{IGBT} transistors are present in the current path at a time t [20, 21].

$$Q_{\text{Cl}} = \frac{1}{2\pi} \int_0^{2\pi} \left[N_{\text{IGBT}}(t) Q_{\text{cl,IGBT}}(t)\, \mathrm{d}t\right]. \tag{12}$$

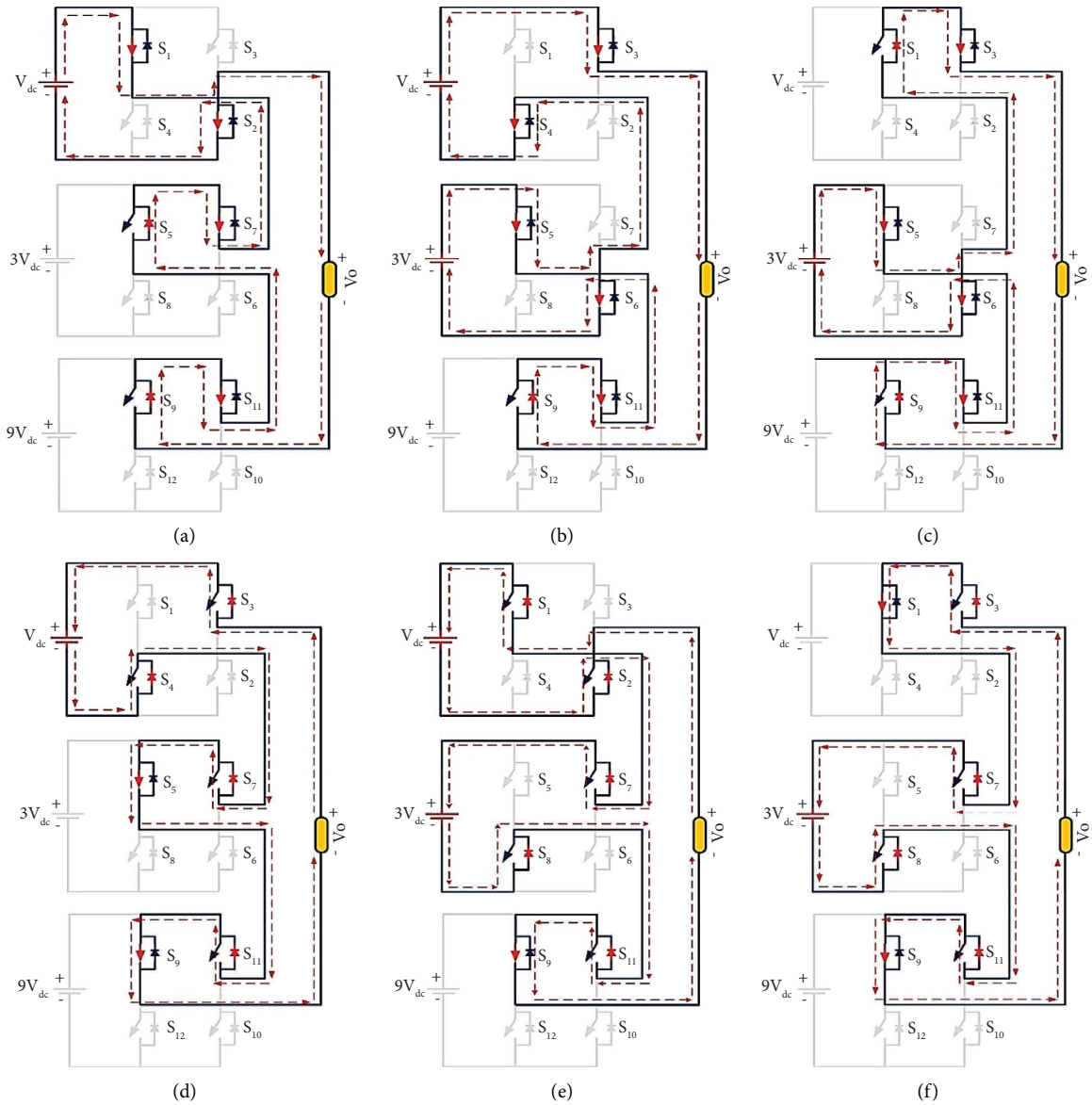

Figure 9: (a–f). Modes of operation of cascaded H-bridge of 27-level MLI.

Table 3: Switching states (ON) of 27-level MLI.

Modes	ON states of switches
0	$S_1, S_3, S_5, S_7, S_9, S_{11}$
1	$S_1, S_2, S_5, S_7, S_9, S_{11}$
2	$S_3, S_4, S_5, S_6, S_9, S_{11}$
3	$S_1, S_3, S_5, S_6, S_9, S_{11}$
4	$S_1, S_2, S_5, S_6, S_9, S_{11}$
5	$S_3, S_4, S_7, S_8, S_9, S_{10}$
6	$S_1, S_3, S_7, S_8, S_9, S_{10}$
7	$S_1, S_2, S_7, S_8, S_9, S_{10}$
8	$S_3, S_4, S_5, S_7, S_9, S_{10}$
9	$S_1, S_3, S_5, S_7, S_9, S_{10}$
10	$S_1, S_2, S_5, S_7, S_9, S_{10}$
11	$S_3, S_4, S_5, S_6, S_9, S_{10}$
12	$S_1, S_3, S_5, S_6, S_9, S_{10}$
13	$S_1, S_2, S_5, S_6, S_9, S_{10}$
−1	$S_3, S_4, S_5, S_7, S_9, S_{11}$
−2	$S_1, S_2, S_7, S_8, S_9, S_{11}$
−3	$S_1, S_3, S_7, S_8, S_9, S_{11}$
−4	$S_3, S_4, S_7, S_8, S_9, S_{11}$
−5	$S_1, S_2, S_5, S_6, S_{11}, S_{12}$
−6	$S_1, S_3, S_5, S_6, S_{11}, S_{12}$
−7	$S_3, S_4, S_5, S_6, S_{11}, S_{12}$
−8	$S_1, S_2, S_5, S_7, S_{11}, S_{12}$
−9	$S_1, S_3, S_5, S_7, S_{11}, S_{12}$
−10	$S_3, S_4, S_5, S_7, S_{11}, S_{12}$
−11	$S_1, S_2, S_7, S_8, S_{11}, S_{12}$
−12	$S_1, S_3, S_7, S_8, S_{11}, S_{12}$
−13	$S_3, S_4, S_7, S_8, S_{11}, S_{12}$

Because of the energy the exchanging misfortunes can be assessed used during turn-off and turn-on cycles in the switches, it is esteemed dependent on straight contrasts of the exchanging voltage and current [20, 21]. The energy value could be as follows:

$$\begin{aligned} \mathrm{Em}_{\mathrm{on},l} &= \int_o^{t_{\mathrm{on}}} v(t) i(t) \\ &= \frac{1}{6} V_{\mathrm{switch},l} I' t_{\mathrm{on}}, \end{aligned} \tag{13}$$

$$\begin{aligned} \mathrm{Em}_{\mathrm{off},l} &= \int_o^{t_{\mathrm{off}}} v(t) i(t) \\ &= \frac{1}{6} V_{\mathrm{switch},l} I' t_{\mathrm{off}}, \end{aligned} \tag{14}$$

where $\mathrm{Em}_{\mathrm{off}}$ and $\mathrm{Em}_{\mathrm{on}}$ are the turn-on and turn-off misfortunes with l. The misfortunes from exchanging are comparable to the amount of the misfortunes from turn-off and turn-on energy, esteemed as follows:

$$Q_{\mathrm{Sl}} = f \sum_{\mathrm{l}=1}^{M_{\mathrm{switch}}} \left[\sum_{s=1}^{M_{\mathrm{on,l}}} \mathrm{Em}_{\mathrm{on,ls}} + \sum_{s=1}^{M_{\mathrm{off},l}} \mathrm{Em}_{\mathrm{off,ls}} \right]. \tag{15}$$

The total loss of power was valued as follows:

$$P_{\mathrm{Totallosses}} = Q_{\mathrm{cl}} + Q_{\mathrm{sl}}. \tag{16}$$

The inverter efficiency (η) is given as follows:

$$\begin{aligned} \eta\% &= \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \\ &= \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{losses}}}, \end{aligned} \tag{17}$$

where P_{in} and P_{out} correspond to the input and output power.

The power output can be assessed in the following way:

$$P_{\mathrm{out}} = V_{\mathrm{rms}} * I_{\mathrm{rms}}. \tag{18}$$

The experimental power output of 718.7 W for twenty-seven-level inverters is obtained using (14) ($V_{\mathrm{rms}} = 282.84$ V and $I_{\mathrm{rms}} = 2.828$ A). The parameter values for calculation are collected from the IGBT CM7FDU datasheet. From the performance characteristics plot the R_{IGBT} is 0.4 and V_{switch} value (0.6 V) is taken, 200 ns turn-off delay, 100 ns turn-off, 250 ns turn-off, and 12 switches turn-off as 300 ns. The proposed inverter design will cover 53 steps in one complete cycle [20, 21]. The losses from the conduction are calculated using equation (9).

$Q_{\mathrm{cl}} = 58.75$ W and $\mathrm{Em}_{\mathrm{off}}$ and $\mathrm{Em}_{\mathrm{on}}$ are calculated from equations (13) and (14). $\mathrm{Em}_{\mathrm{off}} = 0.254$ W and $\mathrm{Em}_{\mathrm{on}} = 0.127$ W.

The switching losses are designed as follows:

$Q_{\mathrm{sl}} = 0.381$ W, total losses are designed using (16) during switching and lead time.

$$\begin{aligned} P_{\mathrm{Totallosses}} &= 58.75 + 0.381 \\ &= 59.131\mathrm{W}. \end{aligned} \tag{19}$$

The η (efficiency) is designed by utilizing equation (17):

$$\begin{aligned} \eta\% &= \frac{718.7}{718.7 + 59.131} \times 100 \\ &= 92.38\%. \end{aligned} \tag{20}$$

The above calculations guarantee the proposed 27-inverter efficiency at 92.38 percent.

4.2. Total Standing Voltage (TSV). The standing voltage of the inverter is estimated using the following equations:

$$\begin{aligned} \mathrm{TSV} &= \sum_{i=1}^{n} V_{SWi}, \\ \mathrm{TSV} &= 2\left(V_{\mathrm{dc}}\right) + 2\left(3V_{\mathrm{dc}}\right) + 2\left(9V_{\mathrm{dc}}\right), \\ \mathrm{TSV} &= 26V_{\mathrm{dc}}, \\ \frac{\mathrm{TSV}}{L} &= \frac{26V_{\mathrm{dc}}}{27} \\ &= 0.962\frac{V_{\mathrm{dc}}}{L}, \\ \text{Total Blocking Voltage} &= V_{\mathrm{dc}} + 3V_{\mathrm{dc}} + 9V_{\mathrm{dc}} \\ &= 13V_{\mathrm{dc}}. \end{aligned} \tag{21}$$

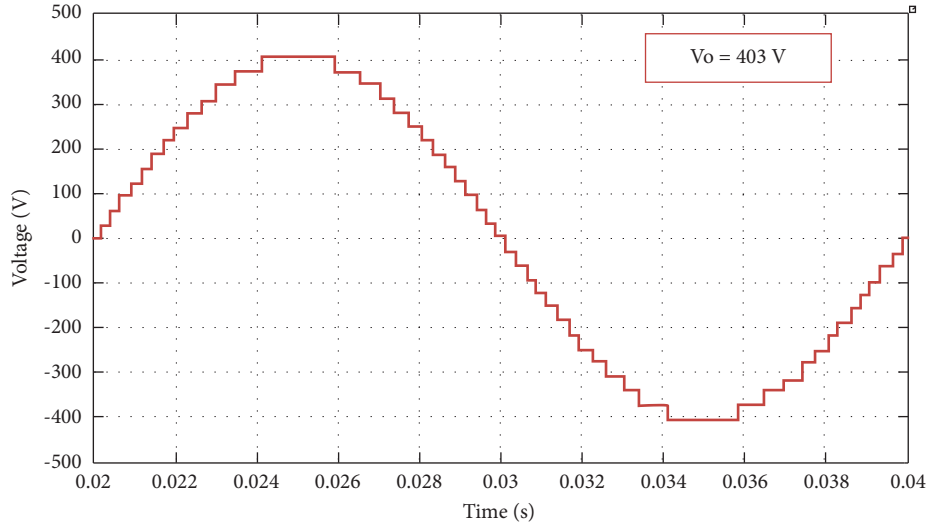

Figure 10: Simulation output waveform of the cascaded H-bridge of 27-level MLI.

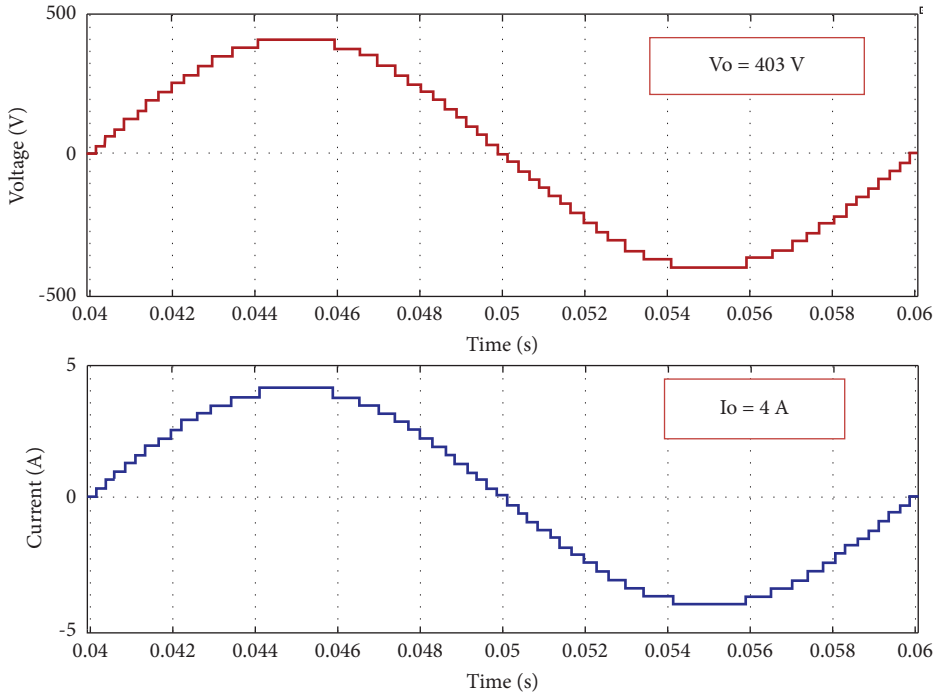

Figure 11: Simulation of 27 output voltage and output current of the inverter.

In open-circuit conditions, the switches will block the voltages of blocking voltages of switches [37];

$$\begin{aligned} &S_1, S_2, S_3 \text{ and } S_4 \text{ is } V_{\text{dc}}, \\ &S_5, S_6, S_7 \text{ and } S_8 \text{ is } 3V_{\text{dc}}, \\ &S_9, S_{10}, S_{11} \text{ and } S_{12} \text{ is } 9V_{\text{dc}}. \end{aligned} \tag{22}$$

Blocking voltages across the switches are as follows:

$$\begin{aligned} S_1 &= S_2 \\ &= S_3 \\ &= S_4 \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{V_{\text{dc}}} \\ &= 13V, \\ S_5 &= S_6 \\ &= S_7 \\ &= S_8 \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{3V_{\text{dc}}} \\ &= 4.33V, \\ S_9 &= S_{10} \\ &= S_{11} \\ &= S_{12} \\ &= \frac{V_{\max}}{V_{\text{block}}} \\ &= \frac{13V_{\text{dc}}}{9V_{\text{dc}}} \\ &= 1.44V. \end{aligned} \tag{23}$$

The total voltage blocked across the switches as follows:

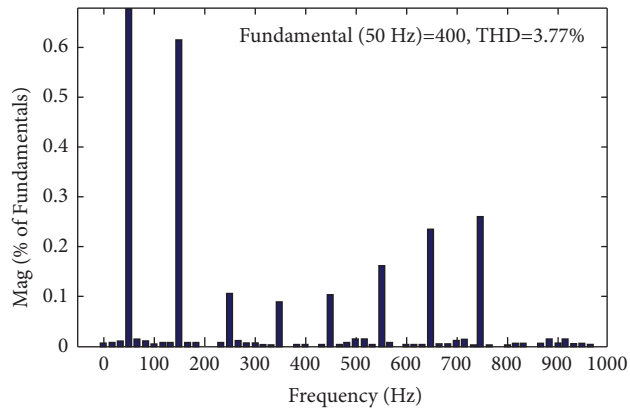

Figure 12: 27-level multilevel inverter simulation THD.

$$\begin{aligned} \text{TSV} &= 4(13) + 4(4.33) + 4(1.44) \\ &= 75.08V, \\ V_{\text{Switch}}^{p.V} &= \frac{\text{Total Voltage}}{\text{Max voltage}} \\ &= \frac{75.08}{13} \\ &= 5.77. \end{aligned} \tag{24}$$

4.3. Cost Function (CF). The cost function of the inverter is estimated using the following equation [37].

$$\text{The Cost Function } CF = N_{\text{SW}} + \alpha V_{\text{Switch}}^{p.V}, \tag{25}$$

where the N_{sw} is the switches count, α is the weighting coefficient, and V_{switch} is the voltage across the switch.

The inverter estimated cost function is tabulated in Table 4.

4.4. Reliability Calculation of the Inverter. The mean time to failure rate (MFFT) is important for the inverters; the reliability analysis is presented for the proposed system. The total MTTF of power electronic circuits can be calculated by estimating the total failure rate (FR) value of the circuit elements that are present [38]. The total FR and λ_T, are calculated by multiplying the number of components, such as switches and diodes by their corresponding FR values.

$$\lambda_T = (\lambda_{PS} * N_{\text{SW}}) + (\lambda_{\text{PD}} * N_D). \tag{26}$$

The total MTTF of the power electronic circuit can be derived from following equation:

Table 4: Cost function.

∝	CF	CF/L
0.5	14.885	0.55
1.5	20.655	0.76
2.5	26.425	0.97
3.5	32.195	1.19

$$\mathrm{MTTF}_T = \frac{1}{\lambda_T}. \tag{27}$$

The MTTFT of the electronic circuits can be calculated based on the number of device counts.

The inverter has 12 switches (N_{SW}) and 12 diodes, respectively, and the total failure rate (FR) and mean time to failure rate (MFFT) are estimated using (26) and (27).

$$\begin{aligned} \mathrm{FRT} &= 0.0000042, \\ \mathrm{MTTFT} &= 238095.2. \end{aligned} \tag{28}$$

5. Comparative Analysis

A boost converter-based CHB staggered inverter is proposed for the utilization of extracted PV energy. The solar photovoltaic is connected to the boost converter, and it enhanced voltage from PV output voltage 60 V to 403 V with the help of the MPPT technique. The boosted output voltage is higher compared to existing converters [22–25] as shown in Table 5 and Figure 13 shows the comparison of the proposed converter with existing converters. The output of the implemented 27-level CBH multilevel inverter has fewer switching losses as well as switch count compared with the existing topologies [26–30] as shown in Table 6 and comparison is shown in Figure 14. As experimental voltage value adapts to disorient situations of injected voltage and power. The inverter which is a linked *PV* module can be a unit with reduced power losses as it consists of fewer driver circuits. This study reports a 27-level inverter using just helped voltage got from a sustainable power source. The inverter proficiency is high and the yield voltage waveform is entirely sinusoidal. The expense is little as the number of intensity switches used is 12. The power switches are reduced apparently due to a reduced number of power driver circuits, also low transmission losses than traditional inverter modules. Expanding the degree of the inverter can get a few points of interest: get a decent voltage wave structure and very low THD 3.77% which is achieved through the experiment as shown in Figure 15. The comparison of implemented inverter THD values with existing topologies. The conventional MLIs are compared with 27MLI is tabulated in Table 7 and Figure 16 shows the comparison of implemented MLI with the conventional MLIs. The reliability analysis conducted for the inverter with existing MLIs is shown in Table 8. The inverter has reliability when compared to existing MLIs in all aspects as shown in Figure 17. The references [26, 27, 29] have less THD compared with the proposed MLI but the MBV of the other topologies are high whereas the MBV of the proposed topology is less, which results in the added advantage of the topology.

Table 5: Comparison of the proposed converter with existing converters.

References	Input voltage (V)	Output voltage (V)
[22]	18	42
[23]	36	60
[24]	12	14.5
[25]	600	700
Proposed method	60	403

6. Experimental Results

The extracted PV two voltages and one programmable DC source are fed to the 27 MLI. The 27-level MLI equipment model setup was used in the model scale and tried tentatively. The social occasion of Simulink block bunches into dSPACE RTI 1104 computerized input/output ports are performed, and the flight of stairs tweaks PWM technique execution in MATLAB/Simulink is performed. To rearrange continuous interfacing applications, by the computerized I/O ports, the 20 yield pins are controlled. From the dSPACE RTI1104, the TLP 250 driver is separated to include, is the beat made. The experimental twenty-seven output waveform is shown in Figure 18(a). The consistent state testing checks with R-load with 400 V alongside the current yield are accomplished with 4 A. Yield current and voltage RMS esteems were to start with 282.84 V and 2.828 A, correspondingly. The staging point between the heap current and the heap voltage is zero, as appeared in the waveform. Consistent state testing with an R-load, competition after here gave the L-load 403 V and 3.4 A, correspondingly, and relating RMS esteems were achieved with 284.96 V and 2.404 A, correspondingly. The output voltage and currents are 403 V and 2.3 A, and the RMS values are 284.96 V and 1.626 A, correspondingly obtained investigational results are given in Figures 18(b)–18(d). The investigational results check at consistent state, load aggravation conditions, executed with R to L load as appeared in Figure 19, executed with L to R load as appeared in Figure 20, correspondingly. In assurance, stacks infrequently happen particularly and they will surely occur in a blend of resistive and inductive burdens. Generally, in a particular spot, when an R (resistive) load is by and by working an unexpected collection of L (inductive)-load corresponding to the R load or the other way around is indistinguishable likely. Figure 21 shows the experimental results of the 27-level multilevel inverter THD trial voltage is 4.02%. The proposed system hardware setup is shown in Figure 22. The experimental output parameters are shown in Tables 9 and 10.

The actualized inverter created a higher number of voltage yield levels with a less number of equipment components and low THD values. Similar aftereffects of the trial have appeared in Tables 9 and 10. The experimental setup component details are mentioned in Table 11.

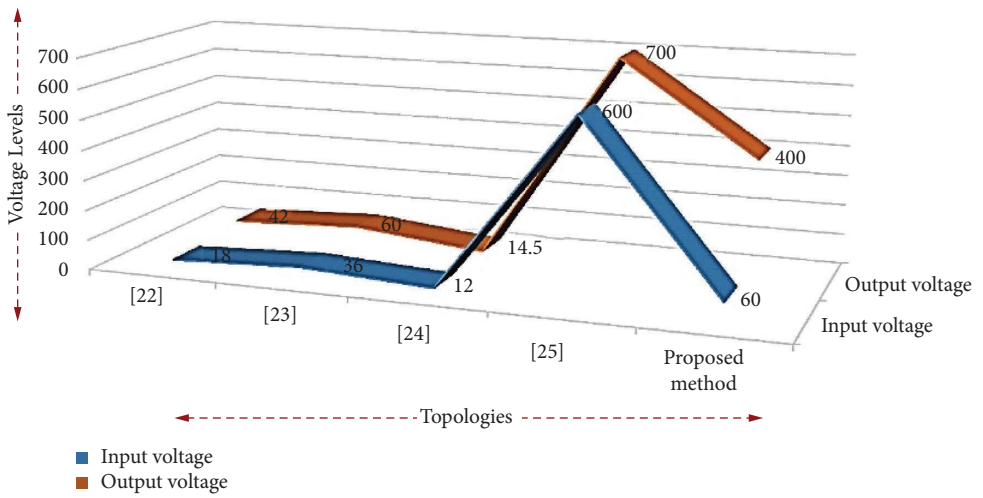

Figure 13: Comparison of the proposed converter with the existing converters.

Table 6: Comparison of implemented MLI with active MLIs.

MLIs	No. of levels	No. of switches	No. of sources	Diodes	(%) THD	(%) Efficiency
[26]	27	12	3	12	1.248	—
[27]	27	13	1	13	2.74	—
[28]	27	12	3	12	13.75	—
[29]	27	13	3	13	2.68	—
[30]	27	36	3	36	5.87	—
[42]	27	14	5	14	2.037	—
27-Level MLI	27	12	3	12	3.77	92.38

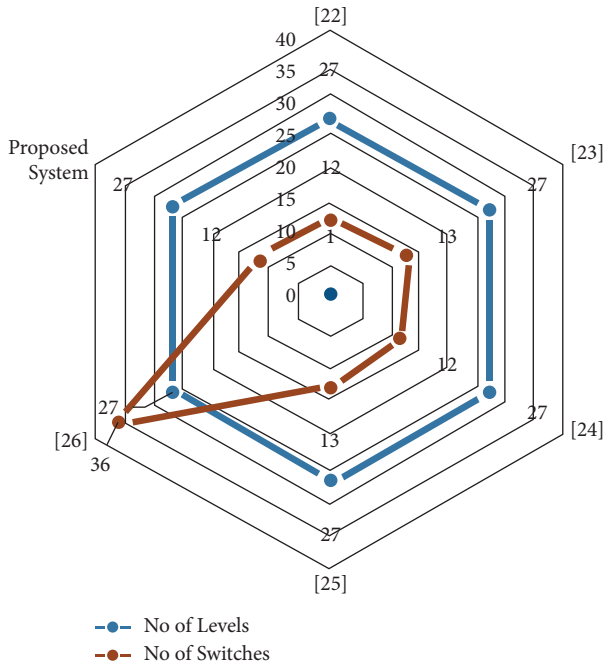

Figure 14: Comparison of implemented inverter levels and switches with the existing topologies.

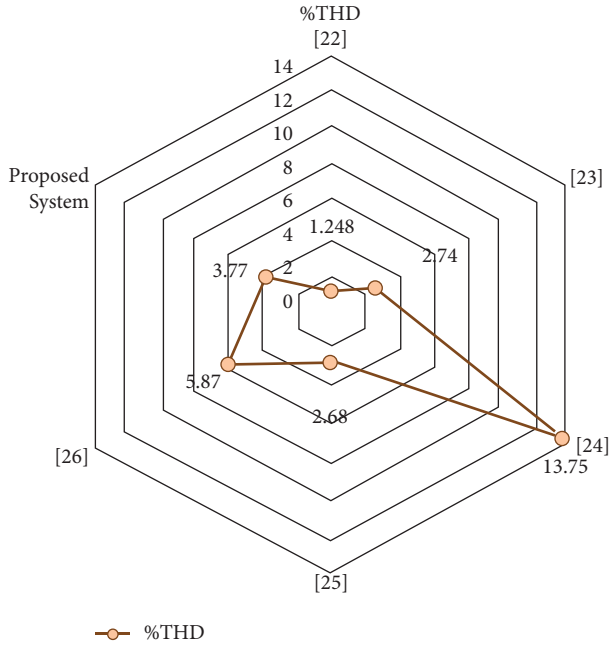

Figure 15: Comparison of implemented inverter THD values with existing topologies.

Table 7: Comparison of implemented MLI with the conventional multilevel inverters.

Required items	CMLI	DCMLI	FCMLI	Proposed MLI
No of levels	27	27	27	27
No of switches	52	52	52	12
Diodes	52	52	52	12
Clamping diode	0	650	0	0
Dc bus capacitor	13	26	26	0
Balancing capacitor	0	0	325	0
Gate-amp	52	52	52	12

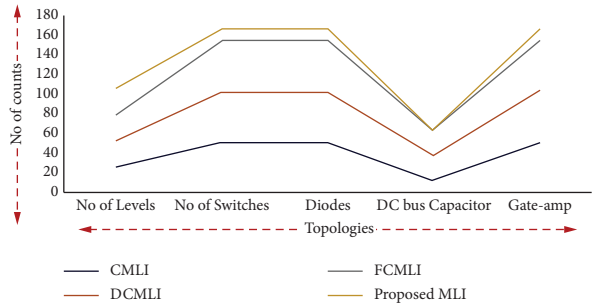

Figure 16: Comparison of implemented MLI with conventional MLIs.

Table 8: Comparison of topologies based on reliability aspects.

Topology	N_{SW}	N_D	FR_T	$MTTF_T$
[26]	12	12	0.0000042	238095.2
[27]	13	13	0.00000455	219780.2
[28]	12	12	0.0000042	238095.2
[29]	13	13	0.00000455	219780.2
[30]	36	36	0.0000126	79365.08
Proposed system	12	12	0.0000042	238095.2

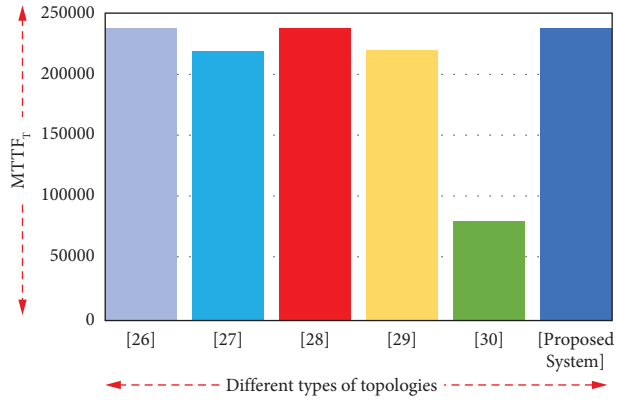

Figure 17: Comparison of topologies based on reliability aspects.

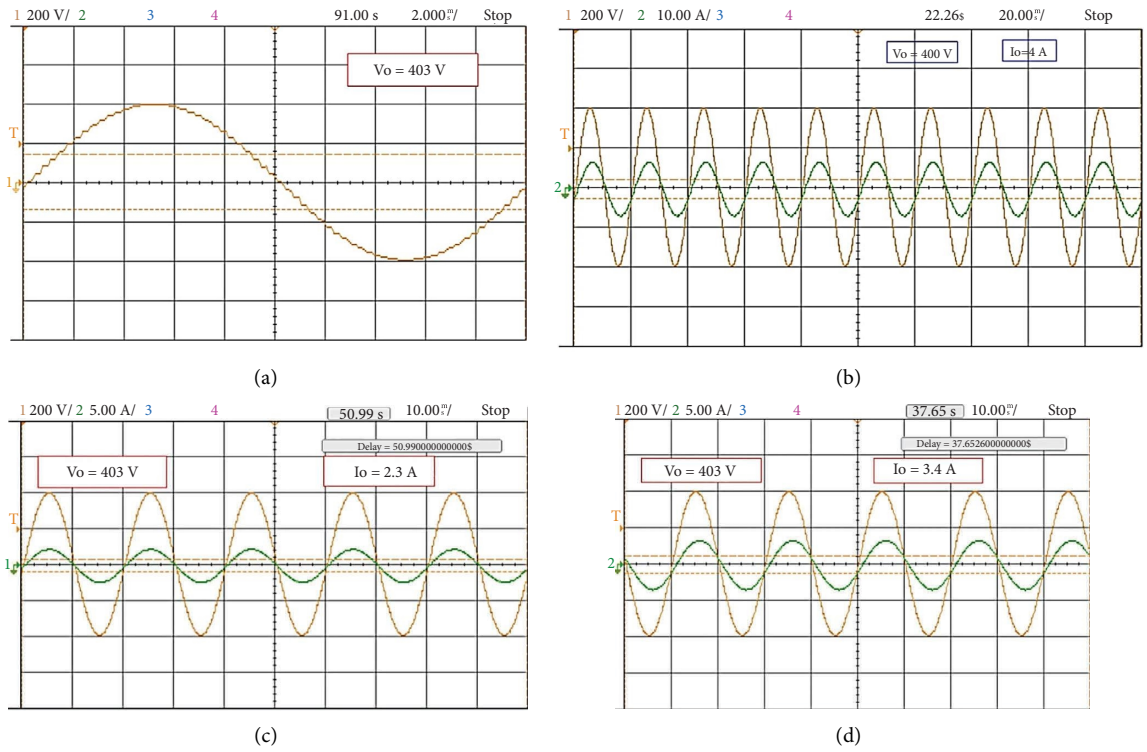

Figure 18: (a) O/P voltage of the actualized inverter. (b) O/P current and voltage of inverter with R load (c) O/P current just as the voltage of the inverter with engine load (d) O/P current and voltage of the inverter with L load.

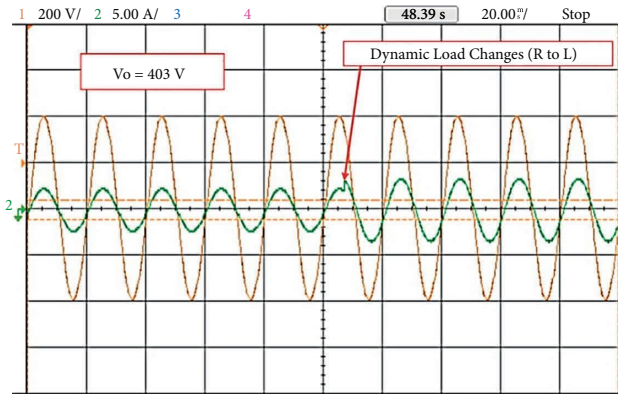

Figure 19: 27-level multilevel inverter dynamic (R to L) loads changes.

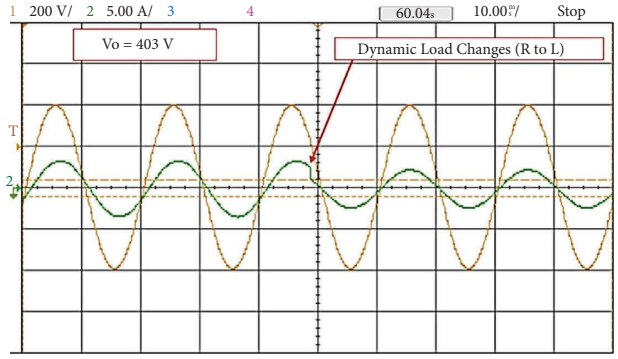

Figure 20: 27-level multilevel inverter dynamic (L to R) loads changes.

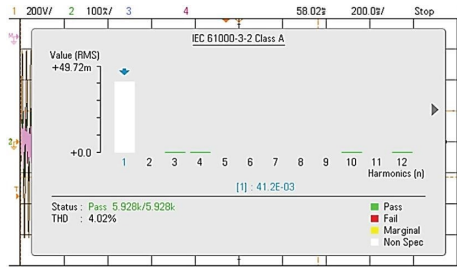

Figure 21: Experimental results of 27-level multilevel inverter THD value.

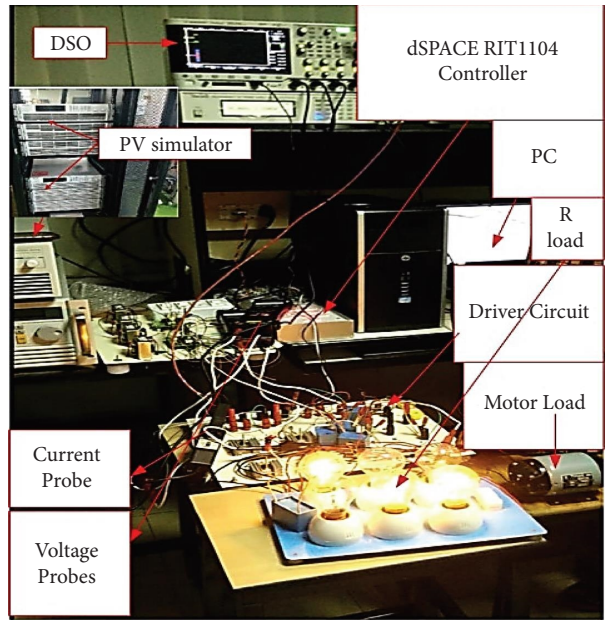

Figure 22: Proposed system hardware setup.

Table 9: Output experimental parameters of 27 MLI.

Inverter type	27 MLI	27 MLI	27 MLI
Load	R (ohms)	L (henry)	Motor (henry)
I_0 (A)	4	3.4	2.3
I_{rms} (A)	2.828	2.404	1.626
V_0 (V)	403	403	403
V_{rms} (V)	284.96	284.96	284.96
P_0 (w)	799.871	679.94	459.89
THD (%)	3.77	3.77	3.77

Table 10: Comparison of experimental and simulation of implemented 27 MLI.

Items	Implemented 27 MLI simulation results	Implemented 27 MLI experimental results
I_0 (A)	4	4
THD	3.77	4.02
V_0 (V)	403	403

Table 11: Experimental specifications.

Sl. no.	Elements	Specifications
1	Inductor	175 mH
2	Programmable-DC sources	500 Volts
3	Driver circuit	TLP250
4	Motor load	0.5 Hp 1-Φ (373 W, 0.75 PF, 230 V)
5	dSPACE controller	RTI1104
6	IGBTs (CM75DU-12H)	75 A, 600 V
7	Resistor	100 Ohms

7. Conclusion

In this study, a boost converter-based CHB staggered inverter for solar PV applications is implemented. Solar PV is associated with the lift converter and improved voltage from PV yield voltage 60 V to 403 V with the help of the MPPT method. The inverter is integrated with a boost converter with solar *PV* applications to generate a pure sinusoidal waveform. A 27-level CHBMLI is implemented with reduced power losses and lower THD. The 27-level topology has been planned and afterward reenacted in MATLAB/Simulink, and it uses 12 switches and three voltage sources to develop 27-level voltage sources THD for 27 levels is 3.77% and efficiency is 92.38%. The inverter has lower TSV, is cost-effective, and has improved reliability. Finally, a detailed comparison with the existing system is given focusing on the advantages of the proposed converter and implementation for the 27-level inverter. The proposed topology is limited to medium-power devices with a restricted number of levels. The proposed system is well suited for electric vehicles and grid-connected applications and FACTs [8].

Data Availability

The data used to support the findings of this study are included in the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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