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Research Article

A Novel Multigain Switched-Capacitor-Based Topology with Reduced Part Count

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In photovoltaic power plants, wind farms, and other types of renewable energy generating facilities, the usage of multilevel inverters (*MLIs*) is a popular and widely used choice. A unique structurally-based step-up self-balanced compact multigain switched capacitor inverter architecture (*MGSCIT*) is proposed in this study. The proposed MGSCIT uses two switched capacitors and nine switches to generate a seven-level (*7L*) output voltage with a voltage gain of three times the input. The suggested topology also includes several other important advantages, such as the minimum number of switching components, three-times voltage gain, inherent self-balancing of capacitor voltage, reduced voltage ripples, reduced voltage, and stresses. The negative voltage levels can be generated without the need for a backend H-bridge (*HB*). The structural design analysis of the proposed MGSCIT, self-balancing mechanism of capacitor voltages, determination of optimum values of capacitance, and control strategy are explained in detail. To demonstrate the benefits of the proposed topology, a fair comparison is offered with the most current 7-level single-source topologies, focusing on the cost function and the number of components per level. Finally, simulation results demonstrate the accuracy of the theoretical analysis, and the prototype built demonstrates the feasibility and effectiveness of the practical findings, with maximum measured efficiency reaching 95.62%. The voltage and current THD are 31.08% and 1.45%, respectively.

1. Introduction

The growing environmental pollution and energy issue of recent years has shifted focus toward the research, development, and implementation of clean and renewable energy sources. Power from renewable sources like solar panels and wind turbines has seen particularly high adoption rates due of their accessibility, environmental friendliness, and dependability. The inverter is an essential aspect of any wind or solar power producing system. Low- and high-power DC-AC power conversion using MLIs is a popular area of study and development. Meanwhile, MLIs have several significant features such as lower dv/dt stress, improved waveform, higher efficiency, and reduced filtering circuit [1, 2]. The three types of conventional MLIs are the neutral point clamped (NPC), flying capacitor (FC), and cascade HB (CHB). These inverters have numerous uses in the commercial and manufacturing sectors. However, they have several limitations such as lack of boosting capability, capacitor voltage balancing a major challenge for FC and NPC, and multiple independent dc sources for CHB [3]. These drawbacks restrict their widespread applications.

The incorporation of SC-based circuits has been a popular method across various families of modernized MLIs. The SCMLI has several advantages over its competitors, including its inductor less/transformer less operation, its voltage-boosting capability, and its intrinsic capacitor self-voltage-balancing performance [4–7]. These groups of topologies are united by the fact that they are made up of two stages. A SC dc-dc converter is utilized in the first stage to provide positive voltage levels, and an HB is used in the second stage to control the polarity of the output voltage. With an HB in existence, the switching components are subjected to a higher peak voltage. It is exceptionally undesirable. An article discusses a 9-level inverter built using only two DC supplies, as outlined in reference [8]. While the design achieves a low device count, it introduces complexity and complications due to its reliance on multiple DC sources. The 9L output voltage is maintained by this configuration. 7L topology is discussed in [9–11]. These topologies, however, require more switching elements and driver circuits. The topology presented in [9] has a 3x boost; however, [10, 11] has less boosting factor, that is 1.5. One of the main drawbacks of the architecture presented in [12, 13] is the high voltage stress across several power switches in the second stage. A 7-level inverter that can produce three times the input voltage is described in [14]. Therefore, the boosting factor is three. The 3x boost is achieved with decreased devices in the SCMLIs disclosed in [15, 16], which provide 7-levels of output voltages. However, their TSV and PIV are more. Additional topologies for achieving triple voltage gain are presented in [17–19]. However, more power components are needed for these topologies. To reduce the need for the extra switching capacitor, a dc source and two T-type voltage-dividing capacitors are combined into a single design [20]. The modular SC inverter recommended in [21] can accommodate both medium and high-voltage applications. Major benefits of the anticipated topology are its modular design and the capacity to increase the input voltage. The generalized SCMLI topology introduced in [22] uses self-balancing capacitors. Using ten switches and two capacitors, the topology can produce five levels with a boost factor of two. This topology's strengths lie in its boosting ability and modular structure. In [23], a novel 4-level, single-stage inverter that may increase voltage is described. The suggested converter does not require a DC power choke, unlike the cascaded architecture. The topology employs 10 switches and a single capacitor to achieve a gain of 2Xin accordance with [24]. However, there are a large number of switches required for the topology [25], thirteen-level inverters fed by a constant dc voltage are presented. However, these topologies still rely heavily on switching components due to the need for a dc source. In [26], a SC architecture with three gains and a cross-switch is described. The disadvantages of this architecture include a longer discharging time than the charging period of capacitors and more switches [27]. Provides additional details on an active neutral point clamped capacitor (ANPC) inverter that can increase voltage by $1.5\,V_{DC}$. In the present research [28], two PWM techniques, multicarrier sine PWM (MCSPWM) and space-vector PWM (SVPWM), are introduced for NPC-MLI systems. The voltage profile, total harmonic distortion, and common mode voltage is only some of the metrics against which the two approaches are measured and analyzed. Three subcells are coupled in an asymmetrical manner to provide a 125-level output voltage in a unique asymmetrical cascaded MLI. The symmetrical layout of the five output voltage levels is made possible by the subcell's six power switches and two DC sources. It became pricey and complicated as a result of the various sources [29]. In [30], the authors propose a more efficient arrangement of symmetrical and asymmetrical MLI. The number and variety of semiconductor devices have decreased as a result of the quantitative and qualitative improvements made in this field. In [31], a MLI based on a hybrid switching capacitor is presented. A comparative research gaps and the solution proposed in this proposed work are presented in Table 1. There is a fundamental element and a scalable "n" module in this structure. The voltage gain provided and the total number of levels synthesized is both functions of the total number of these "n" modules connected in series. When increasing the voltage by a factor of $1:(k+2)$, the terminal voltage can be scaled to $4k+9$ levels for any given number "k" of "n" modules.

From the above literature review, it can be observed that several constraints are present in the recently developed 7-level SCMLs topologies. More active and passive parts, higher voltage stress, and lower boosting factors are some of them. The main motivations of the proposed MGSCIT can be enlisted as follows:

(1) Less semiconductor devices are needed to produce the same number of output voltage levels at reasonable maximum voltage stresses (MVS) across the switches.

(2) There is a threefold increase in voltage at the output.

(3) The capacitor voltage can be balanced without the use of a separate balancing circuit or sensor.

(4) Half of switches are used for all voltage levels; therefore, losses are low.

(5) It does not require H-bridge for the polarity generation.

(6) There is no need for a magnetic circuit to increase the power output.

Below this section, the suggested paper is structured as follows: Proposed MGSCT, working principle, self-balancing mechanism, and assessment of optimum values of capacitance are described in Section 2. Section 3 demonstrates a method for modulation. Different kinds of losses are discussed in Section 4. Further, ensure the viability and performance of both simulation and experimental

Table 1: Research gaps pertaining to SCMLIs and the solution proposed in this work.

Major research gaps related to SCMLI topologies	Solution offered by the topology proposed in this paper
High value of cost function (CF) as defined in (9): In topologies [9–15, 17–20]	Low value of CF due to reduced component count per level and high-resolution waveform
Low voltage gain, in topologies [10, 11, 20]	Offers a voltage gain of 3
High total standing voltage (TSV), [4, 6, 7, 12, 13, 18, 26]	Single-stage topology with low total standing voltage

assessment are presented in Section 5. Section 6 provides a qualitative review of the benefits and drawbacks of various SCMLIs. Finally, this article concludes with Section 7.

2. Proposed Multigain Switched-Capacitor Inverter Topology

2.1. Circuit Description. Figure 1 shows the circuit representation of the multigain 7-level single phase inverter topology based on the switched-capacitor technique. The proposed MGSCIT consists of two capacitors (C_1, C_2), single-input DC source of magnitude V_{dc}, and nine number active power switches ($S_1 \sim S_9$). Here, the power switches are of two types, one type is conventional IGBTs with antiparallel diode and the other one is IGBTs without antiparallel diode (reverse blocking).

Single input DC source of magnitude V_{dc}, and two switched capacitors C_1, C_2 are utilized to generate 7-level ($\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, and 0) alternating output voltage (v_0) with three-times voltage boosting capability $3V_{DC}$. Table 2 displays the intended switching sequence for both positive and negative levels.

The capacitor C_1 charged to V_{DC} through S_1 and S_5, respectively. The capacitor C_2 charged to $2V_{DC}$ through S_2 and S_4, respectively. The charging path of the capacitors is marked by blue, and the output current path is marked by red dotted arrow headline, respectively. Voltage stress on the switching components is presented in Table 3.

2.2. Explanation of the Voltage Level. The following discussion focuses on the analysis of various voltage levels for the proposed MGSCIT positive half cycle.

State-$\boldsymbol{\sigma_1}$ ($\mathbf{v_0 = 0}$): In this state, the load is short-circuited ($v_0 = 0$) through the active switches the S_6, S_7. The capacitor C_1 is charged to V_{dc} through S_1, S_5 as illustrated in Figure 2(a).

State-$\boldsymbol{\sigma_2}$ ($\mathbf{v_0 = +1V_{dc}}$): In this switching states, the input voltage is directly available at the load terminal by switching ON $S_1 - S_6 - S_9$ simultaneously. The capacitor C_1 is charged to V_{dc} through S_1, S_5 as validated in Figure 2(b).

State-$\boldsymbol{\sigma_3}$ ($\mathbf{v_0 = +2V_{dc}}$): In this state the capacitor C_1 is connected in series with the input source to achieve $v_0 = +2V_{dc}$. The capacitor C_2 is charged through C_1-S_2-V_{dc}-S_4-C_2 to $2V_{dc}$ as shown in Figure 2(c).

State-$\boldsymbol{\sigma_4}$ ($\mathbf{v_0 = +3V_{dc}}$): In this state, the capacitor C_2 connected in series with the input source to achieve the output voltage $v_0 = +3V_{dc}$ across the load terminal as shown in Figure 2(d).

Similar analysis can be done for the negative voltage level and their comparable circuit, refer to Figures 2(e)–2(g).

2.3. Self-Balancing Mechanism and Optimization Technique of Capacitor. As shown in Figure 2, the capacitor C_1 is charged during the level of $\pm 1V_{dc}$, and 0 to V_{dc}, and C_2 charged to $2V_{dc}$ during the voltage level of $\pm 2V_{dc}$. The capacitor C_1 and C_2 discharges their stored energy during the level of voltage $\pm 2V_{dc}$ and $\pm 3V_{dc}$, respectively. The continuous process of charging/discharging over one fundamental cycle of voltage makes the capacitor self-balanced automatically irrespective of load [6]. The voltage ripples of the capacitor play a substantial role in the SC inverter design. These ripples should be maintained within a permissible limit. Lower the values of voltage ripples better are the power quality and vice versa. Moreover, voltage ripples are related to the load value, capacitance, and maximum discharging period of the capacitors. Diagrammatic representation of the control scheme is illustrated in Figure 3(a). Also, reference, carrier, and load voltage are Figure 3(b). The longest discharge times for capacitors C_1 and C_2 are depicted in Figure 3(b) as $(\theta_1, \pi - \theta_1)$ and $(\theta_2, \pi - \theta_2)$, respectively. Hence, the discharge amount of the capacitor C_1, C_2 is calculated as

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} n,$$

$$\Delta Q_{C1} = \int_{\theta_1}^{\pi-\theta_1} I_P \sin(\omega\theta) \mathrm{d}\theta, \tag{1}$$

$$\Delta Q_{C2} = \int_{\theta_2}^{\pi-\theta_2} I_P \sin(\omega\theta) \mathrm{d}\theta.$$

When the load is entirely resistive, the voltage ripple can be expressed as

$$\Delta V_{C1} = \frac{1}{2\pi f c_1} \int_{\theta_1}^{\pi-\theta_1} \frac{2V_{dc}}{R} \mathrm{d}\theta,$$

$$\Delta V_{C1} = \frac{\mathrm{V_c}}{\pi \mathrm{f RC_1}} [\pi - 2\theta_1], \tag{2}$$

$$\Delta V_{C2} = \frac{3V_c}{2\pi f \mathrm{RC_1}} [\pi - 2\theta_2].$$

Wherein, the conducting angle (θ_1, θ_2) can be calculated as

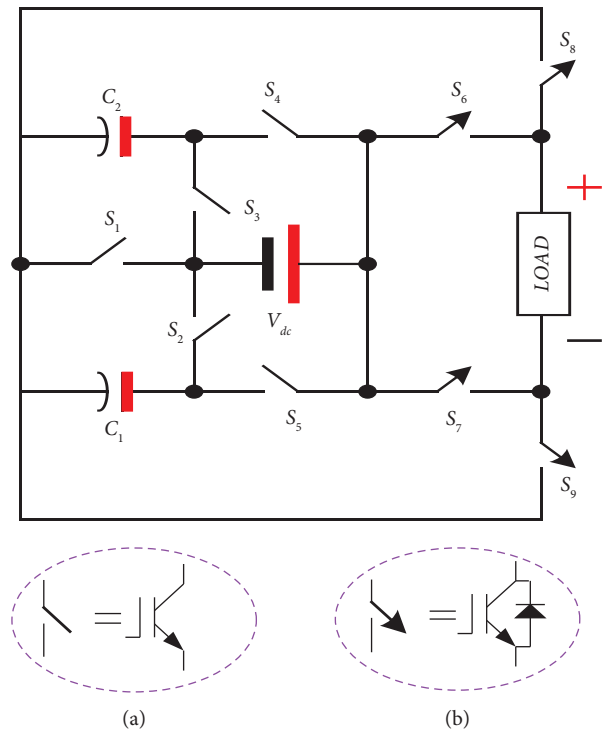


Figure 1: Proposed 7-level MGSC inverter topology: (a) switch without antiparallel diode; (b) switches with antiparallel diode.

Table 2: Switching combinations of MGSCIT.

State	Active switches	v_0 ($^*V_{dc}$)	C_1	C_2
σ_1	$S_1\, S_5 S_6\, S_7$	0	Δ	—
σ_2	$S_1\, S_5 S_6\, S_9$	1	Δ	—
σ_3	$S_2\, S_4 S_6\, S_9$	2	∇	Δ
σ_4	$S_3 S_6\, S_9$	3	—	∇
σ_5	$S_1\, S_5 S_7\, S_8$	−1	Δ	—
σ_6	$S_2\, S_4 S_7\, S_8$	−2	∇	Δ
σ_7	$S_3\, S_7 S_8$	−3	—	∇

Δ = charging, ∇ = discharging, "—" = idle, v_0 = output voltage.

Table 3: Maximum voltage stress on the switching components.

Components	Voltage stress ($^*V_{\mathrm{dc}}$)
S_4, S_5	V_{dc}
$S_1, S_2\, S_3\, S_6, S_7$	$2\,V_{\mathrm{dc}}$
S_8, S_9	$3\,V_{\mathrm{dc}}$
C_1	V_{dc}
C_2	V_{dc}

$$\theta_1 = \frac{\sin^{-1}\left(1\mathrm{Ac}/A_{\mathrm{ref}}\right)}{2\pi f}, \qquad \theta_2 = \frac{\sin^{-1}\left(2\mathrm{Ac}/A_{\mathrm{ref}}\right)}{2\pi f}. \tag{3}$$

3. Switching Strategy

There are primarily three forms of pulse width modulation (*PWM*) [27]: carrier wave PWM, selective harmonic elimination PWM (*SHE-PWM*), and space-vector PWM. Since the switching frequency can be decreased using the SHE-PWM, switching losses can be minimized, and the dc voltage may be used more efficiently. However, putting it into practice is difficult. The SV-PWM technique can be used by inverters with three to five voltage levels. However, due to its complexity, it is unsuitable for inverters that produce more than five voltage levels. In this work, we use a special kind of carrier wave PWMs called phase disposition PWM (*PD-PWM*) to create the switching signals. This approach simplifies the control circuit because it is simple to construct. Six triangular carriers plus a sinusoidal modulation wave are needed to produce pulses for a seven-level inverter. On and off for each switch is determined by a unique logic combination of these pulses. Figure 3(a) shows only the positive half of the cycle being modulated, while a similar method is employed for the negative half of the cycle. Each of the six triangle carriers is broadcast at a constant amplitude (A_c) and frequency (f_c), but with unique phase shifts. The frequency f_o and amplitude A_{ref} characterize a sinusoidal modulation wave. The carrier and reference

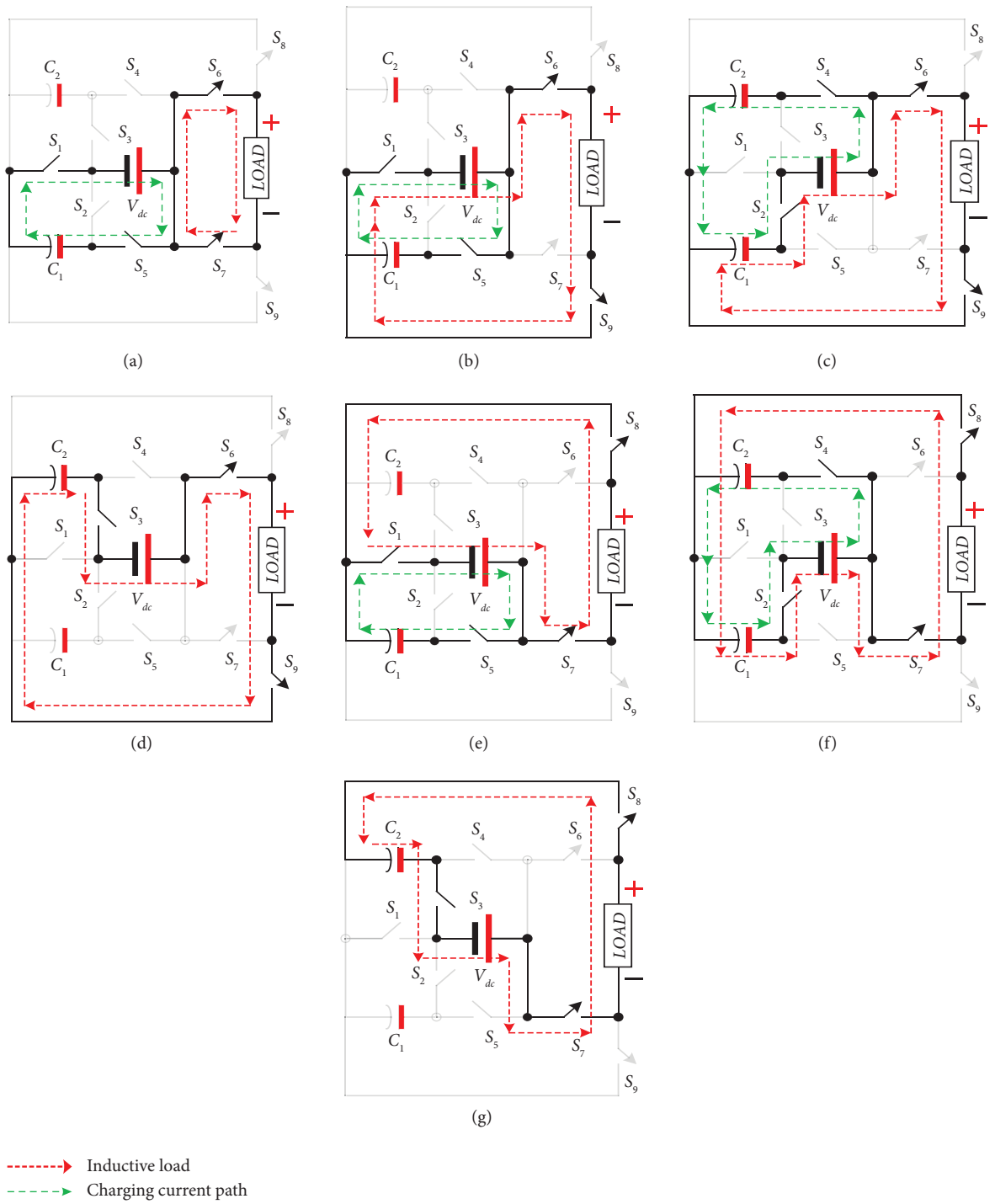
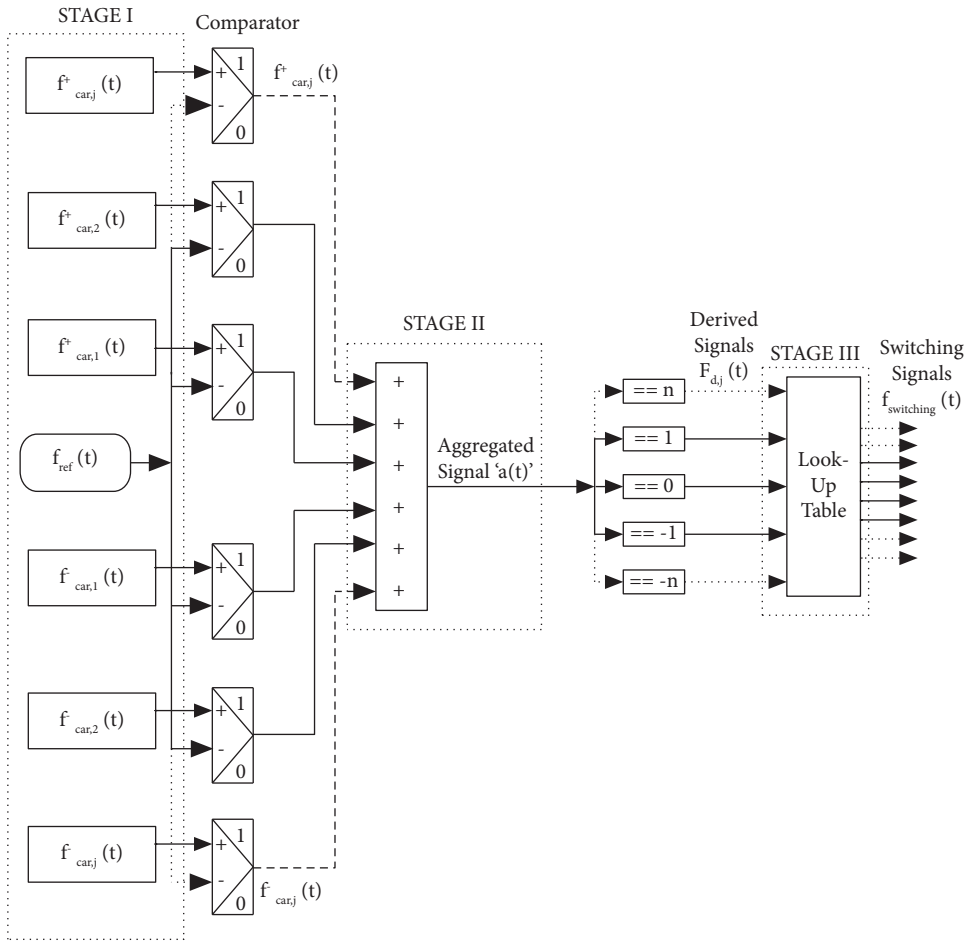


FIGURE 2: Various conduction paths for developing seven levels: (a) $v_0 = 0$; (b) $v_0 = V_{dc}$; (c) $v_0 = 2V_{dc}$; (d) $v_0 = +3V_{dc}$; (e) $v_0 = -1V_{dc}$; (f) $v_0 = -2V_{dc}$; (g) $v_0 = -3V_{dc}$.

waveforms' amplitudes establish the modulation index. The modulation index (M) is thus defined as follows:

$$M = \frac{A_{\text{ref}}}{3A_c}. \tag{4}$$

The suggested inverter can adapt its output to match any changes in modulation index (M). Table 4 presents the link between modulation index (M) and the resulting output level.



(a)

Figure 3: Continued.

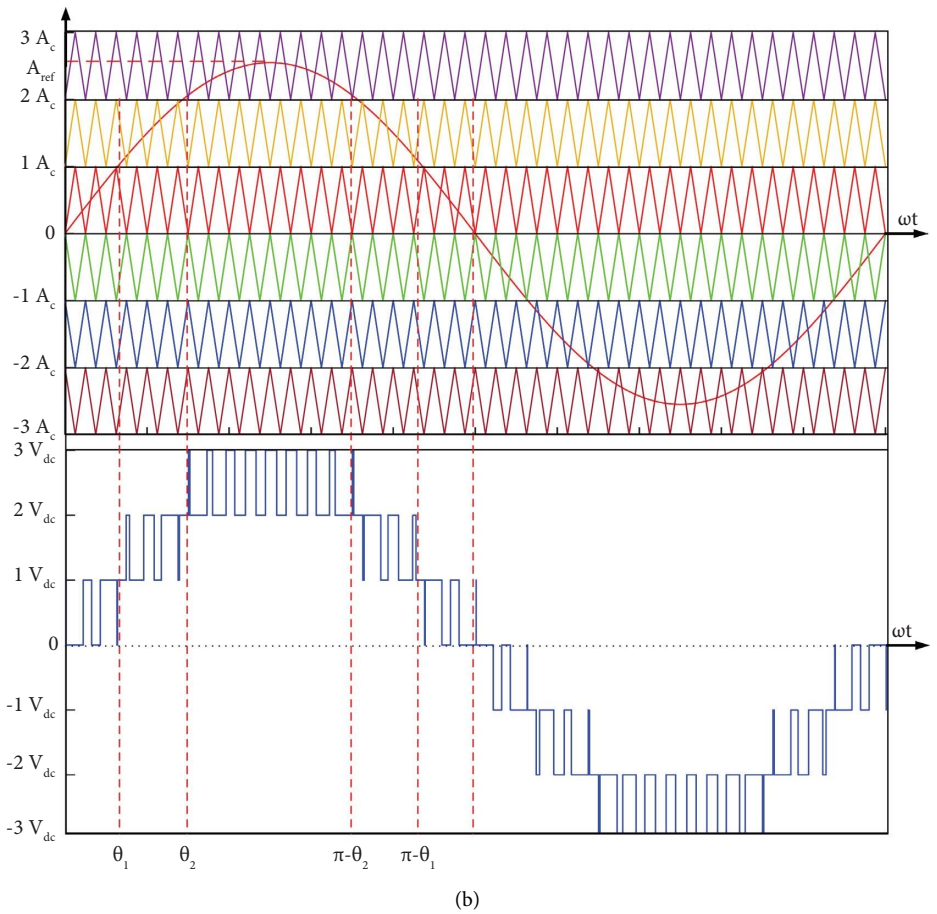


Figure 3: Diagrammatic representation of the (a) control scheme, (b) reference, carrier, and load voltage.

Table 4: Parenthesis of modulation index and output level.

Modulation index (M)	Output level
$0 < M < 1/3$	3
$1/3 < M < 2/3$	5
$2/3 < M < 1$	7

4. Loss Analysis

The proposed MGSCIT has three distinct types of power losses.

4.1. Switching Losses. In the process of switching from one state and another, there is a loss of power, known as switching loss. Therefore, the overall switching power losses can be calculated as [3]

$$P_{\text{sw,loss}} = \frac{f_{\text{sw}}}{6} V_{\text{off}} i(t) [t_{\text{on}} + t_{\text{off}}], \tag{5}$$

where t_{on} and t_{off} are switch on/off times, V_{off} is the blocking voltage, $i(t)$ is the current during the conduction, and f_{sw} is the switching frequency.

4.2. Conduction Losses. This loss is due to the conduction of power switches and diode [15].

$$\begin{aligned} P_{\text{con,loss,sw}} &= V_{\text{on,sw}} I_{\text{sw,avg}} + R_{\text{on,sw}} I^2_{\text{sw,rms}}, \\ P_{\text{con,loss},d} &= V_{\text{on},d} I_{d,\text{avg}} + R_{\text{on},d} I^2_{d,\text{rms}}, \end{aligned} \tag{6}$$

where $V_{\text{on,sw}}$ and $V_{\text{on},d}$ are voltage drop in the on state of the transistor and diode, respectively. $I_{\text{sw,avg}}$ and $I_{\text{sw,rms}}$ are average and RMS current of transistor, respectively. $R_{\text{on,sw}}$ and $R_{\text{on},d}$ are resistance in the on state of the transistor and a diode.

4.3. Ripple Losses (P_{rip}). These losses occur due to the voltage variation of the capacitor and it can be determined as [5]

$$P_{\text{rip}} = f C_i \Delta V^2_{\text{Ci}}. \tag{7}$$

5. Results and Discussion

5.1. Simulated Results. MATLAB/Simulink was used to validate the theory behind the proposed MGSCIT. Table 5 lists all of the input values for the MATLAB/Simulink model. The results of these simulations are depicted in Figure 4. In Figure 4(a) depicts the steady-state analysis of the proposed MGSCIT, which reveals that it produces a 7-level output voltage with equal steps. The magnitude of each step is 50 V. The waveform's maximum values are 150 V.

Table 5: Model parameter for simulation and experimentation.

Circuit parameters	Values
Input source (V_{dc})	50 V
Switching frequency	200 Hz, 5 kHz
Fundamental frequency	50 Hz
Modulation index (MI)	0.95, 0.5, 0.2
Capacitors (C_1, C_2)	470 μF, 1600 μF
Loads	30 Ω, 40 mH
Switches (IGBTs)	FGW30XS65, FGW30X65C

Both the C_1 and C_2 capacitors have achieved equilibrium within the parameters of their respective operating ranges. An inverter's efficacy is determined by its flexibility to respond to changes in load, input voltage, frequency, and the amplitude of modulation waves. The following simulations were run to better evaluate the inverter's functionality under dynamic conditions.

Figure 4(b) displays the simulated outcomes when the load was rapidly altered. It has been observed that quick variations in the load have no effect on the output voltage or the capacitor balancing. Because the voltage on capacitors C_1 and C_2 is balanced at 50 V and 100 V, respectively, sensors and other techniques are unnecessary. These findings demonstrate the inverter's efficiency under various loads.

When the frequency of the modulation wave changes, the proposed inverter can easily readjust to the new conditions. The output voltage and current as a function of frequency are shown in Figure 4(c). The transient response of the inverter is fast enough to allow it to switch between frequencies of 200 and 5000 Hz.

In addition, the value of Ma for the inverter was adjusted in the simulation, as shown in Figure 4(d). In a span of time ranging from 0.1 seconds to 0.14 seconds, Ma is changed twice. In addition to shifts in Ma, the range of possible output values also varies. Whether Ma is 0.95, 0.5, or 0.2, there is no change to the capacitors' natural equilibrium. Convergence of transient processes quickly displays the proposed inverter's enhanced dynamic performance. THD analyses of the proposed inverter are summarized as follows and same is reproduced in revised manuscript. Considering the resistive-inductive load of $R = 40\ \Omega$ and $L = 120$ mH, the FFT analysis of V_0 provides the peak magnitude of the fundamental voltage of 137.2 V with 21.08% of total harmonic distortion (THD) as shown in Figure 4(e). Similarly, the FFT analysis of i_0 provides the peak magnitude of the fundamental current of 2.495 A with 1.74% of THD as shown in Figure 4(f). Plexim software has been used to simulate the proposed MGSCIT to determine its losses. A graphical representation of the distribution of losses is shown in Figure 4(g). Since the capacitors' peak-to-peak ripple values are 2.6 V and 3.7 V, respectively, the ripple loss is estimated to be 3.84 W. Therefore, the overall efficiency of the proposed MGSCIT is 96.2 percent.

5.2. Experimental Validation. To ensure the feasibility of the proposed MGSCIT, it has been validated under steady state and transient conditions by a laboratory prototype. Table 5 provides a summary of the laboratory prototype's specifications. Figures 5(a)–5(e) display the experimental results for both states. Steady-state performance is depicted in Figure 5(a). According to observations, the proposed MGSCIT produces a 7-level output with a peak voltage of 150 V and both the capacitors are self-balanced with small voltage ripples. Transient conditions result such as sudden load change, switching frequency, and magnitude of modulation index (*MI*) are shown in Figures 5(b)–5(d). The experimental results for the sudden shift in load circumstance have been presented in Figure 5(b). Voltage level has been confirmed to be constant at its maximum value of 150 V. In response to this variation in load, capacitors' discharging current is affected, and the capacitors' voltage ripples decrease in value. The change in magnitude of MI is shown in Figure 5(c). It has been observed that it generates 7-level, 5-level, and 3-level for the MI of 0.95, 0.5, and 0.2, respectively.

The change of switching frequency (200 Hz–5 kHz) is properly adapted by the proposed MGSCIT which is shown in Figure 5(d). It is also observed from the waveform that the inverter quickly changes its transient response in both the switching frequencies. Figure 5(e) depicts the efficiency of the inverter at varying power levels. It is clear from the provided curve that maximum efficiency is reached at a specific power level, whereas efficiency drops off sharply before and after. Experimentally validating the proposed topology is depicted in Figure 5(f) as a prototype module. The overall experimental results show a good steady state and transient performance of the proposed MGSCIT.

5.3. Analysis of Results and Practical Applications. As evident from both simulation and experimental outcomes concerning the suggested design, a 7-level waveform is produced with a voltage gain thrice that of the input voltage. Considering potential applications for the recommended topology, various options have emerged from a comprehensive exploration of the literature on Switched-Capacitor Multilevel Inverters (*SCMLIs*).

5.3.1. High-Frequency AC Distribution. The high-frequency alternating current (*HFAC*) power distribution system (*PDS*) has gained traction due to its benefits in various applications, such as telecommunication, spacecraft, and computer systems [28]. HFAC PDS offers reduced power conversion stages, smaller transformer sizes, and compact filters. Notably, this technology is finding new applications in microgrids, buildings, and electric vehicles [29, 32]. However, challenges with capacitor voltage imbalances limit the feasibility of standard multilevel topologies with more than five levels [30]. To address this, Switched-Capacitor Multilevel Inverters (*SCMLIs*) are increasingly preferred for HFAC applications [8], eliminating the need for complex solutions and additional boost converters at low-voltage sites.

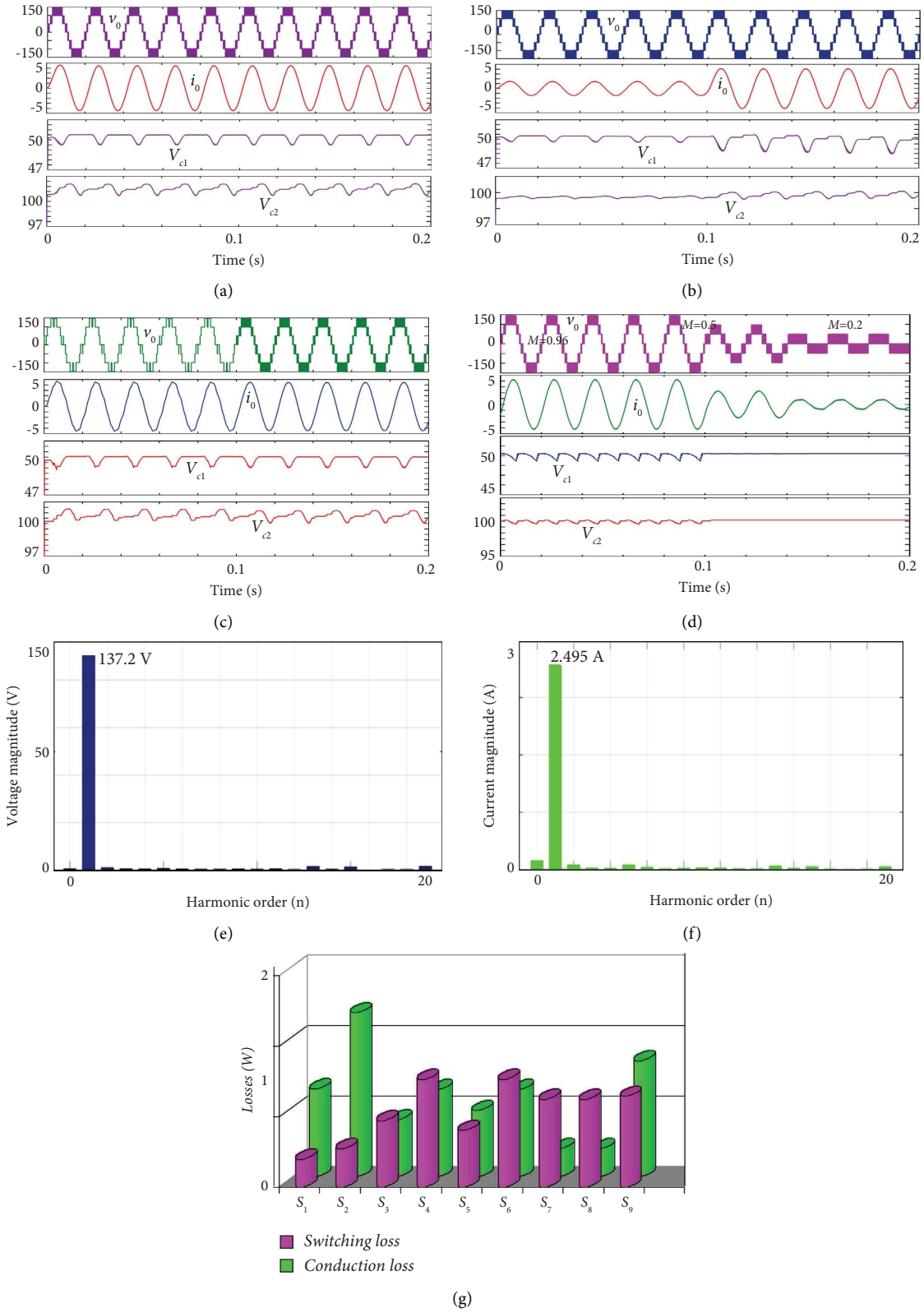
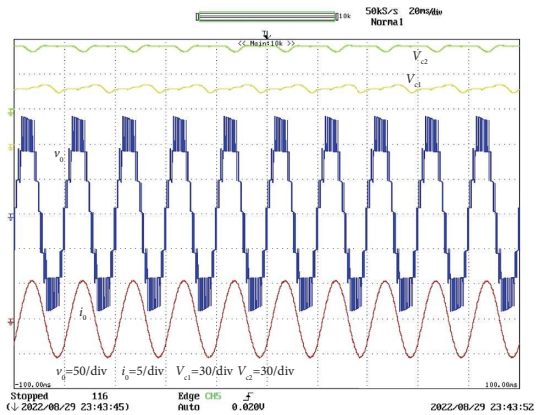


FIGURE 4: Simulation results: (a) steady-state analysis for RL-load, (b) variation in RL-load, (c) variation in frequency, (d) variation in MI, (e-f) voltage and current THD, (g) losses distribution graph.



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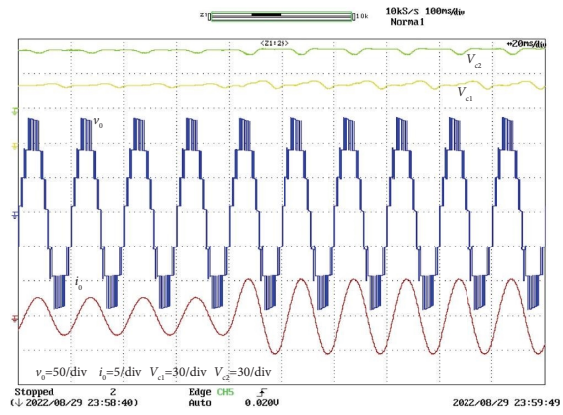

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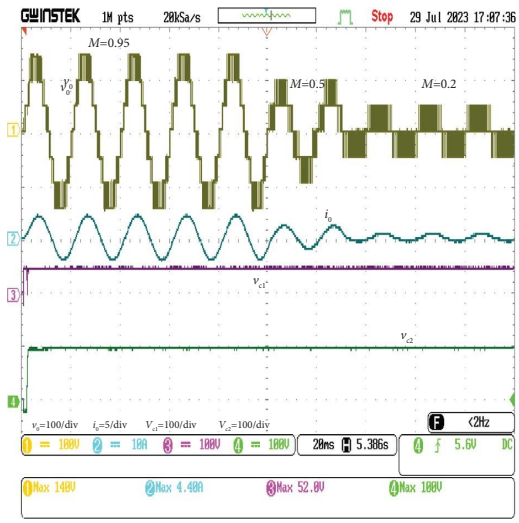

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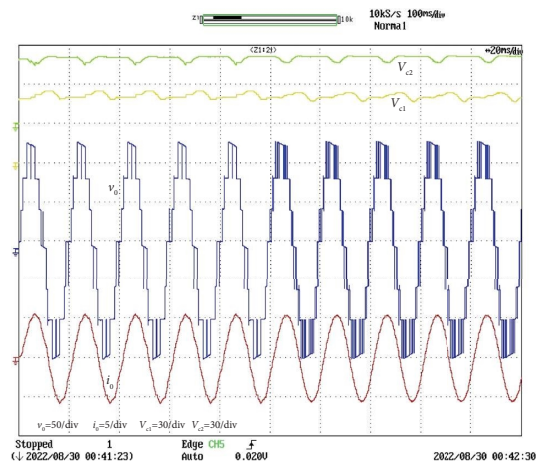

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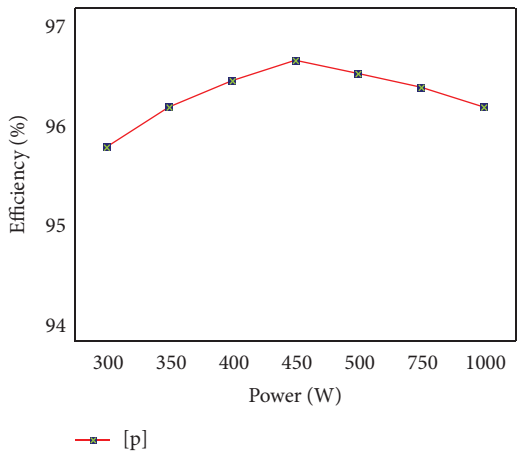
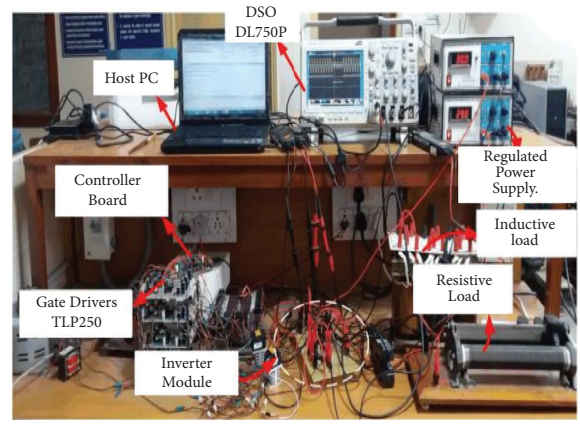


(e)



(f)

FIGURE 5: Experimental results: (a) steady state, (b) variation in load, (c) variation in switching frequency, (d) variation in MI, (e) efficiency curve, (f) prototype module.

Table 6: Comparative analysis with recent topologies.

Ref	N_{sw}	N_c	N_{dri}	N_{ad}	A	B	C	CF	
								$\alpha = 0.5$	$\alpha = 1.5$
[8]remove	14	2	14	2	3	4.57	4.5	4.89	5.53
[9]	16	2	14	—	3	4.57	5.3	4.57	5.7
[10]	10	4	8	—	1.5	3.14	5	3.5	4.21
[11]	10	4	10	—	1.5	3.14	6.3	3.59	4.49
[13]	8	2	8	2	3	2.85	6	3.3	4.14
[12]	8	2	8	2	3	2.85	6.3	3.3	4.2
[14]	12	3	12	—	3	3.85	5.3	4.23	5
[15]	10	3	10	—	3	3.28	6.6	3.75	4.7
[17]	10	2	10	—	3	3.14	6	3.57	4.42
[18]	10	3	10	—	1.5	3.28	5.3	3.66	4.46
[19]	9	3	9	2	3	3.28	5.6	3.64	4.36
[20]	9	2	9	—	1.5	2.85	6	3.3	4.14
[33]	10	3	9	—	1.5	3.14	6	3.57	4.42
[34]	8	2	8	1	3	2.71	6	3.14	4
[32]	8	4	8	2	1.5	3.14	6.67	3.62	4.57
(P)	9	2	9	—	3	2.85	6	3.28	4.14

N_{sw}: no. of switches, N_c: no. of capacitors, N_{dri}: no. of the driver, N_{ad}: no. of auxiliary diode, A: gain, B: component count per level C: per-unit total standing voltage, P: proposed topology.

Table 7: Cost comparison of the newly introduced single-source topology to the proposed 7-level topology.

Component	Part number	Rating	Unit price ($)	[18]	[17]	[16]	[14]	[12]	(P)
IGBT*	IRGP4086PBF	300 V, 70 A	1.87	—	—		—	—	5
	FGPF30N30D	300 V, 30 A	4.68	5	4	8	8	—	2
	IKW30N60T	600 V, 60 A	5.65	2	4	2	4	4	—
	STGWA15H129DF2	1200 V, 30 A	8.67	2	2		—	4	—
Diode*	VS-20ETF06SLHM3	600 V, 20 A	3.1	2	4	4	—	2	2
Capacitor*	ALF20G102KL600	600 V, 1000 μF	48.62	—	—	—		—	
	ALS81H102DE350	300 V, 1000 μF	10.55	—	—	—		—	2
	ALF20G102EC200	200 V, 1000 μF	7.31	2	2	2	2	2	2
	ELG108M100AR2AA	100 V, 1000 μF	3.18	—	—	—			
Gate driver	IR2110		1.8	9	10	10	11	8	9
		Total cost($)		168.2	103.7	93.76	94.46	92.5	76.83

*https://www.digikey.com.

5.3.2. Photovoltaic (PV) Power Generation and Electric Vehicle (EV) Traction Systems. Generating power from renewable sources like photovoltaic (*PV*) systems has limitations due to the relatively low available power. To overcome this, voltage boosting is typically achieved through methods such as cascading PV modules, implementing dc-dc boost inverters, or using step-up transformers. Unfortunately, these techniques come with drawbacks including increased component count, costs, size, and power losses [31]. However, the adoption of Switched-Capacitor Multilevel Inverters (*SCMLIs*) offers advantages like efficient voltage gain, capacitor self-balancing, high-resolution waveforms for grid compatibility, and reduced filtering requirements [33].

6. Comparative Analysis

This section provides a comparison with the current state-of-the-art 7-level topologies. The detail comparative study is shown in Table 6, which shows the performance of all topologies. The common aspects among the 7-level selected topologies are single-input dc source and boosting capability. The comparison has been made based on the following main indicators, numbers of switching components, total standing voltage, gain, and cost function. The component count per level ($F_{C/L}$) and cost function (CF) can be written as [19, 35]. α is the weight factor and depending on the value of the switching components or TSV, it can also assume on one of three

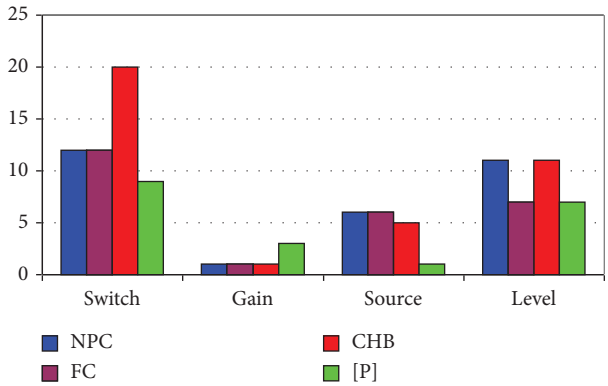


Figure 6: Graphical comparisons with tradition topologies.

possible values ($\alpha < 1, \alpha > 1, \alpha = 1$). $\alpha < 1$ means the switching components are given more importance than TSV. $\alpha > 1$ means TSV is given more importance than the switching components.

$$F_{C/L} = \frac{N_{sw} + N_{dri} + N_c + N_{ad}}{N_l}, \tag{8}$$

$$\text{CF} = \frac{N_{sw} + N_{dri} + N_c + N_{ad} + \alpha \text{TSV}_{pu}}{N_l}. \tag{9}$$

TSV_{pu} is the per-unit total standing voltage which is the sum of the peak inverse voltage of the diode and maximum blocking voltage across the switch to the peak amplitude of the load voltage.

$$\text{TSV}_{pu} = \frac{[\text{TSV} + \text{PIV}]}{V_{max}}. \tag{10}$$

As per Table 6, the suggested MGSCIT has the least $F_{C/L}$ among [8–12, 14–20, 32, 33]. The proposed MGSCIT has a higher enhancing factor than [10, 11, 18, 20]. In contrast to the proposed MGSCIT, the topologies [10–17, 19] all shares the same boosting factor. When compared to other topologies, the suggested MGSCT offers the lowest cost function. Considering these factors, the suggested MGSCIT emerges as the most cost-effective of the current topologies. A cost comparison has been explored and presented in Table 7 to further highlight the various merits of the suggested MGSCIT. For this cost analysis, all topologies have been configured with the same voltage parameters. In addition, all factors were given equal weight in the cost analysis. Table 7 shows that the suggested MGSCIT has the lowest component cost compared to the other topologies. Figure 6 displays a visual contrast between conventional and contemporary topologies. The visual comparisons clearly demonstrate that the recommended design surpasses others in performance.

7. Conclusion

This paper introduces novel 7-level MGSCIT to reduce the number of active switches and gate drivers. This results in minimized overall costs and device count. In addition, the proposed design capacitances possess a self-balancing nature. A simple PWM scheme based on logic gates has been utilized, eliminating the need for sensors to balance SC voltages. This enhancement contributes to the cost-effectiveness of the proposed topology. The effectiveness of the design is validated through the presented simulation and experimental results, which confirm its operational principles and its ability to manage various load scenarios. Furthermore, a comprehensive comparative study underscores the advantages of the proposed topology in contrast to recent studies, highlighting its suitability for diverse applications, such as grid-connected photovoltaic systems. Furthermore, the drawbacks associated with switched capacitor multilevel inverters (MLIs) include high inrush, dimensions, expenses, and imbalanced capacitor voltage. Future research directions to minimize high inrush current and capacitance voltage balancing when one capacitor is used to charge another capacitor.

Data Availability

The data used to support the findings of this study are available from the corresponding authors upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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