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*Research Article*

# Optimized Control for MMCs with Reduced Power Loss and Extended Lifetime

**Jifeng Zhao,[1] Jia Pei,[1] Yun Sun,[2] Rujin Wang,[2] Jun Hang,[1] and Shichuan Ding [1]**

[1]*College of Electrical Engineering and Automation, Anhui University, Hefei, China*
[2]*State Key Laboratory of High-End Compressor and System Technology, Hefei, China*

Correspondence should be addressed to Shichuan Ding; dsc@ahu.edu.cn

Modular multilevel converters (MMCs) are widely applied to medium and high voltage occasions. The total power consumption of the submodule (SM) and the maximum power consumption of power devices in the SM are related to the operating costs and lifetime of the MMC. Existing literature only considers total power loss optimization or maximal power consumption optimization in MMC's SM. In this article, a reduced loss and extended lifetime power loss optimum control (RLEL-PLOC) is introduced to inject the first-best second harmonic circulation into the MMC's arm current. Compared with the conventional power loss optimization control, the proposed control could decrease the maximal power consumption of the semiconductor devices without increasing the total loss of the SM. According to study results of the MMC, compared with the circulating current suppression control (CCSC) method, the total power consumption of the SM could be reduced by 4.2% and the maximal power dissipation in the SM could be reduced by 5.4% with RLEL-PLOC. PSCAD simulation and MMC prototype experiment are also carried out, and the research results verified the availability of the put forward RLEL-PLOC for MMCs.

## 1. Introduction

Modular multilevel converters (MMCs) were put forward by A. Lesnicar at the beginning of the 21st century [1, 2]. Recently, MMCs have attracted widespread attention from multiple industries because of its superiorities of modularization, relatively low power dissipation, better power quality, and convenient scalability [3, 4]. The modular multilevel converter plays a significant role in the occasions of energy storage, drive systems for hydrogen fuel cell compressor motors, and renewable energy grid connection [5].

The MMC is composed of numerous submodules (SMs), each of which contains multiple power devices. Power loss in these power devices constitutes a significant part of operating costs [6, 7]. Therefore, decreasing the total energy loss is essential for the MMC's economical operation [8, 9]. The maximal power consumption of the semiconductor devices would affect the lifetime of MMCs [10, 11].

Currently, the existing methods to optimize power loss for MMCs are mainly divided into three types: the SM devise majoritization-based technique, the switching frequency diminution-based technique, and the circulation dominate-based technique. Reference [12] proposes an SM with a shunt group diode with inferior conduction voltage descent to optimize the MMC's loss. References [13, 14] propose an SM with an inferior conduction voltage descend power devices that can optimize the MMC's power loss. However, the SM devises the majoritization-based technique to increase the system design complexity.

Reducing the switching frequency can also optimize the power loss of MMCs. References [15, 16] present a capacitor voltage equilibrium technology to lower the power consumption at low-switching frequency. Reference [17] brings in a mixed pulse width modulation (PWM) which can operate with the one-time frequency modulation method of part SMs to optimize power loss. However, the low switching frequency would affect the MMC's output current wave.

Circulating current control is widely adopted in the power loss optimization of MMCs. Reference [9] proposes an optimization method to control the SM's power consumption and the SM's capacitor voltage fluctuation value of MMC by adjusting the second harmonic circulation current (SHCC). Literature [18] presents a circulating current suppression control (CCSC) method to optimize the power loss by eliminating the SHCC of MMC's arm current. Literature [19] presents an SHCC control method to reduce the submodule capacitance value and the power consumption provoked by the SHCC injection. Reference [20] presents an SHCC control method by decreasing the MMC arm current's maximum value to decrease the power consumption of MMCs. Literature [21] introduces an SHCC control technique by controlling the current rating of semiconductor devices to optimize MMC's power loss. Literature [22] proposes a power consumption majorization control in view of the infusion of the supreme second harmonic circulation current into MMC's arm current to decrease MMC's power loss. Literature [23] puts forward a power consumption majorization dominant to improve the power consumption in SMs. However, the circulating current dominate-based technology either only considers the total power loss optimization and neglects the maximal power consumption optimization in SMs or only considers the maximum power loss optimization, and the total power consumption optimization is not considered. Simply combining the abovementioned methods cannot optimize the total loss and maximum loss at the same time.

In conclusion, the SM devise majorization-based technique can optimize the MMC's power loss, while increasing the system design complexity. Reducing the switching frequency can also optimize the power loss of MMCs, but the low switching frequency would affect the MMC's output current wave. This paper proposes a multi-target power loss optimum control (RLEL-PLOC) by inpouring first-best second harmonic circulation into the bridge arm. The contribution of this paper can be summarized as follows:

(1) The proposed RLEL-PLOC can achieve total power loss optimization and maximal power dissipation optimization in SMs, which can improve the energy transmission efficiency to reduce the operating costs of the MMC and reduce the power loss stress of the semiconductor device with the maximum power dissipation in SMs to improve the lifetime of MMCs simultaneously.

(2) Using the circulating current control to optimize the power loss of MMCs to avoid increasing the system design complexity and reducing the switching frequency would affect the MMC's output current wave.

(3) Compared with CCSC, capacitor voltage ripples could be reduced under most operating conditions with the proposed RLEL-PLOC, which can improve the economy and portability of the MMC.

The other parts of the article are arranged as follows. Part II represents the MMC including the formation of MMCs and the circulating current of MMCs. Part III puts forward the RLEL-PLOC for MMCs. Sections IV and V introduce the simulation and experimental research of MMCs, respectively, to verify the RLEL-PLOC. In the end, Part VI proposes the summary.

## 2. Descriptions of MMCS

*2.1. Composition of the MMC.* The principal collocation of the MMC is displayed in Figure 1(a), including 6 arms. Each arm is made up of $n$ tantamount submodules and an inductance, $L_s$. Figure 1(b) demonstrates the $i$-th ($i = 1, 2, \ldots, n$) submodule in phase A's upper arm, which contains the switch/diode ($T_1/T_2$, $D_{11}/D_2$), and the capacitor $C_i$ [24]. Normally, the $i$-th drive signal $S_i$ controls the $i$-th SM as

$$S_i = \begin{cases} 1, & T_1 \text{ is on and } T_2 \text{ is off,} \\ 0, & T_1 \text{ is off and } T_2 \text{ is on.} \end{cases} \quad (1)$$

As is displayed in Table 1, there are two statuses of the submodule, which are "On" status and "Off" status. Once $S_i = 1$, the submodule is in "On" and the export voltage $u_i$ is equivalent to the voltage $u_{ci}$. When $S_i = 0$, the submodule is in "Off" and $u_i$ equals 0. In the "On" status, the charge or discharge of the SM capacitor $C_i$ is regulated by the bridge arm's current direction. As seen in Figure 1(b), Under the "On" status, if bridge arm current $i_{au} > 0$, the electric capacity is charged, increasing the voltage $u_{ci}$, and if $i_{au} < 0$, the capacitor discharged, resulting in abate of the capacitor voltage $u_{ci}$. In the "Off" status, the relevant capacitor is by way, and voltage $u_{ci}$ keeps constant, despite the bridge arm current direction [23, 24].

*2.2. Circulating Current of the MMC.* In case the power grid voltage latitude and phase position are $E_m$ and 0, the power grid's current $i_{ga}$ in the A phase is

$$i_{ga}(t) = I_m \sin(\omega t + \varphi), \quad (2)$$

with

$$\begin{cases} I_m = \dfrac{\sqrt{P^2 + Q^2}}{3E_m/2}, \\[3mm] \varphi = tg^{-1}\left(\dfrac{Q}{P}\right), \end{cases} \quad (3)$$

where $I_m$ denotes grid current latitude, $\varphi$ denotes grid power factor angle, $P$ denotes grid active power, $Q$ denotes grid reactive power, and $\omega$ denotes the fundamental angular frequency.

Phase A's arm current could stand for as

$$\begin{cases} i_{au} = \dfrac{i_{dc}}{3} + \dfrac{i_{ga}}{2} + i_{2fa}, \\[3mm] i_{al} = \dfrac{i_{dc}}{3} - \dfrac{i_{ga}}{2} + i_{2fa}, \end{cases} \quad (4)$$
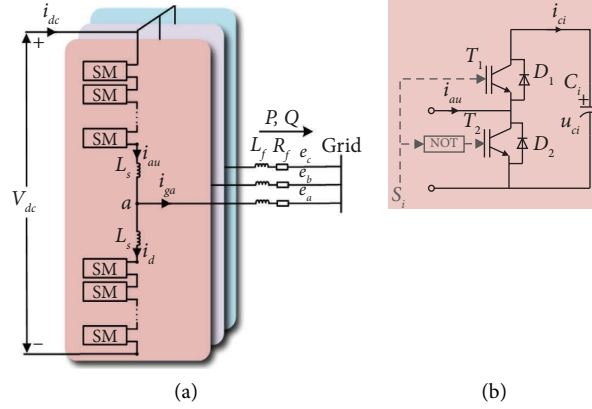
FIGURE 1: (a) Structure schematic diagram of MMC; (b) submodule formation.

TABLE 1: Operation statuses for SMs.

| SM status | $S_i$ | $T_1$ | $T_2$ | $u_i$ | $i_{au}$ | $C_i$ | $u_{ci}$ |
|---|---|---|---|---|---|---|---|
| On | 1 | On | Off | $u_{ci}$ | ≥0 | Charge | Ascend |
| | | | | | <0 | Discharge | Debased |
| Off | 0 | Off | On | 0 | ≥0 or <0 | Byway | Invariant |

TABLE 2: On-state circumstances in SM.

| Operating state | $S_i$ | $i_{au}$ | $T_1$ | $D_1$ | $T_2$ | $D_2$ |
|---|---|---|---|---|---|---|
| 1 | 1 | >0 | 0 | $i_{au}$ | 0 | 0 |
| 2 | | <0 | $-i_{au}$ | 0 | 0 | 0 |
| 3 | 0 | >0 | 0 | 0 | $i_{au}$ | 0 |
| 4 | | <0 | 0 | 0 | 0 | $-i_{au}$ |

where $i_{au}$ and $i_{al}$ are the current of the upper bridge arm and lower bridge arm. $i_{2fa}$ is phase A's second harmonic circulation, which could be described as

$$i_{2fa}(t) = I_{2fm} \sin(2\omega t + \theta_{2f}),\qquad(5)$$

where $I_{2fm}$ and $\theta_{2f}$ are the latitude and phase position of the $i_{2fa}$. $i_{dc}$ is the direct current (DC) side current and can be described as

$$i_{dc} = \frac{P}{V_{dc}},\qquad(6)$$

where $V_{dc}$ is the dc-link voltage.

## 3. Proposed Multitarget Power Loss Optimal Strategy for the MMC

*3.1. Power Loss in the SM.* The power loss in three-phase MMC is majorly produced by the switches ($T_1/T_2$) and the diodes ($D_1/D_2$), including the on-state loss and switching loss [6]. Table 2 describes the on-state situation of the power devices in the $i$-th SM [23].

(1) Once $i_{au} < 0$ and $S_i$ is 1, the $i_{au}$ runs past $T_1$ and $T_1$'s current is $i_{T1} = -i_{au}$. In other situations, $i_{T1} = 0$. Therefore, the conduction loss $P_{T1\_con}$ of $T_1$ is

$$P_{T1\_con} = \frac{1}{T}\int_0^T i_{T1} \cdot S_i \cdot (U_{T0} + R_{T0} \cdot i_{T1} \cdot S_i)\mathrm{d}t,\qquad(7)$$

where $U_{T0}$ and $R_{T0}$ are on-state zero-current collector-emitter voltage and on-state collector-emitter resistance for the switch, respectively. $T$ is the fundamental cycle and $T = 2\pi/\omega$.

(2) Once $i_{au} > 0$ and $S_{ii}$ is 1, the $i_{au}$ runs past $D_1$ and $D_1$'s current is $i_{D1}$ is equal to $i_{au}$. In other situations,

$i_{D1} = 0$. Therefore, the conduction loss $P_{D1\_con}$ of $D_1$ is

$$P_{D1\_con} = \frac{1}{T}\int_0^T i_{D1} \cdot S_i \cdot (U_{D0} + R_{D0} \cdot i_{D1} \cdot S_i)\mathrm{d}t,\qquad(8)$$

where $U_{D0}$ and $R_{D0}$ are on-state zero-current voltage drop and on-state resistance for the diode, respectively.

(3) Once $i_{au} > 0$ and $S_i$ is 0, the $i_{au}$ runs past $T_2$ and $T_2$'s current $i_{T2}$ is equal to $i_{au}$. In other situations, $i_{T2} = 0$. Therefore, the conduction loss $P_{T2\_con}$ of $T_2$ is

$$P_{T2\_con} = \frac{1}{T}\int_0^T i_{T2} \cdot (1 - S_i) \cdot [U_{T0} + R_{T0} \cdot i_{T2} \cdot (1 - S_i)]\mathrm{d}t.$$
$$(9)$$

(4) Once $i_{au} < 0$ and $S_i$ is 0, the $i_{au}$ runs past $D_2$ and $D_2$'s current is $i_{D2}$ is equal to $-i_{au}$. In other situations, $i_{D2} = 0$. Therefore, conduction loss $P_{D2\_con}$ of $D_2$ is

$$P_{D2\_con} = \frac{1}{T}\int_0^T i_{D2} \cdot (1 - S_i) \cdot [U_{D0} + R_{D0} \cdot i_{D2} \cdot (1 - S_i)]\mathrm{d}t.$$
$$(10)$$

The switching loss of power devices comprises the open power consumption and shutoff power consumption of the switch and the opposite recovery power consumption of the diode. Table 3 shows the switching circumstances of the power device in SMs.

(1) Once $i_{au} > 0$ and $S_i$ varies from 1 to 0, the diode $D_1$ shuts off and the switch $T_2$ opens. The reverse-recovery loss $P_{D1\_rec}$ and open loss $P_{T2\_on}$ are

TABLE 3: Switching situations in SM.

| $i_{au}$ | $S_i$ | Switch movement | | Switching loss |
| | | Turn off | Turn on | |
| --- | --- | --- | --- | --- |
| >0 | $1 \longrightarrow 0$ | $D_1$ | $T_2$ | $P_{rec\_D1}, P_{on\_T2}$ |
| | $0 \longrightarrow 1$ | $T_2$ | $D_1$ | $P_{off\_T2}$ |
| <0 | $1 \longrightarrow 0$ | $T_1$ | $D_2$ | $P_{off\_T1}$ |
| | $0 \longrightarrow 1$ | $D_2$ | $T_1$ | $P_{rec\_D2}, P_{on\_T1}$ |

$$\begin{cases} P_{D1\_rec} = \dfrac{1}{T} \sum_0^T \left[ E_r(i_{D1}(t)) \cdot \left( \dfrac{U_c}{U_r} \right) \right], \\[4mm] P_{T2\_on} = \dfrac{1}{T} \sum_0^T \left[ E_o(i_{T2}(t)) \cdot \left( \dfrac{U_c}{U_r} \right) \right], \end{cases} \quad (11)$$

where $E_r$ is the opposite-recovery capacity of the diode and $E_o$ is the open capacity of the switch. $U_c$ is the submodule capacitor voltage mean value, and $U_r$ is the test voltage in the manufacturer's manual.

(2) Once $i_{au} > 0$ and $S_i$ varies from 0 to 1, the $D_1$ opens and the $T_2$ shuts off. The turn-off loss $P_{T2\_off}$ can be described as

$$P_{T2\_off} = \frac{1}{T} \sum_0^T \left[ E_f(i_{T2}(t)) \cdot \left( \frac{U_c}{U_r} \right) \right], \quad (12)$$

where $E_f$ is the shutoff capacity of the switch.

(3) Once $i_{au} < 0$ and $S_i$ varies from 1 to 0, the diode $D_2$ opens and the switch $T_1$ shuts off. The turn-off loss $P_{T1\_off}$ could be described as

$$P_{T1\_off} = \frac{1}{T} \sum_0^T \left[ E_f(i_{T1}(t)) \cdot \left( \frac{U_c}{U_r} \right) \right]. \quad (13)$$

(4) Once $i_{au} < 0$ and $S_i$ varies from 0 to 1, the diode $D_2$ shuts off and the switch $T_1$ opens. The reverse-recovery loss $P_{D2\_rec}$ and turn-on loss $P_{T1\_on}$ could be described as

$$\begin{cases} P_{D2\_rec} = \dfrac{1}{T} \sum_0^T \left[ E_r(i_{D2}(t)) \cdot \left( \dfrac{U_c}{U_r} \right) \right], \\[4mm] P_{T1\_on} = \dfrac{1}{T} \sum_0^T \left[ E_o(i_{T1}(t)) \cdot \left( \dfrac{U_c}{U_r} \right) \right]. \end{cases} \quad (14)$$

The total power loss $P_{T1}, P_{D1}, P_{T2}$, and $P_{D2\_}$ of the $T_1, D_1, T_2$, and $D_2$ can be expressed as

$$\begin{cases} P_{T1} = P_{T1\_con} + P_{T1\_on} + P_{T1\_off}, \\[2mm] P_{D1} = P_{D1\_con} + P_{D1\_rec}, \\[2mm] P_{T2} = P_{T2\_con} + P_{T2\_on} + P_{T2\_off}, \\[2mm] P_{D2} = P_{D2\_con} + P_{D2\_rec}. \end{cases} \quad (15)$$

The total power consumption $P_{loss}$ of the SM can be written as

$$P_{loss} = P_{T1} + P_{D1} + P_{T2} + P_{D2}. \quad (16)$$

Figure 2 describes the power consumption of the semiconductor power devices in the MMC's SM running with the various operating conditions $\varphi$, wherein the CCSC [18] is employed. The Infineon power device module FZ750R65KE3 is employed in MMCs. The power consumption of semiconductor devices in SMs can be calculated based on (7)–(15) [25]. In Figure 2, the power consumption of semiconductor power devices in the SM trans with the alter of power operating conditions $\varphi$.

Figure 3 describes the power consumption in the SMs, where the CCSC is employed. The total power consumption $P_{loss}$ in the SM could be calculated according to (16). In Figure 3, the total power consumption $P_{loss}$ of the SM trans along with the trans of operation conditions.

### 3.2. Proposed Multitarget Power Loss Optimization Method.
As shown in Figure 4, this paper proposes RLEL-PLOC for the MMC, which can largely decrease the maximal power consumption of the semiconductor devices in SMs without increasing the total power consumption of the submodule. This method will inject the first-best second harmonic current into the MMC's bridge arm, for the sake of improving the efficiency and lifetime of the MMC.

At an assigned $P$ and $Q$, the $I_m$ and $\varphi$ could be derived in view of (3) and the grid current $i_{ga}$ could be derived in view of (2). The DC side current $i_{dc}$ could be derived according to (6). In Figure 4, multifarious $i_{2fa}$ is thought of with diverse latitude and phase position pairs $(I_{2fm}, \theta_{2f})$ of the second harmonic current. In every pair of $(I_{2fm}, \theta_{2f})$, according to (4), we can obtain the upper arm current $i_{au}$. The power loss
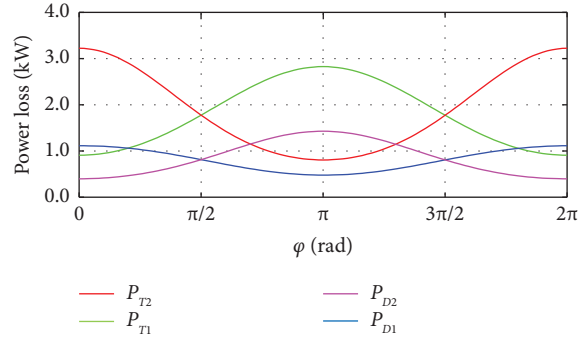
FIGURE 2: Power consumption of the semiconductor devices in SMs under various operating conditions.
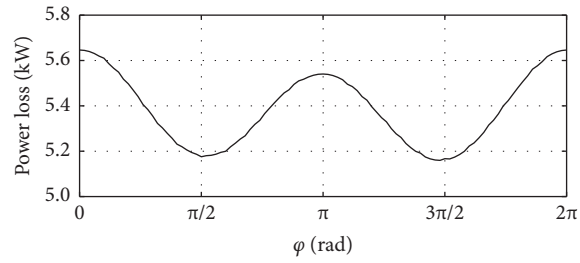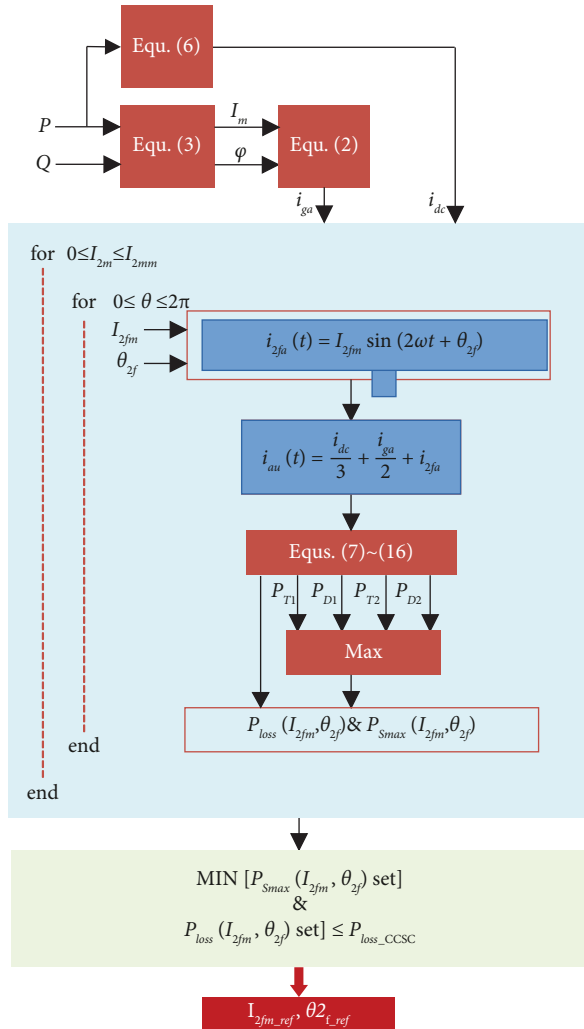


FIGURE 3: SM's power consumption.



FIGURE 4: Proposed RLEL-PLO method.

$P_{T1}$, $P_{D1}$, $P_{T2}$, and $P_{D2}$ and the total power loss $P_{loss}$ could be calculated in view of (7)–(16). The maximum power loss $P_{Smax} = \text{Max}(P_{T1}, P_{D1}, P_{T2}, P_{D2})$ in the SM can be obtained under each pair of ($I_{2fm}$, $\theta_{2f}$). The RLEL-PLO algorithm needs to be satisfied

$$\text{MIN}\left[P_{\text{Smax}}\left(I_{2\text{fm}}, \theta_{2f}\right)\right],$$
$$\text{s.t.} \qquad\qquad\qquad\qquad\qquad (17)$$
$$P_{\text{loss}}\left(I_{2\text{fm}}, \theta_{2f}\right) \leq P_{\text{loss\_CCSC}},$$

where $P_{loss\_CCSC}$ is the SM's total power loss with CCSC. In (17), we minimize the power loss set ($P_{Smax}$ set), meanwhile making the [$P_{loss}$ set] not exceed $P_{loss\_CCSC}$. According to the constraint conditions shown in Figure 4, the optimal second harmonic circulation reference values ($I_{2fm\_ref}$, $\theta_{2f\_ref}$) that meet the conditions can be obtained by mathematically solving (17).

### 3.3. Proposed Multitarget Optimization Control.

Figure 5 describes the MMCs' RLEL-PLOC which is proposed. Figure 5(a) represents the MMCs' $P$ control and $Q$ control [25], where the dq frame components of the grid current and voltage are $i_d$, $i_g$ and $e_d$, $e_f$, respectively. The filtered inductance of the grid is $L_f$. The voltage phase angle of the grid side is $\theta_e$. The $i_{d\_ref}$ and $i_{q\_ref}$, are the current references yielded by the given $P$ and $Q$ conditions. Then, $u_{a\_ref}$, $u_{b\_ref}$, and $u_{c\_ref}$ are the voltage references emerged according to the complex dominant method of power grid current.

Figure 5(b) describes the calculation of the dq frame component under the circulation references $i_{d\_2f\_ref}$ and $i_{q\_2f\_ref}$ conditions. Under the given power conditions, the optimum amplitude and phase angle ($I_{2fm\_ref}$, $\theta_{2f\_ref}$) of circulating current reference under the second-order harmonic condition could be obtained according to the RLEL-PLOC. Moreover, the circulating current references $I_{2fa\_ref}$, $I_{2fb\_ref}$, and $I_{2fc\_ref}$ of three-phase second harmonic circulation could be acquired, respectively. Afterward, the dq frame component of $i_{d\_2f\_ref}$ and $i_{q\_2f\_ref}$ under the second-order harmonic condition could be calculated by park transform under the three-phase condition for $I_{2fa\_ref}$, $I_{2fb\_ref}$, and $I_{2fc\_ref}$.

Figure 5(c) describes the circulating current's complex control. Each phase's arm currents are turned by the bandpass filter (BPF) to acquire the circulating current $i_{2fa}$, $i_{2fb}$, and $i_{2fc}$ of the second-order harmonic circulating current. Then, according to the park transform for three-phase to obtain $i_{d\_2f}$ of the $d$-axis component and $i_{q\_2f}$ of the $q$-axis component. The vector control can deduce the voltage reference values $u_{a\_2f\_ref}$, $u_{b\_2f\_ref}$, and $u_{c\_2f\_ref}$.

Figure 5(d) describes the upper arm $y_{uj\_ref}$ and lower arm $y_{lj\_ref}$ in phase $j$'s reference signals which are derived from $2(-u_{j\_ref} + u_{j\_2f\_ref})/V_{dc}$ to $2(u_{j\_ref} + u_{j\_2f})/V_{dc}$, respectively. As is shown in Figure 5, the presented control could achieve total power dissipation optimization and the highest power dissipation optimization of the SM simultaneously.

### 3.4. Discussion of Put Forward RLEL-PLOC.

Figure 6(a) illustrates the semiconductor devices' power loss with assorted power factor angle $\varphi$. Figure 6(b) elaborates the SM's total power dissipation in the MMC in a different power factor angle $\varphi$. Through Figure 6(a), it is noteworthy that the maximal power dissipation in SMs is efficaciously lowered by the RLEL-PLOC which is proposed under the whole running status. From Figure 6(b), it can be noticed that the proposed RLEL-PLOC has lower SM's total power loss in contrast with CCSC under all operating conditions.

Figures 7(a)–7(e) describe power loss under the proposed RLEL-PLOC of the $T_1$, $T_2$, $D_1$, $D_2$, and $P_{loss}$ of MMCs, where the MMC operates at $\varphi = 0$. As is demonstrated in Figure 7, the power loss $P_{T1}$, $P_{T2}$, $P_{D1}$, $P_{D2}$, and $P_{loss}$ changes along with the second harmonic circulation's change and $T_2$ has the maximal power dissipation among the semiconductor devices. Compared with the CCSC, the maximal power loss of $T_2$ is largely decreased by the RLEL-PLOC with the most appropriate point ($I_{2fm}$, $\theta_{2f}$) as (132, 4.84). Meanwhile, compared with the CCSC, the SM's whole power loss is largely decreased by the RLEL-PLOC with the first-best point ($I_{2fm}$, $\theta_{2f}$) as (132, 4.84).

Figures 8(a)–8(e) describe the power loss under the proposed RLEL-PLOC of the $T_1$, $T_2$, $D_1$, $D_2$, and $P_{loss}$ of MMCs, where the MMC operates at inverter pattern under $\varphi = \pi$. As is shown in Figure 8, the power loss of the $T_1$, $T_2$, $D_1$, $D_2$, and $P_{loss}$ trans along with the second harmonic circulation current's change and $T_1$ has the maximal power dissipation among the semiconductor devices. Compared with the CCSC, the maximal power loss of $T_1$ is largely decreased by the RLEL-PLOC with the most appropriate point ($I_{2fm}$, $\theta_{2f}$) as (184, 1.76). Meanwhile, compared with the CCSC, the SM's whole power loss is largely decreased by the RLEL-PLOC with the first-best point ($I_{2fm}$, $\theta_{2f}$) as (184, 1.76).

## 4. Simulation Studies

As is shown in Figure 9, the simulation studies of the MMC are accomplished by applying the software of PSCAD to confirm the availability of the put-forward RLEL-PLOC. The major simulation arguments are shown in Table 4.

### 4.1. MMCs Operating at $\varphi = 0$.

Figure 10 represents the simulation results of the MMC operating at $\varphi = 0$ in four dominant approaches comprising with CCSC method, with the RLEL-PLOC method, with literature 23's method, and with literature 22's method. Figure 10(a) describes the currents $i_{au}$, $i_{bu}$, and $i_{cu}$ in the arm in the MMC with the CCSC method. Figure 10(b) describes the MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ under the CCSC method. Figure 10(c) represents the $i_{au}$, $i_{bu}$, and $i_{cu}$ of MMCs under the RLEL-PLOC method. Figure 10(d) represents MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ of the under RLEL-PLOC method. Figure 10(e) represents the $i_{au}$, $i_{bu}$, and $i_{cu}$ of MMCs the under literature 23's method. Figure 10(f) represents MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ of the under literature 23's method. Figure 10(g) represents the $i_{au}$, $i_{bu}$, and $i_{cu}$ of MMCs under the literature
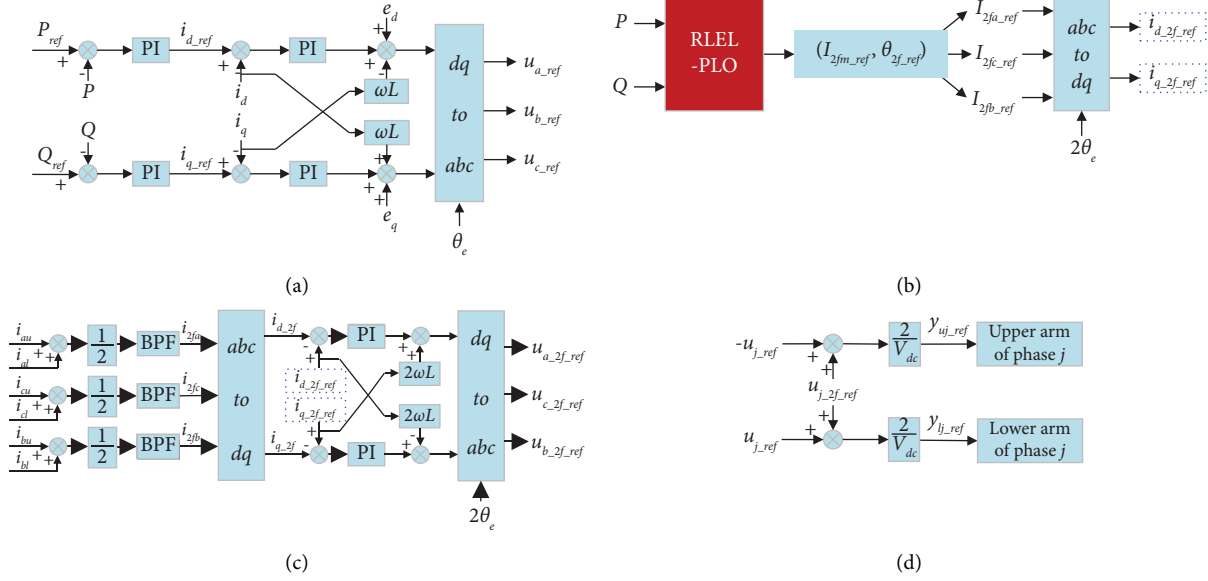
(a)

(b)

(c)

(d)

Figure 5: (a) MMCs' ($P$) and ($Q$) control; (b) the circulating current references of second-order harmonic's calculation; (c) circulating current's vector control; (d) MMCs' reference semaphore for phase $j$.
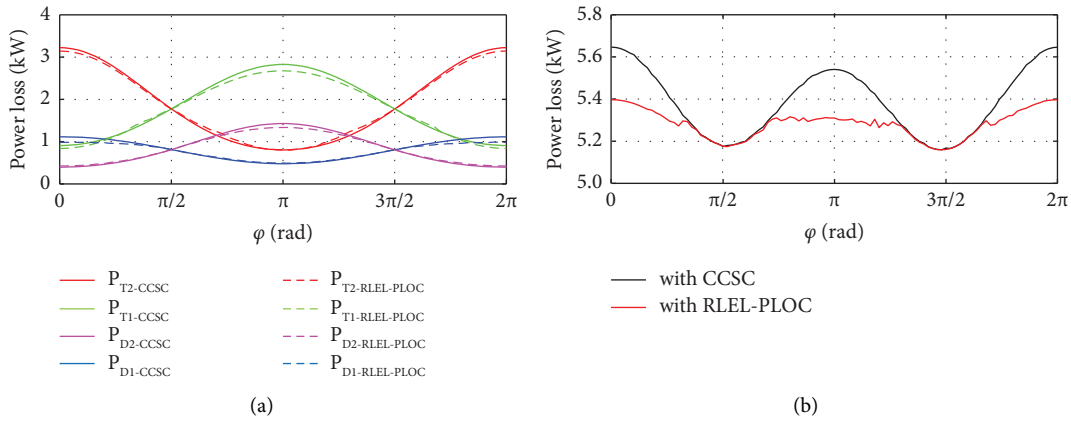


(a)

(b)

Figure 6: (a) Power loss of the semiconductor power devices of the MMC's SM in CCSC and the RLEL-PLOC; (b) total power dissipation of the MMC's SM in the CCSC and the RLEL-PLOC.

22's method. Figure 10(h) represents MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ of the under literature 22's method. Figure 10(i) displays the power dissipation and total power dissipation in SMs of the MMC with the CCSC method, with the RLEL-PLOC method, with literature 23's method, and with literature 22's method. It could be noticed that compared with the CCSC method, the maximum power loss of $T_2$ of the RLEL-PLOC method is reduced by 2.5% from 3224 W to 3144 W, and $P_{loss}$ is reduced by 4.4% from 5646 W to 5397 W. It also could be noticed that compared with the RLEL-PLOC method, although the maximum power loss of $T_2$ of the literature 23's method is reduced by 0.7% from 3144 W to 3122 W, $P_{loss}$ is increased by 5.1% from 5397 W to 5671 W. Compared with the RLEL-PLOC method, although $P_{loss}$ of the literature 22's method is reduced by 1.2% from 5397 W to 5334 W, the maximum power loss of $T_2$ of the literature 22's method is increased by 2.1% from 3144 W to 3209 W.

### 4.2. MMCs Operating at $\varphi = \pi$.

Figure 11 represents the simulation results of modular multilevel converters operating at $\varphi = \pi$ in four dominant approaches comprising with the CCSC method, with the RLEL-PLOC method, with literature 23's method, and with the literature 22's method. Figure 11(a) describes the MMC's $i_{au}$, $i_{bu}$, and $i_{cu}$ with CCSC. Figure 11(b) describes the MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ with CCSC. Figure 11(c) illustrates the MMC's $i_{au}$, $i_{bu}$, and $i_{cu}$ of under RLEL-PLOC. Figure 11(d) illustrates the MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ under RLEL-PLOC. Figure 11(e) represents the $i_{au}$, $i_{bu}$, and $i_{cu}$ of MMCs under the literature 23's method. Figure 11(f) represents MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ of the under literature 23's method. Figure 11(g) represents the $i_{au}$, $i_{bu}$, and $i_{cu}$ of MMCs under the literature 22's method. Figure 11(h) represents MMC's grid current $i_{ga}$, $i_{gb}$, and $i_{gc}$ of the under literature 22's method. Figure 11(i) represents the power loss of the $T_1$, $D_1$, $T_2$, $D_2$, and $P_{loss}$ of the MMC's SM with the CCSC method, with the RLEL-PLOC
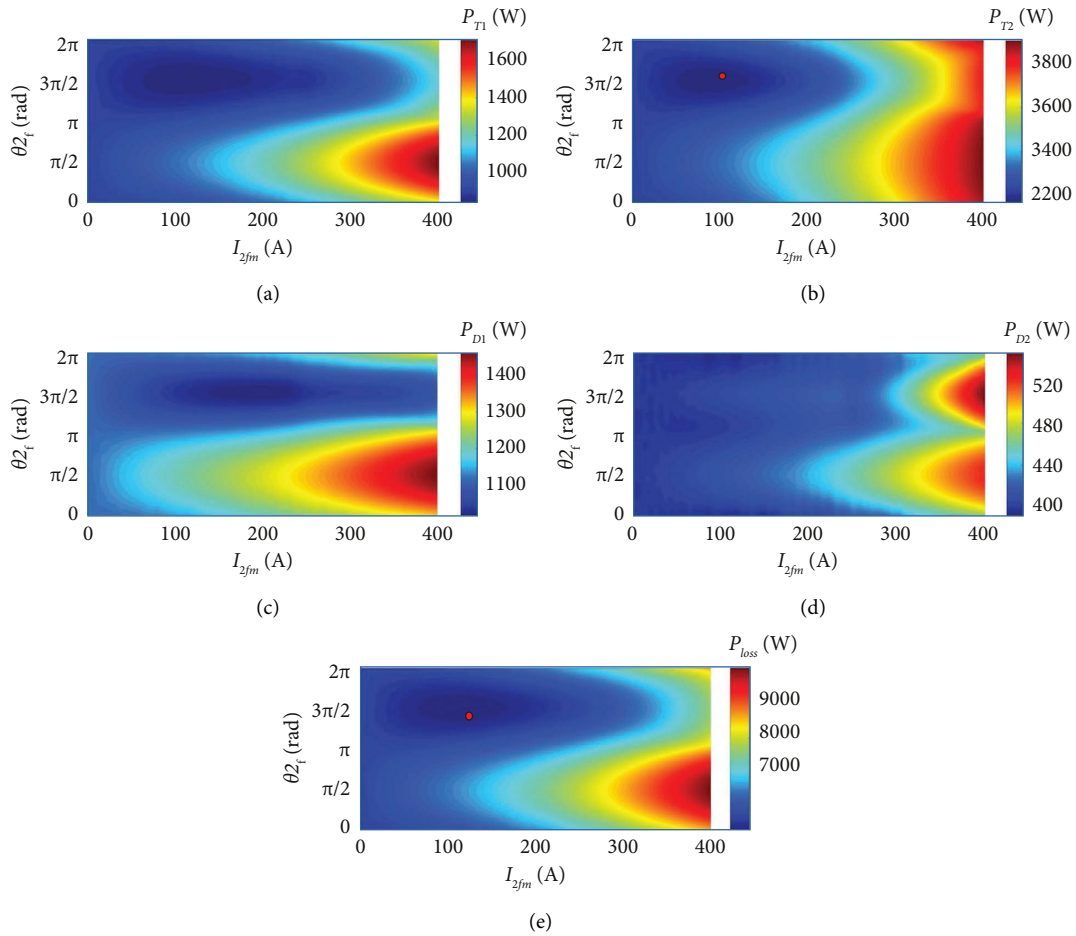
Figure 7: Relation of the MMC operates at $\varphi = 0$. (a) $T_1$'s power loss; (b) $T_2$'s power loss; (c) $D_1$'s power loss; (d) $D_2$'s power dissipation; (e) total power dissipation of the SM.



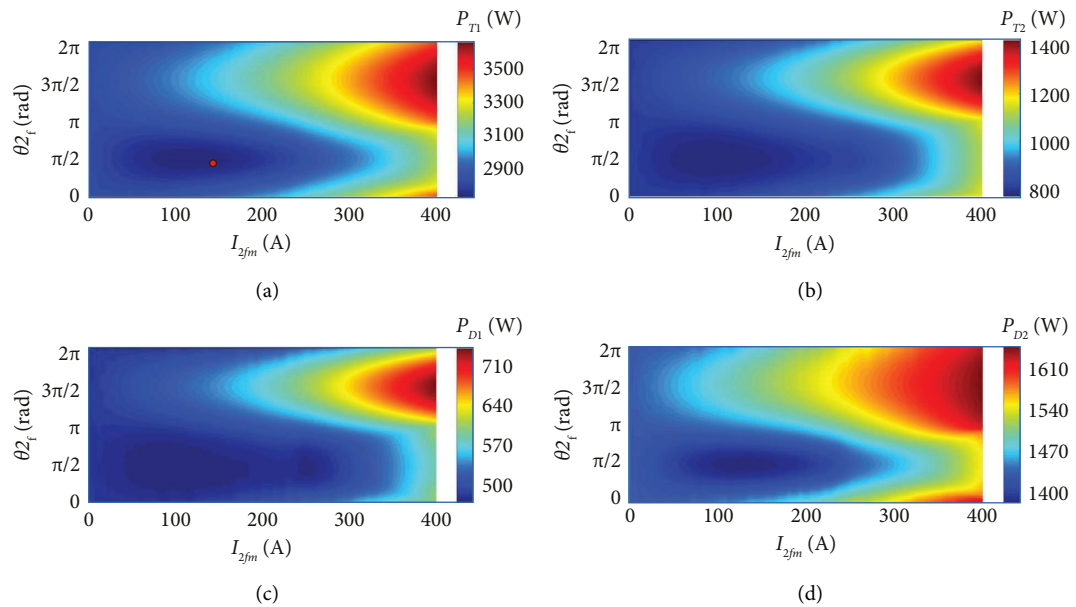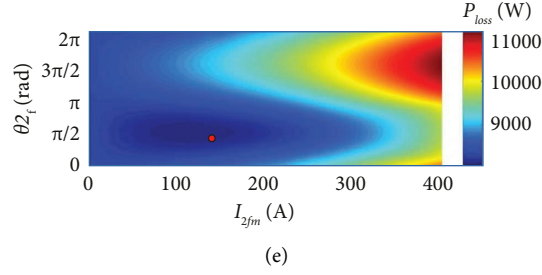Figure 8: Continued.

(e)

FIGURE 8: Relation of the MMC operates at $\varphi = \pi$. (a) $T_1$'s power loss; (b) $T_2$'s power loss; (c) $D_1$'s power loss; (d) $D_2$'s power dissipation; (e) total power dissipation of the SM.
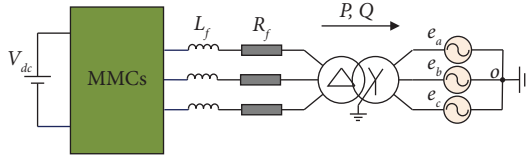


FIGURE 9: Principle block diagram of simulation research.

TABLE 4: Simulation system arguments.

| Arguments | Extent |
|---|---|
| MMC's power (MW) | 75 |
| Parameter of MMC's grid voltage (kV) | 75 |
| The voltage of DC $V_{dc}$ (kV) | 150 |
| Arm's SM number $n$ | 50 |
| Capacitance $C$ of nominal SM capacitance $C$ (mF) | 3.5 |
| Inductance in arm $L_s$ (mH) | 45 |
| Filter inductor $L_f$ (mH) | 2 |

method, with the literature 23's method, and with the literature 22's method, respectively. It could be noticed that compared with the CCSC method, the maximum power loss of $T_1$ of the RLEL-PLOC method is reduced by 5.4% from 2828 W to 2675 W, and $P_{loss}$ is reduced by 4.2% from 5541 W to 5310 W. It also could be noticed that compared with the RLEL-PLOC method, although the maximum power loss of $T_1$ of the literature 23's method is reduced by 2.8% from 2675W to 2601W, $P_{loss}$ is increased by 4.7% from 5310 W to 5561 W. Compared with the RLEL-PLOC method, although $P_{loss}$ of the literature 22's method is reduced by 1.7% from 5310 W to 5221 W, the maximum power loss of $T_1$ of the literature 22's method is increased by 2% from 2675 W to 2729 W.

*4.3. Analysis of Behavior about Capacitor Voltage Ripples.* The SM's capacitor capacitance has a significant influence on the operation, size, and cost for MMCs. The capacitance of SM will decrease along with the decrease of the capacitor voltage ripple. Therefore, the capacitance voltage ripple index is crucial for MMC systems [26]. The capacitor voltage ripple $V_{rip}$ could be estimated by

$$V_{\text{ripple}} = \frac{V_{c,p} - V_{c,v}}{2U_c} \times 100\%, \tag{18}$$

where $V_{c,p}$ is the SM capacitor voltage's peak value and $V_{c,v}$ is the SM capacitor voltage's valley value.

Figure 12 displays the SM's capacitor voltage ripples in different angle $\varphi$ under two dominant techniques comprising CCSC and in proposed RLEL-PLOC which could be deduced from the (18) and simulation study system in Section 4. It could be noticed that the RLEL-PLOC has lower capacitor voltage ripples under most operating conditions, which can improve the economy and portability of the MMC.

*4.4. Discussion of the Simulation Results.* According to the simulation results, it could be obtained that compared with CCSC, the proposed RLEL-PLOC method could decrease both the total power loss and the maximum power loss of the semiconductor devices in the SM. Compared with the RLEL-PLOC method, other methods cannot reduce the total power loss and the maximum power loss of the semiconductor devices in the SM at the same time. Furthermore, the increased loss percentage is high, which will have an adverse impact on the economics or the lifetime of the MMC.

# 5. Experimental Verification

Figure 13 illustrates the experimental platform photo which was constructed in the lab to validate the put-forward RLEL-PLOC for the MMC. The MMC's dc bus is made up of a DC voltage source and a resistive load, which are connected in parallel. The SM uses Infineon's module FF75R12YT30 as the power device. The particular experimental equipment arguments are displayed in Table 5.

*5.1. Analysis of Experimental Waveforms.* Figure 14 displays the behavior of the MMC running at rated conditions in four control techniques including with the CCSC method, with the RLEL-PLOC method, with the literature 23's method, and with the literature 22's method. Figure 14(a) displays the MMC's $i_{au}$, $i_{bu}$, $i_{cu}$, and $i_{bo}$ with the CCSC method, where $i_{bo}$ is the B-phase's output current of the MMC. Figure 14(b) displays the MMC's $i_{au}$, $i_{bu}$, $i_{cu}$, and $i_{bo}$ with the RLEL-PLOC method. Figure 14(c) displays the MMC's $i_{au}$, $i_{bu}$, $i_{cu}$, and $i_{bo}$ with the literature 23's method. Figure 14(d) displays the MMC's $i_{au}$, $i_{bu}$, $i_{cu}$, and $i_{bo}$ with the literature 22's method. Figure 14(e) represents the power loss of the $T_1$, $D_1$, $T_2$, $D_2$,
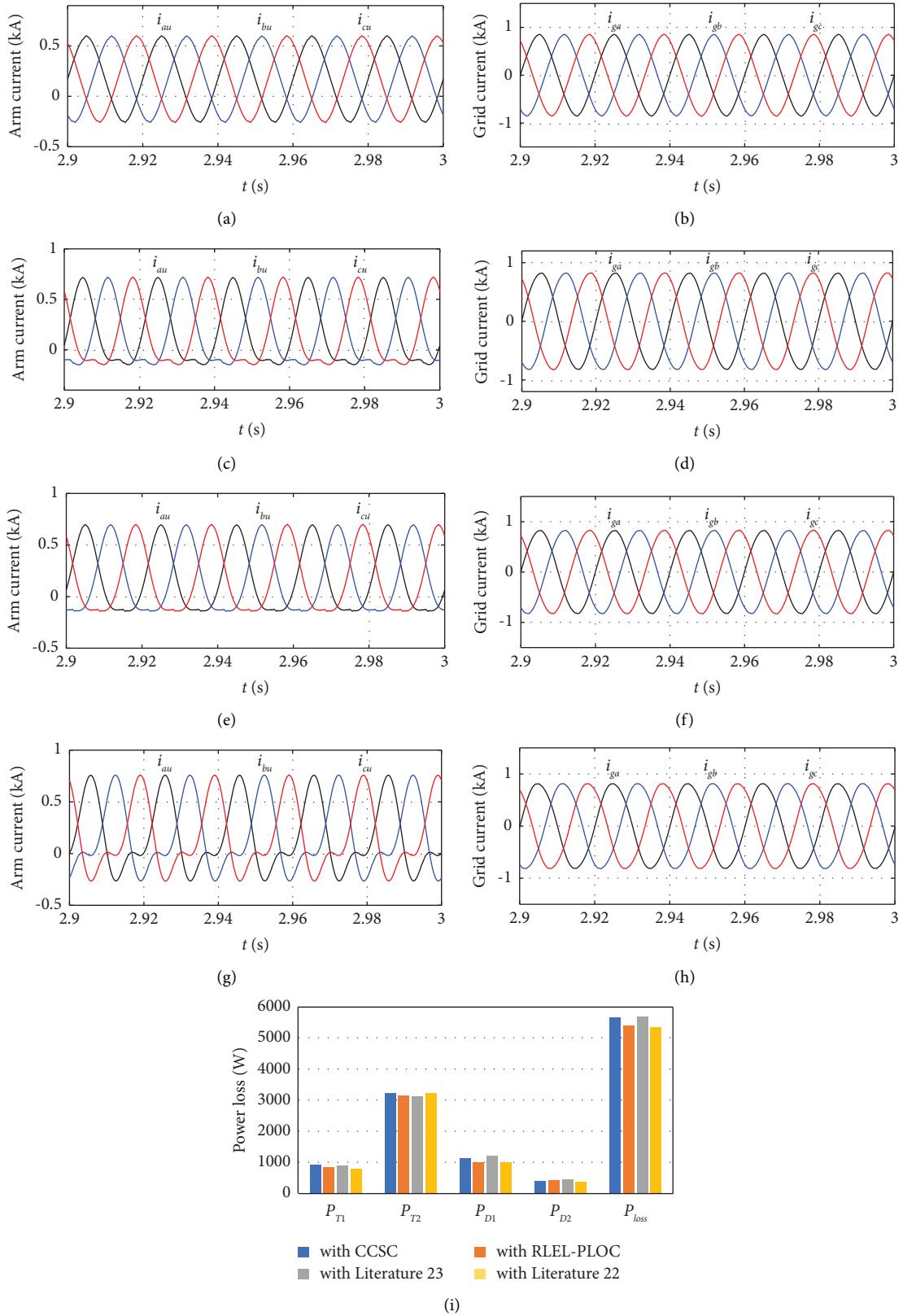
(a)



(b)



(c)



(d)



(e)



(f)



(g)



(h)



(i)

Figure 10: MMCs operating at $\varphi = 0$. (a) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the CCSC method; (b) $i_{ga}$, $i_{gb}$, and $i_{gc}$ in the CCSC method; (c) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the RLEL-PLOC method; (d) $i_{ga}$, $i_{gb}$, and $i_{gc}$ with the RLEL-PLOC method; (e) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the literature 23's method; (f) $i_{ga}$, $i_{gb}$, and $i_{gc}$ in the literature 23's method; (g) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the literature 22's method; (h) $i_{ga}$, $i_{gb}$, and $i_{gc}$ with the literature 22's method; (i) total power loss and power loss of the semiconductor device in four dominate techniques.
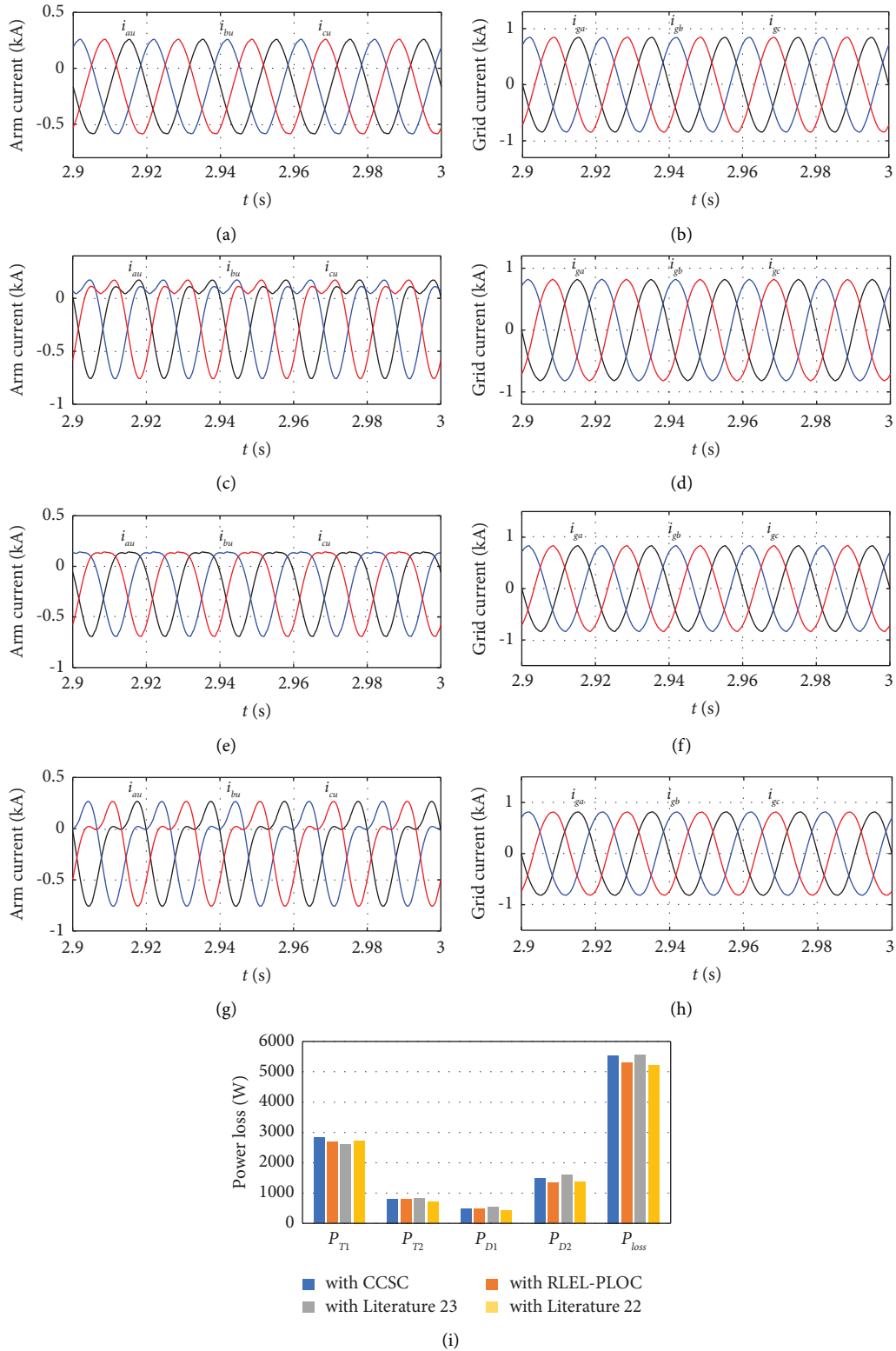
FIGURE 11: MMCs operating at $\varphi = \pi$. (a) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the CCSC method; (b) $i_{ga}$, $i_{gb}$, and $i_{gc}$ in the CCSC method; (c) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the RLEL-PLOC method; (d) $i_{ga}$, $i_{gb}$, and $i_{gc}$ with the RLEL-PLOC method; (e) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the literature 23's method; (f) $i_{ga}$, $i_{gb}$, and $i_{gc}$ in the literature 23's method; (g) $i_{au}$, $i_{bu}$, and $i_{cu}$ in the literature 22's method; (h) $i_{ga}$, $i_{gb}$, and $i_{gc}$ with the literature 22's method; (i) total power loss and power loss of the semiconductor device in four dominate techniques.
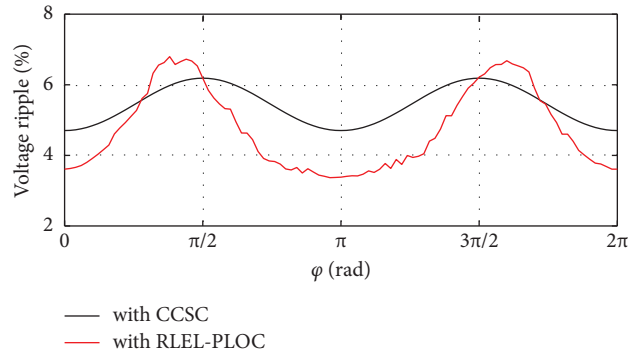
FIGURE 12: SM's capacitor voltage ripples with a different angle $\varphi$ under two dominant techniques.
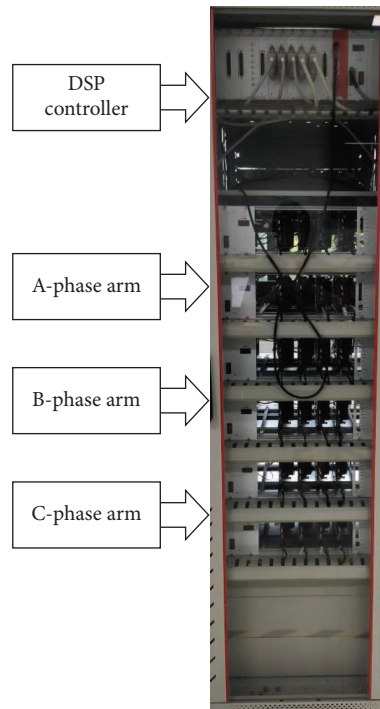


FIGURE 13: Physical drawing of experimental facilities.

TABLE 5: Experimental system arguments.

| Argument | Magnitude |
|---|---|
| Parameter of DC side voltage $V_{dc}$ (V) | 120 |
| SM's number in the arm $N$ | 4 |
| SM's capacitance value (mF) | 2.2 |
| Arm's inductance value $L_s$ (mH) | 2 |
| Parameter of the carrier frequency (kHz) | 10 |

and $P_{loss}$ of the MMC's SM with the CCSC method, with the RLEL-PLOC method, with the literature 23's method, and with the literature 22's method, respectively. It could be noticed that compared with the CCSC method, the maximum power loss of $T_2$ of the RLEL-PLOC method is reduced by 1.1% from 2.74 W to 2.71 W, and $P_{loss}$ is reduced by 1.7% from 5.15 W to 5.06 W. It also could be noticed that compared with the RLEL-PLOC method, although the maximum power loss of $T_2$ with the literature 23's method is reduced by 1.5% from 2.71 W to 2.67 W, $P_{loss}$ is increased by 3% from 5.06 W to 5.21 W. Compared with the RLEL-PLOC method, although $P_{loss}$ of the literature 22's method is reduced by 0.6% from 5.06 W to 5.03 W, the maximum power loss of $T_2$ with the literature 22's method is increased by 7.4% from 2.71 W to 2.91 W. Hence, the put-forward RLEL-PLOC has an obvious advantage among the existing methods.
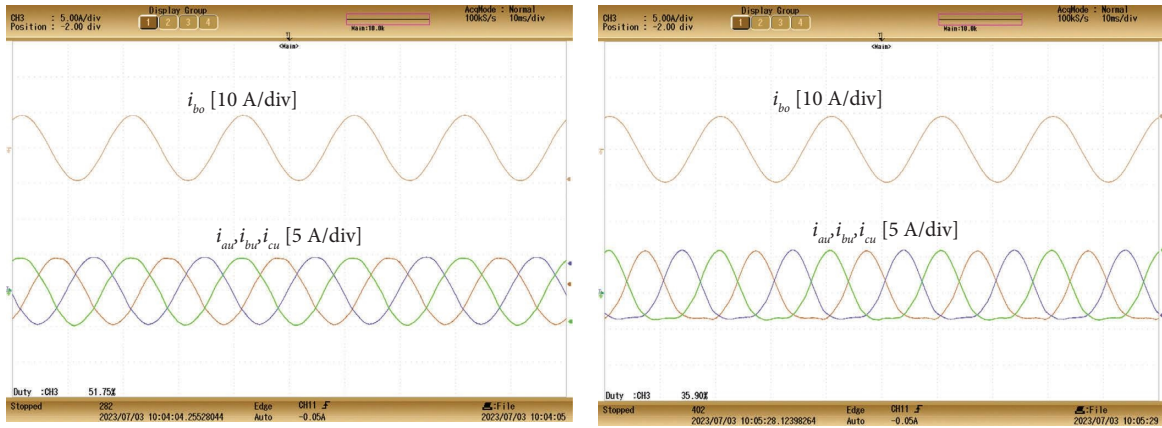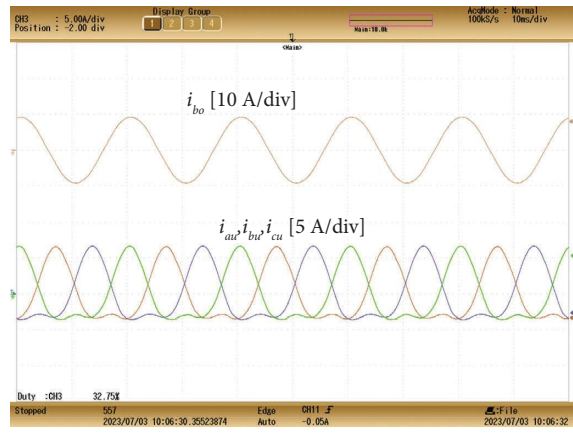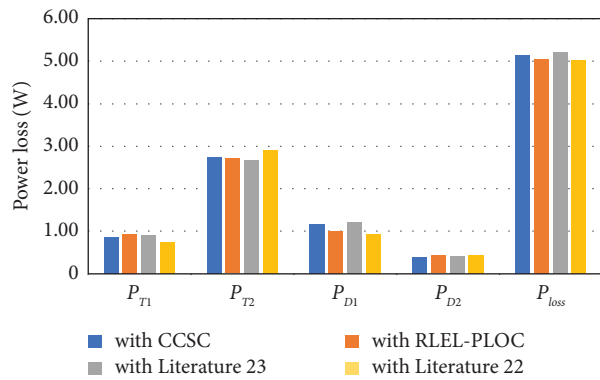
(a)



(b)
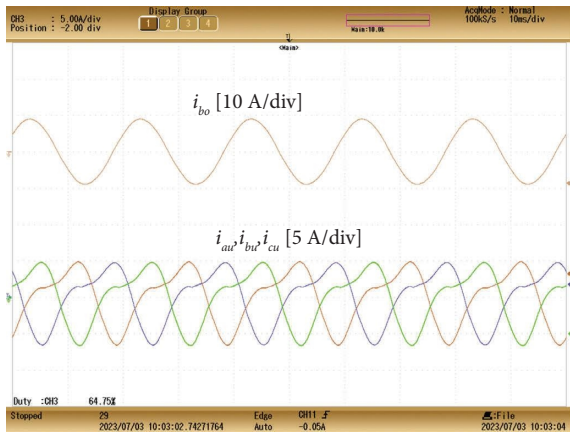


(c)



(d)



(e)

FIGURE 14: (a) Arm currents $i_{au}$, $i_{bu}$, and $i_{cu}$ and B-phase output current $i_{bo}$ in the CCSC method; (b) arm currents $i_{au}$, $i_{bu}$, and $i_{cu}$ and B-phase output current $i_{bo}$ in the RLEL-PLOC method; (c) arm currents $i_{au}$, $i_{bu}$, and $i_{cu}$ and B-phase output current $i_{bo}$ in the RLEL-PLOC method; (d) arm currents $i_{au}$, $i_{bu}$, and $i_{cu}$ and B-phase output current $i_{bo}$ in the RLEL-PLOC method; (e) total power loss and power loss of the semiconductor device in four dominate techniques.

*5.2. Discussion of the Experimental Results.* According to the experimental results, it could be deduced that the proposed RLEL-PLOC method could decrease both the total power loss and the maximum power loss of the semiconductor power devices in the SM compared with CCSC. Compared with the RLEL-PLOC method, other methods cannot reduce the total power loss and the maximum power loss of the semiconductor power devices in the SM at the same time. Moreover, the increased loss percentage is high, which will have an adverse effect on the economics or the lifetime of the MMC.

## 6. Conclusion

This manuscript proposes an RLEL-PLOC by inpouring the first-best second harmonic circulation current into the arm of the MMC to optimize SM's power consumption. Compared with the CCSC, the proposed RLEL-PLOC can simultaneously achieve total power loss optimization and maximal power loss optimization in the arm's SM. Furthermore, the operation cost caused by power loss could be reduced, and the lifetime of the MMC could be improved. Besides, the capacitor voltage ripples under most operation circumstances could be reduced by the proposed RLEL-PLOC. The research results prove the availability of the put-forward RLEL-PLOC for the MMC.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

## Disclosure

We confirm that this work is original and has not been published elsewhere nor is it currently under consideration for publication elsewhere. We wish to submit a new manuscript entitled "Optimized Control for MMCs with Reduced Power Loss and Extended Lifetime" for consideration by the Journal of International Transactions on Electrical Energy Systems.

## Conflicts of Interest

The authors declare no conflicts of interest.

## Acknowledgments

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