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Research Article

Design of Digital Control System for DC/DC Converter of On-Board Charger

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Vehicle charging power supply is widely used because of its small size and portability. Aiming at the problems of slow dynamic response, subharmonic, oscillation and limited soft-switching range of phase-shifted full-bridge DC/DC converter, the paper proposed a modified PSFB converter by introducing clamp diodes at the primary side of the transformer to suppress voltage oscillation of the transformer's secondary side. Also, digital peak current phase-shifting control and slope compensation are introduced to avoid subharmonic oscillation. Dynamic dead-time control technology introduced adjust the dead-time in different load ranges through the dead-time adjustment subroutine. Finally, an experimental platform of on-board charging phase-shifted full-bridge DC/DC converter is established. The experimental results show that the power supply eliminates subharmonic oscillation, achieves a wide range of soft-switching, improves the dynamic performance and antiinterference ability of the system, and optimizes the power efficiency.

1. Introduction

The electric vehicle has many advantages, such as high energy utilization rate, no pollution, and so on [1]. EV batteries are connected to the power grid through charging power supply. There are two main types of on-board charging power supply: one is uncontrolled rectifier isolated DC/DC converter, which has high harmonic and power factor which cannot meet the requirements. The other is an isolated DC/DC converter with active power factor correction, in which AC/DC converter is a boost type, which can realize power factor correction and improve the power density of the system. DC/DC converter has the key energy conversion part of vehicle charging power which directly affects its efficiency [2]. Phase Shift Full Bridge (PSFB) topology is widely used in the field of vehicle charging power supply because of its high efficiency, high power density, and easy realization of Zero Voltage Switch (ZVS) [3].

At present, there are many charging modes, such as constant current-constant voltage charging, variable current intermittent charging, and multistage constant current charging [4]. Constant-current-voltage constant-charge, first large current constant-current, and then constant-voltage charge, not only avoids the phenomenon of current overcharge but also reduces the amount of gas evolution. In constant voltage mode, the output current of the converter gradually decreases from full load to zero. In order to maintain good soft-switching characteristics, the dead time T_d between the drive signals of the bridge arm should be shortened accordingly. Although the voltage-controlled PSFB DC/DC converter has simple control mode, it has some problems such as slow regulation speed and limited soft-switching range [5]. It has the advantages of fast dynamic response, simple transformer bias, and overload protection circuit [6]. When duty cycle $D > 0.5$, subharmonic oscillation will occur, which can be solved by introducing slope compensation [7].

The analog control chip has some shortcomings such as the temperature drift, fixed control parameters, and slow response speed. The configuration of digital control parameters is flexible and the dead-time T_d can be adjusted by software, which avoids the difficulty of soft-switching in light load due to the fixed dead-time under analog control conditions. As for digital control, single voltage loop of digital control is analyzed and designed in the literature [8]. The average current mode phase-shifted full-bridge soft switch with digital control is proposed in the literature [9], which has good antinoise performance, but it is very complex to debug the two sets of parameters of voltage inner loop and outer loop. The peak current control is given in the literature [10]. Phase-shifted full-bridge scheme, but there is no dead-time research.

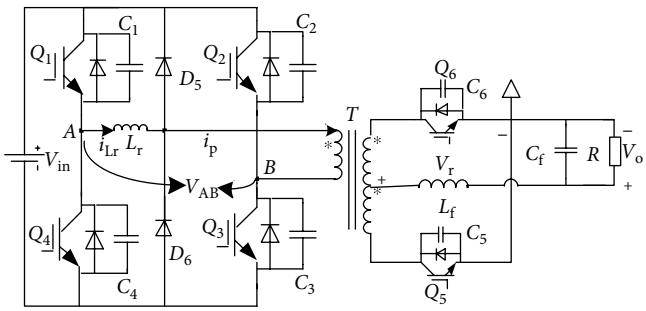

Figure 1: Main circuit of PSFB DC/DC converter.

Therefore, a new PSFB DC/DC ZVS PWM converter is designed in this paper. The clamp diode is added to the primary side of the transformer and the synchronous rectification technology is used to the secondary side. The digital peak current phase-shifting control and slope compensation are introduced to avoid subharmonic oscillation. The implementation mechanism of digital PWM is analyzed, and dynamic dead-time control technology is proposed, that is, to adjust the dead-time in different load ranges through the automatic dead-time adjustment subroutine. Finally, the driving circuit and sampling circuit are designed. It realizes a wide range of soft-switching, improves the dynamic performance, and anti-interference ability of the system, and improves the power supply efficiency.

2. DC/DC Converter of Vehicle Charging Power Supply

2.1. Main Circuit of DC/DC Converter. Figure 1 shows the main circuit topology of a novel PSFB ZVS PWM DC/DC converter with clamping diodes. The input voltage is V_{in} and the switching frequency is $f_s = 100\,\text{kHz}$. The full-bridge switches Q_1–Q_4 are composed of MOSFET. L_r is a resonant inductor, C_1–C_6 is divided into junction capacitors on Q_1–Q_6; L_f and C_f form output filters; N is the ratio of the transformer; the advantage of this topology is that clamping diodes D_5 and D_6 are added to the original side of the transformer to suppress voltage oscillation of the transformer's secondary side; at the same time, the Synchronous Rectification (SR) technology is introduced into the transformer's secondary side. The SR tubes Q_5 and Q_6 are composed of MOSFET, which reduces the conduction loss of the rectifier.

2.2. Subharmonic Oscillation. The peak current-mode control is to determine the output PWM wave by comparing the actual inductance current with the output of the voltage outer loop. However, when duty cycle $D > 0.5$, the disturbance of current i_p on the primary side of the transformer increases with the increase of period, and eventually produces oscillation. The oscillation frequency of this disturbance is half of the switching frequency, so it is called subharmonic oscillation. For this reason, the slope compensation technology is introduced to suppress subharmonic oscillation.

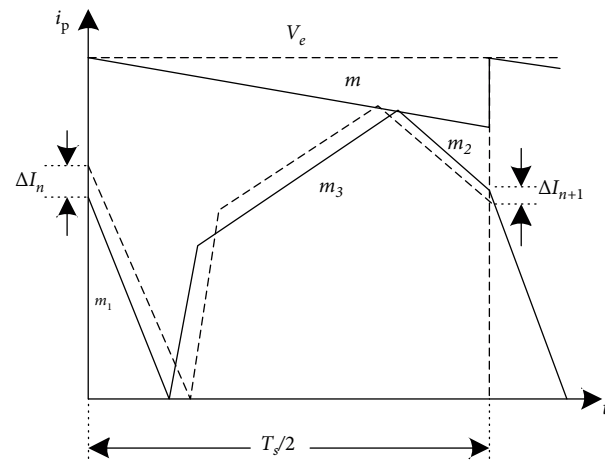

Figure 2: Waveform of primary current i_p of the transformer before and after disturbance.

2.3. Limited Soft-Switching Range of PSFB DC/DC Converter. The switching process of PSFB DC/DC converter is realized by resonance, so it is not instantaneous to decrease the voltage V_{ds} from V_{in} to 0. If the dead time T_d between the driving signals of the bridge arm switch is too short, the V_{ds} will not be switched on before it is reduced to zero, and the switch will lose its soft-switching characteristic; if the dead time T_d is too long, the two switches will be switched on. When the terminal voltage V_{ds} drops to 0, the switch fails to turn on in time. The V_{ds} rises again through resonance, and the switch also loses its soft-switching characteristic. Thus, the soft-switching range of vehicle charging power supply is severely limited under the condition of constant voltage charging mode and wide load current variation. Therefore, an automatic dead-time control technology is proposed to realize a wide range of soft-switching.

3. Peak Current Mode Slope Compensation Analysis

3.1. Slope Compensation Technology. Subharmonic oscillation can be avoided by introducing slope compensation. That is to say, the slope signal with slope m is subtracted from the current loop control V_e. The change of i_p disturbance of the primary current of the transformer with slope compensation is shown in Figure 2. The solid line represents its steady-state waveform and the dotted line represents the waveform after disturbance.

As can be seen from Figure 2, when there is a current disturbance, its variation is

$$\frac{\Delta I_{n+1}}{\Delta I_n} = \frac{(m_2 - m)(m_1 - 2m_2 - m_f)}{(m + m_3)(m_f + m_1)}, \tag{1}$$

where, ΔI_n is the nth current disturbance at the end of the natural flow. $m_1 = V_{in}/L_r$; $m_2 = (V_D + V_{mos})/L_r$ (V_D and V_{mos} are on-voltage drop of diode and MOS respectively); $m_3 = (V_{in} - NV_o)/(N^2 L_r + L_r)$; $m_f = V_o/NL_f$; m is slope of slope compensation current.

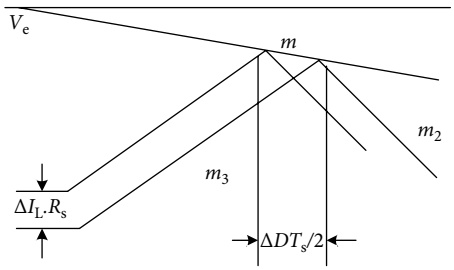

Figure 3: Duty cycle change caused by primary current disturbance.

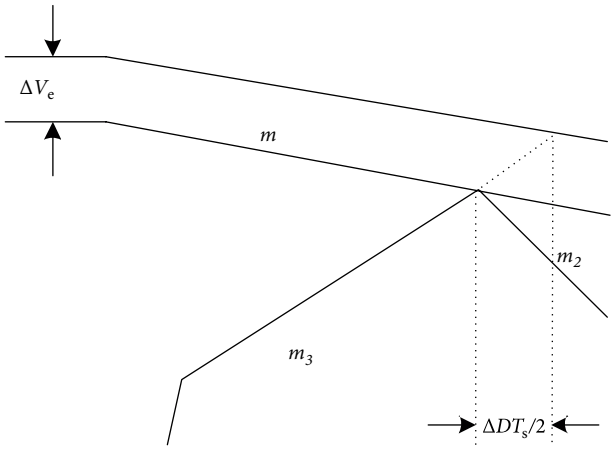

Figure 4: Duty cycle change caused by output voltage error disturbance.

When there is a current disturbance, the necessary condition for system stability is

$$\left|\frac{\Delta I_{n+1}}{\Delta I_n}\right| < 1. \tag{2}$$

According to expression (1), (2), when $m = (0\text{–}2)m_2$, the disturbance can be suppressed, and when $m = 2m_2$, the current disturbance can be completely suppressed.

3.2. Small-Signal Model of PSFB DC/DC Converter. The small-signal modeling of PSFB DC/DC converter has been done by foreign scholars. Two important transfer functions are given in reference [11].

The transfer function of the control variable $\hat{d}(s)$ to the output voltage $\hat{v}_o(s)$ is

$$G_{vd}(s) = \frac{V_{in}/N}{s^2 L_f C_f + s\left(L_f/R + R_d C_f\right) + R_d/R + 1}. \tag{3}$$

The transfer function of the control variable $\hat{d}(s)$ to the sampling current $\hat{i}_L(s)$ is

$$G_{id}(s) = \frac{\left[s^2 L_f C_f + s\left(L_f/R + RC_f\right) + 1\right]V_{in}/NR}{s^2 L_f C_f + s\left(L_f/R + R_d C_f\right) + R_d/R + 1}, \tag{4}$$

where, $R_d = 2L_r f_r/N_s^2$, $f_r = T_s/2$.

Table 1: Design parameters of DC/DC converters.

Parameter	Value
Rated input voltage V_{in}/V	300–500
Output voltage V_o/V	12
Output current I_o/A	50
Transformer ratio N	21
Resonant inductance L_r/μH	26
Resonant capacitor C_f/nF	7.5
Output filter inductor L_f/μH	2
Switching frequency f_s/kHz	100

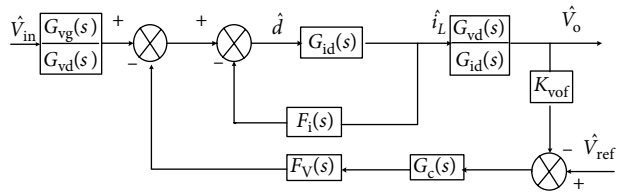

Figure 5: Block diagram of peak current mode control system.

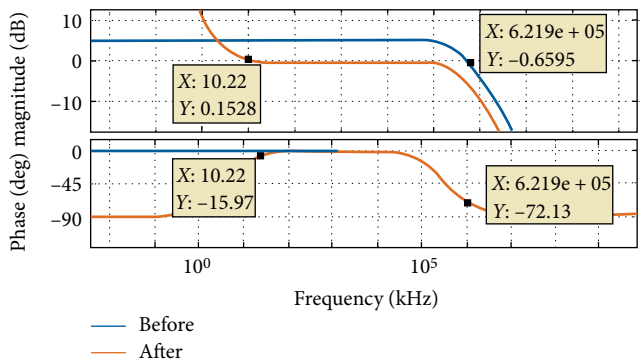

Figure 6: BODE diagram before and after compensation.

3.3 Feedback Loop Transfer Function. In the peak current control mode, the duty cycle changes caused by the disturbance of the original current and output voltage errors of the transformer with slope compensation are shown in Figures 3 and 4, respectively.

The duty cycle of the transformer caused by current disturbance ΔI_L is ΔD, $F_i(s)$ is defined as the current loop feedback function, and R_s is the equivalent sampling resistance.

$$F_i(s) = \frac{\hat{D}}{\hat{I}_L} = \frac{\Delta D}{\Delta I_L} = \frac{R_s f_s}{m + m_3}. \tag{5}$$

The change in the duty cycle caused by the disturbance ΔV_e of error voltage V_e is ΔD. $F_V(s)$ can be obtained from Figure 5.

$$F_V(s) = \frac{\hat{D}}{\hat{V}_e} = \frac{\Delta D}{\Delta V} = \frac{f_s}{m + m_3}. \tag{6}$$

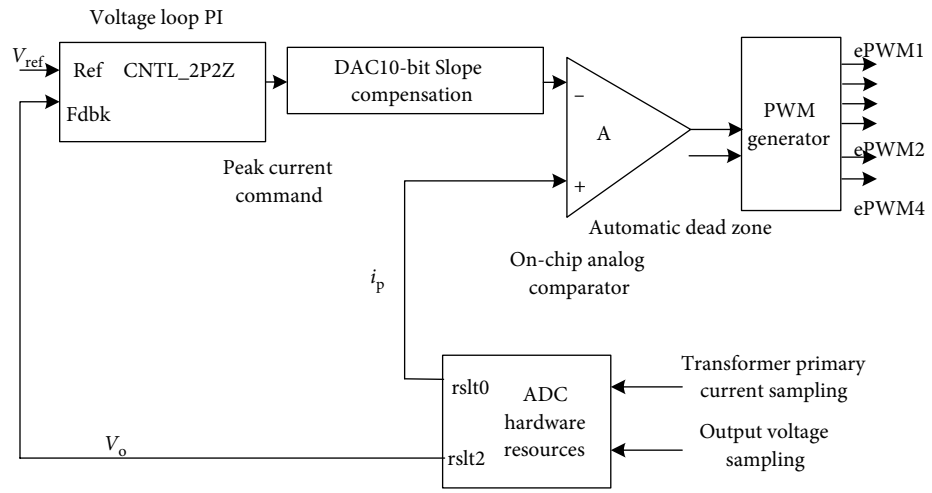

Figure 7: Digital peak current control system.

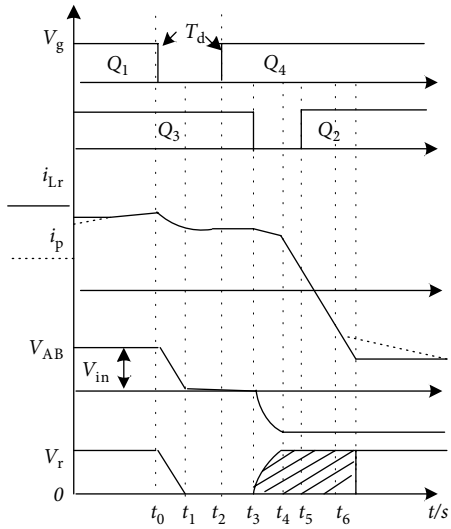

Figure 8: Operating waveforms of DC/DC converter.

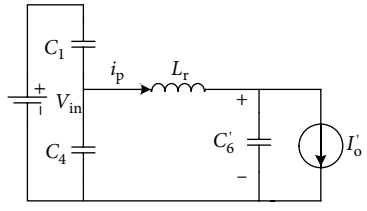

Figure 9: The equivalent circuit at (t_0, t_1).

Define $F_V'(s)$ as feedback function of voltage loop, and $G_c(s)$ as transfer function of voltage loop compensation network, then

$$F_V'(s) = \frac{f_s}{m + m_3} G_c(s). \tag{7}$$

3.4. Transfer Function of Control System. The small-signal model of peak current mode control system with slope compensation is shown in Figure 5. K_{vof} is the output voltage feedback coefficient.

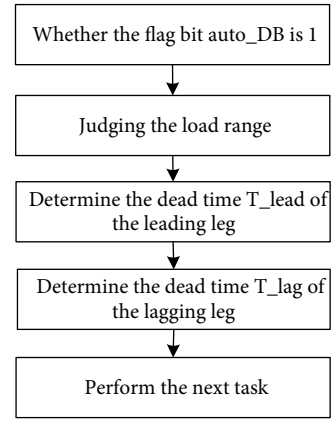

Figure 10: Automated dead zone task flow chart.

PI regulator is used in the voltage outer loop, that is, the transfer function of compensation network $G_c(s)$ is

$$G_C(s) = K_{pi} + \frac{K_{ii}}{s}. \tag{8}$$

The open-loop transfer function $G_o(s)$ of peak current control is obtained as follows

$$G_o(s) = F_V(s) G_C(s) K_{vof} \cdot \frac{G_{vd}(s)}{1 + F_i(s) G_{id}(s)}. \tag{9}$$

After substituting the parameters in Table 1, the PI coefficients are calculated as $K_{pi} = 0.524$ and $K_{ii} = 11900$ according to the requirements of the open-loop frequency characteristics of the control system. Figure 6 shows BODE diagrams before and after current open-loop transfer function compensation. The open-loop cut-off frequency before compensation is much larger than the switching frequency, and the open-loop amplitude-frequency characteristic passes through the zero decibel line with −40 dB/dec, so the system is very unstable. After compensation, the open-loop amplitude-frequency characteristic passes through the zero decibel line with −20 dB/dec, the cut-off frequency is 10.22 kHz, and the phase margin is 164-degree stable.

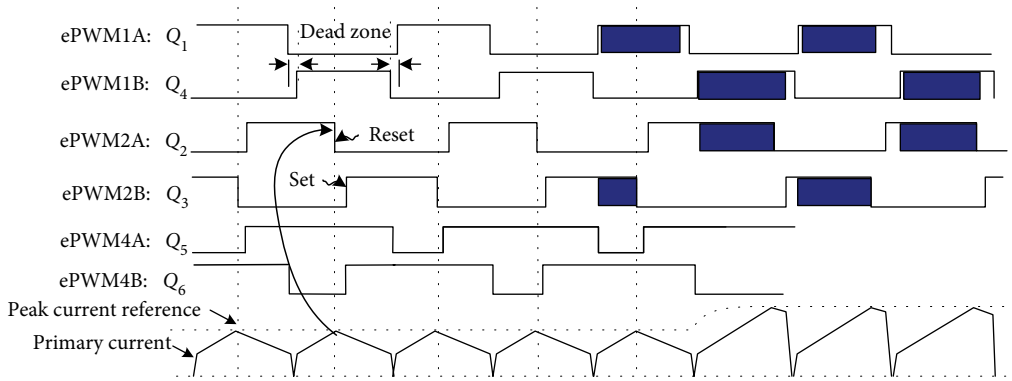

Figure 11: Implementation mechanism of digital PWM.

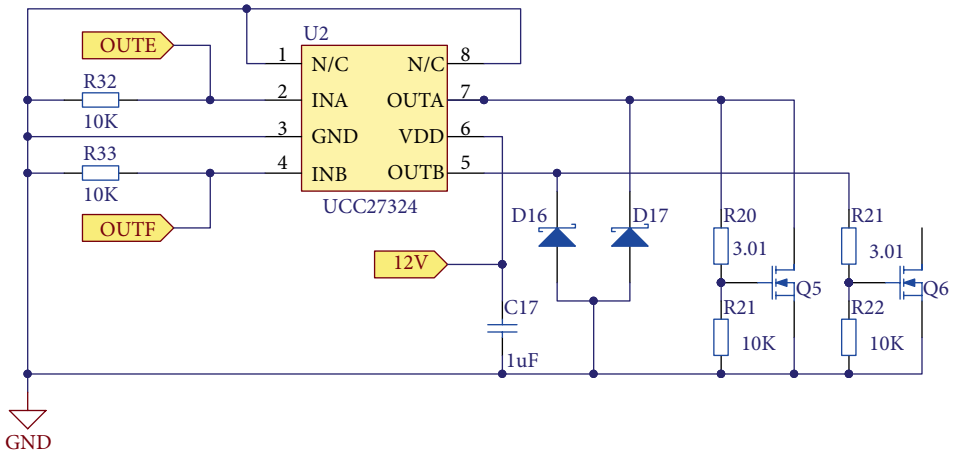

Figure 12: Synchronous rectification drive circuit schematic.

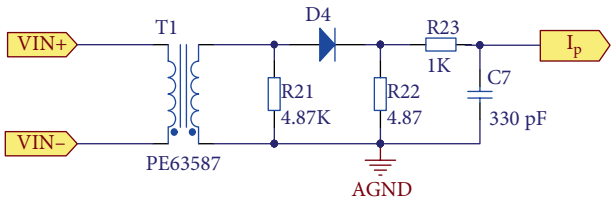

Figure 13: Transformer primary current sampling circuit.

By using trapezoidal summation approximate integral link and the difference between two points approximate differential link, the analog PID controller is discretized to digital PID controller, and the digital PI control of voltage loop is realized by calling CNTL_2P2Z macromodule of DSP TMS320F28027. The macro module realizes second-order control by using bipolar and bi-zero points.

4. Software Design of Digital PSFB DC/DC Converter

4.1. Digital Control System of Peak Current. The microcontroller uses TI's TMS320F28027 because it has advanced on-chip control peripherals including enhanced ADC, on-chip analog comparator, DAC and high precision PWM generator. In addition, it also has a unique programmable on-chip slope compensator, which can provide slope compensation of at least 0.04 V/μs. At the same time, the software can adjust the dead time T_d to achieve a wide range of soft-switching.

The digital peak current control system is shown in Figure 7. By sampling output voltage V_o and primary current i_p of transformer by ADC, the difference between output voltage V_o and reference voltage V_{ref} are entered into the digital PI controller, slope compensation is added into DAC, compared with the primary current i_p of transformer by analog comparator, PWM generator generate PWM signals to drive Q_1–Q_6. EPWM1A and ePWM1B drive switches Q_1 and Q_4; ePWM2A and ePWM2B drive switches Q_2 and Q_3; ePWM4A and ePWM4B drive SR tubes Q_5 and Q_6.

4.2. Automatic Dead Zone Control Technology. Figure 8 shows the half-cycle operating waveform of the proposed PSFB DC/DC converter, which is in turn the driving waveform of switch Q_1–Q_4, the primary current i_p, the resonant inductance current i_{Lr}, the voltage V_{AB} between the neutral points of the primary two arms, and the secondary voltage V_r. The dead time between the driving signals of the same bridge arm is T_d.

The equivalent circuit at (t_0, t_1) is shown in Figure 9. At t_0, the switch Q_1 is switched off. At this time, the resonant inductance L_r, the junction capacitor C_1 of switch Q_1, the junction

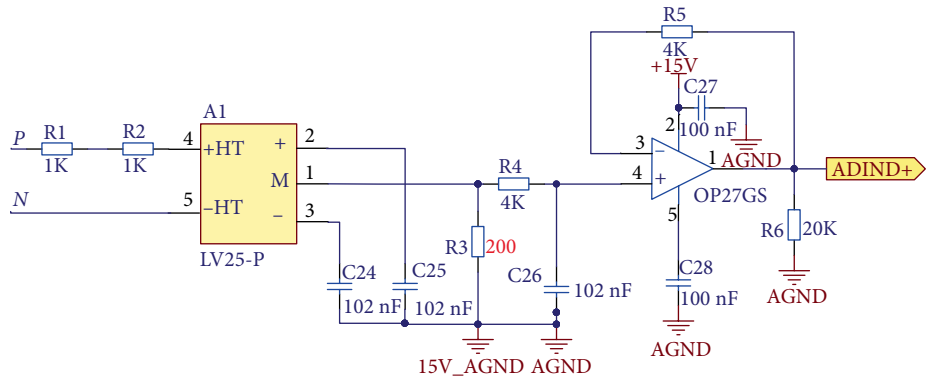

Figure 14: Output voltage sampling circuit.

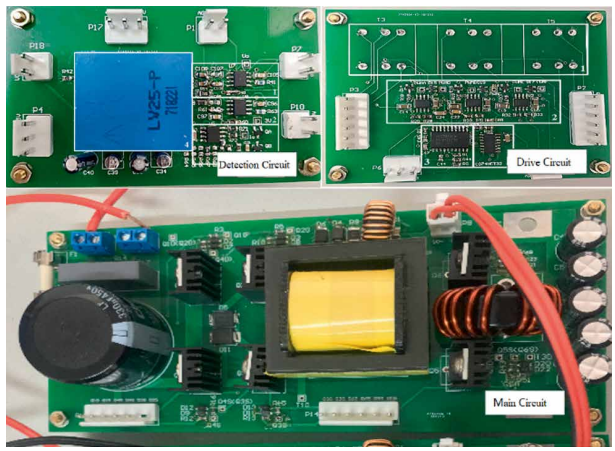

Figure 15: Driving circuit, detection circuit, and main circuit.

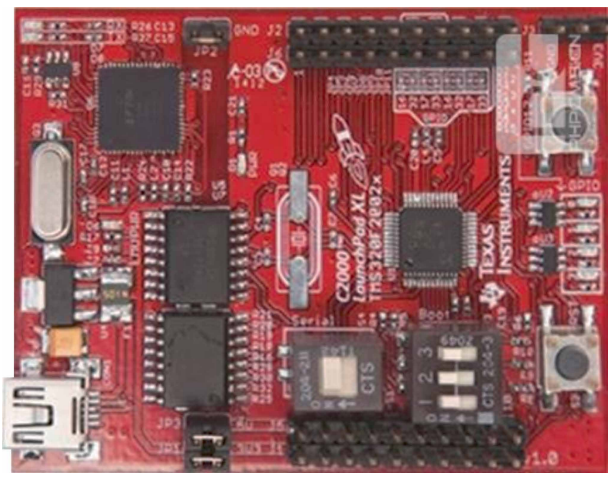

Figure 16: Control circuit board.

capacitor C_4 of switch Q_4, and the junction capacitor C_6 of SR Q_6 resonate, C_1 charges, and C_4 and C_6 discharge. The primary current i_p and resonant inductance current i_{Lr} of transformer begin to decrease.

At this point, the voltage V_{C1} of the switch Q_1 junction capacitor C_1 is

$$V_{C1}(t) = \frac{I_o'}{2C_1 + C_6'}t + \frac{C_6'}{2C_1(2C_1 + C_6')}\frac{I_o'}{\omega_0}\sin\omega_0, \quad (10)$$

where, I_o' and C_6' are the equivalent values of output current I_o and junction capacitance C_6 of SR tube Q_6 on the original side of transformer, respectively.

$$\omega_0 = \sqrt{\frac{2C_1 + C_6'}{2C_1C_6'L_f}}. \quad (11)$$

At t_1, the resonance ends, and at this time $V_{C1} = V_{in}$, the resonance process time T_r is obtained by substitution (10). The larger I_o' and the smaller T_r, the shorter the dead time T_d.

Therefore, the dead-time T_d can be adjusted according to the load current I_o, so that the switch can achieve a wide range of soft-switching, which is called automatic dead-time technology. Figure 10 is the automatic dead-zone task flow chart. First, the dead zone auto-adjustment flag auto_DB is detected, and if it is 1, the program is executed. The output current sampling is connected with ADC channel 9, and result register for ADC channel 9 is read to obtain the current load. The load range is divided into 12 cases according to the switch-case statement, corresponding to the leading-leg dead-time count value T_lead and the lagging-leg dead-time count value T_lag, respectively. By assigning T_lead (T_lag) to the rising-edge delay register DBRED and the falling-edge delay register DBFED of ePWM1 (ePWM2) module respectively, the dead-time of the leading-lag (lagging-leg) can be automatically adjusted..

4.3. Implementation Mechanism of Digital PWM. The generation mechanism of the phase-shifted PWM signal is shown in Figure 11. The on-chip analog comparator compares the primary current of the transformer with the peak current reference of slope compensation. The comparator output is connected to the PWM generator. The ePWM1 module is set up to run in the incremental and subtractive counting mode, while the other PWM modules run in the incremental counting mode.

After the interruption, the counting mode of the time-base control register TBCTL of the ePWM1 module is detected. When TBCTL is detected to be incremental mode, ePWM2A is forced to reset and ePWM2B is placed after the automatic

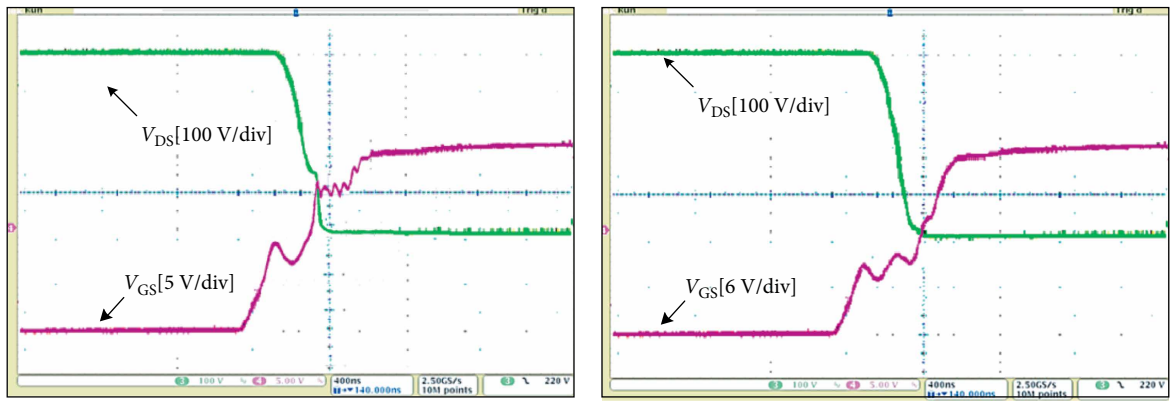

FIGURE 17: The soft-switching waveform comparison of lagging arm Q_3 before and after dead-time T_d adjustment under light load. (a) T_d=1 μs and (b) T_d=2 μs.

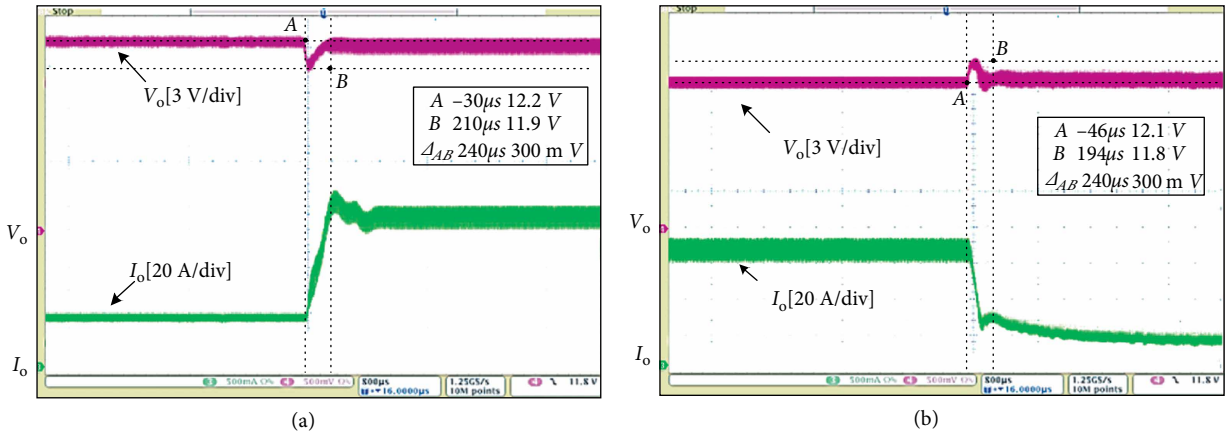

FIGURE 18: Output voltage and output current waveforms when the load is abrupt. (a) 0–80% load mutation and (b) 80–0% load mutation.

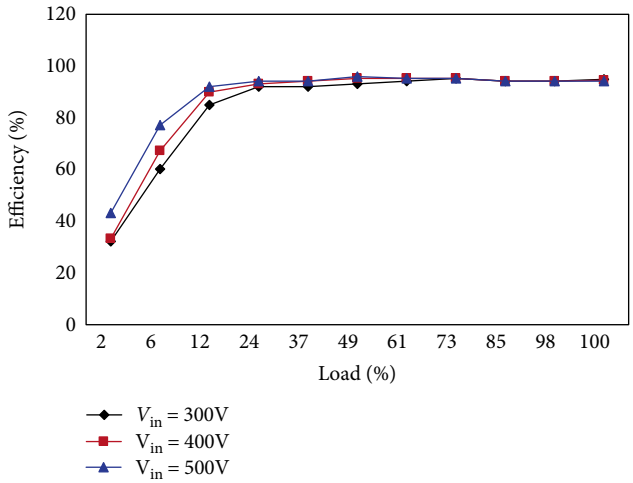

FIGURE 19: Relationship between load and efficiency at different input voltages.

dead time. When TBCTL is in the decrement mode, ePWM2B is forced to reset and ePWM2A is set after the automatic dead time. In this way, the phase shift control of ePWM2 module relative to the ePWM1 module is realized.

The driving signal of $Q_5(Q_6)$ of SR transistor is obtained by "or" logic from the driving signal of $Q_4(Q_1)$ of leading-leg and $Q_2(Q_3)$ of lagging-leg, so that the load current flows through the SR tube channel for the highest proportion of time, and the overall conduction loss is minimized.

5. Digital PSFB DC/DC Converter Hardware Design

5.1. Drive Circuit Design. The source of the SR transistors Q5 and Q6 is connected to the output voltage GND, so GND is used as the reference driving circuit. The driver chip is selected as UCC27324, which can provide high peak current for capacitive load. The synchronous rectifier driver circuit is shown in Figure 12. UCC27324 provides up to 4 A current in the Miler flat area during MOS switch switching. The full-bridge switch tube on the original side of the transformer is also driven by UCC27324, but transformer isolation must be provided.

5.2. Sampling Circuit Design. The primary current ip of the transformer passes through the current transformer and is sampled by the resistor to obtain a voltage signal, which is

sent to the AD sampling port. The current transformer adopts PE63587 with turn ratio of 1 : 100. Figure 13 is the primary current sampling circuit of the transformer.

The output voltage sampling circuit is shown in Figure 14. The LV25-P of LEM company is selected as the voltage sensor. The current rating of the primary side of the sensor is l0 mA. When the rated output voltage V_o =12 V and two 1 K/6 W current limiting resistors are connected in series on the primary side of the sensor, the current I_{n1} =6 mA on the primary side of the sensor is converted to the current I_{n2} =15 mA on the secondary side of the sensor. Controller A/D detection range is 0–3.3 V, sampling resistance R3 =3 V/15 mA = 200. The post-stage circuit is connected with a voltage tracker whose amplification factor is 1, and the operational amplifier chip adopts OP27GS. The output voltage of 12 V passes through DC resistance voltage divider and voltage tracker, and finally, the input value of AD sampling of 2.472 V is obtained.

6. Experiment

According to the design requirements of the vehicle charging power supply, the experimental platform of PSFB DC/DC converter is built. The main experimental parameters are shown in Table 1. The driving circuit, the detecting circuit, and the main circuit are as shown in Figure 15. The primary H-bridge of the transformer adopts the MOSFET module of the Infineon model SPP20N60CFD, and the SR tube adopts MOSFET module of the Fairchild Semiconductor model FDP032N08. Figure 16 shows the control board using Piccolo TMS320F28027.

Figure 17 shows the drain-source voltage V_{DS} and driving voltage V_{GS} waveforms of the lagging arm Q_3 before and after dead-time T_d adjustment under light load. It is difficult to turn on zero voltage for lagging leg Q_3 when the dead time is 1 μs, as shown in Figure 17(a) . When the dead time is increased to 2 μs, the switch can achieve zero-voltage switching better, as shown in Figure 17(b). It shows that the soft switch with wide range can be realized by adding automatic dead-zone technology.

In the case of rated input voltage V_{in} =400 V, Figure 18(a) is the waveforms of output voltage and output current when the load changes from 0% to 80%, and Figure 18(b) is the waveforms of output voltage and output current when the load changes from 80% to 0%. From the analysis in the figure, it can be seen that for the step change of 80% in the load, the output peak deviation can be less than 3% of the rated output, and the stabilization time is about 240 μs, which has good dynamic performance and antiinterference ability.

The relationship between load and efficiency under different input voltages are shown in Figure 19. It can be seen that when the maximum input voltage is 500 V, the rated voltage is 400 V, and the minimum input voltage is 300 V, the system efficiency is above 95% in the range of 10–100% load, which can achieve a wide output range of load current and is affected by the change of input voltage very little, and meets the charging requirements of the vehicle charging power supply.

7. Conclusion

Aiming at the problems of DC/DC converter, which is the core part of the electric vehicle charging power supply, a digital control system of PSFB DC/DC converter is designed, which adopts peak current mode control, introduces slope compensation to eliminate the subharmonic oscillation. Dynamic dead-time control technology is proposed, which realizes a wide range of soft-switching, reduces switching losses and improves power supply efficiency. Experiments show that system efficiency is above 95% in the range of 10–100% load. The digital phase-shifting control based on TMS320F28027 is used to realize the step change of 80% in load, the peak deviation of output is less than 3% of rated output, and the stabilization time is less than 240 s, which improves the dynamic response speed and antiinterference ability of the digital control system.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors confirm that this article content has no conflicts of interest.

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