Hindawi
Journal of Advanced Transportation
Volume 2022, Article ID 7840102, 14 pages
https://doi.org/10.1155/2022/7840102

Research Article

An Effective Charger for Plug-In Hybrid Electric Vehicles (PHEV) with an Enhanced PFC Rectifier and ZVS-ZCS DC/DC High-Frequency Converter

G. Kanimozhi,[1] **L. Natrayan**,[2] **S. Angalaeswari**,[3] **and Prabhu Paramasivam**[4]

[1]*Centre for Smart Grid Technologies, School of Electrical Engineering, Vellore Institute of Technology, Chennai, Tamil Nadu, India*
[2]*Department of Mechanical Engineering, Saveetha School of Engineering, SIMATS, Chennai 602105, Tamil Nadu, India*
[3]*School of Electrical Engineering, Vellore Institute of Technology, Chennai, Tamil Nadu, India*
[4]*Department of Mechanical Engineering, College of Engineering and Technology, Mettu University, Metu 318, Ethiopia*

Correspondence should be addressed to G. Kanimozhi; kanimozhi.g@vit.ac.in, L. Natrayan; natrayan07@gmail.com, and Prabhu Paramasivam; prabhuparamasivam21@gmail.com

Received 20 February 2022; Revised 17 April 2022; Accepted 11 May 2022; Published 1 June 2022

Academic Editor: Mohammad Miralinaghi

A plug-in hybrid electric vehicles (PHEV) charger adapter consists of an AC/DC power factor correction (PFC) circuit accompanied by a full-bridge isolated DC/DC converter. This paper introduces an efficient two-stage charger topology with an improved PFC rectifier as front-end and a high-frequency zero voltage switching (ZVS). Current switching (ZCS) DC/DC converter is the second part. The front-end converter is chosen as bridgeless interleaved (BLIL) boost converter, as it provides the advantages like lessened input current ripple, capacitor voltage ripple, and electromagnetic interference. Resettable integrator (RI) control technique is employed for PFC and DC voltage regulation. The controller achieves nonlinear switching converter control and makes it more resilient with the faster transient response and input noise rejection. The second stage incorporates a resonant circuit, which helps in achieving ZVS/ZCS for inverter switches and rectifier diodes. PI controller with phase shift modulator is used for second-stage converter. It improves the overall efficacy of the charger by lowering the switching losses, lowering the voltage stress on the power semiconductor devices, and reversing recovery losses of the diodes. The simulations and experimental results infer that the overall charging efficiency increases to 96.5%, which is 3% higher than the conventional two-stage approach using the interleaved converter.

1. Introduction

In order to reduce the fuel consumption and fuel emission, the world is moving towards eco-friendly vehicles, [1] namely electric vehicles (EV), hybrid electric vehicles (HEV), and PHEV. Highly efficient batteries, its fast-changing technologies, and charging infrastructure are the key sources for the electric vehicles. Battery chargers are crucial in the field of battery and electric car technology [2]. A traditional combustible engine plus an electric engine powered by a pluggable external electric source propels PHEVs [3]. In normal driving conditions, PHEVs can store enough electricity from the grid to drastically reduce their gasoline usage [4]. The recent developments in PHEV motor drive and battery charging technologies have increased the demand for PHEV vehicles in the market. Researchers focus on improving the same to speed up the commercialization of the vehicle in the market.

Batteries [5] such as nickel metal hybrid, lithium polymer, and lithium-ion are predominantly used in electric vehicles for its best efficiency, safety, energy density, and cost factor. At all power levels, a battery charger can allow unidirectional or bidirectional power transfer. The bidirectional power flow [6] includes a vehicle-to-grid (V2G) mode to the grid-to-vehicle interface (G2V). In a utility-connected microgrid, a battery charger configuration for PHEV applications using a back-to-back (B2B) converter is also proposed [7]. Depending on the vehicle's power requirements, this proposed structure can operate in four different modes: grid-to-vehicle (G2V),

microgrid-to-vehicle (M2V), vehicle-to-grid (V2G), and vehicle-to-microgrid (V2M).

The IEC-62196 specifies the general parameters of the charging process [4], and therefore, how energy is delivered. In order to charge the automobiles, users have four options. They are slow charging, semi-fast charging, fast charging, and ultrafast charging. Two different types of chargers for charging the battery are considered, namely high-speed charger and on-board charger [8]. PHEV applications support on-board charger for residential charging. From a 230 V supply, 3.3 kW on-board charger can charge a 16 kWh exhausted battery pack in around 4 hours.

The charger architectures [8] are broadly classified as single-stage and two-stage chargers. Two-stage architecture is preferred, as it gives low-frequency ripple rejection. Front part of two-stage architecture is AC-DC converter, and back end has DC/DC converter. The power architecture of a two-stage battery charger depicted in Figure 1 includes AC/DC PFC circuit accompanied by a second part isolated DC/DC converter.

A variety of PFC rectifier circuits with linear and nonlinear control methods [9] have been developed as front-end converters. A multilevel converter configuration is the viable choice if larger power ratings are required. Most commonly used topologies for the front-end converter are dual boost converter [7], bridgeless PFC converter [10], interleaved PFC boost converter [11], and phase shifted boost converter [12]. The interleaving concept reduces the current ripple at the supply end and also EMI filter requirement. On the other hand, the drawbacks of the conventional interleaved converters include increased output voltage ripple, cost, design complexity, the thermal problem due to the presence of diode bridge rectifiers, voltage and current stress on the semiconductor devices, and electromagnetic interferences (EMI).

A BLIL PFC boost converter with four-channel interleaving is considered as front-end converter, since it overcomes the drawbacks of the conventional converters. The second part of the two-stage charger is an isolated resonant DC/DC converter. Various topologies for obtaining zero voltage switching are available. Higher circulating primary winding current is one of the major downsides of the traditional isolated DC/DC converter to attain ZVS resulting in greater conductive losses of switches. Alternatively, ZVS eliminates noise and harmonics in high-frequency converters. Many topologies with soft switching technique, such as phase shifted ZVS topology [13], LLC resonant topology [14], and RCD voltage clamping [15], are reported in the literature to diminish the switching losses, voltage stress across the switches, and diode's reverse recovery loss. The proposed second-stage resonant converter overcomes the above-mentioned losses with lesser number of components, thereby increasing the overall efficiency of the charger. Miralinaghi et al. [16] suggested scheme on operation and integration of two buck-boost converter based on a single-phase bidirectional inverter under a maximum power point trackers (MPPT) on DC distribution system. The power factor correction and grid connection fulfilment were obtained by bidirectional inverter with a full-bridge configuration. The power flow between DC bus and AC grid was controlled by an inverter control system, and it was regulated DC bus to a certain range of voltages [16].

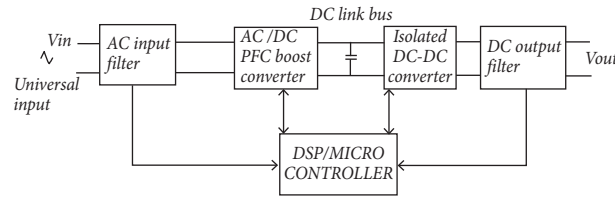


Figure 1: Block diagram of the battery charger unit.

Tran suggested scheme on operation and integration of two buck/boost converter based on a single-phase bi-directional inverter under a maximum power point trackers (MPPT) on DC distribution system. With a thin PV array, the MPPT technique was formed by two buck and boost converter, it reduced the voltage stress. The power factor correction and grid connection fulfilment were obtained by bidirectional inverter with a full-bridge configuration [17]. Miralinaghi et al. [18] suggested a scheme on soft switching charging and discharging converter with the zero-voltage discharge function. The battery voltage can be discharged by the converter until it becomes zero. In the charging operation at turn-on period, the zero voltage switching was achieved, and in discharging operation at turnoff period, the zero current switching was achieved [18]. He et al. [19] suggested scheme on single DC single source with less magnetite topologies for minimizing the power balance issues. For minimizing the zero-sequence current, a sine-triangle pulse width modulation was used. To obtain a staircase voltage waveform using power electronic switches under low-rated based on multilevel inverter concept. As that the requirement of series-connected switches increases, it depends on the number of increasing voltage level [19]. This paper introduces an efficient two-stage charger topology with improved PFC rectifier as front end with a nonlinear controller and a high-frequency ZVS-ZCS DC/DC converter as the second stage with ACM controller as displayed in Figure 2.

This article is structured in the following manner: Section 2 designates the first stage of battery charger system with nonlinear PFC algorithm and the second stage is resonant DC/DC converter explained in Section 3. The requisite designed equations of the converter and its specifications of the suggested battery charger are addressed in Section 4. The simulation results are detailed in Section 5. Finally, Section 6 carries the conclusion report based on the results obtained.

2. Front-End PFC Boost AC/DC Converter

BLIL PFC boost converter [20–23] shown in Figure 2 includes four inductors ($L1, L2, L3$, and $L4$), four power MOSFET's ($Q1$ to $Q4$), four diodes ($D1$ to $D4$), and an intermediate DC link capacitor (C_{01}). As the term suggests, the bridge rectifier with diodes is abolished. Compared with the traditional interleaved boost converter, four channel

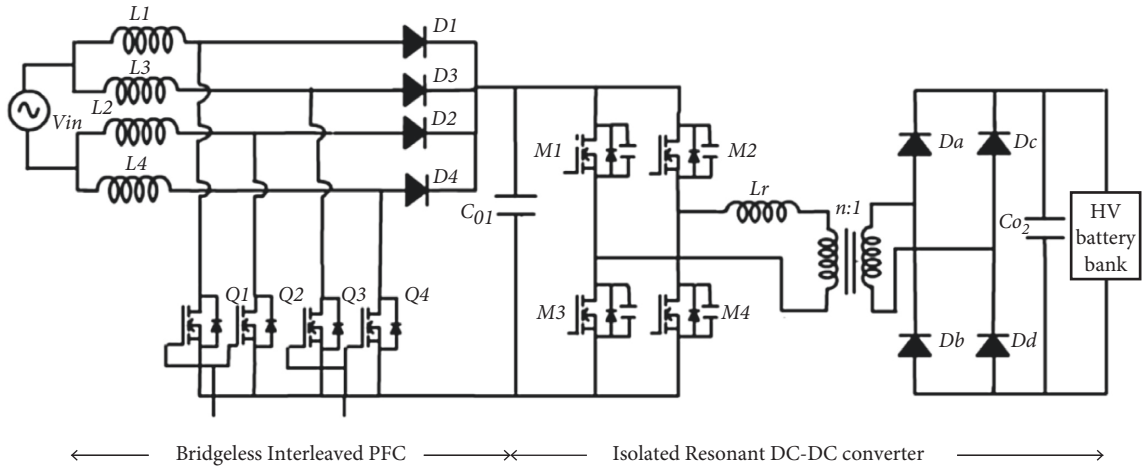


Figure 2: Proposed battery charger unit.

interleaving lessened the input current ripple. The total current flowing through the inductors $L1/L2$ and $L3/L4$ will be the input current. Since the ripple current in the inductors [$L1/L2$ and $L3/L4$] are now out of phase, they negate each other, thus minimizing the ripple of input current [24]. Interleaving decreases output capacitor current ripple, current stress on the devices, and, furthermore, the circuit EMI [25].

BLIL boost converter is implemented with the PFC control algorithm, which improves power factor and power quality of the input current according to IEC 61000-2-3 standard, and the load voltage is regulated to the preferred value. The PFC [26, 27] is designed in several ways, such as boundary conduction mode (BCM), continuous conduction mode (CCM), and discontinuous conduction mode (DCM). Average current mode (ACM) control is one of most commonly used methods in boost PFC converters to accomplish high power factor and minimal distortion. Any disturbance in the line voltage is compensated in the ACM control technique, increasing the output voltage's immunity to variations in the supply line. This method drawback includes detecting input current, input voltage, output voltage, and multiplier circuit all of which add to the circuit complexity. When a transient occurs, the outer voltage loop reaction is slow, and it takes many switching cycles to achieve stability. These disadvantages are rectified by incorporating nonlinear control technique.

The BLIL boost converter considered in this work operates in CCM mode, and the control scheme incorporated is resettable integrator control technique. Resettable integrator (RI) technique [28–30] shown in Figure 3 is a nonlinear technique proposed for converters operating at constant frequency. This does not require input voltage sensor, multipliers, and input current error compensator as like average current mode control. The vital advantage of this control method is that it the harmonics are removed as well as the transients are traced. The output signal is combined here until it approaches the reference signal. The converter switching frequency, f_0, is much higher than the frequency of the input signal $x(t)$ or the reference signal $V_r(t)$, and therefore, $x(t)$ and $V_r(t)$ can be taken as fixed value. Let $y(t)$ be the output variable.

$$y(t) = \frac{1}{T_S}\int_0^{T_{\text{on}}} x(t)\mathrm{d}t = \frac{1}{T_S}x(t)\int_0^{T_{\text{on}}} \mathrm{d}t = x(t)\delta(t), \quad (1)$$

where $\delta(t)$ is the duty cycle and T_s is the total interval. The power device's duty cycle is controlled when the chopped waveform equals the input reference as stated in the-following equation:

$$\int_0^{T_S} x(t)\mathrm{d}t = \int_0^{T_S} V_r(t)\mathrm{d}t\, y(t) = \frac{1}{T_S}\int_0^{T_S} x(t)\mathrm{d}t = \frac{1}{T_S}\int_0^{T_S} V_{\text{ref}}(t)\mathrm{d}t = V_r(t). \quad (2)$$

In different converter topologies, this control approach may be extended to leading edge and trailing edge modulation. The theoretical waveform of the control technique is depicted in Figure 4. The sensed output voltage V_{sen} is fed to an amplifier. The amplified error voltage $V_c(t)$ is tuned by PI controller that is integrated with a resettable integrator, and for each switching cycle, a variable magnitude ramp voltage $V_m(t)$ is generated. The inductor current I_{sen} is compared with the ramp voltage as shown in Figure 3. When the voltages are equal, the integrator resets. Therefore, the integrator resets for each switching time and the ramp voltage begins at "0" for consecutive switching period. Thus, in one switching period this discards the supply-fed disturbances and load disruptions.

3. Isolated Resonant DC/DC Converter

The PHEV charger second part consists of an isolated resonant DC/DC converter [31], which can be operated in CCM, BCM, and DCM mode. In this case, the converter is operated in DCM mode, with high switching (100 kHz) frequency to lessen the passive components size, the ratio of transformer turns, and the current stress on primary end switches. The primary winding of the transformer is coupled

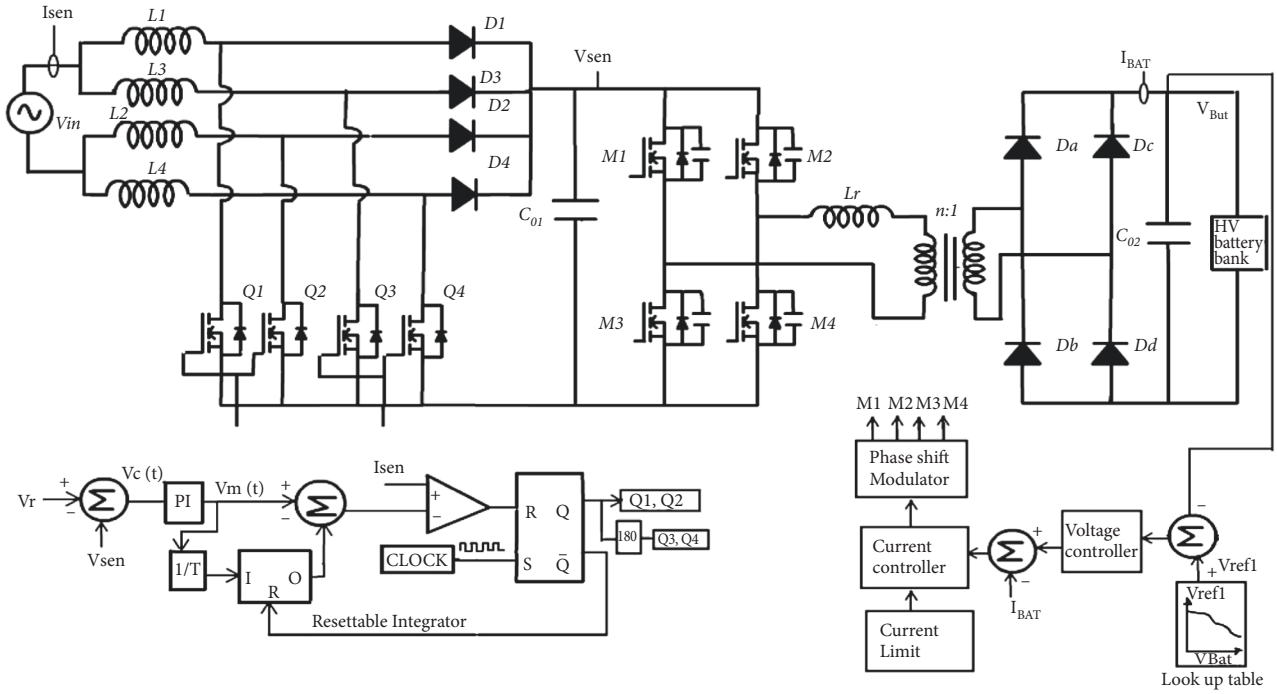


Figure 3: Overall control structure.

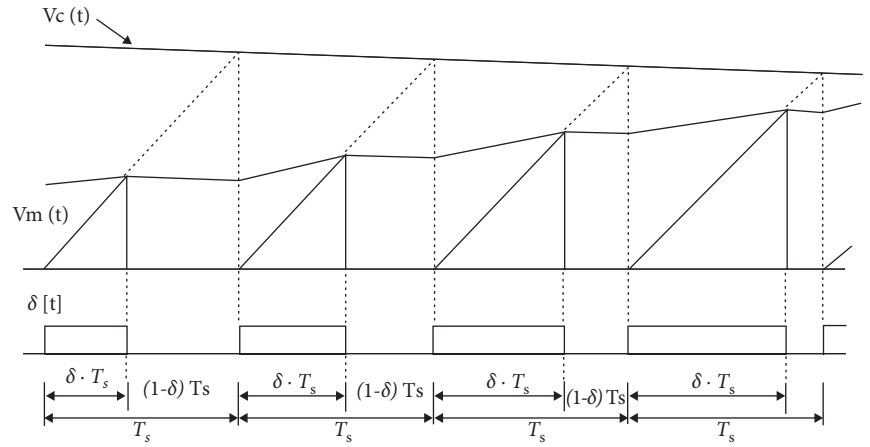


Figure 4: Theoretical waveform of RI technique.

to the inverter circuit as portrayed in Figure 2. The inverter switches and rectifier diode's resonant switching are achieved by fixing the duty cycle of the lower group devices of the inverter $M3$ and $M4$ as 50%, while upper switches ($M1$ and $M2$) are PWM controlled [32]. The power semiconductor devices are modelled with parasitic capacitances and parallel diodes. All the parasitic capacitances of switches and inductors are together taken in the output capacitance. Theoretical waveforms for the operation of isolated resonant DC-DC converter are shown in Figure 5.

It can be seen that the ZV switching-on and ZC switching-off is accomplished for the inverter's lower switches, while the upper leg devices attain ZCS turnoff. The diodes in the rectifier circuit connected next to the transformer secondary will accomplish zero current turnoff. At the time instant $t = to$, the power devices $M1$ and $M4$ are turned on and the current streams through $M1$-Lr- primary winding of the transformer and $M4$. At time $t = t_1$, $M1$ turns off and the primary current follows an alternative path via. M_4-parasitic capacitance of M_3 and Lr.

The resonant inductor's current i_{Lr} is expressed as follows:

$$i_{Lr}(t) = \frac{V\mathrm{dc} - (V_0/n)}{Lr}(T - t_0). \tag{3}$$

At the same interval, the diodes $Da\mathrm{D}_1$ and Dd will start D_4 conducting on the rectifier side. The direction of the secondary current through D_1-load and D_4 is achieved. Power devices $M1\mathrm{M}_1$ and M_4 have now attained ZCS during OFF state. At time instant $t = t_3$, the switches $M2M_2$ and $M3$ are

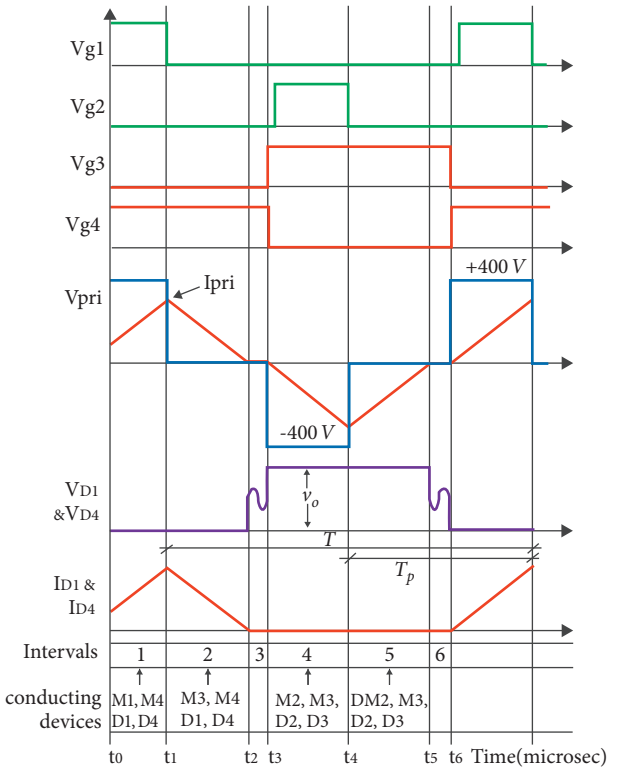


Figure 5: Theoretical waveform second-stage resonant isolated DC/DC converter.

triggered ON, and D_1 and D_4 are now reverse biased, while DbD_2 and D_3 are forward biased. The resonant inductor current is currently, as per the initial condition $i_{Lr}(0) = i_{\text{pri}} i_{L_r}(0) = i_E$, provided by the following equation:

$$i_{Lr}(t) = i_{\text{pri}} - \frac{V_o}{n * Lr}(T - t_1), \tag{4}$$

where i_{pri} is the primary current of the transformer. The time instants $t = t_4, t_5$, and t_6 are the negative equivalents of the intervals t_1 to t_3. For the diodes on the rectifier side of the circuit ZCS turn-on and ZCS turnoff are accomplished. The isolated resonant DC/DC converter removes the need of traditional RCD voltage clamping circuit in this case, thereby reducing the total losses and enhancing the charger performance.

The full-bridge DC/DC converter control method incorporates a phase shift of lagging leg switches with respect to leading leg switches realized by conventional ACM control as shown in Figure 3. Here, the battery terminal voltage of the battery is set to the current reference and the charging graph determines the power required to charge the battery bank. Thus, the full-bridge inverter duty ratio is determined by the charging curve and the terminal voltage of the battery.

4. Design Considerations

This section discusses the presented two-stage battery charger design. The four-channel interleaving inductors of BLIL boost rectifier are designed based on the input ripple current ΔI_L, and it is specified as

$$\Delta I_L = \frac{V_{\text{in}}\sqrt{2}D}{fs.Lb/2}, \tag{5}$$

where $V_{\text{in}} = \sqrt{2}Vs \sin \omega t$ is the maximum value of the input voltage, and f_s is the switching frequency of rectifier. $Lb = L1 = L2 = L3 = L4$ are boost inductors. Two inductors of equal value are connected to each phase. The duty cycle D is expressed as

$$D = 1 - \frac{V_{\text{inp}}}{V\text{bus}}, \tag{6}$$

where Vbus is the bus voltage of the boost converter. The output power P_o is given as

$$Po = V\text{bus} * I\text{bus}. \tag{7}$$

Here, Ibus is the rectifier output current. The MOSFET used in the rectifier has duty cycle $\delta_{Q(\theta)}$, and it is expressed as

$$\begin{aligned}\delta_Q(\theta) &= 1 - \frac{|V_{\text{in}}(\theta)|}{V_o} \\ &= 1 - \frac{V_p|\sin\theta|}{V_o},\end{aligned} \tag{8}$$

where V_p is the input peak value. Assuming the current flowing through the inductor as sinusoidal, its expression is given as follows:

$$i_{L=I_p|\sin\theta|}, \tag{9}$$

where I_P is the input current's maximum value. The instantaneous current of MOSFET $i_Q(\theta)$ and its root mean square (RMS) value $i_Q(\text{rms})$ may be given as follows:

$$i_{Q(\theta)=Ip|\sin\theta|}\delta_{Q(\text{rms})},$$

$$i_Q(\text{rms}) = \left[\frac{1}{\pi}\int_0^{\pi}\left[I_p|\sin\theta|\left(1 - \frac{V_p|\sin\theta|}{V_o}\right)\right]^2\right]^{1/2} d\theta. \tag{10}$$

The duty cycle of the diode $\delta_D(\theta)$ can be stated as

$$\delta_D(\theta) = 1 - \delta_Q(\theta) = \frac{V_{p|\sin\theta|}}{V_o}. \tag{11}$$

The instantaneous value of diode current is

$$i_D(\theta) = I_p|\sin\theta|\left(\frac{V_p|\sin\theta|}{V_o}\right). \tag{12}$$

RMS value of diode current can be expressed as

$$i_D(\text{rms}) = \left[\frac{1}{\pi}\int_0^{\pi}\left[I_p|\sin\theta|\left(\frac{V_p|\sin\theta|}{V_o}\right)\right]^2\right]^{1/2} d\theta. \tag{13}$$

The output capacitor current has low ($I_{c\text{-rms(low)}}$) and high-frequency components ($I_{c\text{-rms(high)}}$) and is given as

$$I_{c-\mathrm{rms}}(\mathrm{low}) = \frac{I_o}{\sqrt{2}} = \frac{\sqrt{2}}{2}\frac{P_o}{V_o},$$
$$I_{c-\mathrm{rms}}(\mathrm{high}) = \frac{P\mathrm{in}}{V_o}\sqrt{\frac{16V_o}{6\pi V_p} - \frac{P_o^2}{P_{in}^2}}. \quad (14)$$

The capacitor C_{01} is expressed as

$$C_{01} = \frac{2Po * T_h}{V^2\mathrm{bus} - (V\mathrm{bus} * 0.75)}, \quad (15)$$

where P_0 is the output power and T_h is the maximum hold up time for the line frequency 50 Hz.

$$G = \frac{V_o}{V\mathrm{in}} = \frac{1}{1-D}. \quad (16)$$

And thus, the voltage stress V_{st} across the power devices is given as

$$V_{st} = GV\mathrm{in} = V_o. \quad (17)$$

The second-stage isolated DC/DC converter with voltage gain (G) is formulated as follows:

$$G = \frac{V_o}{V\mathrm{dc}} = \frac{2 * n}{1 + \sqrt{1 + 4 * k/D^2}}, \quad (18)$$

where k is the standardized time constant $(k = 4n^2L_R/R_0T)$ and n is the turn's ratio of the transformer, and it is given as

$$n = \frac{V_o}{V\mathrm{dc} * D}. \quad (19)$$

The duty ratio for the inverter switch is set at 0.377 as it gives the optimal gain value. The turn's ratio of the transformer is obtained as 1.326 from (19). The voltage gain ranges from 0.1 to 0.5 for different values of D, and k from 0.1 to 1 has been calculated and plotted using MATLAB as shown in Figure 6. The resonant inductor value (L_rL_r) is given as

$$L_r = \frac{k * R * T}{4 * n^2}$$
$$L_r = \frac{k * R_0 * T}{4 * n^2}, \quad (20)$$

where R is the output resistance of the converter and T is the switching interval. Thus, the value of L_r is 176 μH from (20). The RMS value of current passing through the inverter switches $M1$ and $M2$, $I_{M12(\mathrm{rms})}$, is given as

$$I_{M12(\mathrm{rms})} = \sqrt{\frac{1}{T}\int_{t_0}^{t_1} i_{Lr}(t)^2 \mathrm{d}t}, \quad (21)$$

and the RMS value of current through inverter switches $M1$ and $M2$, $I_{M12(\mathrm{rms})}$, is given as

$$I_{M12(\mathrm{rms})} = \sqrt{\frac{1}{T}\left[\int_{t_0}^{t_1} i_{Lr}(t)^2 \mathrm{d}t + \int_{t_1}^{t_2} i_{Lr}(t)^2 \mathrm{d}t\right]}. \quad (22)$$

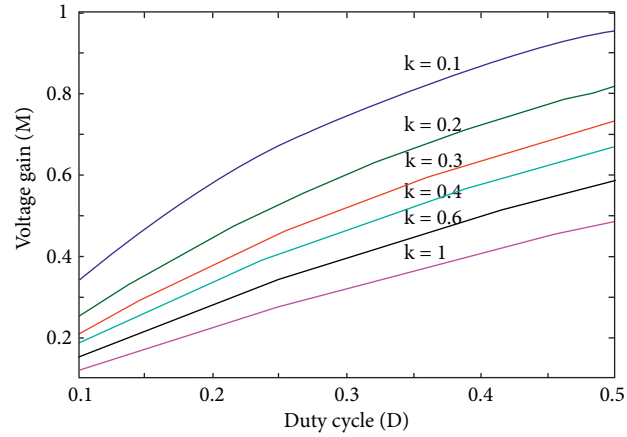


Figure 6: Voltage gain (M) versus duty cycle (D) plot for different values of k.

Table 1: Specifications of the proposed charger.

Parameters	Value (units)
Bridgeless PFC boost rectifier	
Power output (P_0)	300 W
Switching frequency (fs)	80 kHz
Inductors $(L1, L2, L3, L4)$	0.58 mH
Capacitor (C_1)	470 μF
Efficacy (η)	97%
Isolated resonant DC/DC converter	
Switching frequency (f_{sw})	100 kHz
Transformer turns ratio	1.326 : 1
Resonant inductor (L_r)	176 μH
Output capacitor (C_2)	470 μF
Efficacy (η)	96.5%

The average current through the antiparallel diodes of MOSFETs $M3$ and $M4$, I_{D34}, is given by

$$I_{D34} = \frac{1}{T}\int_{t_1}^{t_3} i_{Lr}(t)\mathrm{d}t. \quad (23)$$

The output filter capacitor C_{02} value is determined using capacitor RMS current Ic_{02}.

$$Ic_{02} = \sqrt{\frac{1}{T_P}\int_{t_0}^{T_P}\left(i_r(t) - I_o\right)^2 \mathrm{d}t},$$
$$C_{02} = \frac{I_{C02(\mathrm{rms})}}{4\pi f_s V_r}. \quad (24)$$

The critical component value for the prototype is given in Table 1.

5. Simulation Results

The simulation of the proposed charger is carried out for 300 W using PSIM. The converter is simulated under varying supply conditions. Figure 7(a) shows the simulated dynamic response of the converter when the input voltage is adjusted from 230 V to 110 V at time $t = 0.48$ s using conventional control technique. After two cycles of lowering the supply

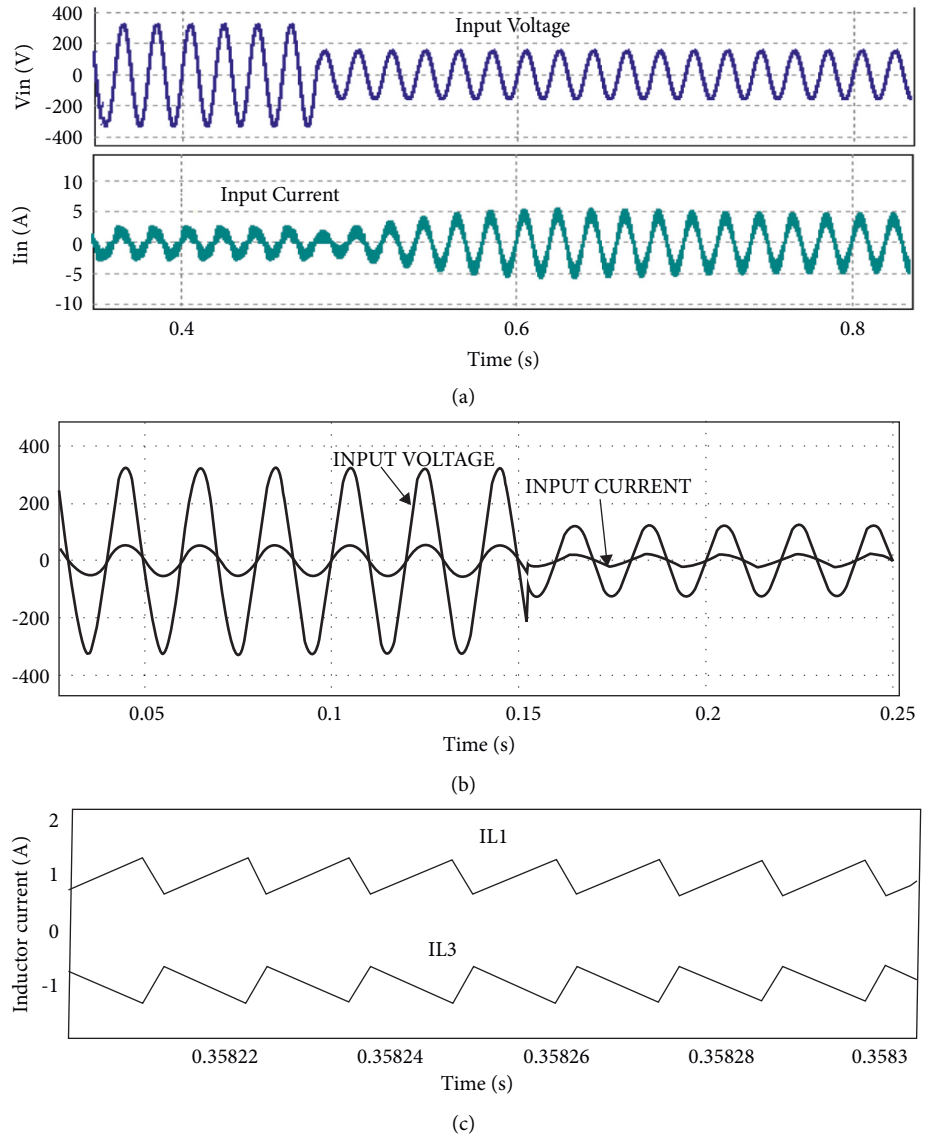


FIGURE 7: (a) Input supply voltage and current waveforms presenting power factor with 230 Vrm_s and 110 Vrms for conventional controller. (b) Input supply voltage and current waveforms presenting high power factor with 230 Vrms and 110 Vrms for RI controller. (c) Current through inductors L_1 and L_3.

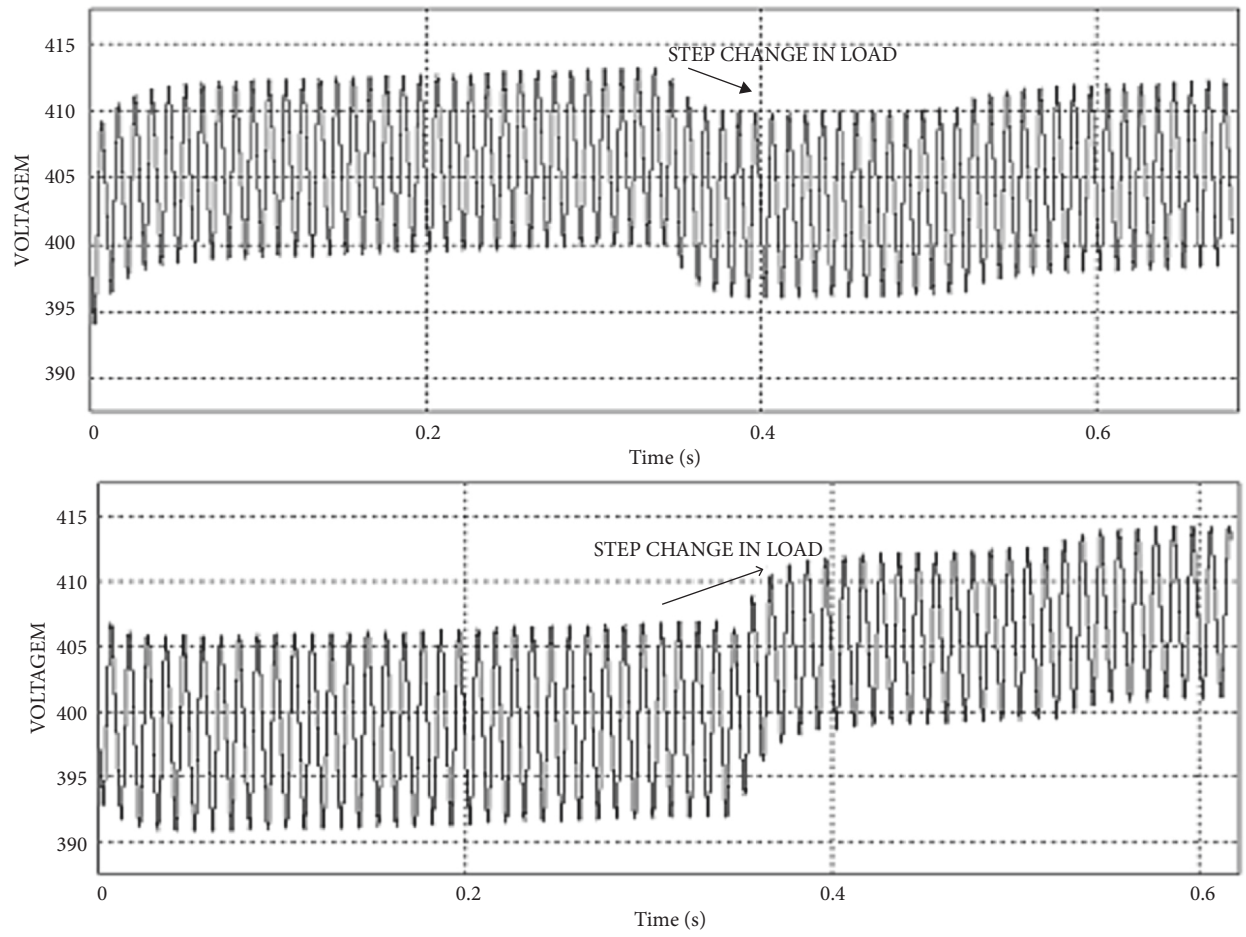
voltage, the input current begins to track the voltage, bringing the power factor closer to 0.9. This is due to the slow external voltage loop, which senses the change in output voltage first and then adjusts the current reference correspondingly.

The duty cycle of the switches is adjusted, resulting in the typical controller's slow response.

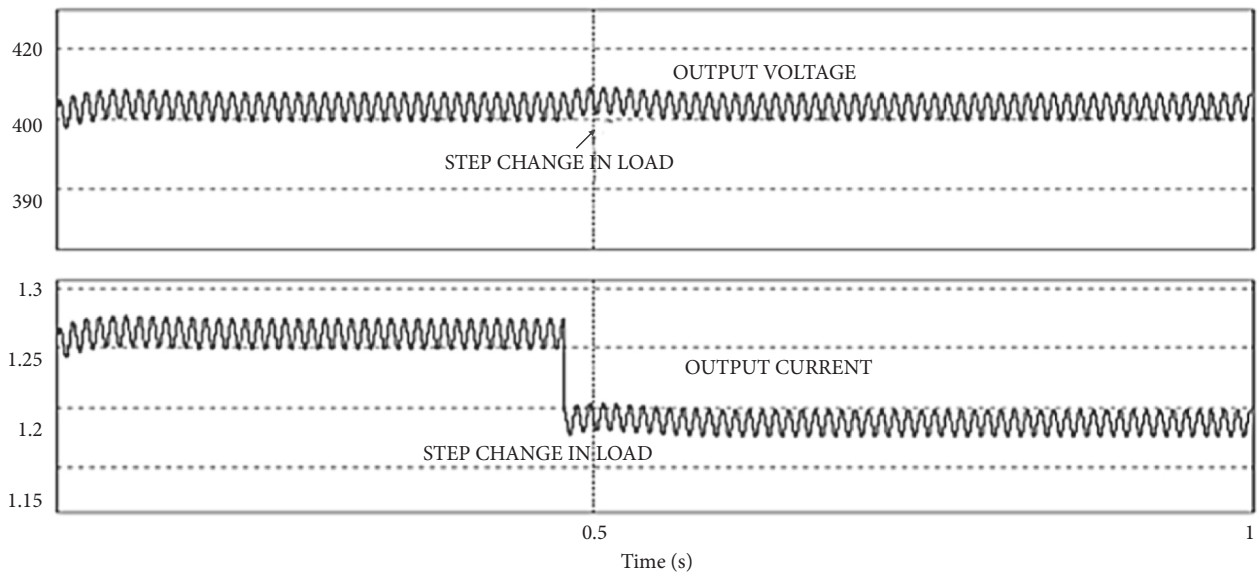
Figure 7(b) illustrates that when the supply voltage is changed from 230 V to 110 V, the power factor (PF) of the input supply is closer to unity. The interleaving inductors reduce the input current ripple in the proposed BLIL converter, and it is shown in Figure 7(b). Gain of PI controller ($K_p = 1$; $K_i = 33.33$) evaluated for PFC with input variations for predicting the performance of RI. It is obvious that the input power factor remains 0.99 for both the cases, in spite of the change in input voltage. Here, the input current traces the instantaneous value of input voltage very fast, and hence, Figure 7 shows a very good power factor with the proposed controller.

The output voltage and output current regulations are observed by introducing a step change in load at t = 0.38 s. Figure 8(a) shows the response of the output voltage when a positive and negative step load change is introduced at time $t = 0.38$, respectively. It takes more than 4 cycles ($t > 0.08$ s) to attain the steady-state condition. The output voltage and output current regulations of RI controller are observed by introducing a step change in load at t = 0.48 s. A positive step load change (300 W to 350 W) and a negative load change (300 W to 250 W) are introduced at t = 0.48 s as shown in Figures 8(b) and 8(c). The controller rejects the disturbances in one switching cycle, which eliminates the overshoot and undershoot of voltage across the device.

For the second-stage converter, the trailing edge gating pulses $vg1$ and $vg2$ with a duty cycle of 37.77% are given to the



(a)



(b)

Figure 8: Continued.

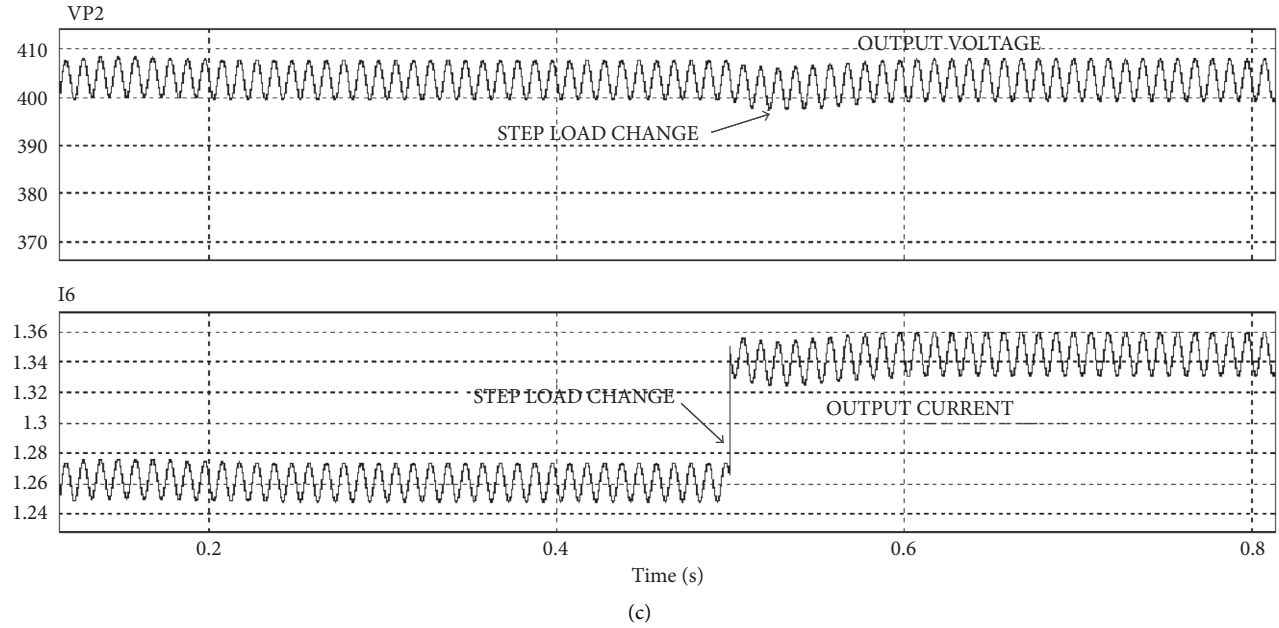


Figure 8: (a) Dynamic response of the ACM controller for step change in the load at $t = 0.38$ s. (b) Output voltage and output current for negative step load change at $t = 0.48$ s. (c) Output voltage and output current for a positive step load change at $t = 0.48$ s.

upper pair of switches $M1M_1$ and $M2$. The gating pulses G_4 for $M3$ ($vg3M_3$) and $M4$ ($vg4$) is fixed with 50% duty cycle.

The inverter's ZVS and ZCS turn-on and turnoff, as well as the converter side diodes' ZCS turn-on and turnoff, are accomplished. This rectifies a 300 V voltage and conducts it to the load, where 1 A is the current through the diode.

6. Hardware Results

The prototype feeding the resistive load shown in Figure 9 is designed and tested for 300 W. For the front-end converter, ferrite core inductors of 5.8 mH are connected with 600 V, 99 mΩ Rdson MOSFET for each channel of BLIL boost PFC converter. A 600 V and 6 A silicon carbide diodes are chosen as fast diodes. A resettable integrator PFC controller using IR1150 is used to enhance the PF on the supply side, and UC2895 IC is used as phase shift controller on DC/DC converter. MOSFETs with 600 V, 80 mΩ Rdson, 450 pF parasitic capacitance, are selected as switches for the inverter in the second stage and 400 V/47 μF capacitor for filtering output current ripples.

The converter is tested for (230–110) Vrms under variable load conditions. The waveforms shown in Figures 10(a) and 10(b) are observed on the input side for 230 Vrms and 110 Vrms, respectively, which depicts the input power factor closer to unity. Harmonic spectra of the input current waveform are shown in Figure 10(c), which illustrates that the THD is less than 5% at 110 V input, which is required for PHEV battery chargers to satisfy the IEC standard 61000 3-2 class D requirements.

The inverter gating pulses with duty cycle 37% for switches ($M1$ and $M2$) and 50% for the switches ($M3$ and $M4$) is observed in Figure 11(a). The DC/DC converter waveforms are shown for variable load conditions, focussing that the soft switching can be achieved. The input voltage with 136 V peak to peak for 100 W, appearing across the transformer primary winding, is shown Figure 11(b).

From the waveform, the passive interval (voltage zero instant) in DCM mode can also be observed. ZCS turn-on and turnoff can be attained for the diode ($D3$), which is depicted in Figure 11(c). The DC output voltage 294 V and output current 0.991 A obtained from the diode bridge rectifier is shown in Figure 12(a).

7. Comparison

The proposed topology is compared with the existing front-end converter topology controlled by conventional ACM technique in terms of THD, semiconductor loss distribution, and overall efficacy of the charger system.

The loss distribution for interleaved boost and BLIL boost converter is presented in Figure 12(b) for the following operating conditions: $V_{in} = 230$ V, $V_{out} = 400$ V, switching frequency (fs) = 80 kHz, and output power $P_0 = 300$ W. Conduction losses, switching losses, $1/2CV^2$, and gate charge losses are considered for MOSFET. As SiC diodes are chosen, reverse recovery losses are negligible. The presence of bridge rectifier in interleaved boost converter contributes large portion of loss (approximately 3 W). From the Figure 12(b), total device losses of BLIL converter have lower losses (~3.9 W) when compared to interleaved boost converter. Moreover, the second-stage converter has soft switching achieved for FETs and diodes. Hence, the loss contribution of DC/DC converter is comparatively less compared to conventional DC/DC converter resulting in highly efficient battery charger.

THD of the input current from Figure 13(a) clearly indicates that it complies with IEC standard 61000 3-2 class

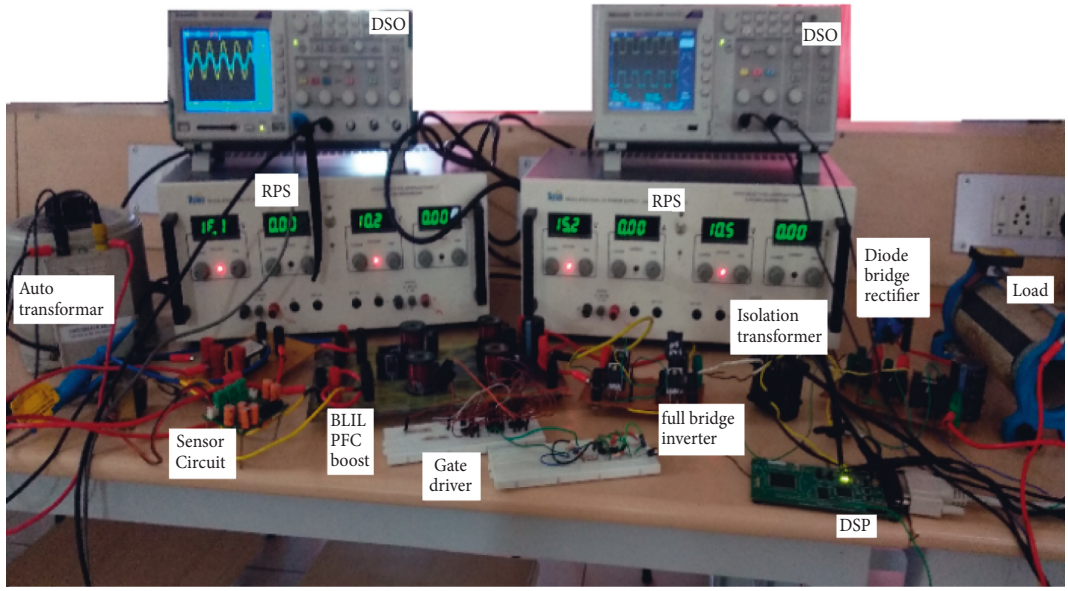


Figure 9: Experimental setup.

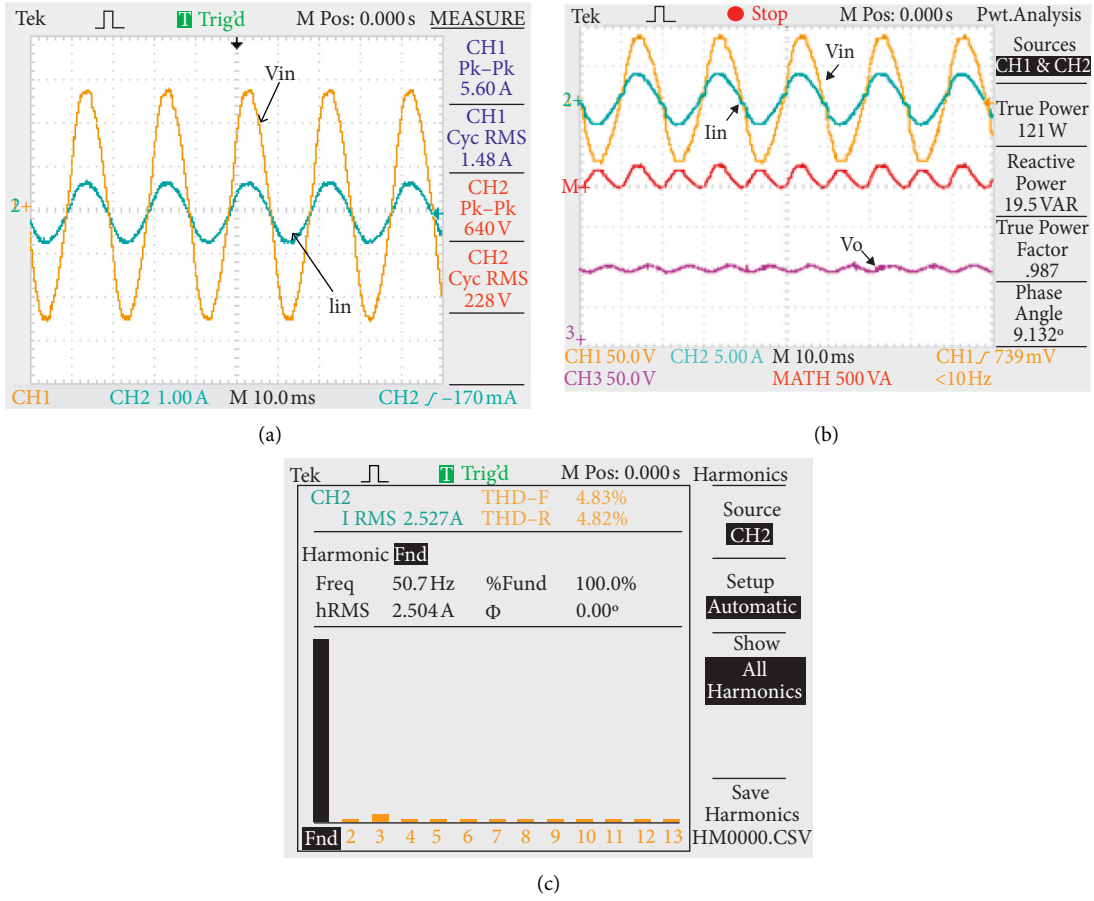


Figure 10: (a) Input voltage and input current waveform of 300 W BLIL boost converter. (b) BLIL boost converter tested for 120 W. (c) THD of input current for 300 W at 110 V input voltage.

D limit when the converter is operated at 230 V and 110 V at full load condition. Figure 13(b) is the comparison graph of traditional interleaved and BLIL boost converter as front-end converter for variable output power. The graph implies that the peak efficiency of the charger with BLIL PFC converter is 96.5%, whereas the traditional interleaved converter efficiency is 93%. The comparison of the charger setup with respect to control technique is analysed and

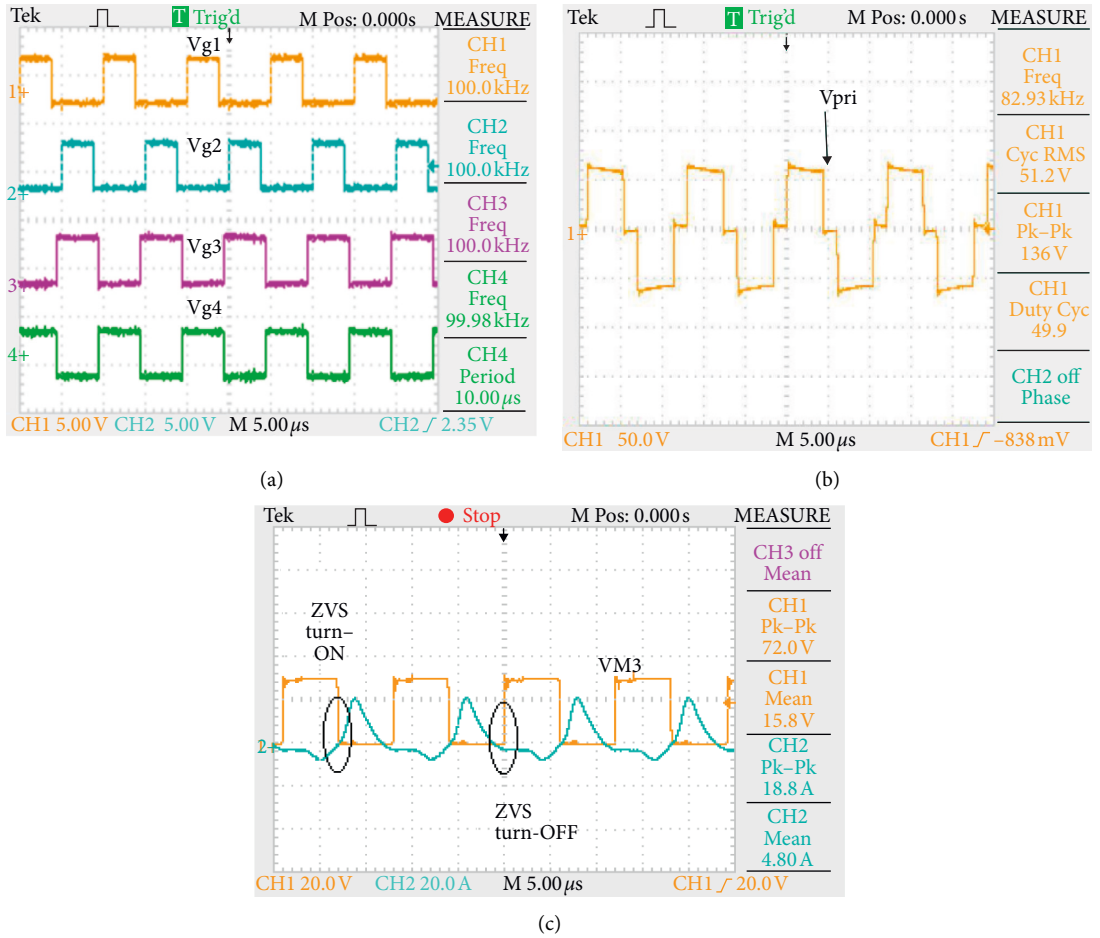


FIGURE 11: (a) Gating pulses to Switches $M1\,(Vg1)$, $M2\,(Vg2)$, $M3\,(Vg3)$, and $M4\,(Vg4)$, (b) Transformer primary voltage for 100 W, and (c) ZCS turn-on and turnoff of diodes for 180 W.

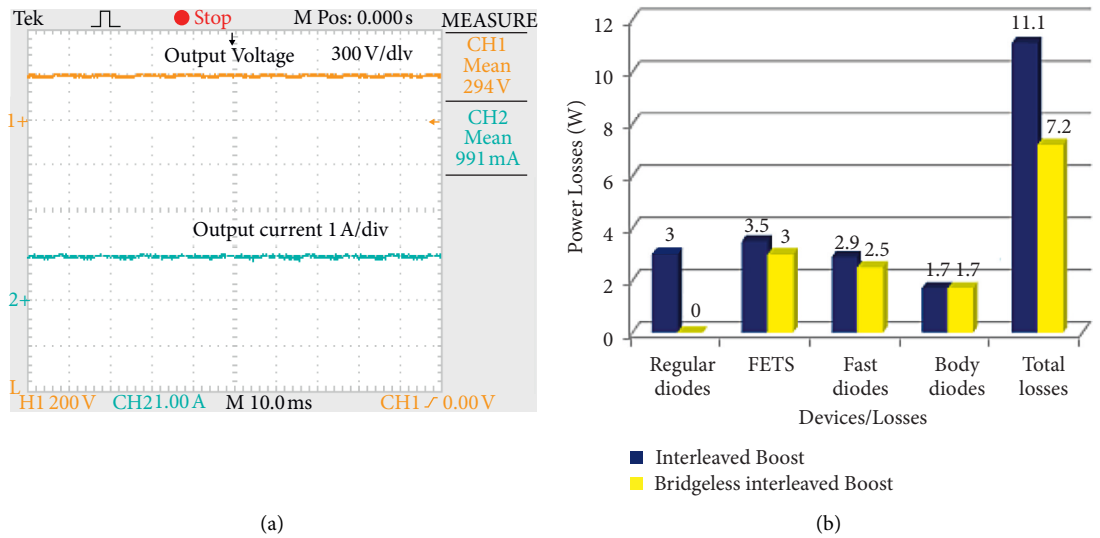


FIGURE 12: (a) Output voltage and output current waveform for 300 W. (b) Device loss distribution for interleaved boost and BLIL boost converter for 300 W prototype.

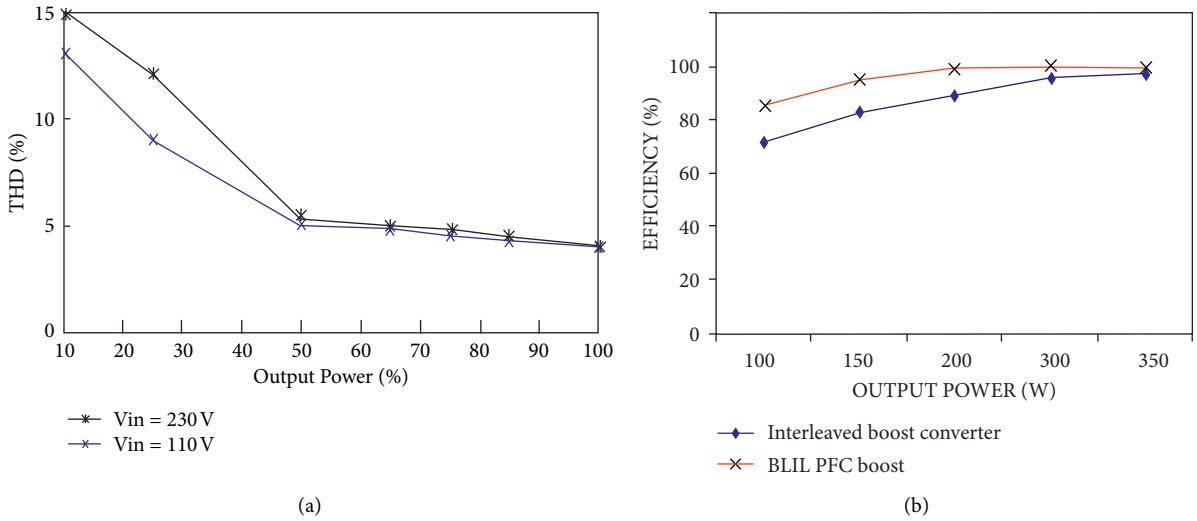


FIGURE 13: (a) Total harmonic distortion vs output power (%) for $V_{in} = 110$ V and $V_{in} = 230$ V. (b) Efficacy of the converter under variable load condition.

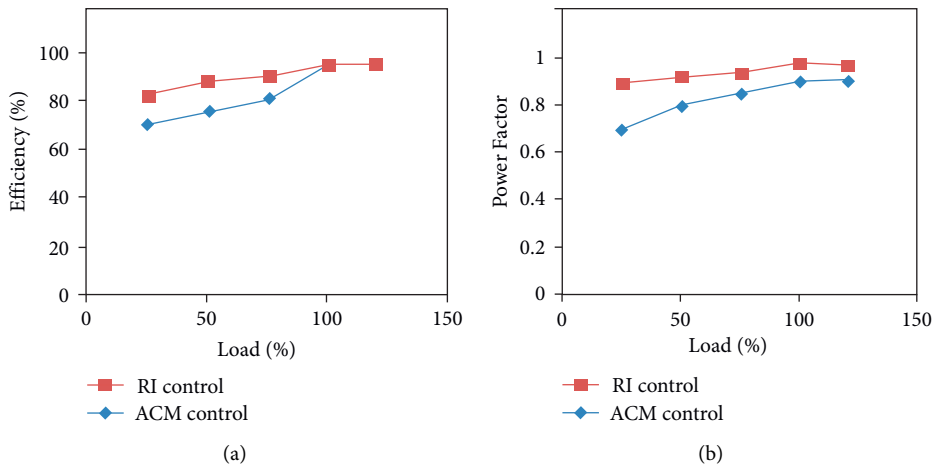


FIGURE 14: (a) Efficacy vs load power (%). (b) Power factor vs load (%).

shown in Figures 14(a) and 14(b). From the graph, it is inferred that the efficacy and power factor of the front-end converter of the charger are high for RI control than ACM control.

8. Conclusion

A high-performance two-stage converter topology for PHEV battery charger with improved PFC rectifier as front-end and a high-frequency ZVS-ZCS DC/DC converter as the second stage has been discussed in this paper. The operation, design considerations, and performance comparison with the traditional two-stage approach are presented. A non-linear RI control technique is implemented for the front-end converter, which corrects power factor closer to unity in one switching cycle at variable load powers. THD of the input current is less than 5%, which is compliant with the IEC 61000 3-2 standard. For PFC converter and DC/DC converter, respectively, the proposed charger achieves a peak efficiency of 96.5% at 80 kHz and 100 kHz switching frequency. It operates for a wide output load variation. Thus, the overall designated charger unit achieves an efficiency of 3.5% higher than the conventional battery charger unit.

Data Availability

The data used to support the findings of this study are included in the article. Should further data or information be required, these are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

The authors thank and acknowledge the management of Vellore Institute of Technology Chennai for their support to

carry out this research work. The authors appreciate the supports from Saveetha School of Engineering, SIMATS, Chennai.

References

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 3, pp. 641–660, 2004.

[2] J. P. M. Figureueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase PFC topologies based on the boost converter," in *Proceedings of the IEEE/IAS Int. Conf. Ind. Appl. (INDUSCON)- 9th*, pp. 1–6, Sao Paulo, Brazil, November 2010.

[3] J. A. Sanguesa, V. Torres-Sanz, P. Garrido, F. J. Martinez, and J. M. Marquez-Barja, "A review on electric vehicles: technologies and challenges," *Smart Cities*, vol. 4, no. 1, pp. 372–404, 2021.

[4] I. Rahman, P. M. Vasant, B. M. Singh, and M. A. A. Wadud, "Optimisation of PHEV/EV charging infrastructures: a review," *International Journal of Energy Technology and Policy*, vol. 10, no. 3/4, pp. 280–296, 2014.

[5] A. Khaligh and Z. Li, "Battery, ultracapacitor, fuel cell, and hybrid energy storage systems for electric, hybrid electric, fuel cell, and plug-in hybrid electric vehicles: state of the art," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 6, pp. 2806–2814, 2010.

[6] K. Fahem, D. E. Chariag, and L. Sbita, "On-board bidirectional battery chargers topologies for plug-in hybrid electric vehicles," in *Proceedings of the Presented at the International Conference on Green Energy Conversion Systems (GECS)*, Hammamet, Tunisia, March 2017.

[7] K. Nagarajan, A. Rajagopalan, S. Angalaeswari, L. Natrayan, and W. D. Mammo, "Combined economic emission dispatch of microgrid with the incorporation of renewable energy sources using improved mayfly optimization algorithm," *Computational Intelligence and Neuroscience*, vol. 2022, Article ID 6461690, 22 pages, 2022.

[8] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An automotive onboard 3.3-kW battery charger for PHEV application," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 8, pp. 3466–3474, 2012.

[9] W. Frank, M. Reddig, and M. Schlenk, "New control methods for rectifier-less PFC-stages," in *Proceedings of the IEEE International Symposium on Industrial Electronics, 2005. ISIE 2005*, vol. 2, pp. 489–494, Dubrovnik, Croatia, June 2005.

[10] L. Huber, Y. Yungtaek Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1381–1390, 2008.

[11] M. O'Loughlin, "An interleaving PFC pre-regulator for high-power converters," *Texas Instruments*, vol. 7, pp. 1–14, 2006.

[12] F. Musavi, W. Eberle, and W. G. Dunford, "A phase shifted semi-bridgeless boost power factor corrected converter for plug in hybrid electric vehicle battery chargers," in *Proceedings of the 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 821–828, Fort Worth, TX, USA, March 2011.

[13] Y. Yungtack Jang, M. M. Jovanovic, and Y.-M. Chang, "A new ZVS-PWM full-bridge converter," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1122–1129, 2003.

[14] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1746–1756, 2011.

[15] B. Gu, J. S. Lai, N. Kees, and C. Zheng, "Hybrid-switching full-bridge DC-DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1132–1144, 2013.

[16] M. Miralinaghi, G. H. de Almeida Correia, S. E. Seilabi, and S. Labi, "Designing a network of electric charging stations to mitigate vehicle emissions," in *Proceedings of the 2020 Forum on Integrated and Sustainable Transportation Systems (FISTS)*, pp. 95–100, IEEE, Delft, Netherlands, November 2020.

[17] C. Q. Tran, M. Keyvan-Ekbatani, D. Ngoduy, and D. Watling, "Dynamic wireless charging lanes location model in urban networks considering route choices," *Transportation Research Part C: Emerging Technologies*, vol. 139, no. 2022, Article ID 103652, 2022.

[18] M. Miralinaghi, B. B. Keskin, Y. Lou, and A. M. Roshandeh, "Capacitated refueling station location problem with traffic deviations over multiple time periods," *Networks and Spatial Economics*, vol. 17, no. 1, pp. 129–151, 2017.

[19] J. He, H. Yang, T.-Q. Tang, and H.-J. Huang, "An optimal charging station location model with the consideration of electric vehicle's driving range," *Transportation Research Part C: Emerging Technologies*, vol. 86, pp. 641–654, 2018.

[20] L. S. C. e Silva, F. J. M. de Seixas, and M. A. G. de Brito, "Bridgeless interleaved boost PFC converter with variable duty cycle control. XI Brazilian Power Electron," *Confins*, vol. 7, pp. 397–402, 2011.

[21] C.S. S. Anupama, L. Natrayan, E. L. Lydia et al., "Deep learning with backtracking search optimization based skin lesion diagnosis model," *Computers, Materials & Continua*, vol. 70, no. 1, pp. 1297–1313, 2021.

[22] R. K. Rai, A. Dixit, S. Pundhir, and J. Peter, "Advanced integrated bidirectional AC/DC and DC/DC converter for plug-in hybrid electric vehicles," in *Proceedings of the 2020 International Conference on Futuristic Technologies in Control Systems & Renewable Energy (ICFCR)*, pp. 1–6, Malappuram, India, September 2020.

[23] B. Das, P. K. Panigrahi, and C. K. Samant, "Impact analysis of plug-in hybrid electric vehicle on integration with micro grid -A review," in *Proceedings of the 2020 IEEE International Symposium on Sustainable Energy, Signal Processing and Cyber Security (iSSSC)*, pp. 1–5, Gunupur Odisha, India, December 2020.

[24] D. K. Jain, S. K. S. Tyagi, S. Neelakandan, M. Prakash, and L. Natrayan, "Metaheuristic optimization-based resource allocation technique for cybertwin-driven 6G on IoE environment," *IEEE Transactions on Industrial Informatics*, vol. 18, no. 7, pp. 4884–4892, 2022.

[25] W. Chuanyun, X. Ming, F. C. Lee, and L. Bing, "EMI study for the interleaved multi-channel PFC," in *Proceedings of the Power Electron. Spec. Conf. 2007. PESC 2007*, pp. 1336–1342, IEEE, Orlando, FL, USA, June 2007.

[26] P. Asha, L. Natrayan, B. T. Geetha et al., "IoT enabled environmental toxicology for air pollution monitoring using AI techniques," *Environmental Research*, vol. 205, Article ID 112574, 2022.

[27] F. Musavi, W. Eberle, and W. G. Dunford, "A High-Performance Single-phase AC-DC Power Factor Corrected Boost Converter for Plug in Hybrid Electric Vehicle Battery Chargers," in *Proceedings of the Energy Convers. Congr. Expo.*

ECCE 2010, pp. 3588–3595, IEEE, Atlanta, GA, USA, September 2010.

[28] T. Jin and K. M. Smedley, "Operation of one-cycle controlled three-phase Active power filter with unbalanced source and load," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1403–1412, 2006.

[29] D. Yang, M. Yang, and X. Ruan, "One-cycle control for a double-input DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4646–4655, 2012.

[30] M. Orabi, R. Haron, and a El-Aroudi, "Comparison between nonlinear-carrier control and average-current-mode control for PFC converters, power electron," in *Proceedings of the Spec. Conf. 2007. PESC 2007*, pp. 1349–1355, IEEE, Orlando, FL, USA, June 2007.

[31] A. S. Tandon, N. Yalla, A. Praneeth, V. Anand, and P. Kumar, "Design of GaN Based 72V,3.3KW LLC Resonant Converter for On-Board EV Charger," in *Proceedings of the 2021 IEEE Madras Section Conference (MASCON)*, pp. 1–6, IEEE, Chennai, India, August 2021.

[32] J. S. V. S. Kumar and P. Mallikarjuna Rao, "Performance analysis of PID controller and sliding mode control for electric vehicle applications in interleaved double boost converter," in *Intelligent Computing in Control and Communication*, G. C. Sekhar, H. S. Behera, J. Nayak, B. Naik, and D. Pelusi, Eds., vol. 702, Springer, Lecture Notes in Electrical Engineering, , pp. 47–59, 2021.