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Research Article

Fault-Tolerant Control Strategy for Neutral-Point-Clamped Three-Level Inverter

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A fault-tolerant control technique is discussed for the Neutral-Point-Clamped (NPC) three-level inverter, which ensures that the NPC inverter operates normally even under device failures. A two-level leg is added to the NPC inverter; when the device open circuit fault occurs, the load of this faulty phase is connected to the neutral point of this two-level leg through the bidirectional thyristors. An improved Space Vector Pulse Width Modulation (SVPWM) strategy called "addition and subtraction substitution SVPWM" is proposed to effectively suppress fluctuation in capacitor neutral-point voltages by readjusting the sequence and action time of voltage vectors. The fault-tolerant topology in this paper has the advantages of fewer switching devices and lower circuit costs. Experimental results show that the proposed fault-tolerant system can operate in balance of capacitor neutral-point voltages at full output power and the reliability of the inverter is greatly enhanced.

1. Introduction

Compared with the conventional two-level inverters, multilevel inverters have the advantages of lower voltage stress, better waveform spectrum, less voltage change rate, and waveform distortion [1–3]. Therefore, it is widely used in various electric power conversion and power transmission applications, such as inverter system, low-voltage motor drives, and wind power generation [4–6]. However, there are many switching devices in multilevel inverters, and the control of these switches becomes more complex, which leads to a significant increase in failure rate. Then the reliability of the circuit is greatly deteriorated. If the open fault is not dealt with in time, the voltage stress of certain switch will increase owing to the fluctuation of capacitor neutral-point voltages. What is worse, the entire circuit operates abnormally, causing serious accidents or incalculable economic losses [7–9]. In some applications, higher reliability of the circuit is required that it is even expected that the circuit should keep working for a period under the device failures. So, in recent years, the research of fault-tolerant control for multilevel inverters has attracted wide attention from scholars [10–12].

For three-level inverters, there are a variety of fault-tolerant control methods. The fault-tolerant control of the Active Neutral-Point-Clamped (ANPC) inverter using the redundant switching states has been proposed in [13]. The inverter can operate in balance of capacitor neutral-point voltages with symmetrical three-phase output after the proposed fault-tolerant control method is applied. However, the amplitude of output voltage and current are greatly decreased. A load-type fault-tolerant solution of the ANPC inverter has been proposed in [14, 15]. The basic idea of this method is to keep the faulty leg at O level, which is achieved by connecting the faulty leg to the neutral point of the DC-link capacitor. Similarly, the inverter can only operate at reduced rated power. The fault-tolerant of half-bridge switches and neutral-point switches in T-type inverter has been proposed in [16, 17]. The redundant switching states are used to synthesize the reference vector of the rotational voltage in SVPWM algorithm, which enables the inverter to operate normally in the fault condition. However, for the open fault of half-bridge switches, the DC-link voltage utilization ratio is half of this inverter. The fault-tolerant control of the T-type inverter using the additional leg has

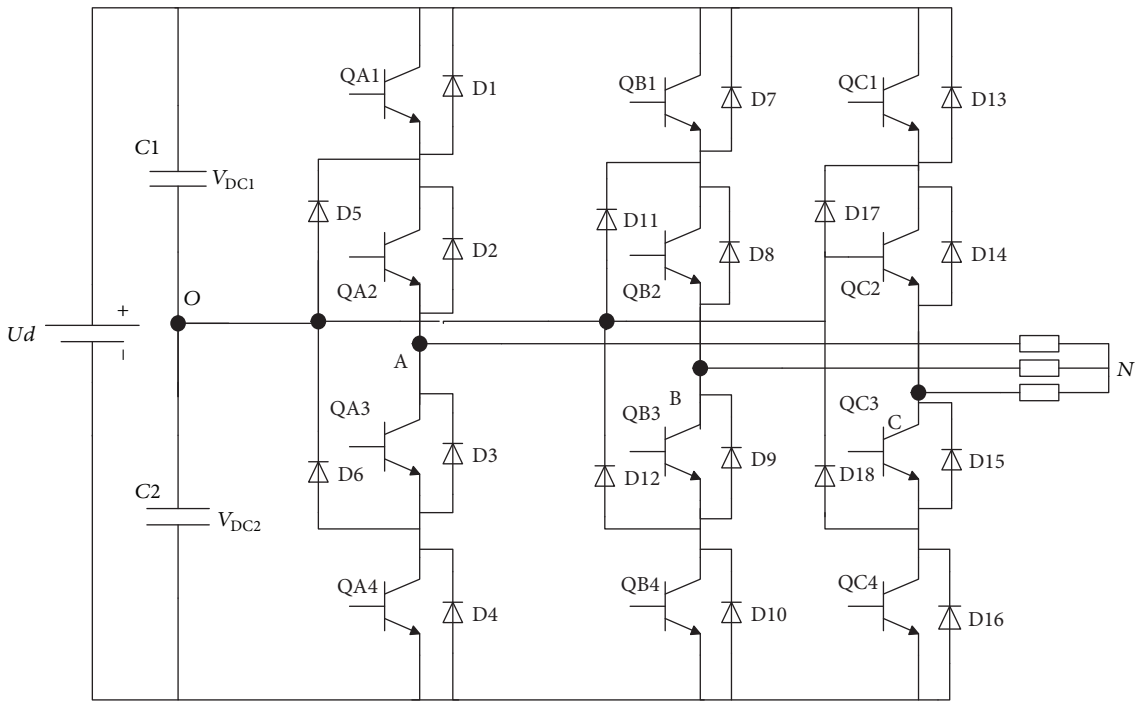

Figure 1: The main circuit of NPC three-level inverter.

been proposed in [18]. The one-phase bridge of the T-type inverter is used as the additional leg. Once a fault is detected, the faulty phase is connected to the additional leg by the corresponding bidirectional thyristors. The inverter can output the full-rated power in any fault condition, with higher manufacturing costs and larger size and weight. The eight-switch three-phase inverters (ESTPIs) reconfigured topologies for the NPC inverter have been proposed in [19]. When the device open circuit fault occurs, the corresponding bidirectional thyristors of the faulty leg is triggered, and the faulty leg is connected to the neutral point of the DC-link capacitor. However, the inverter can only operate at half output power; also the amplitude of the output voltage is decreased by half. The fault-tolerant control of the NPC inverter using the asymmetric leg has been proposed in [20]. The faulty leg is isolated by the bidirectional thyristors under device failures, and an asymmetric two-level leg is added to the inverter. To eliminate the low-order harmonic component of the output phase voltages, the bipolar Sinusoidal Pulse Width Modulation (SPWM) method is used to control the asymmetric leg. The inverter can operate in balance of three phases' output without reducing the output power of the original circuit. A software redundancy fault-tolerant control algorithm of the NPC inverter has been proposed in [21]. This method is implemented by using the redundant voltage vectors, with some limitations that apply only to open circuit fault and short circuit fault of outer switches.

When the open circuit fault of inner switches occurs in the NPC three-level inverter, some voltage vectors are lost, and the synthesis of the possible voltage vectors for reference voltage cannot be implemented. Consequently, the reconfiguration of the circuit is required for fault-tolerant control. In order to ensure the NPC inverter can output the full-rated power under device failures, a two-level leg serves as the additional leg for the faulty phase in this paper. When the open circuit fault occurs in the NPC inverter, the faulty leg is connected to the additional leg through the bidirectional thyristors. Both the switching states P and N, generated by modifying the SVPWM algorithm, are employed to control the additional leg. In addition, in order to accurately suppress the fluctuation of the capacitor neutral-point voltages, an improved SVPWM strategy called "addition and subtraction substitution SVPWM" is proposed to readjust the sequence and action time of voltage vectors in SVPWM algorithm.

2. Description of NPC Inverter

Figure 1 shows the main circuit of NPC three-level inverter. There are three switching states for each leg [22], namely, P, O, and N. For instance, the relation between switching states and switching sequence of phase A is listed in Table 1.

In Table 1, "1" indicates that the power device is turned on and "0" indicates turn-off. The symbol "+" represents the current flows from the power supply to the load; on the contrary, the symbol "−" represents the current flows from the load to the power supply.

It can be known from Figure 2 that the NPC inverter has 27 combinations of switching states that correspond to 27 space voltage vectors, divided into four classes according to their magnitudes, namely, zero-, small-, medium-, and large-voltage vectors [23, 24].

Table 1: Switching states in NPC three-level inverter.

Switching states	Switching sequence									
	QA1	QA2	QA3	QA4	D1	D2	D3	D4	D5	D6
P+	1	1	0	0	0	0	0	0	0	0
P−	0	0	0	0	1	1	0	0	0	0
O+	0	1	0	0	0	0	0	0	1	0
O−	0	0	1	0	0	0	0	0	0	1
N+	0	0	0	0	0	0	1	1	0	0
N−	0	0	1	1	0	0	0	0	0	0

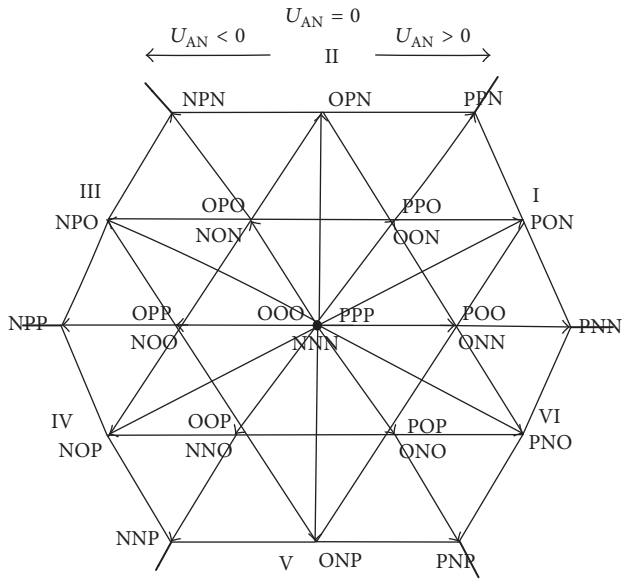

Figure 2: Voltage vector distribution of NPC three-level inverter.

3. Effect of the Switching States on Neutral-Point Voltages

When the open circuit fault occurs in NPC three-level inverter, the absence of the switching states leads to the change in the current flow paths. Consequently, an undesirable bridge arm phase voltage is generated, which can bring out the distortion of the load phase current, resulting in the fluctuation of the capacitor neutral-point voltages. The analysis is illustrated with QA1 and QA2 single-switch fault of phase A. The direction of the current flows from the power supply to the load is defined as the positive direction $I_a > 0$.

(1) QA1 Fault. The current can only flow through the switch QA2 and the diode D5 to the load under the switch QA1 fault, while the inverter operates in the P state and the current $I_a > 0$. The load is connected to the neutral point of DC side and the inverter operates in the O state, as shown in Figure 3(a). The solid line represents that the inverter operates normally, whereas the dotted line denotes the inverter under the QA1 fault condition. The bridge arm phase voltage varies from $+1/2U_d$ to zero, which causes the distortion of load phase current. Under these circumstances, all voltage vectors that start with "P" are undesirable, including small-voltage vectors [PPO], [POO], and [POP]; medium-voltage vectors [PON] and [PNO]; and large-voltage vectors [PNN], [PPN], and [PNP], as shown in Figure 4(a). These impossible voltage vectors are replaced by the voltage vectors enclosed with brackets that start with "O"; conversely, the voltage vectors that start with "O" or "N" state in phase A are desirable, because the QA1 fault has no effect on them. That is, the number of the current branches flowing to load from the neutral point of DC side is more than that in the normal state. Therefore, the upper capacitor voltage V_{DC1} is greater than the lower capacitor voltage V_{DC2}.

(2) QA2 Fault. As illustrated in Figure 3(a), one condition is that the QA2 fault occurs in the case that the inverter operates in the P state and the current $I_a > 0$, the current flows through the diodes D3 and D4 to the load, and the inverter operates in the N state. This condition brings out the change in the magnitude of bridge arm phase voltage and current. The other one is that the inverter operates in the O state and the current $I_a > 0$. In the same way, the current flows through the diodes D3 and D4 to load, and the switching state is N, as shown in Figure 3(b). The solid line means the inverter in the normal state and the dotted line indicates the inverter under the QA2 fault condition. Thus, it can be observed from Figure 4(b) that all voltage vectors beginning with "P" and "O" are crossed out and these voltage vectors are replaced by the voltage vectors beginning with "N"; the number of the current branches flowing to load from the neutral point of DC side is less than that in the normal state. Similarly, it can be derived that V_{DC2} is greater than V_{DC1}.

In summary, the device open circuit fault can cause unbalance of the capacitor neutral-point voltages in the NPC inverter.

4. Fault-Tolerant Topology and Working Principle

As shown in Figure 4, when the QA1 open circuit fault occurs, the equivalent stator flux circle can still be synthesized by adjusting the sequence of the available voltage vectors based on vector superposition theorem, but the voltage utilization ratio is half. In contrast, the inverter has no fault tolerance ability in case of the QA2 fault because there is no redundant voltage vectors to synthesize the stator flux circle in the area $U_{AN} > 0$. Therefore, in order to enable the NPC inverter to operate at full output power under the device failures, a

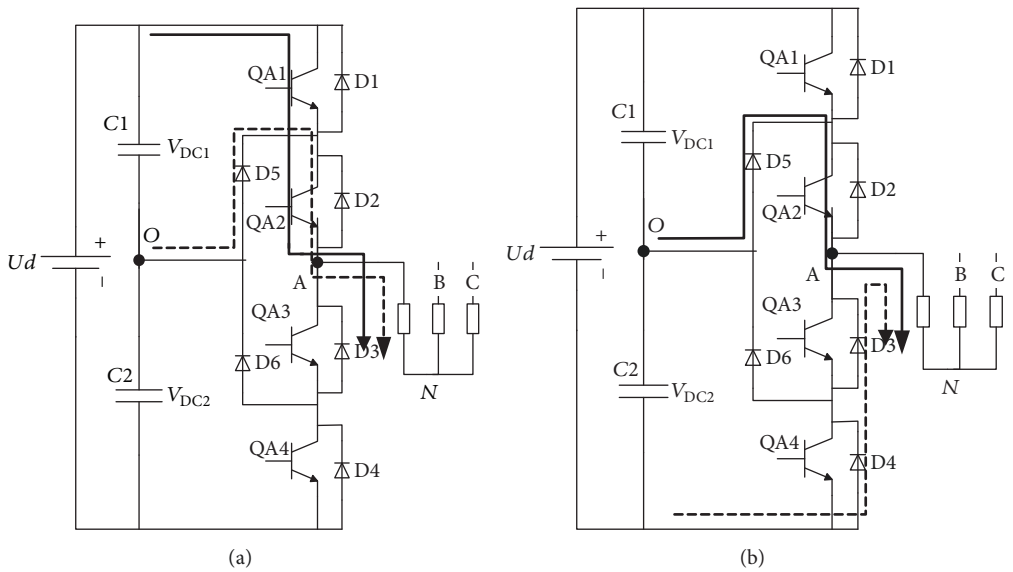

Figure 3: Change of current paths under open circuit fault. (a) QA1 fault. (b) QA2 fault.

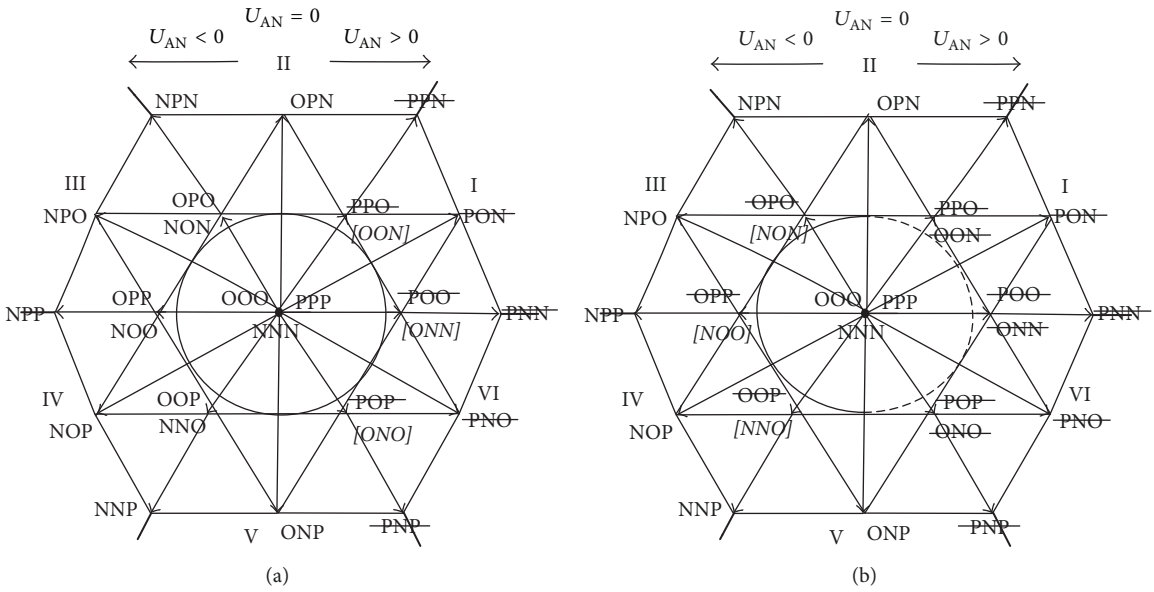

Figure 4: Voltage vector distribution under device open fault of phase A. (a) QA1 fault. (b) QA2 fault.

two-level leg is added to the main circuit of the NPC three-level inverter, which consists of two switches Q1 and Q2 and corresponding antiparallel diodes D19 and D20. In addition, six bidirectional thyristors *Trx*1 and *Trx*2 ($x = a$, b, and c) are used to constitute the fault-tolerant topology of the NPC inverter, as shown in Figure 5.

When the NPC inverter operates normally, *Trx*1 ($x = a$, b, and c) are connected and *Trx*2 ($x = a$, b, and c) are disconnected. If the open fault of phase A occurs, the faulty phase is isolated by *Tra*1, and the midpoint O′ of this two-level leg is connected to load of the faulty phase through *Tra*2. Both the switching states P and N, generated by modifying the SVPWM algorithm, are aimed at controlling the two switches Q1 and Q2 of this two-level leg. Obviously, the O state is not available. It is essential to readjust the sequence and action time of voltage vectors. In general, the proposed reconfiguration topology can maintain the neutral-point voltages balance and operate at full output power under any fault condition.

5. SVPWM Strategy of Addition and Subtraction Substitution

After the fault reconstruction topology is adopted, different voltage vector distribution can be obtained, as illustrated in Figure 6.

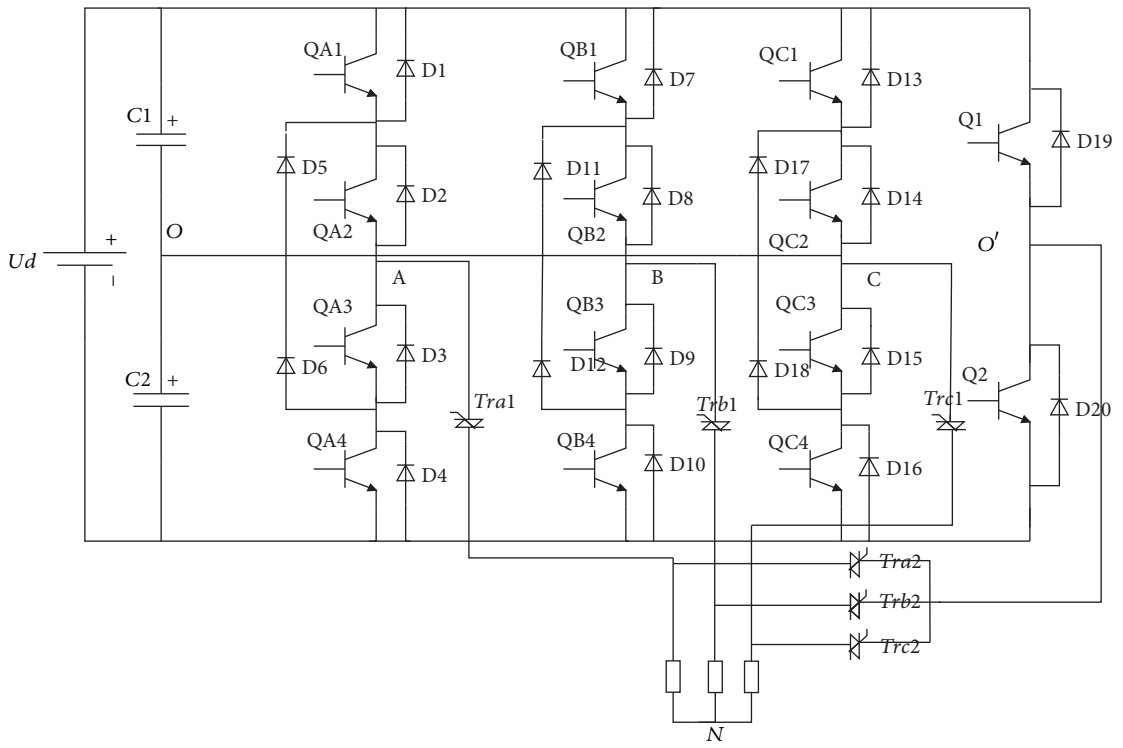

Figure 5: Fault-tolerant topology of NPC inverter.

Table 2: Substitution law of voltage vectors.

Region	Voltage vectors
I	[OOO] → [PPP], N-type → P-type
II-1, 3, 5	[OOO] → [PPP], N-type → P-type, [OPN] → [PPO]+ [NON]
II-2, 4, 6	[OOO] → [NNN], P-type → N-type, [OPN] → [PPO]+ [NON]
III	[OOO] → [NNN], P-type → N-type,
IV	[OOO] → [NNN], P-type → N-type
V-1, 3, 5	[OOO] → [NNN], P-type → N-type, [ONP] → [POP]+ [NNO]
V-2, 4, 6	[OOO] → [PPP], N-type → P-type, [OPN] → [POP]+ [NNO]
VI	[OOO] → [PPP], N-type → P-type

The equivalent stator flux circle can still be synthesized by adjusting the sequence of the available voltage vectors, and the inverter can output the full-rated power. An improved SVPWM strategy called "addition and subtraction substitution SVPWM" is proposed to effectively suppress the fluctuation of the capacitor neutral-point voltages. The fault-tolerant control of NPC inverters is carried out by adjusting the sequence and operation time of voltage vectors. The research is conducted only taking phase-A fault as an example.

If the phase-A fault occurs, the faulty phase A is replaced with a two-level leg, which is controlled by the switching states P and N. Therefore, the switching states that start with "O" are prohibited, as shown in Figure 6, and these undesirable voltage vectors should be replaced by other voltage vectors of the same size. Namely, N-type voltage vectors ([OON], [ONN], and [ONO]) in the regions I, II-1, II-3, II-5, and VI are replaced, respectively, with P-type voltage vectors ([PPO], [POO], and [POP]). For the purpose of restraining the fluctuation of the capacitor neutral-point voltages effectively, P-type voltage vectors ([OPO], [OPP], and [OOP]) in the opposite regions IV, V-1, V-3, V-5, and III should be replaced, respectively, with N-type voltage vectors ([NON], [NOO], and [NNO]). However, there are no redundant voltage vectors in the medium-voltage vectors ([OPN] and [ONP]) in regions II and V. In this paper, the medium-voltage vectors are replaced by the small-voltage vectors adjacent to them. Table 2 presents the substitution law of voltage vectors in each region.

"Addition and subtraction substitution SVPWM" is simply defined by adding or subtracting a minimum action time (T_{low}) to the three-phase action times (T_a, T_b, and T_c) to realize the substitution of voltage vectors in the SVPWM algorithm. The sequence and action time of voltage vectors are adjusted by replacing the undesirable voltage vectors with the remaining voltage vectors of the same size, where T_{low}

Table 3: The sequence and action time of voltage vectors in each region.

Region	Switching sequence	Action time
I-1	POO-PPO-PPP-PPP-PPO-POO	M
I-2	POO-PPO-PPP-PPP-PPO-POO	$M1$
I-3	PON-POO-PPO-PPO-POO-PON	$M1$
I-4	PON-POO-PPO-PPO-POO-PON	$M2$
I-5	PNN-PON-POO-POO-PON-PNN	$M2$
I-6	PON-PPN-PPO-PPO-PPN-PON	$M2$
IV-1	NNN-NNO-NOO-NOO-NN0-NNN	$M2$
IV-2	NNN-NNO-NOO-NOO-NN0-NNN	$M1$
IV-3	NNO-NOO-NOP-NOP-NOO-NNO	$M1$
IV-4	NNO-NOO-NOP-NOP-NOO-NNO	M
IV-5	NOO-NOP-NPP-NPP-NOP-NOO	M
IV-6	NNO-NNP-NOP-NOP-NNP-NNO	M

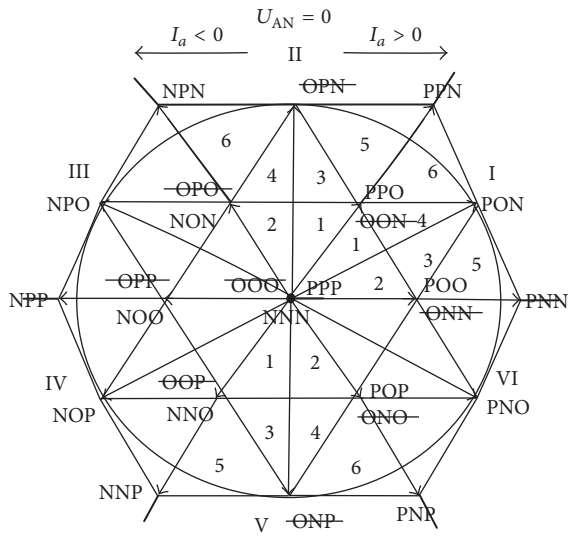

Figure 6: Voltage vector distribution after the fault tolerance.

Table 4: Experimental parameters.

Dc-link voltage	400 V
Fundamental frequency	$f_n = 50$ Hz
Switching frequency	$f_k = 3$ kHz
Sampling time	$T = 1e-4$
Neutral capacitance	$C1 = C2 = 0.008$ F
RL load	4Ω/3 mH

represents the minimum value among T_a, T_b, and T_c. In this method, the N-type voltage vectors can be substitute for the P-type voltage vectors after T_{low} is added to T_a, T_b, and T_c. In contrast, the P-type voltage vectors take the place of the N-type voltage vectors by subtracting T_{low} to T_a, T_b, and T_c. The process will be explained in two regions I-1 and III-2.

The sequence and action time of voltage vectors in region I-1 in the normal state are shown in Figure 7(a). The undesirable N-type voltage vectors [ONN] should be replaced by the P-type voltage vectors [POO], and this process is achieved by subtracting T_{low} in three-phase action times (T_a, T_b, and T_c), as shown in Figure 7(b), where T_{low} is T_b. Similarly, the impossible voltage vectors [OON] and [OOO] should be changed to [PPO] and [PPP]. Finally, according to the principle that the switching states can only be changed once or unchanged, the redefined sequence and action time of voltage vectors should be rearranged, as shown in Figure 7(c).

The sequence and action time of voltage vectors in region III-2 in the normal state is shown in Figure 8(a). In order to replace the impossible P-type voltage vectors [OPO] with N-type voltage vectors [NON], T_{low} is added in three-phase action times (T_a, T_b, and T_c), where T_{low} is T_c. The redefined sequence and action time of voltage vectors can be obtained as given in Figure 8(b). Therefore, the redefined sequence and action time of voltage vectors in each region listed in Table 3 can be summed up.

$$
\begin{aligned}
M &= \frac{T1}{2}, \frac{T2}{2}, \frac{T3}{2}, \frac{T3}{2}, \frac{T2}{2}, \frac{T1}{2} \\
M1 &= \frac{T3}{2}, \frac{T1}{2}, \frac{T2}{2}, \frac{T2}{2}, \frac{T1}{2}, \frac{T3}{2} \\
M2 &= \frac{T2}{2}, \frac{T3}{2}, \frac{T1}{2}, \frac{T1}{2}, \frac{T3}{2}, \frac{T2}{2}.
\end{aligned}
\tag{1}
$$

M, $M1$, and $M2$ represent the action time of voltage vectors corresponding to the different switching sequence.

6. Experiment Verification

In order to validate the improved SVPWM strategy proposed previously, a laboratory prototype of the NPC three-level inverter with fault-tolerant capability is built based on the dSPACE DS1007 platform, as shown in Figure 9. The main experimental parameters are listed in Table 4. Figure 9 shows the overall structure of the experimental platform, including NPC inverter, three-phase load, DS1007, and PC. The main boards used in the experiment are DS5202 and ACMC (AC Motor Control). DS5202 provides 8 channels with maximum sampling frequency of 10 MHz, and EV1048 not only can be

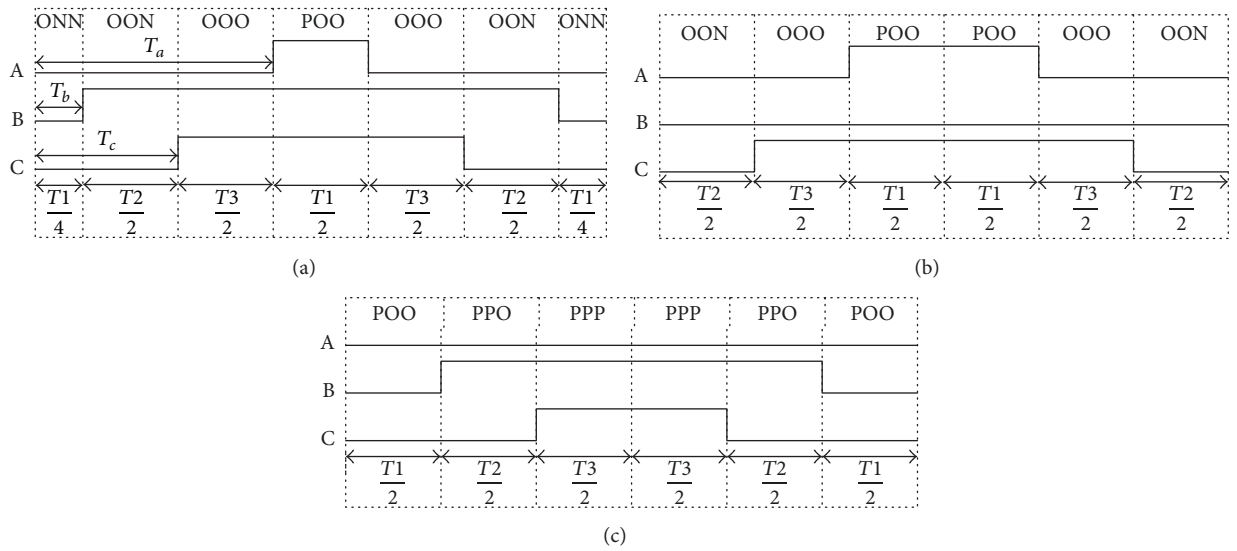

Figure 7: The sequence of voltage vectors and its action times in region I-1. (a) Conventional switching sequence. (b) After T_{low} is subtracted. (c) After the switching sequence is rearranged.

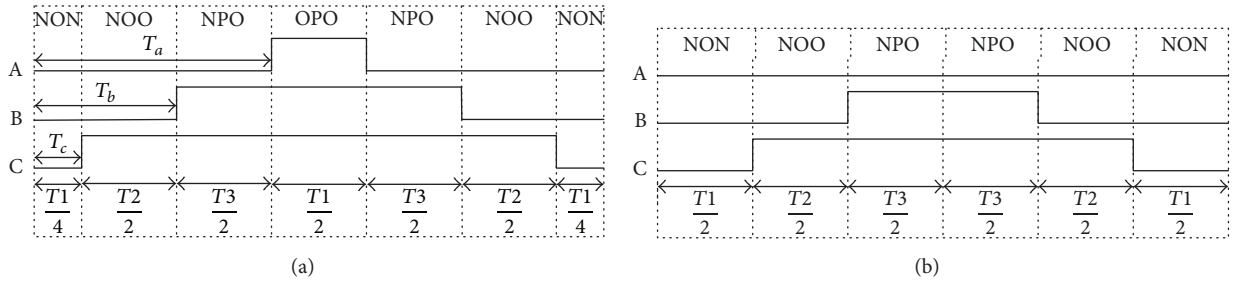

Figure 8: The sequence of voltage vectors and its action times in region III-2. (a) Conventional switching sequence. (b) After the switching sequence is rearranged.

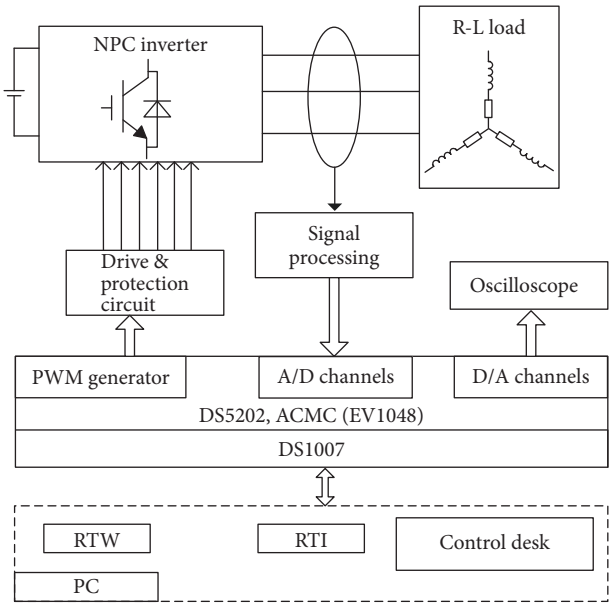

Figure 9: Experimental structure diagram.

used for AD sampling but also generate PWM signal to drive the inverter circuit. In the experiment, the QA1 open fault is set up and fault-tolerant control is carried out.

Figure 10 shows the different experimental waveforms of the output voltages, current, and capacitor neutral-point voltages without and with fault-tolerant control in sequence. The waveforms of phase-A bridge arm phase voltage U_{ao} and line-to-line voltage U_{ab} are given in Figure 10(a), respectively. It can be observed from Figure 10(a) that the phase voltage U_{ao} exhibits three levels and the line-to-line voltage U_{ab} shows five levels under the normal condition. When the fault occurs, the amplitude of the phase voltage U_{ao} in positive half period is decreased from $+1/2U_d$ to zero, and a zero level appeared for a long time. Similarly, the amplitude of line-to-line voltage U_{ab} in positive half period is lower than that of the normal condition. The voltage waveforms are the same as that under the normal condition when the proposed method is adopted for fault-tolerant control; namely, U_{ao} is three-level waveform with constant output amplitude and U_{ab} is five-level waveform with constant output amplitude.

Figure 10(b) shows the waveforms of current I_a in phase-A without and with fault-tolerant control, respectively. It can

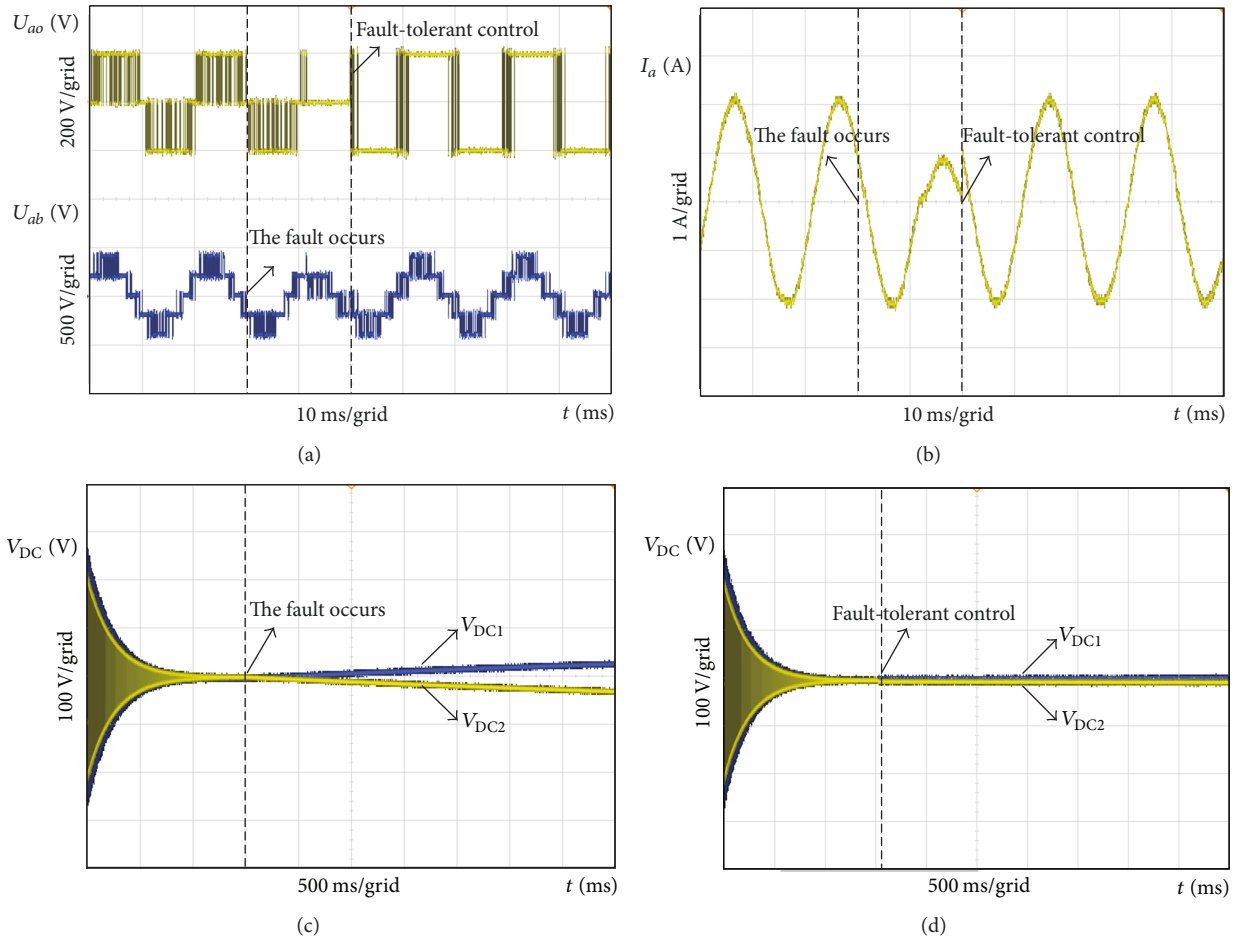

FIGURE 10: Experimental waveforms. (a) U_{ao} and U_{ab}. (b) I_a. (c) Capacitor neutral-point voltages before fault-tolerant control. (d) Capacitor neutral-point voltages after fault-tolerant control.

be seen from Figure 10(b) that the current I_a is sinusoidal before the fault occurs, but when the fault occurs, the amplitude of the load phase current I_a in positive half period is approximately reduced to half of the normal condition, and the waveform is obviously distorted. The load phase current I_a is still sinusoidal with constant amplitude after the proposed fault-tolerant method is applied, and the inverter can operate normally.

Figures 10(c) and 10(d) show the capacitor neutral-point voltages without and with fault-tolerant control, respectively. As shown in Figure 10(c), when the fault occurs, the neutral-point voltage of the capacitor fluctuates obviously, and $V_{DC1} > V_{DC2}$. The fluctuation of the neutral-point voltage of the capacitor is well suppressed by the fault-tolerant control, as shown in Figure 10(d). Obviously, the correctness of the fault-tolerant strategy is proved by experiments.

7. Conclusion

In order to enable the NPC inverter to operate at full output power under the device failures, a two-level leg is taken as the additional leg of the faulty phase in this paper, which is controlled with the two switching states P and N. In addition, an improved SVPWM strategy called "addition and subtraction substitution SVPWM" is proposed to readjust the sequence and action time of voltage vectors in SVPWM algorithm. The main advantages of the proposed fault-tolerant SVPWM strategy include the following:

(1) The proposed fault-tolerant topology has fewer switching devices and lower costs.

(2) The inverter is operated continuously without reduced output power by the proposed method. Therefore, the proposed fault-tolerant SVPWM strategy can be applied for all kinds of applications.

(3) The distortion of capacitor neutral-point voltages is eliminated well after the proposed fault-tolerant method is applied.

(4) The two switches Q1 and Q2 of this two-level leg should withstand the entire input DC voltage after fault-tolerant control. Therefore, the proposed method is more suitable for the NPC inverter with medium- or low-voltage power supply.

The effectiveness and fault-tolerant operation of the proposed SVPWM strategy are demonstrated by both simulation and experimental results under various types of faults.

Conflicts of Interest

The authors declare that they have no conflicts of interest regarding the publication of this paper.

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References

[1] T. Wang, H. Xu, J. Han, E. Elbouchikhi, and M. E. H. Benbouzid, "Cascaded H-bridge multilevel inverter system fault diagnosis using a PCA and multiclass relevance vector machine approach," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7006–7018, 2015.

[2] J. He, N. A. O. Demerdash, N. Weise, and R. Katebi, "A fast on-line diagnostic method for open-circuit switch faults in SiC-MOSFET-based T-type multilevel inverters," *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2948–2958, 2017.

[3] U.-M. Choi, H.-G. Jeong, K.-B. Lee, and F. Blaabjerg, "Method for detecting an open-switch fault in a grid-connected NPC inverter system," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2726–2739, 2012.

[4] K. Ma and F. Blaabjerg, "Modulation methods for neutral-point-clamped wind power converter achieving loss and thermal redistribution under low-voltage ride-through," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 835–845, 2014.

[5] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, 2013.

[6] O. S. Senturk, S. Munk-Nielsen, R. Teodorescu, L. Helle, and P. Rodriguez, "Power density investigations for the large wind turbines' grid-side press-pack IGBT 3L-NPC-VSCs," in *Proceedings of the 4th Annual IEEE Energy Conversion Congress and Exposition (ECCE '12)*, pp. 731–738, IEEE, Raleigh, NC, USA, September 2012.

[7] J.-S. Lee and K.-B. Lee, "An open-switch fault detection method and tolerance controls based on SVM in a grid-connected t-type rectifier with unity power factor," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 7092–7104, 2014.

[8] D. J. Chen, Y. Z. Ye, and R. Hua, "Fault diagnosis of three level inverter in bullet train based on waveform real-time analysis," *Transactions of China Electrotechnical Society*, vol. 29, no. 6, pp. 106–113, 2014.

[9] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734–2752, 2010.

[10] L. L. Jiang, W. Z. Ma, and L. H. Li, "Fault tolerant control strategy for modular multilevel converters," *Power System source*, vol. 38, no. 9, pp. 2497–2503, 2014.

[11] J. Amini and M. Moallem, "A fault-diagnosis and fault-tolerant control scheme for flying capacitor multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1818–1826, 2017.

[12] S. Ceballos, J. Pou, J. Zaragoza, E. Robles, J. L. Villate, and J. L. Martín, "Fault-tolerant neutral-point-clamped converter solutions based on including a fourth resonant leg," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2293–2303, 2011.

[13] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 519–533, 2012.

[14] Z. Wang, B. Zhang, Y. Wang, Y. Zhang, and M. Cheng, "Analysis and control of active neutral-point-clamping three-level inverters under fault tolerant operation modes," in *Proceedings of the 18th International Conference on Electrical Machines and Systems (ICEMS '15)*, pp. 2140–2146, Pattaya, Thailand, October 2015.

[15] A. I. L. de Lacerda and E. R. C. da Silva, "Fault tolerant Active Neutral Point Clamped inverter: short-circuit and open-circuit failures," in *Proceedings of the 24th IEEE International Symposium on Industrial Electronics (ISIE '15)*, pp. 1068–1073, Rio de Janeiro, Brazil, June 2015.

[16] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2660–2673, 2015.

[17] U.-M. Choi, K.-B. Lee, and F. Blaabjerg, "Diagnosis and tolerant strategy of an open-switch fault for t-type three-level inverter systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 495–508, 2014.

[18] S. Xu, J. Zhang, and J. Hang, "Investigation of a fault-tolerant three-level T-type inverter system," in *Proceedings of the 7th Annual IEEE Energy Conversion Congress and Exposition (ECCE '15)*, pp. 1632–1638, Montreal, Canada, September 2015.

[19] Y. C. Liu, X. L. Ge, and X. Y. Feng, "Research on the comparison of SVPWM algorithm for two level and three level NPC inverter single bridge fault reconfiguration topology," *Proceedings of the CSEE*, vol. 36, no. 3, pp. 775–783, 2016.

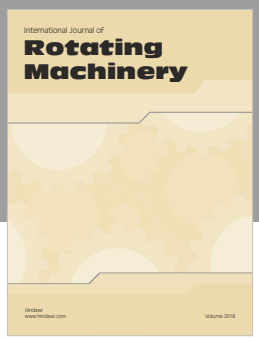
[20] D. J. Chen, Y. Z. Ye, and R. Hua, "Research on Fault Tolerant Topology and control of NPC three level inverter," *Control Engineering of China*, vol. 21, no. 2, pp. 258–267, 2014.

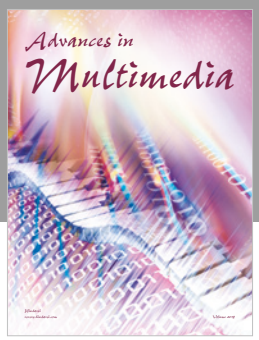
[21] D. B. Matos, J. O. Estima, and A. J. M. Cardoso, "Performance of a synchronous reluctance motor drive with a fault-tolerant three-level neutral point clamped inverter," in *Proceedings of the 22nd International Conference on Electrical Machines (ICEM '16)*, pp. 1152–1159, Lausanne, Switzerland, September 2016.

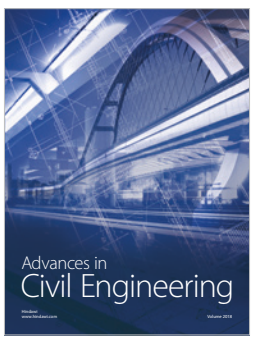
[22] J.-S. Lee, K.-B. Lee, and F. Blaabjerg, "Open-switch fault detection method of a back-to-back converter using NPC topology for wind turbine systems," *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 325–335, 2015.

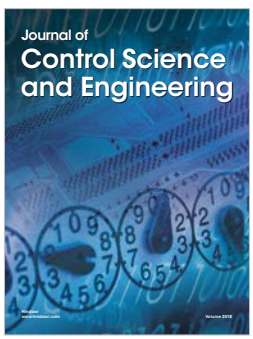
[23] Z. Wang, Y. Z. Wang, J. Chen, and M. Cheng, "Fault-Tolerant Control of NPC three-level inverters-fed double-stator-winding PMSM drives based on vector space decomposition," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8446–8458, 2017.

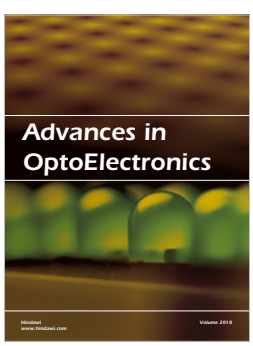
[24] U.-M. Choi and K. B. Lee, "Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems," *IET Power Electronics*, vol. 6, no. 7, pp. 1390–1398, 2013.

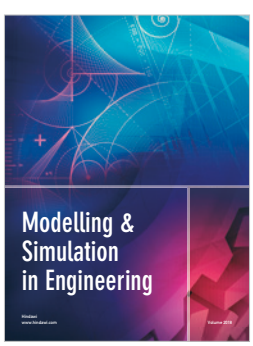


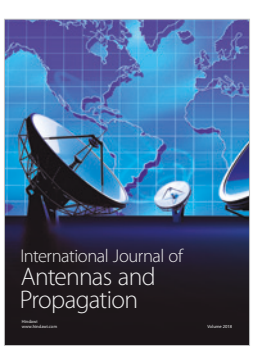


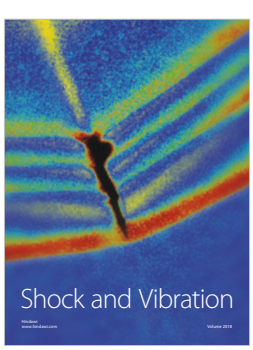


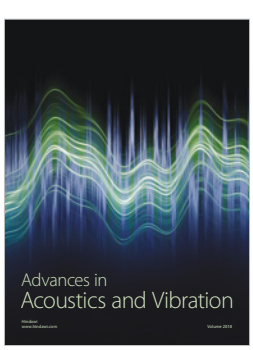












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