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Research Article

Research on Dual-Carrier Pulse-Train-Controlled Buck Converter

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In order to solve the low-frequency oscillation of pulse-train- (PT-) controlled switching converter operating in a continuous conduction mode (CCM), a dual-carrier pulse-train (DCPT) control technique is proposed in this paper. With the CCM buck converter as an example, the operational principle, pulse control law, and output voltage ripple of the DCPT-controlled converter are studied. The experimental results are provided to verify the theoretical analysis and simulation results. Compared with the PT-controlled converter, the DCPT-controlled CCM buck converter enjoys much better operating characteristics and smaller output voltage ripple.

1. Introduction

With the development of electronic technology, the steady-state performance and transient response of power supplies are very important in many electronic devices. However, for pulse-width modulation (PWM) switching DC-DC converters, with the disadvantages of slow transient response and complicated compensational network, it is hard to meet the requirements of modern electronic equipments [1–4].

In order to get a great transient response, a pulse-train (PT) control technique for DC-DC converter was proposed [5]. When the PT-controlled switching converter operates in discontinuous conduction mode (DCM), the output voltage will increase during each high-energy pulse P_H and decrease during each low-energy pulse P_L, which improves the transient characteristic of the converter. Qin and Xu [6] proposed a multiple pulse-train (MPT) control technique by setting several duty cycle pulses to get better output characteristics. Qin and Xu [7] introduced a current-referenced pulse-train (CRPT) control technique to enlarge the load range and improve the voltage accuracy of the converter. Considering the spectrum of the switching converter, the bi-frequency pulse-train (BFPT) control technique was proposed [8]. However, all the control techniques mentioned above were used in DCM converters, which limited the applications.

Wang et al. [9] applied the PT control technique to a buck converter operating in the continuous conduction mode (CCM) and indicated that the low-frequency oscillation existed at this time, which confused the pulse control law and enlarged the output voltage ripple. In order to solve this problem, several control techniques have been proposed. By limiting the valley value of the inductor current, the valley current mode PT (VCM-PT) controlled buck converter eliminated the low-frequency oscillation, but it limited the output power range at the same time [10]. By detecting the load current, the sliding current valley PT (SCV-PT) controlled buck converter changed the valley value of the inductor current adaptively and improved the output power range of the converter [11]. However, load current, inductor current, and output voltage were detected at the same time for SCV-PT control, which is quite complicated. Sha et al. [12] indicated that by limiting the peak value of the capacitor current within one switching cycle, the low-frequency oscillation could be eliminated, although the control parameters were complicated to design. By controlling the leading edge of the pulse, the pulse phase shift-based PT (PPS-PT) control was proposed [13]. Although the

PPS-PT-controlled buck converter could eliminate the low-frequency oscillation, it weakened the transient characteristic. In [14], the PT control technique was applied to boost converter operated in the pseudo continuous conduction mode (PCCM). This converter enjoyed wide power range without low-frequency oscillation, but the efficiency of the converter was poor due to the freewheeling phase. In addition, by improving the topology of the converter, the low-frequency oscillation could be suppressed, but it was complicated to the integration of the switching converter [15–20].

In this paper, a dual-carrier pulse-train (DCPT) control technique is proposed and studied in detail. In the DCPT-controlled CCM buck converter, the capacitor current is limited to the preset valley current by a carrier signal at the beginning of each switching cycle. The output voltage will increase during one P_H switching cycle and decrease during each P_L switching cycle, which indicates that the low-frequency oscillation did not exist in the DCPT-controlled converter. The theoretical analysis, simulation, and experimental results verify that the DCPT-controlled CCM buck converter enjoys small output ripple and fast transient response.

2. Operational Principle

For a buck converter, when the switch S is on, the inductor current will increase with a slope of $(V_{in} - V_o)/L$; when S is off, the inductor current will decrease with a slope of V_o/L. Since the capacitor current reflects the ripple of the inductor current completely, the slope of the capacitor current is also $(V_{in} - V_o)/L$ or V_o/L when the switch is on or off, respectively. If a control signal v_{saw} with a slope of V_o/L is applied to the capacitor current, the capacitor current will move along with the trajectory of v_{saw} after the switch turns off.

Figure 1(a) shows the schematic diagram of the DCPT-controlled buck converter. In the controller, a comparator is used to compare the output voltage of the switching converter with a reference value, a sense resistor connected to the output capacitor and its auxiliary circuit are employed to obtain the capacitor current, and two D/A converters are acquired to generate the carrier signals. Besides that, there is no extra compensational network in the controller, which indicates the DCPT-controlled converter enjoys convenient design process and fast response. The main working waveforms including capacitor current i_c, control pulse control signal v_p, and output voltage v_o are shown in Figure 1(b). The carrier signals $v_{saw,H}$ and $v_{saw,L}$ generated by the controller have the same valley current I_v and slope V_{ref}/L. However, the frequency of $v_{saw,H}$ or $v_{saw,L}$ is different, which is f_H or f_L, respectively. Because the control pulse is generated by comparing the capacitor current with the carrier signal in the DCPT controller, the switching frequency of the converter is also f_H or f_L correspondingly.

The working principle of the DCPT-controlled buck converter is as follows. The carrier signal v_{saw} is chosen between $v_{saw,H}$ and $v_{saw,L}$. When v_{saw} decreases to the valley current I_v, the switch S turns on immediately, and the output voltage is compared with the reference voltage V_{ref}. If $v_o < V_{ref}$, the carrier signal $v_{saw,H}$ is selected as v_{saw}. When the capacitor current $i_c > v_{saw,H}$, the switch S turns off, which is recorded as a high-energy pulse P_H. Similarly, if $v_o \geq V_{ref}$ at the time when v_{saw} decreases to I_v, the carrier signal $v_{saw,L}$ will be selected. When $i_c > v_{saw,L}$, S turns off, which is recorded as the low-energy pulse P_L. When the converter operates in a steady state, the DCPT controller will generate a pulse train, which consists of P_H and P_L to stabilize the output voltage.

3. Steady-State Analysis

3.1. Design of Control Parameters. In order to avoid low-frequency oscillation, the output voltage should be increased during P_H and decreased during P_L. Based on this principle, the control parameters, the frequencies of the carrier signals, and the valley current can be designed properly.

Figure 2 shows the capacitor current waveform of the DCPT-controlled buck converter within one switching cycle. For the switching converter with a low output voltage, the on-state voltage of the diode has a significant influence on the process of control law analysis. When the on-state voltage V_D of the diode is considered, the rising or falling slope of the capacitor current is $(V_{in} - V_o)/L$ or $(V_o + V_D)/L$, respectively.

During t_1 or t_2, the peak value of the capacitor current I_p can be expressed as

$$I_p = \frac{V_{in} - V_o}{L} t_1, \tag{1}$$

$$I_p = \frac{V_o + V_D}{L} t_2. \tag{2}$$

By combining equations (1) and (2), we have

$$t_1 + t_2 = \frac{LI_p (V_{in} + V_D)}{(V_{in} - V_o)(V_o + V_D)}. \tag{3}$$

Based on Figure 2 and equation (3), the area of the triangle ABC can be written as

$$S_{\Delta ABC} = \frac{1}{2}(t_1 + t_2) I_p = \frac{(V_{in} + V_D) L I_p^2}{2(V_{in} - V_o)(V_o + V_D)}. \tag{4}$$

The area of the quadrangle $BCED$ within one switching period T is

$$S_{BCED} = -\frac{1}{2}(t_1 + t_2 + T) I_v = -\frac{(V_{in} + V_D) L I_v I_p}{2(V_{in} - V_o)(V_o + V_D)} - \frac{1}{2} I_v T. \tag{5}$$

Similarly, the areas of the triangle BOD and the triangle CFE can be expressed as

$$S_{\Delta BOD} + S_{\Delta CFE} = S_{OFED} - S_{BCED} = -\frac{1}{2} I_v T + \frac{(V_{in} + V_D) L I_v I_p}{2(V_{in} - V_o)(V_o + V_D)}. \tag{6}$$

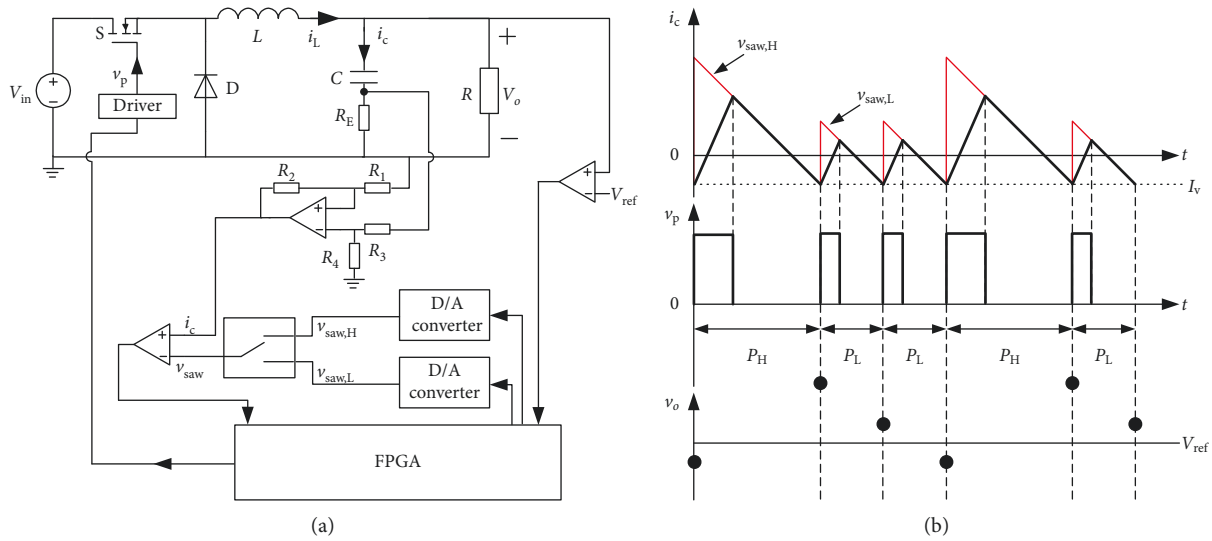


Figure 1: Working principle diagram of the DCPT-controlled buck converter. (a) Schematic diagram. (b) Working waveforms.

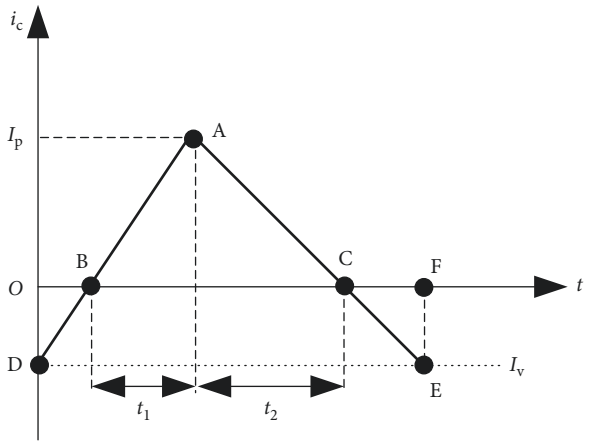


Figure 2: Capacitor current of the DCPT-controlled buck converter.

According to equation (6), the charge variation of the output capacitor during one switching cycle T can be calculated as

$$\Delta q = S_{\Delta ABC} - (S_{\Delta BOD} + S_{\Delta CFE}) = \frac{(V_{in} + V_D)LI_p^2}{2(V_{in} - V_o)(V_o + V_D)} + \frac{1}{2}I_v T - \frac{(V_{in} + V_D)LI_v I_p}{2(V_{in} - V_o)(V_o + V_D)}. \quad (7)$$

During the conduction time of the switch, I_p can be written as

$$I_p = I_v + \frac{V_{in} - V_o}{L}DT = I_v + \frac{(V_{in} - V_o)(V_o + V_D)}{L(V_{in} + V_D)}T. \quad (8)$$

By combining equations (7) and (8), it is available that

$$\Delta q = I_v T + \frac{(V_{in} - V_o)(V_o + V_D)}{2L(V_{in} + V_D)}T^2. \quad (9)$$

Therefore, the variation of the output voltage within one switching cycle can be calculated as

$$\Delta v_o = \frac{\Delta q}{C} = \frac{I_v}{C}T + \frac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T^2. \quad (10)$$

By choosing different T_H or T_L, the variation of the output voltage within P_H or P_L can be obtained as

$$\begin{cases} \Delta v_o^H = \dfrac{I_v}{C}T_H + \dfrac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T_H^2, \\ \Delta v_o^L = \dfrac{I_v}{C}T_L + \dfrac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T_L^2. \end{cases} \quad (11)$$

Based on equation (11), the output voltage iterative equation of the DCPT-controlled buck converter can be expressed as

$$v_{o,n+1} = \begin{cases} v_{o,n} + \dfrac{I_v}{C}T_H + \dfrac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T_H^2, & v_{o,n} < V_{ref}, \\ v_{o,n} + \dfrac{I_v}{C}T_L + \dfrac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T_L^2, & v_{o,n} \geq V_{ref}. \end{cases} \quad (12)$$

According to the principle of the DCPT control technique, $\Delta v_o^H > 0$ and $\Delta v_o^L < 0$ should be guaranteed. Therefore, it is available that

$$-\frac{(V_{in} - V_o)(V_o + V_D)}{2LC(V_{in} + V_D)}T_H < I_v < -\frac{(V_{in} - V_o)(V_o + V_D)}{2L(V_{in} + V_D)}T_L. \quad (13)$$

The control parameter I_v can be determined by the preset input voltage range of the converter. Since the falling slope of the carrier signals $v_{saw,H}$ and $v_{saw,L}$ is V_{ref}/L, the peak value of the carrier signals can be calculated when the frequencies of the carrier signals f_H and f_L and the valley current I_v are

determined. Based on the analysis above, the parameters of the researched the DCPT-controlled buck converter are listed in Table 1.

From equation (12), it can be known that the output voltage variations Δv_o^H and Δv_o^L vary with the input voltage V_{in}. In order to achieve $\Delta v_o^H > 0$ and $\Delta v_o^L < 0$, V_{in} would be limited within a valid range.

Assuming the output voltage variation is zero in one P_H switching cycle ($\Delta v_o^H = 0$), the lower boundary of the input voltage for the DCPT-controlled buck converter will be calculated as

$$V_{in,min} = \frac{(V_o + V_D)^2 T_H}{(V_o + V_D)T - 2LI_v} - V_D. \quad (14)$$

Similarly, assuming the output voltage variation is zero in one P_L switching cycle ($\Delta v_o^L = 0$), the upper boundary of the input voltage will be

$$V_{in,max} = \frac{(V_o + V_D)^2 T_L}{(V_o + V_D)T - 2LI_v} - V_D. \quad (15)$$

Substituting the parameters of Table 1 into equation (14), the operating range of the input voltage can be calculated, which is [8.11 V, 19 V]. When the input voltage varies in this range, the output voltage will increase during each P_H and decrease during each P_L; thus, the low-frequency oscillation can be avoided.

By using equation (12), the relationship between the output voltage variation $\Delta v_o^H > 0$ and $-\Delta v_o^L < 0$ and the input voltage V_{in} can be obtained, as shown in Figure 3. It can be seen that, with the increasing input voltage, the variation of the output voltage $\Delta v_o^H > 0$ increases and $-\Delta v_o^L < 0$ decreases.

3.2. Analysis of Pulse Control Law. According to the principle of charge balance, the variation of the output voltage is zero in a whole pulse train, that is,

$$\mu_H \Delta v_o^H + \mu_L \Delta v_o^L = 0. \quad (16)$$

By combining equations (12) and (16), it can be obtained that

$$\frac{\mu_H}{\mu_L} = -\frac{(V_{in} - V_o)(V_o + V_D)T_L^2 - 2LI_v T_L (V_{in} + V_D)}{(V_{in} - V_o)(V_o + V_D)T_H^2 - 2LI_v T_H (V_{in} + V_D)}. \quad (17)$$

Substituting the parameters shown in Table 1 into equation (17), the relationship between the pulse ratio μ_H/μ_L and the input voltage V_{in} can be obtained, as shown in Figure 4. It can be known that, the pulse ratio μ_H/μ_L decreases gradually with the increase of V_{in}, which is caused by the increase of $\Delta v_o^H > 0$ and the decrease of $-\Delta v_o^L < 0$. Therefore, the proportion of the high-energy pulse P_H in the pulse train gradually decreases with the increase in the input voltage.

According to equation (17), the typical pulse train of the DCPT-controlled buck converter in the condition of different input voltages can be obtained, as listed in Table 2.

Table 1: Parameters of the DCPT-controlled buck converter.

Parameters	Value
Rated input voltage, V_{in}	12 V
Reference voltage, V_{ref}	5 V
Inductor, L	100 μH
Capacitor, C	560 μF
Equivalent series resistance, R_E	30 mΩ
Frequency f_L of carrier, $v_{saw,L}$	40 kHz
Frequency f_H of carrier, $v_{saw,H}$	20 kHz
Valley current, I_v	−0.5 A

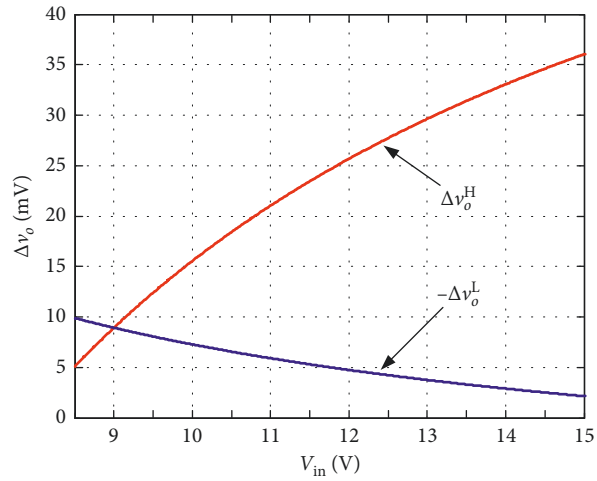


Figure 3: Output voltage variation versus input voltage of the DCPT-controlled buck converter.

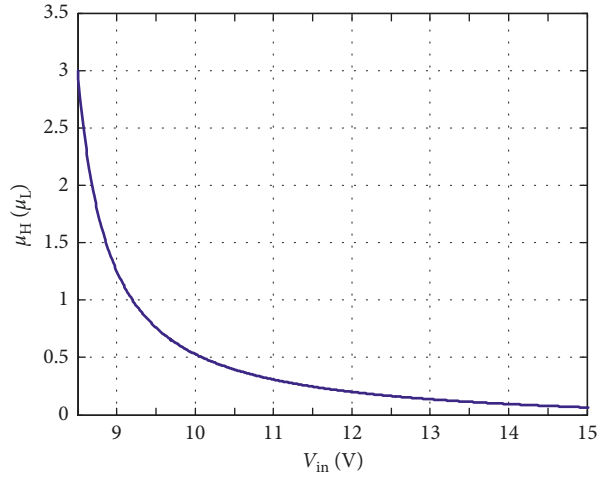


Figure 4: Pulse ratio versus input voltage of the DCPT-controlled buck converter.

3.3. Analysis of the Output Voltage Ripple. To analyse the output voltage variation, the capacitor current i_c and output voltage v_o of the DCPT-controlled buck converter within one switching cycle are shown in Figure 5.

During $[0, t_{on}]$, the capacitor current $i_c(t)$ and the output voltage of the converter can be written as

Table 2: Pulse train of the DCPT-controlled buck converter at different voltages.

V_{in} (V)	μ_H/μ_L	Pulse train
8.49	3	$3P_H$-$1P_L$
8.68	2	$2P_H$-$1P_L$
9.2	1	$1P_H$-$1P_L$
10.83	1/3	$1P_H$-$3P_L$
12	1/5	$1P_H$-$5P_L$

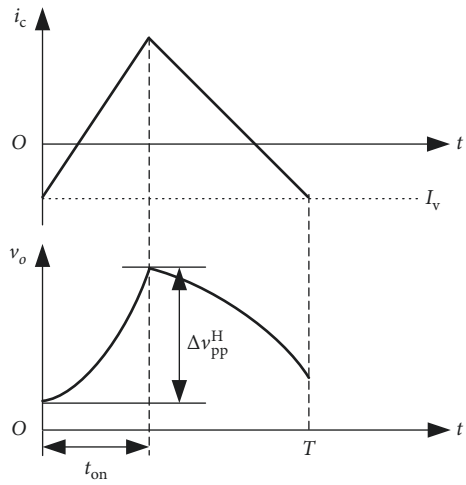


Figure 5: Capacitor current and output voltage of the DCPT-controlled buck converter.

$$i_c(t) = I_v + \frac{V_{in} - V_o}{L}t, \tag{18}$$

$$v_o(t) = \frac{1}{C}\int_0^t i_c(t)dt + i_c(t)R_E\frac{I_v}{C}t + \frac{V_{in} - V_o}{2LC}t^2 + \frac{V_{in} - V_o}{L}R_E t. \tag{19}$$

By taking the derivation of equation (19), one obtains

$$\frac{dv_o(t)}{dt} = \frac{I_v}{C} + \frac{V_{in} - V_o}{2LC}t + \frac{V_{in} - V_o}{LC}R_E. \tag{20}$$

Substituting the parameters listed in Table 1 into equation (20), it can be known that the output voltage rises to the maximum at the time t_{on}. Therefore, it is available that

$$\Delta v_{pp}^H = \frac{I_v}{C}t_{on} + \frac{V_{in} - V_o}{2LC}t_{on}^2 + \frac{V_{in} - V_o}{L}R_E t_{on}. \tag{21}$$

For the DCPT-controlled buck converter, the output voltage ripple is closely related to the pulse train. Taking the pulse train $2P_H$-$1P_L$ as an example, the capacitor current i_c and the output voltage v_o are shown in Figure 6(a). Obviously, the output voltage ripple of the converter is $\Delta v_o = \Delta v_{pp}^H + \Delta v_o^H$ at this time.

In general, when the pulse train is nP_H-$1P_L$, the output voltage ripple of the converter is

$$\Delta v_o = (n-1)\Delta v_{pp}^H + \Delta v_o^H. \tag{22}$$

When the pulse train is $1P_H$-nP_L, the capacitor current i_c and the output voltage v_o are shown in Figure 6(b). Apparently, the output voltage ripple on this condition is

$$\Delta v_o = \Delta v_{pp}^H. \tag{23}$$

By using equations (21)–(23), the output voltage ripple Δv_o of the DCPT-controlled buck converter can be calculated, as listed in Table 3. For the DCPT-controlled buck converter, the output voltage ripple increases gradually with the increase of the input voltage.

4. Simulation and Experimental Results

4.1. Simulation Results. To verify the theoretical analysis, the simulation results are provided in Figure 7, which include carrier signal v_{saw}, control pulse v_p, capacitor current i_c, and output voltage v_o.

As shown in Figure 7(a), when the input voltage equals to 8.68 V, the pulse train is $2P_H$-$1P_L$, the pulse ratio is $\mu_H/\mu_L = 2$, and the output voltage ripple is 40 mV, which are consistent with the theoretical analysis. Similarly, as shown in Figures 7(b)–7(d), when the input voltage equals to 9.2 V, 10.83 V, or 12 V, the pulse train is $1P_H$-$1P_L$, $1P_H$-$3P_L$, or $1P_H$-$5P_L$, the pulse ratio is 1, 1/3, or 1/5, and the output voltage ripple is 40 mV, 55 mV, or 60 mV, respectively.

According to Figure 7, the following conclusion of the DCPT-controlled buck converter can be obtained: as the input voltage V_{in} increases, μ_H/μ_L decreases gradually, i.e., the proportion of P_H in the pulse train decreases, which is consistent with the theoretical analysis in Section 3.2.

In addition, the value of the capacitor current at the beginning of each switching cycle is equal to the preset valley current I_v due to the traction of the carrier signals. Since the capacitor current reflects the ripple of the inductor current, the value of the inductor current is constant at the beginning of each switching cycle. Therefore, the variation of the output voltage is only influenced by the control pulse P_H or P_L, which indicates that the low-frequency oscillation does not exist in the DCPT-controlled buck converter.

4.2. Experimental Results. In order to verify and test the proposed technique, a prototype of the DCPT-controlled buck converter is designed with the parameters in Table 1. In the prototype, the control scheme is achieved by an FPGA device, with a type of EP4CE15F17C8. An operational amplifier OPA228 and a 10 mΩ sense resistor connected with the output capacitor are employed to obtain the capacitor current. Two D/A DAC0808 converters are applied to generate the carrier signals, and an analogue multiplexer CD4051 is used to select the carrier signal between $v_{saw,H}$ and $v_{saw,L}$. Besides, the type of the comparators in this prototype is LM393.

When the input voltage equals to 8.68 V, the experimental waveforms are shown in Figure 8(a). The pulse train is $2P_H$-$1P_L$, and the output voltage ripple is 40 mV approximately. Similarly, when the input voltage equals to 9.2 V, 10.83 V, or 12 V, the pulse train is $1P_H$-$1P_L$, $1P_H$-$3P_L$,

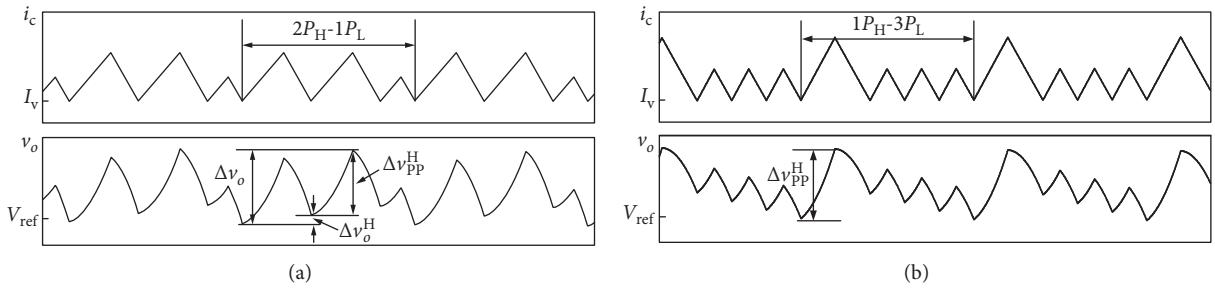


Figure 6: Output voltage ripple of the DCPT-controlled buck converter. (a) The case of $2P_H$-$1P_L$. (b) The case of $1P_H$-$3P_L$.

Table 3: The output voltage ripple of the DCPT-controlled buck converter.

V_{in} (V)	Δv_o^H (mV)	Δv_{pp}^H (mV)	Δv_o (mV)
8.49	3.3	34.3	40.9
8.68	4.9	36.3	41.2
9.2	8.9	41.5	41.5
10.83	19.1	52.2	52.2
12	24.8	57.7	57.7

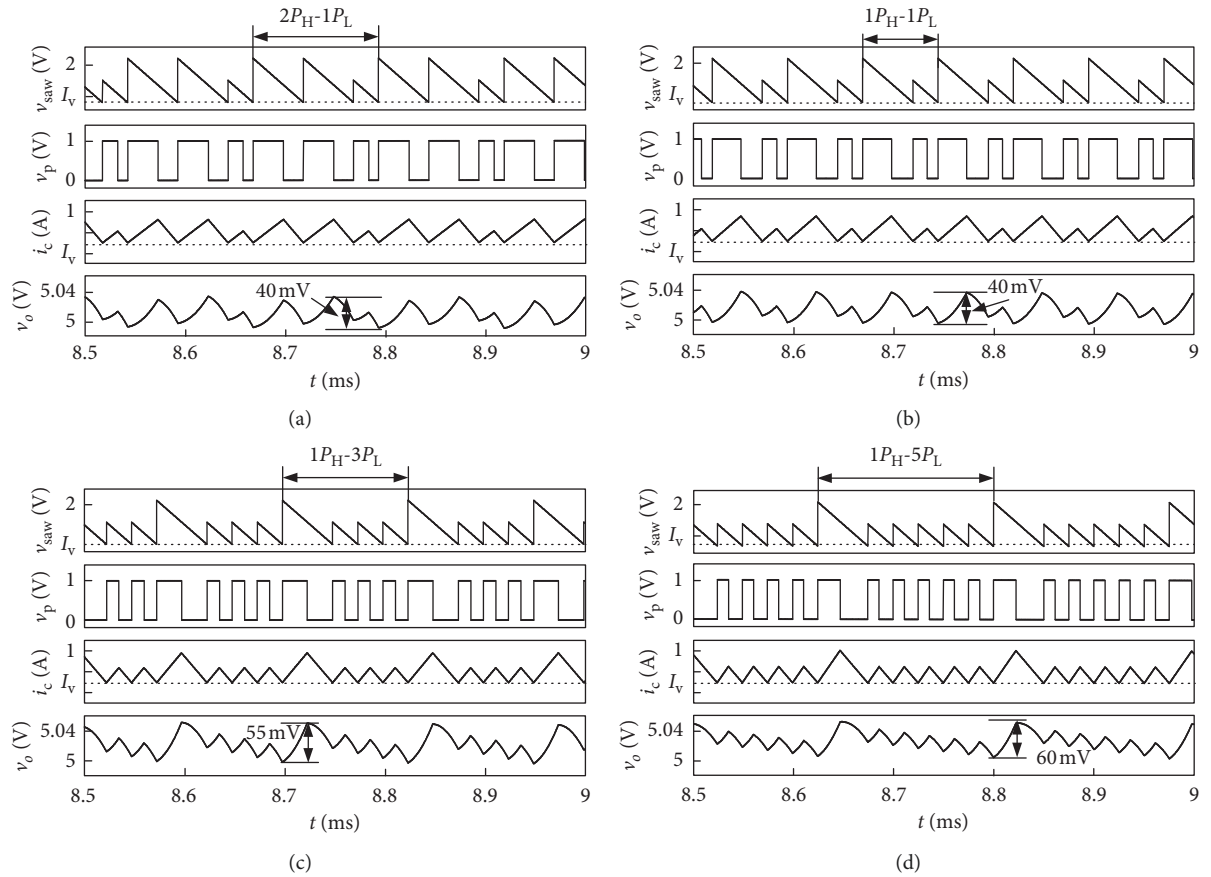


Figure 7: Simulation waveforms of the DCPT-controlled buck converter. (a) $V_{in} = 8.68$ V. (b) $V_{in} = 9.2$ V. (c) $V_{in} = 10.83$ V. (d) $V_{in} = 12$ V.

or $1P_H$-$5P_L$ and the output voltage ripple is 40 mV, 50 mV, or 60 mV, respectively.

According to the principle of DCPT control, the control pulse is generated by comparing the capacitor current with the carrier signals. It can be seen from Figure 8 that the combination of the carrier signals changes with the variation of the input voltage, which causes the variation of the pulse train. Based on the experimental results, it can be known that the DCPT-controlled buck converter can operate in a steady state by adjusting the pulse train when the input voltage changes.

In order to study the transient response of the DCPT control method, the experimental transient waveforms are

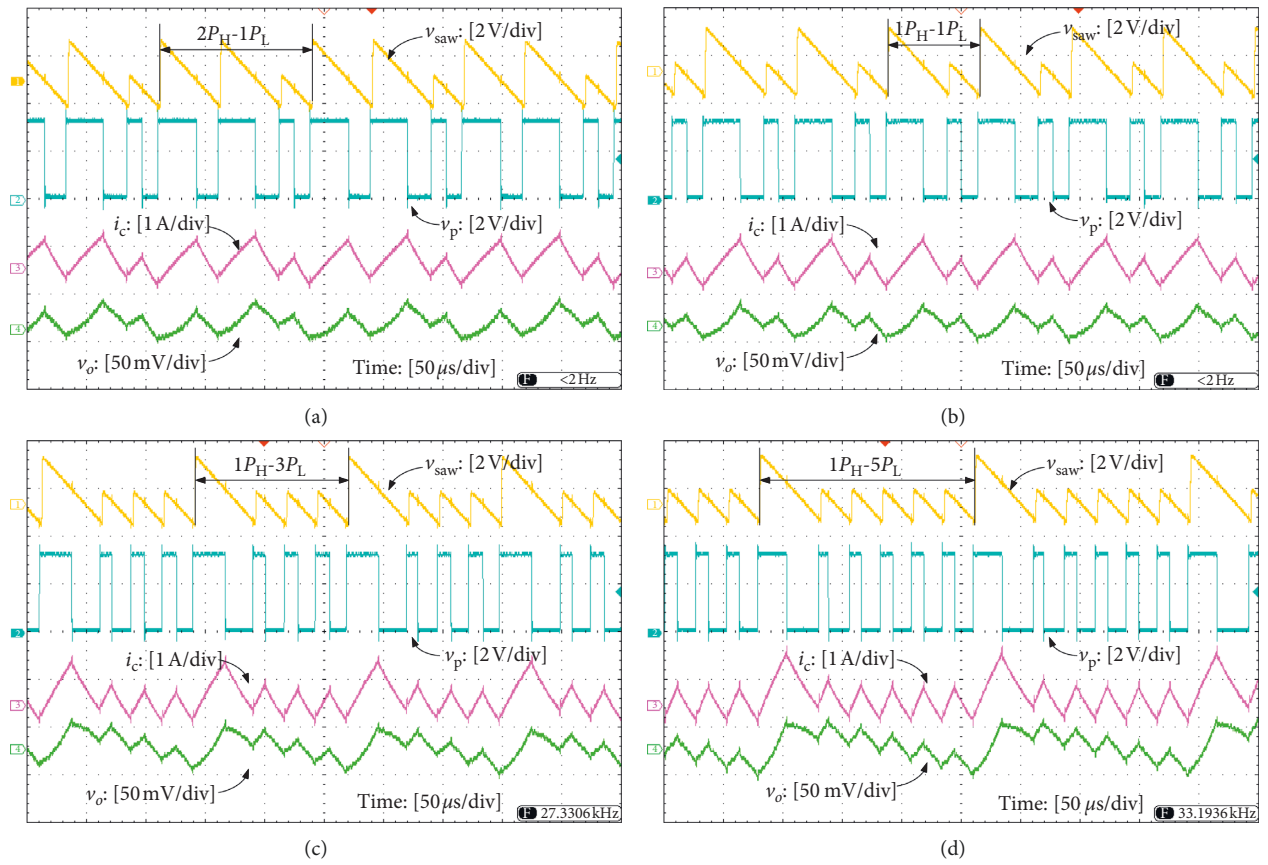


Figure 8: Experimental waveforms of the DCPT-controlled buck converter. (a) $V_{in} = 8.68$ V. (b) $V_{in} = 9.2$ V. (c) $V_{in} = 10.83$ V. (d) $V_{in} = 12$ V.

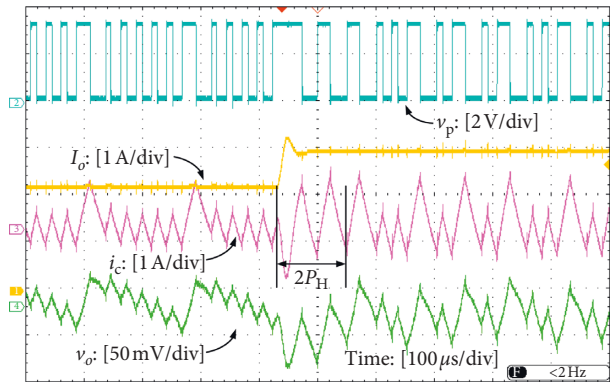
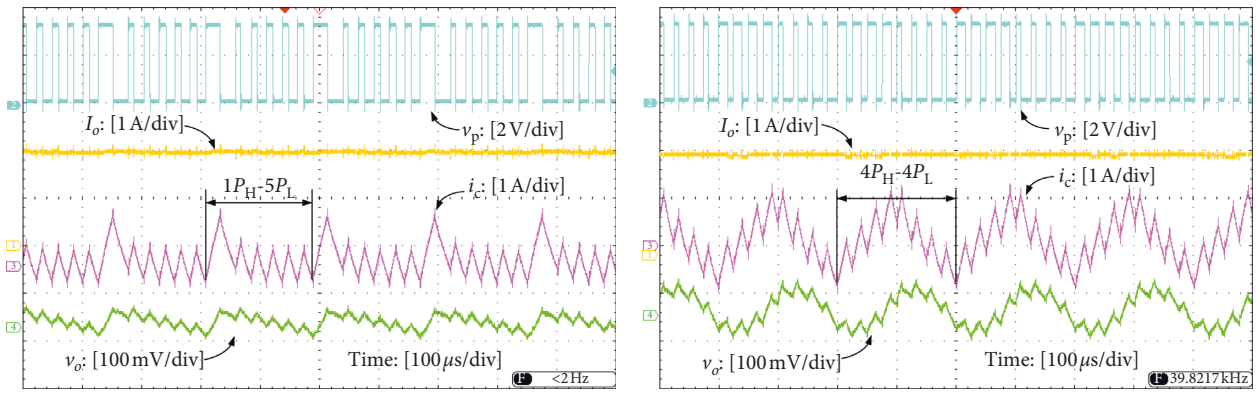


Figure 9: Experimental transient waveforms of the DCPT-controlled buck converter while load changes.

provided in Figure 9. When the load current increases from 2A to 3A, two high-energy pulses are generated successively by the controller to stabilize the output voltage, and this converter enjoys excellent transient response. Considering the parasitic parameters such as the on-state resistor of the MOSFET, when the load current increases, the input voltage of the inductor will decrease slightly, which causes the proportion of P_H in the pulse train to increase.

In order to verify the suppression effect on the low-frequency oscillation, the comparative experimental results are provided in Figure 10. The control parameters of traditional PT-controlled buck converter are as follows: $D_H = 0.6$, $D_L = 0.3$, and $T = 25\,\mu$s.

As shown in Figure 10(a), the pulse train is $1P_H$-$5P_L$ for the DCPT-controlled CCM converter and the output voltage ripple is 60 mV. In contrast, the pulse train of the PT-controlled buck converter is $4P_H$-$4P_L$, and the output voltage ripple is 120 mV, as shown in Figure 10(b). This phenomenon of successive several high-energy pulses followed by successive several low-energy pulses indicates that the low-frequency oscillation exists in the PT-controlled CCM converter. The low-frequency oscillation has not occurred in



(a) (b)

Figure 10: Experimental waveforms.(a) DCPT-controlled buck converter. (b) PT-controlled buck converter.

the DCPT-controlled CCM buck converter. The proposed DCPT control technique enjoys much better output characteristics compared with the traditional PT control technique.

5. Conclusions

In this paper, a dual-carrier pulse-train control technique is proposed. With the CCM buck converter as an example, the operational principle is analysed in detail. Based on the output voltage variation of the DCPT-controlled buck converter within one switching cycle, the pulse control law and the output voltage ripple are analysed. The simulation and experimental results verify the theoretical analysis and indicate that there is no low-frequency oscillation in the DCPT-controlled CCM buck converter. Compared with the traditional PT control technique, the DCPT-controlled buck converter enjoys better control characteristics and much smaller output voltage ripple.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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