

## Retraction

# **Retracted: High-Performance Control Simulation of PFC Converter for Electric Vehicle Charger**

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This article has been retracted by Hindawi, as publisher, following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of systematic manipulation of the publication and peer-review process. We cannot, therefore, vouch for the reliability or integrity of this article.

Please note that this notice is intended solely to alert readers that the peer-review process of this article has been compromised.

Wiley and Hindawi regret that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

## References

 B. Zhu, S. Sun, and Y. Jia, "High-Performance Control Simulation of PFC Converter for Electric Vehicle Charger," *Journal* of Control Science and Engineering, vol. 2023, Article ID 4069603, 7 pages, 2023.



## Research Article

# **High-Performance Control Simulation of PFC Converter for Electric Vehicle Charger**

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In order to solve the problems of low power factor and large harmonic pollution of some electrical equipment connected to the power grid, such as electric vehicle charger system, the author proposes a high-performance control simulation study of a PFC converter for electric vehicle charger. Using the staggered parallel boost power factor correction circuit topology of electric vehicle chargers as the front stage, its high power factor and low harmonic current characteristics can reduce the pollution to the power grid, and the detailed design process and loss analysis of the circuit are given. Through the digital control method and hardware optimization design, the loss is reduced, and the conversion efficiency of the power factor correction converter in the full power range is high, which meets the efficiency requirements of the platinum version and achieves the goal of energy saving and environmental protection. The test results show that the actual efficiency of the experimental prototype is 97.43%, 97.55%, and 97.36%, which are far higher than the efficiency requirements of the platinum version. *Conclusion*. The high-performance control of the PFC converter of the electric vehicle charger has certain guiding significance for the application in the electric vehicle.

## 1. Introduction

At present, under the development trend of the increasing number of new energy-electric vehicle users, the impact of the charger connected to the power grid cannot be ignored. Therefore, there are higher requirements for the power quality of the grid side of the prestage circuit of the charger [1]. In the traditional rectifier system, the AC power is obtained from the grid side, rectified by an uncontrolled rectifier bridge, and then fed into the electrical load [2]. This method makes the power factor in the circuit low and increases the harmonic content of the current in the circuit [3]. In addition, there are switching elements, diodes, and filter capacitors and inductors with large values in the control system circuit, these are all nonlinear components, and their nonlinearity will seriously pollute the quality of the power grid [4]. If an AC circuit is added to improve the power factor after passing through the rectifier bridge, the harmonic content of the current can be effectively reduced and the power factor on the grid side can be improved with only a small increase in cost [5].

The research and development of chargers have become a key technical problem in solving electric vehicle charging, in order to realize convenient and timely charging of power batteries anytime, anywhere, and enhance the public's interest and confidence in using electric vehicles [6]. Power factor correction technology is a very important part of the onboard charging system, which is a necessary device to meet the green environmental protection requirements of power electronic products, and is a key technology in the development of onboard chargers in the future [7]. At the same time, another main reason why the power factor correction circuit must be installed in the vehicle charger system is to meet the requirements of international regulations on the harmonic content and power factor of the power supply, making the electromagnetic environment cleaner [8].

The power factor correction circuit is mostly after a series of filtering and rectification of the AC power, then carrying out the control adjustment of power factor correction [9]. In the charger, due to the large power of the whole machine, especially under low voltage and high current, the loss that occurs on the rectifier bridge when the current is rectified by the rectifier bridge cannot be ignored [10]. Therefore, the traditional bridge PFC topology structure due to the existence of the rectifier bridge, the efficiency of the whole machine cannot be further improved [11]. In order to reduce losses and improve the efficiency of the whole PFC circuit, more and more people have begun to pay attention to new topologies in recent years [12]. Among these topologies, the bridgeless PFC topology has received extensive attention due to its simple structure, reliability, and less peripheral devices in the control circuit [13], as shown in Figure 1.

## 2. Literature Review

The choice of the operating mode of the PFC converter depends on the required power rating, the cost of the overall system, and the allowable stress on the switches of the PFC converter [14]. The PFC converter provides low current stress on the switch for operation in continuous inductor conduction mode (CCM), but requires sensing of supply voltage, DC bus voltage, and supply current for its operation [15]. PFC converters operating in discontinuous inductor conduction mode (DCM) provide inherent power factor correction for AC power supplies, without any sensing requirements. But the current stress in DCM operation is high, therefore used for low-power applications [16]. The boost PFC converter is the most widely used configuration.

In recent years, electric vehicles powered by clean energy have developed vigorously, contributing to energy conservation, emission reduction, and environmental protection [17]. Corresponding onboard chargers for electric vehicles have also become a new industry, as the connection between the power grid and the power battery of electric vehicles, they must have the function of power factor correction [18]. Boost circuit is widely used in PFC technology because of its simple topology, high efficiency, and easy control; its energy storage inductor can suppress electromagnetic interference and radio frequency interference and can achieve larger output power [19]. The interleaved parallel boost PFC circuit has a strong advantage in the occasion of larger power capacity, by connecting multiple boost converters with interleaved control in parallel, the output of higher power capacity can be effectively achieved, and it avoids the uneven current caused by the direct parallel connection of the switch tubes, reduces the capacity requirements of the switch tubes, and the input current is shared by multiple switch tubes at the same time, which increases the input current ripple frequency and reduces the input ripple current amplitude, it is beneficial to the design of the filter circuit and the reduction of switching loss.

Some scholars have adopted a two-stage isolated structure of boost-APFC and DC-DC converter, in which the DC-DC converter is composed of a full-bridge resonant converter and a synchronous rectifier, and the overall efficiency of the charger can reach 92.5% [20]. In order to further improve the efficiency of the whole machine, it is necessary to study the design of the prestage boost-APFC of the onboard charger. Compared with the ordinary boost converter, the interleaved parallel boost converter has the characteristics of high power factor, high efficiency, and strong control ability. Combining the working principle of the interleaved parallel boost PFC circuit, the author analyzes the closed-loop control theory of CCM peak current, based on digital control, a 4 kW experimental prototype is designed for verification, which can provide a technical solution with a high power factor, low input current ripple and high efficiency for the onboard charger of electric vehicles so that the conversion efficiency of the PFC converter can meet the requirements of the platinum version.

## 3. Methods

3.1. Analysis of the Working Principle of Interleaved Parallel Boost PFC. The interleaved parallel boost PFC circuit is based on the single-channel boost PFC circuit and adds an inductive path in parallel with it. In the interleaved parallel mode, there is a time difference of 50% of the period between the two switches. The waveform diagram of each part of the interleaved parallel mode is shown in Figure 1.  $g_1, g_2$  is the state of the two switches,  $i_{L1}, i_{L2}$  is the current waveform, and  $i_{D1}, i_{D2}$  is the freewheeling diode current waveform. Due to the superposition of the two inductor currents, the ripple of the input current ripple is doubled, which effectively reduces the high-frequency harmonic content in the input current, thereby reducing the small EMI filter size.

In order to obtain a higher power factor, the author adopts CCM mode. The switches S1 and S2 have two states of on and off, respectively, in the continuous mode of the inductor current, the circuit may have four working states.

- (1) Mode 1. The switches S1 and S2 are turned on at the same time, the inductor current  $i_{L1}$ ,  $i_{L2}$  both rises, and the output capacitor  $C_0$  releases energy
- (2) Modal 2. The switch tube S1 is turned off, S2 is turned on, and the inductor current  $i_{L1}$  drops and  $i_{L2}$  rises
- (3) Modal 3. The switch tube S1 is turned on, and S2 is turned off, at this time, the inductor current  $i_{L1}$  rises and  $i_{L2}$  falls
- (4) Modal 4. The switches S1 and S2 are both turned off, the current  $i_{L1}$ ,  $i_{L2}$  of the two inductors decreases, and the output capacitor  $C_0$  stores energy

Through theoretical analysis of the working state and circuit characteristics of the boost PFC converter in the continuous mode of the inductor current, it is concluded that the staggered parallel circuit has the advantages of reducing the input current ripple, reducing the size of the inductor core, and improving the power level of the PFC circuit.

3.2. Parameter Design of Main Components. The main parameter design of the staggered parallel boost PFC includes the design of the output filter inductor, the selection of the output capacitor, the selection of the switch tube, and the selection of the power diode, through loss analysis, the one



FIGURE 1: High-performance control of PFC converter for electric vehicle charge.

with the smallest loss is selected. The technical requirements of the design are as follows: the output voltage  $V_0$  is 400 V, and its maximum value  $V_{o\_max}$  is 408 V; the maximum output current  $I_{0-max}$  is 10 A; the input minimum voltage  $V_{in\_min}$  is 180 V; the input normal voltage is 220 V; efficiency  $\eta$  is 0.95; the rated output power  $P_o$  is 4 kW; the power factor requires a PF value of 0.99; and the switching frequency  $f_0$  is 60 kHz.

#### 3.2.1. Inductor Design and Loss Analysis

(1) Calculate the Inductance. First of all, the minimum inductance can be calculated according to the inductor current ripple requirements, the parameters of the two inductors are the same, and they are calculated according to the two conditions of the minimum input voltage (180 V) and the input rated voltage (220 V).

The RMS value of the input current at the rated load is the following formula:

$$I_{in\_\max\_rms} = \frac{P_0}{\eta \cdot V_{in\_\min\_rms} \cdot PF}.$$
 (1)

In the formula,  $P_o$  is the output power;  $\eta$  is the efficiency;  $V_{in\_\min\_ms}$  is the average value of the minimum input voltage; PF is the power factor requirement.

The maximum input current amplitude is  $\sqrt{2}$  times the RMS value of the input current at the rated load, and the maximum input average current is  $2/\pi$  times the maximum input current amplitude. As far as the peak value of the input voltage is concerned, the maximum duty cycle is obtained when the input voltage is the smallest.

$$D_{\max} = \left(V_o - \sqrt{2} \cdot V_{in\_\min\_rms}\right) \cdot V_o^{-1}.$$
 (2)

The maximum allowable ripple of the inductor current

$$\Delta I_{L-\max} = 0.2 \cdot I_{in_{\max-pk}} \cdot \left(\frac{1-2 \cdot D_{\max}}{1-D_{\max}}\right)^{-1}.$$
 (3)

According to the maximum ripple allowed by the inductor current, the minimum inductance can be obtained from (2) and (3) as the following equation:

$$L_{\min} = \frac{\sqrt{2} \cdot V_{\text{in\_min\_rms}} \cdot D_{\max}}{\Delta I_{L\_\max} \cdot f}.$$
 (4)

In the same way, it can be deduced that the minimum inductance value required when inputting the rated voltage  $V_{in_{nor}}$  is the following equation:

$$\nu_{\rm nor} = \frac{\sqrt{2} \cdot V_{\rm in\_nor\_rms} \cdot D_{\rm nor}}{\Delta I_{L\_nor} \cdot f}.$$
(5)

Compare the two cases, whichever is greater. Select the magnetic ring model: CS467060, the material is Sendust (iron silicon aluminum powder), and the relevant parameters of the magnetic core are as follows: the core path  $L_e$  is 10.74 cm, the inductance  $L_A$  per turn of the magnetic core is  $135 \text{nH} \cdot \text{N}^{-2}$ , the cross-sectional area  $A_e$  of the core is  $1.99 \text{ cm}^2$ , the thickness of the magnetic ring is 46.74 mm, the inner diameter  $D_0$  of the magnetic ring is 24.13 mm, the core volume  $V_e$  is  $21.373 \text{ cm}^3$ , the core permeability  $\mu$  is  $60 \mu_0$  (unit:  $\text{H} \cdot \text{m}^{-1}$ ).

(2) Analysis of Inductance Loss. Inductance loss mainly considers copper loss and core loss; During the working process of the converter, the inductance stores and releases energy, which causes the change of the B-H curve of the magnetic core to generate the winding loss  $P_{cu}$  as the following formula:

$$P_{cu} = R_{cu} \times \left(\frac{1}{2}I_{in-\max_{rms}}\right)^2,\tag{6}$$

where R<sub>cu</sub> is the DC resistance of the copper wire.

The duty cycle function, half of the magnetic flux density change function, and the core loss function are the following equations:

$$D(t) = \frac{V_o - \sqrt{2} \cdot V_{in\_\min\_rms} \sin(wt)}{V_o},$$
(7)

$$\Delta B(t) = \frac{1}{2} \times \frac{\sqrt{2} \cdot V_{in\_\min\_ms} \cdot \sin(wt) \cdot D(t)}{N \cdot A_e \cdot 10^{-4} \cdot f} \times 10^4.$$
(8)

$$P(t) = f \cdot \left(\frac{a}{\Delta B(t)^{3}} + \frac{b}{\Delta B(t)^{2.3}} + \frac{c}{\Delta B(t)^{1.65}}\right)^{-1} + d \cdot \Delta B(t)^{2} \cdot f^{2}.$$
(9)

where a, b, c, d are the core loss parameters provided by micrometal,  $a = 7.89 \times 10^9$ ,  $b = 7.11 \times 10^8$ ,  $c = 8.89 \times 10^6$ ,  $d = 2.85 \times 10^{-14}$ ;  $\Delta B(t)$  is the AC magnetic flux density in a switching cycle; f is the switching frequency;  $V_e$  is the core volume.

From equations (7)–(9), the total loss of the magnetic core and the total loss of the inductance can be calculated as the following equation:

$$P_{\text{core}} = \frac{2}{T} \times \int_{0}^{2/T} P(t) dt \times 10^{-3} \times V_e,$$

$$P_{L_otal} = (P_{\text{core}} + P_{cu}) \times 2.$$
(10)

#### 3.2.2. Selection of Switch Tube and Power Diode

(1) Switch Tube Selection and Loss Analysis. The withstand voltage  $U_{ds}$  of the switch tube is the sum of the maximum output voltage, the peak voltage, and a certain margin reserved.

$$U_{ds} = V_{o_2 \max} \times (1 + k_2 + k_3). \tag{11}$$

Among them  $k_2$  is the impulse current coefficient, the value is 0.1;  $k_3$  is the margin coefficient, and the value is 0.1.

Since the two switches are connected in parallel, the maximum current  $I_{mos}$  is taken as half of the peak value of the maximum inductor current, and considering the uneven current and inrush current of the parallel switch tubes, the current stress of the switch tubes should leave a large margin, which is

$$I_{ds} = I_{mos} \times (1 + k_1 + k_2).$$
(12)

Among them  $K_1$  is the uneven current coefficient, which takes the value of 0.05;  $K_2$  is the residual coefficient, which takes the value of 0.1.

According to the voltage and current stress of the switch tube, the parameters of the selected MOSFET STW48NM60N and MOSFET IXFK44N60 are shown in Table 1. The loss of the interleaved parallel PFC circuit is mainly composed of the loss of the filter inductor and the loss of the switching tube. The switch loss consists of on-state loss, turn-on loss, turn-off loss, and drive loss. Next, the loss analysis of the selected MOSFET switch is carried out.

When the MOS tube is turned on, the voltage drops from 400 V to 0 V, and the current starts to rise from 0A. The envelope function of the minimum value of the inductor current is the following equation:

$$I_{L\_nor\_pk\_min} = \frac{I_{in\_nor\_pk} - \Delta I_{L\_nor}}{2},$$

$$I_{s\_on}(t) = \frac{I_{L\_nor\_pk\_min}}{2} \times \sin(\omega t).$$
(13)

TABLE 1: Different device parameters at 25°C.

Parameter	STW48NM60N	IXFK44N60
Breakdown voltage $V_{DSS}/V$	600	600
Drain current $I_D/A$	44	44
Total gate charge $Q_{as}/nC$	124	330
Rise time $t_r/ns$	18	50
Fall time $t_f/ns$	25.5	40
Drive voltage $U_{as}/V$	12	12
On resistance $R_{ds}^{gs}$ / $\Omega$	0.07	0.13

In the formula,  $I_{\text{in_nor_}pk}$  is the input current amplitude under the rated input voltage;  $\Delta I_{L_n\text{or}}$  is the maximum allowable ripple of the inductor current in equation (3).

The average turn-on loss  $P_{on\_once}$  of each switching cycle and the total turn-on loss  $P_{on\_four}$  of the four switches are expressed as follows:

$$P_{\text{on\_once}} = \frac{2}{T} \int_{0}^{T/2} \frac{1}{2} \cdot \frac{V_0}{2} \cdot \frac{I_{sson_{\text{on}}}(t)}{2} t_f \cdot dt,$$

$$P_{\text{on\_four}} = P_{\text{on\_once}} \times f \times 4.$$
(14)

where  $t_f$  is the switch fall time.

When the MOS tube is turned off, the voltage rises from 0 V to 400 V, and the current drops to 0A from the rising peak value of the inductor current. The envelope function of the inductor's current peak value is as follows:

$$I_{L\_nor\_pk\_\max} = \frac{I_{in\_nor\_pk} + \Delta I_{L\_nor}}{2},$$

$$I_{s\_off}(t) = \frac{I_{L\_nor\_pk\_\max}}{2} \cdot \sin(\omega t),$$
(15)

where  $I_{in\_nor\_pk}$  is the input current amplitude at the rated input voltage;  $\Delta I_{L_2nor}$  is the maximum allowable ripple of the inductor current in formula (16).

The average turn-off loss  $P_{\text{off}_{off}_{once}}$  per switching cycle and the total turn-off loss  $P_{\text{off}_{four}}$  of the four switches are as follows:

$$P_{\text{off\_once}} = \frac{2}{T} \int_{0}^{T/2} \frac{1}{2} \cdot \frac{V_o}{2} \cdot \frac{I_{s\_off\_ff}(t)}{2} t_r \cdot dt, \qquad (16)$$
$$P_{\text{off\_four}} = P_{\text{off\_once}} \times f \times 4,$$

where  $t_r$  is the switch rise time.

The conduction loss  $P_{sustain_{four}}$  and the total drive loss  $P_{gs_{four}}$  are as follows:

$$P_{\text{sustain}\_\text{four}} = I_{in\_nor\_rms}^2 \times \frac{R_{ds}}{4},$$

$$P_{gs\_four} = U_{gs} \times (Q_{gs} \times f) \times 4.$$
(17)

In the formula:  $R_{ds}$  is the on resistance;  $U_{gs}$  is the driving voltage;  $Q_{qs}$  is the gate charge.

Combining the above loss analysis, the total loss of the four MOS tubes can be obtained as the following formula

$$P_{MOS} = P_{on\_four} + P_{off\_four} + P_{sustain\_four} + P_{gs\_four}.$$
 (18)

#### Journal of Control Science and Engineering

According to the above principles of MOSFET loss calculation, the losses listed in Table 1 are compared, as shown in Figure 2. It can be clearly seen from Figure 2 that Using MOSFET STW48NM60N reduces the loss of the switch tube by 17.768 W than IXFK44N60, so the switch tube chooses STW48NM60N.

(2) Diode Selection and Loss Analysis. For the selection of power diodes, considering that when the load is switched from heavy load to no-load, the output voltage will instantly increase a lot, and a certain margin must be left, the diode reverses withstand voltage.

$$U_{d_{-\max}} = V_{o_{-\max}} \cdot (1 + k_{rise} + k_3).$$
(19)

Among them  $k_{rise}$  is the voltage rise coefficient, the value is 0.05;  $K_3$  is the margin coefficient, the value is 0.1.

The calculation of the maximum current flowing through the reference switch tube (maximum effective value + uneven current + margin).

$$I_{d_{foward}} = \frac{I_{in_{min}_{rms}}}{4} \left(1 + k_1 + k_3\right).$$
(20)

According to the reverse withstand voltage and withstand current of the power diode, the power diodes are selected as silicon carbide C3D10060A from Cere and DHG10I600PA from IXYS, the parameters are shown in Table 2.

When the switch tube is turned off, the power diode will generate a forward loss, at this time, the current is the drop value of the inductor current, and the average current can be obtained from the following formula:

$$D_{\text{off}}(t) = 1 - D(t) = \frac{\sqrt{2 \cdot U_{in\_nor} \cdot \sin(\omega t)}}{V_o},$$

$$T_{r\_pk\_one}(t) = \frac{I_{in\_nor\_pk} \cdot \sin(\omega t)}{4}.$$
(21)

Integrate into half cycle to get forward loss equation

 $I_{no}$ 

$$P_{\text{dio}\_\text{forward}} = \frac{2}{T} \times \int_{0}^{T/2} \left[ U_{\text{dio}\_\text{forward}} \times I_{\text{nor}\_\text{pk}\_\text{one}}(t) \times D_{\text{off}}(t) \right] dt.$$
(22)

The average duty cycle is calculated from the following equation:

$$D_{\text{avg}} = \frac{2}{T} \times \int_{0}^{T/2} D(\theta) d\theta.$$
 (23)

The reverse loss can be expressed as the following equation:

$$P_{\rm dio\_reverse} = V_o \times I_{\rm dio\_reverse} \times D_{\rm avg}.$$
 (24)

The switching loss of a single power diode can be expressed as the following equation:

$$P_{\rm turn} = \frac{1}{2} \cdot C_{\rm dio} \cdot V_o^2 \cdot f.$$
<sup>(25)</sup>

where  $I_{\text{dio reerse}}$  is the reverse leakage current.



FIGURE 2: Switch loss comparison.

TABLE 2: Different device parameters at 125°C.

Parameter	C3D10060A	DHG10I600PA
Reverse voltage V <sub>RRM</sub> /V	600	600
Continuous forward current $I_F/A$	. 10	10
Forward voltage $U_{dio forward}/V$	2.0	2.20
Reverse leakage current $I_{\text{dio reverse}}/\mu A$	200	1500
Junction capacitance $C_{dio}/pF$	42	44

The total loss of the four power diodes is

$$P_{di\ o} = \left(P_{\text{dio}_{\text{forward}}} + P_{\text{dio}_{\text{reverse}}} + P_{\text{turn}}\right) \times 4.$$
 (26)

In order to compare the loss distribution of the two power diodes, the main losses of the selected two types of diodes are compared, as shown in Figure 3. It can be seen from Figure 3 that the loss of DHG10I600PA is slightly higher than that of C3D10060A, considering the overall efficiency, the selected power diode model is C3D10060A.

3.2.3. Output Capacitor Co. The value of the withstand voltage  $U_{co}$  of the output capacitor is similar to the selection of the previous switch tube and diode, and it is also the sum of the maximum output voltage, the peak voltage, and a certain margin reserved.

The capacitance value of the capacitor is calculated according to the power-off maintenance time. Therefore, Co can be obtained by the following equation:

$$C_o = \frac{T_{\text{hold}} \cdot I_{o\_\text{max}}}{V_o}.$$
 (27)

In the formula,  $T_{hold}$  is the power-off maintenance time, take 50 ms;  $I_{o \max}$  is the maximum output current 10 A.

*3.2.4. Total Loss.* Through the analysis and calculation of the loss distribution of each part, the loss distribution of the selected device is shown in Figure 4, it can be seen that the loss of the filter inductor, diode, and switch tube accounts for the main part, we can start by optimizing these three parts to



FIGURE 3: Comparison of the main losses of the two diodes.



FIGURE 4: Converter loss distribution.

further improve the efficiency of the converter, and meet the requirements of onboard chargers.

## 4. Results and Analysis

Build a staggered parallel boost PFC experimental prototype, the control chip adopts 56F8013VFAE, a member of Freescale's commonly used chip 56F8013 series. According to the working mode of the interleaved parallel PFC, the doubleclosed-loop SPWM control strategy of the instantaneous value feedback of the output voltage and the inductor current is used to control the on and off of the switches S1 and S2 to realize rectification, the overall control block diagram is shown in Figure 5. The instantaneous current feedback of the inductor is used as the current inner loop, which can effectively improve the system's dynamic response and antiload disturbance capability, and can also realize the current limiting protection function, the output voltage outer loop can realize voltage regulation control and reduce waveform distortion.

The working waveforms of the interleaved parallel boost PFC circuit under different loads in actual working



FIGURE 5: Variation of PF value and THD value with input power.



FIGURE 6: Efficiency as a function of input power.

conditions include 56.5% load, 103.4% load input voltage  $u_{in}$ , input current  $i_{in}$ , the input current, inductor current, and the  $u_{ds}$  waveform of the drain-source voltage drop of the switch tube, shown in Figure 5, it can be seen that, at different loads, the input current phase tracking of the output voltage of the interleaved parallel PFC can achieve close to unity power factor.

At full load, the power factor value is 0.998. Figure 6 shows the variation of the PF value and THD value of the prototype with the output power. As can be seen from the Figure, when the load power is between 775.45 and 4248.1 W, the power factor of the system is always kept above 0.99, which meets the design requirements. The efficiency requirements of the platinum version of the power supply under three loads of 20%, 50%, and 100% are 90%, 94%, and 91%, respectively. The efficiency of the prototype as a function of input power is shown in Figure 6. It can be clearly seen from Figure 6 that the actual efficiency of the prototype is 97.43%, 97.55%, and 97.36%, which are far higher than the efficiency requirements of the platinum version. At the same time, it has a certain guiding significance for the application of electric vehicles.

## 5. Conclusion

The author proposes a high-performance control simulation study of the PFC converter for electric vehicle chargers, aiming at the prestage PFC part of the onboard chargers for electric vehicles, a digital control-based medium, and high power interleaved parallel average current boost PFC is proposed. The working principle of the converter continuous conduction mode (CCM) is analyzed, and the design of key circuit parameters, detailed circuit design process, and loss analysis are given. Through more detailed loss calculation, compared with components with smaller loss parameters, the loss is significantly reduced, and the efficiency of the whole machine is also improved accordingly. The experimental results verify the correctness of the theoretical analysis.

## **Data Availability**

The data used to support the findings of this study are available from the corresponding author upon request.

## **Conflicts of Interest**

The authors declare that they have no conflicts of interest.

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