Hindawi Publishing Corporation
Journal of Engineering
Volume 2016, Article ID 7345232, 8 pages
http://dx.doi.org/10.1155/2016/7345232

Research Article

Fault Tolerant Operation of ISOP Multicell Dc-Dc Converter Using Active Gate Controlled SiC Protection Switch

Yusuke Hayashi, Yoshikatsu Matsugaki, and Tamotsu Ninomiya

Green Electronics Research Institute, Kitakyushu (GRIK), 1-8-409 Hibikino, Wakamatsu-ku, Kitakyushu, Fukuoka 808-0135, Japan

Correspondence should be addressed to Yusuke Hayashi; hayashi@grik.jp

Received 24 August 2016; Accepted 29 November 2016

Academic Editor: Yuh-Shyan Hwang

An active gate controlled semiconductor protection switch using SiC-MOSFET is proposed to achieve the fault tolerant operation of ISOP (Input Series and Output Parallel) connected multicell dc-dc converter. The SiC-MOSFET with high temperature capability simplifies the configuration of the protection circuit, and its on-resistance control by the active gate controller realizes the smooth protection without the voltage and the current surges. The first laboratory prototype of the protection switch is fabricated by using a SiC-MOSFET with a high frequency buck chopper for the active gate controller. The effectiveness of the proposed protection switch is verified, taking the impact of the volume reduction into account.

1. Introduction

The next generation dc distribution system has been proposed to realize the highly electrified low carbon society [1, 2]. A lot of power electronics converters are installed for the flexible power control in the system as shown in Figure 1. To achieve the flexible power control for the effective use of the electric power and the prevalence of the power converters, the high power density (highly efficient and ultracompact) dc-dc converters are indispensable.

The multicell dc-dc converter topology is one of options to accomplish the high power density. The intensive studies have been conducted [3–7], and the ISOP (Input Series and Output Parallel) multicell dc-dc converter using sixty-four low voltage cell converters has been reported as the 384 V-384 V, 19.2 kW converter with the power density of 10 W/cm^3 [8].

One of the features of the ISOP multicell dc-dc converter is the fault tolerance operation which realizes the continuous power delivery after the defect of the single cell converter. The protection methodology using a semiconductor power switch, a current limiting inductor, and a reverse blocking diode has been already proposed [9]. However, the volume of the current limiting inductor affects the total power density of the multicell dc-dc converter significantly.

In this paper, the protection circuit using the SiC protection switch with the active gate control is newly proposed to downsize the volume of the protection components. In Section 2, the configuration of the multicell dc-dc converter and the conventional protection methodology for the fault tolerant operation are shown. In Section 3, the details of the protection circuit using SiC power device with the active gate control are introduced. In Section 4, the first laboratory prototype of the protection circuit using SiC-MOSFET is fabricated and its effectiveness is verified.

2. Multicell Dc-Dc Converter and Protection Methodology for Fault Tolerant Operation

2.1. Configuration of Multicell Dc-Dc Converter. The conceptual diagram of the multicell dc-dc converter is shown in Figure 2. The multicell dc-dc converter consists of a lot of low voltage and low power dc-dc cell converter modules. The higher rated voltage at the input side of the multicell dc-dc converter V_{IN} is achieved by connecting the cell converter modules in ISOP (Input Series and Output Parallel). The higher rated voltage at the output side V_{OUT} is also accomplished by connecting the cell modules in IPOS (Input Parallel and Output Series). The features of the multicell converter are summarized as follows:

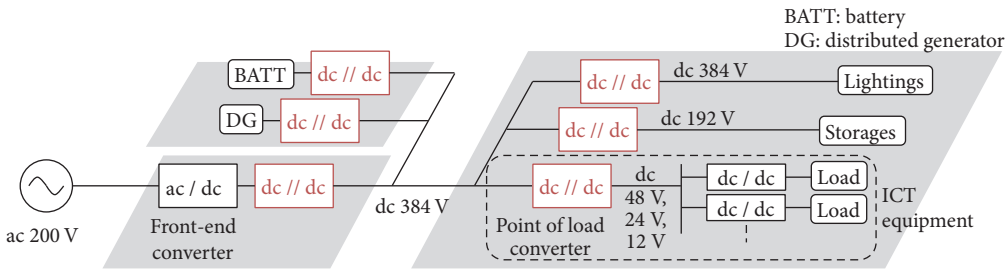

Figure 1: Configuration of next generation dc distribution system for environmentally friendly data centers [1].

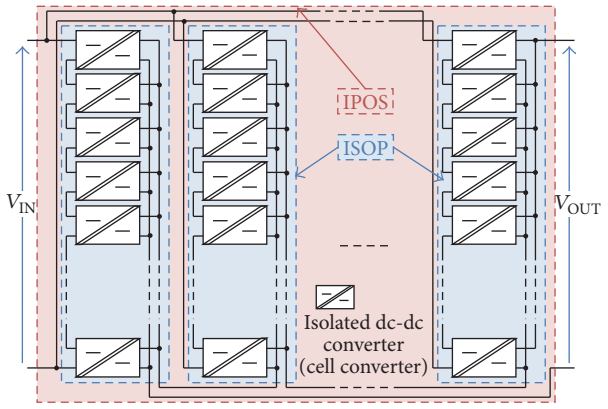

Figure 2: Conceptual diagram of multicell dc-dc converter based on ISOP-IPOS connection topology.

(i) The efficiency η (%) and the power density D_p (W/cm^3) of the multicell converter depend on the single cell converter.

(ii) The I/O (Input/Output) voltages of the multicell converter are designed arbitrarily by the number of cell converters connected in ISOP and IPOS.

(iii) The utilization of the nonregulated (the constant duty ratio) dc-dc converter for the cell converter achieves the balanced voltage and current sharing among cell converters without any complicated feedback control systems [10].

(iv) The low voltage stress of the cell converter enables employing the low voltage and ultralow loss semiconductor power devices [11].

From the aforementioned features, the design of the single cell converter plays an important role in improving the performance of the multicell dc-dc converter. Now, the 384 V-384 V, 19.2 kW multicell converter with the power density of 10 W/cm^3 has been already developed by using the highly integrated dc-dc cell converter modules connected in ISOP-IPOS [8].

On the other hand, the multicell converter has the following drawbacks:

(i) The reliability of the multicell converter is generally lower than the reliability of the conventional single converter because of the total count of the electronic parts.

(ii) In the case of ISOP connection topology, the defect of the single cell converter module leads directly to the system failure of the multicell converter.

The protection circuit is indispensable for each cell converter in the ISOP multicell dc-dc converter to enhance the total converter reliability and to prevent the system failure.

2.2. Protection Methodology for Fault Tolerant Operation. The input terminal has to be shorted and the output terminal has to be opened for the defective cell converter in the ISOP multicell dc-dc converter to keep supplying the electric power. The basic protection methodology for the fault tolerant operation of ISOP dc-dc converter has been already reported [9].

Figure 3 shows the circuit configuration of the ISOP multicell dc-dc converter with the conventional protection circuit. The protection circuit consists of the semiconductor power switch Q, the gate driver for the switch, the current limiting inductor L, and the reverse blocking diode D. The protection behavior in the case of the failure of the cell converter 1 is described as follows:

(1) In the steady state, the input voltage V_{IN} is equally divided by the total number of cell converters N and the divided voltages are injected to each cell ($V_{Cik} = V_{IN}/N, k = 1, 2, \ldots, N$).

(2) After the cell converter 1 fails and its gate control stops, the input cell voltage V_{Ci1} increases because the input and the output terminals of the cell converter 1 are opened.

(3) The switch Q_1 is turned on to short the input terminal of the cell converter 1 when the voltage V_{Ci1} exceeds the threshold for the overvoltage detection.

(4) The input cell voltage V_{Ci1} approaches to 0 V, and the input voltage V_{IN} is injected to the remained cell converters. Each input voltage of the remained cell converter rebounds to $V_{IN}/(N-1)$.

The successful behavior for the fault tolerant operation has been already reported. However, the large resonant

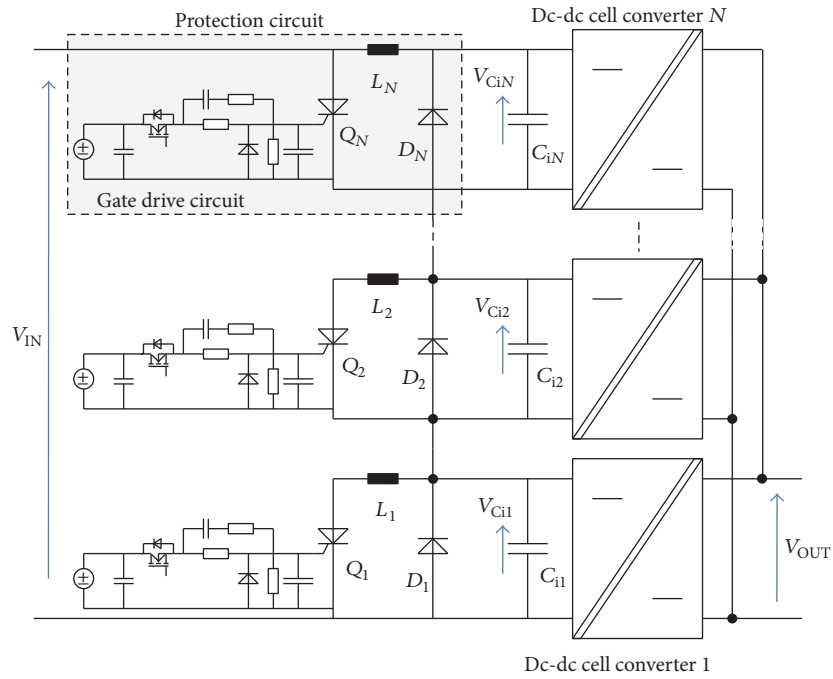

Figure 3: ISOP multicell dc-dc converter and conventional protection circuit.

current appears in case the switch Q_1 is turned on because of the current limiting inductor L_1 and the input capacitor C_{i1}. The massive inductors are required beside all cell converters to suppress the resonant current through the switch Q_1. The inductor volume prevents the fabrication of the high power density multicell dc-dc converter.

3. Active Gate Controlled SiC Protection Switch for Fault Tolerant Operation

3.1. Protection Methodology Using Active Gate Controlled Semiconductor Power Switch. Figure 4 shows the proposed protection circuit to remove the current limiting inductor. The proposed circuit consists of the protection switch Q and the active gate controller. The active gate controller provides the variable on-resistance of the protection switch Q, controlling the gate to source voltage of the switch Q linearly [12–16]. In this paper, the high frequency buck chopper circuit was applied to the achieve the variable on-resistance for the active gate control.

In Figure 4, the protection switch Q_k is turned on in the case of the defect of the dc-dc cell converter k. Under the high-speed switching operation, the surge current from the capacitor C_{ik} flows through the protection switch Q_k because of no current limiting inductors. The high resistance of the protection switch Q_k is achieved instantaneously by the active gate controller to suppress the surge current at first. Then the resistance of the switch Q_k is gradually decreased to short the input terminal of the defective cell converter.

Figure 5 shows the circuit configuration to confirm the behavior of the active gate control experimentally. The defect of the dc-dc cell converter 1 is assumed here, and the protection switch Q_1 is turned on gradually by the gate driver based on the high frequency buck chopper. Parameters for the experiment are shown in Table 1.

Table 1: Parameters for active gate control operation.

Input voltage V_{IN}	48 V
Output resistance R_{OUT}	13 Ω
Input capacitance C_{i1}, C_{i2}	22 μF, 22 μF
Dc-dc cell converters 1, 2	48 V-48 V, 300 W (V048F480T006 from VICOR)
Protection switch Q_1	SiC-MOSFET (1.2 kV, 80 mΩ from CREE)
Gate transistors Q_{g1}, Q_{g2}	GaN-FET (100 V, 16 mΩ from EPC)
Frequency of Q_{g1}, Q_{g2}	100 kHz
Gate inductance L_g	330 μF
Gate voltage V_G	15 V

Figure 6 shows the relationship between the actively controlled gate to source voltage and the drain current of the protection switch Q_1. The gate to source voltage was varied from 0 V to 15 V during (a) 1.0 ms, (b) 2.5 ms, and (c) 5.0 ms here. In the case of the transition time of 1.0 ms, the current surge appeared because of the higher speed switching operation and the peak current was over 10.0 A. In the case of the transition time of 5.0 ms, the high di/dt of the drain current disappeared and the peak value was significantly suppressed to approximately 5 A. This means that the active

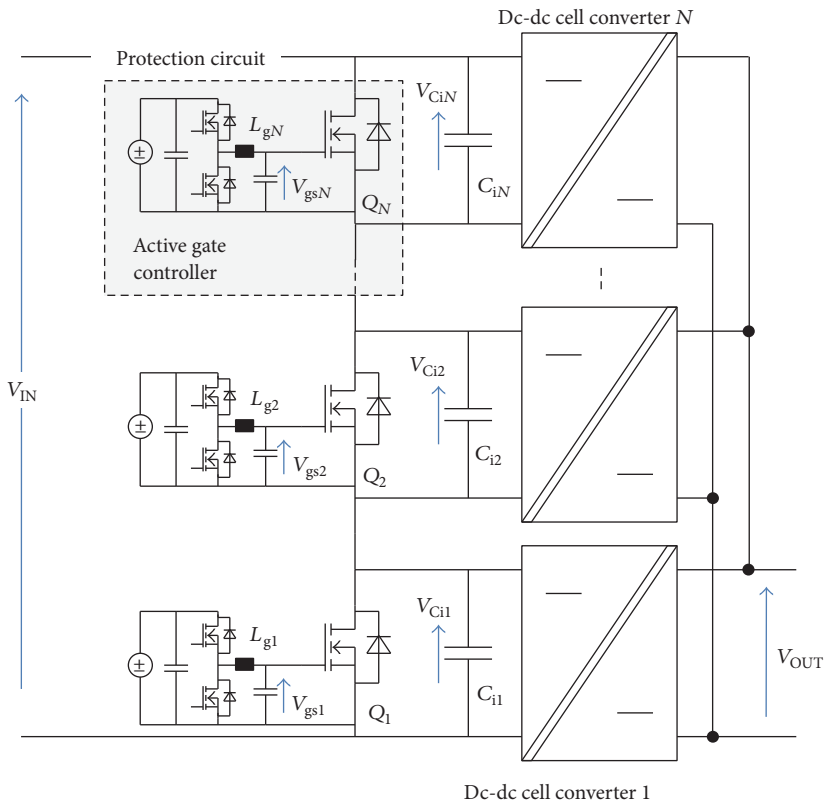

Figure 4: ISOP multicell dc-dc converter and active gate controlled SiC protection switch.

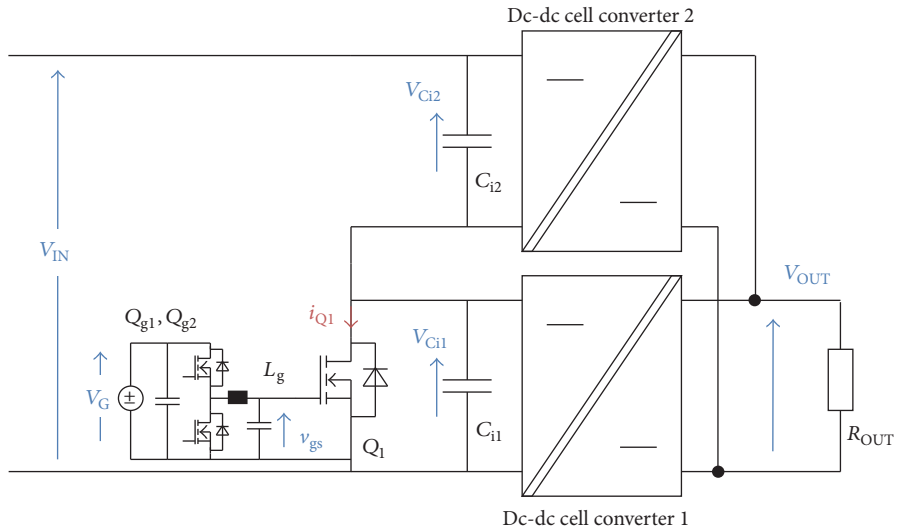

Figure 5: Circuit configuration for experiment of surge current suppression by active gate control.

gate controlled semiconductor protection switch enables suppressing the current surge without the current limiting inductor.

3.2. SiC Power Device for Protection Switch. The stored energy in the input capacitor C_{ik} is absorbed by the protection switch in the proposed protection circuit. The semiconductor device which has large SOA (Safe Operating Area) is appropriate for the protection switch. The SiC power device with the ultralow on-resistance and the high temperature capability is one of attractive options.

Figure 7 shows the current capability of the commercially available Si and SiC MOSFETs. The maximum value for the pulsed current density of the SiC-MOSFET and three

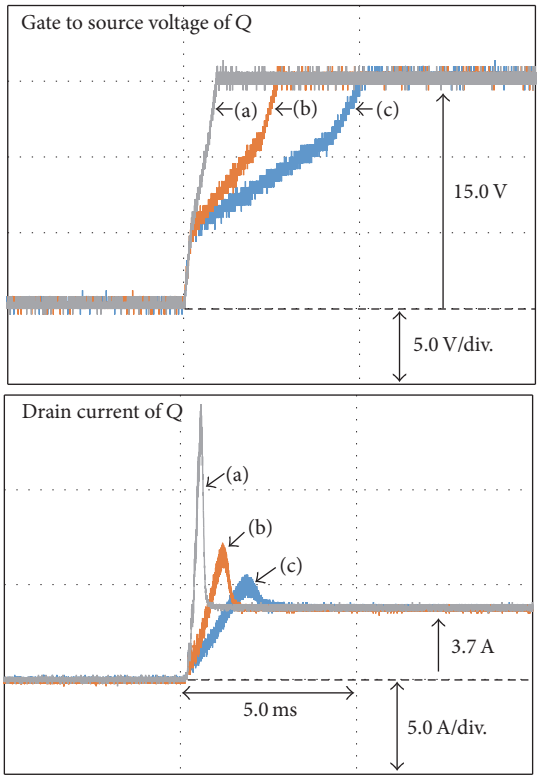

Figure 6: Active gate controlled gate to source voltage and drain current of protection switch.

Si SJ (Super Junction) MOSFETs are compared, taking the chip areas for the above power devices into account. In this figure, the SiC-MOSFET has the higher current density to keep the normal operation. The plateau area where the maximum current density is independent of the horizontal axis in Figure 7 represents the maximum heat dissipation density of the power devices [12]. One of features of SiC power devices with the low on-resistance and the high temperature capability is shown here. This means that the SiC power device is suitable for the protection circuit of ISOP multicell converter.

4. Experiment for Fault Tolerant Operation of ISOP Multicell Dc-Dc Converter Using Active Gate Controlled SiC Protection Switch

4.1. Fault Tolerant Operation of ISOP Multicell Converter Using Four Cell Converters. The prototype of the protection system for the ISOP multicell dc-dc converter has been fabricated by using the SiC-MOSFET (1200 V, 80 mΩ from CREE) and the 100 kHz buck chopper for the active gate control. The circuit configuration is based on Figure 4 ($N = 4$), and the experimental apparatus is shown in Figure 8. This consists of four dc-dc cell converter modules (V048T480T006 from Vicor) and the SiC protection switch connected to the cell converter 1 mainly. The detailed parameters for this experiment are shown in Table 2.

Table 2: Parameters for fabricating four cell ISOP converters with protection switch.

Input voltage V_{IN}	dc 96 V
Resistive load	6 Ω (electric load)
Protection switch Q_1	SiC-MOSFET (1.2 kV, 80 mΩ from CREE)
Active gate controller	100 kHz buck chopper GaN-FET (100 V, 7 mΩ from EPC)
Output inductance L_{g1} for active gate control	330 μH (10% ripple for 100 kHz operation)
Cell converter	V048F480T006 (48 V-48 V, 300 W from VICOR)
Input cell capacitor C_{ik} $(k = 1, 2, 3, 4)$	22 μF
Number of cell converters	4
FPGA	Cyclone III

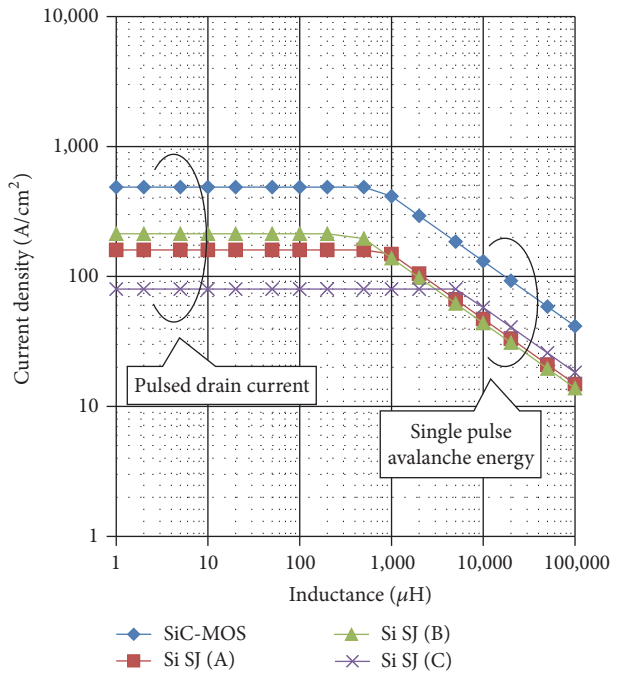

Figure 7: Maximum current density of Si and SiC power devices for safe operation.

The experimental result in case the cell converter 1 failed is shown in Figure 9. The gate to source voltage V_{gs1} of SiC-MOSFET, the input cell voltages V_{Ci1}, V_{Ci2}, V_{Ci3}, and V_{Ci4}, the output voltage V_{OUT}, and the drain current through the SiC-MOSFET I_{Q1} are shown in this figure. In the steady state, all input cell voltages are kept at 24 V (= V_{IN} 96 V/4 cells). After the overvoltage detection of V_{Ci1}, the SiC-MOSFET Q_1 is turned on to short the input terminal of the cell converter 1. The voltage waveform V_{gs1} means that the on-resistance of the SiC-MOSFET is controlled to decrease gradually by the active gate control. The cell voltage V_{Ci1} approaches 0 V and

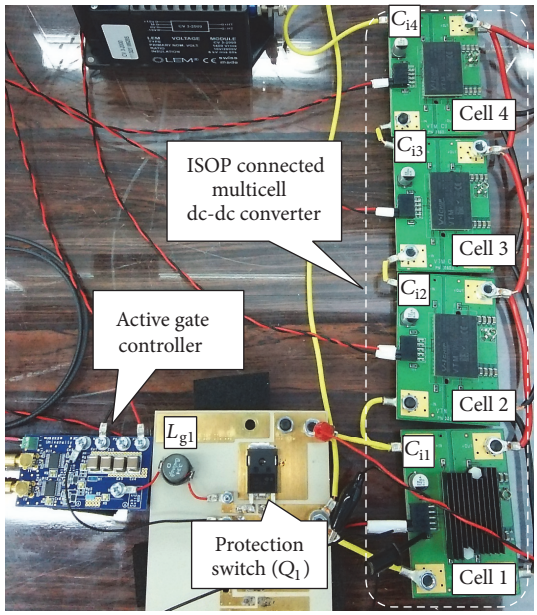

FIGURE 8: Experimental apparatus for fault tolerant operation of ISOP multicell converter using SiC protection switch.

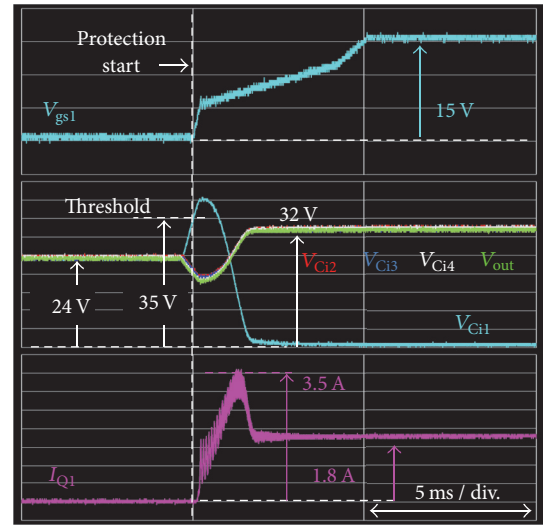

FIGURE 9: Measurement result of ISOP converter using 4 cell converters under fault tolerant operation.

the input voltages of the remained cell converters rebound to 32 V (= V_{IN} 96 V/3 cells) without any surge. The current I_{Q1} also increases gradually without surges and the electric power is kept supplying to the load through the remained three cell converters.

In Figure 9, the input cell voltages V_{Ci2}, V_{Ci3}, and V_{Ci4} had no unbalances and no surges during the transition. This was accomplished by applying both the ISOP connection topology for equal current sharing of the cell converters and the proposed active gate controlled SiC protection switch.

The behavior of the ISOP connected multicell converter has been already analyzed [10]. The input voltage of the ISOP converter is equally divided to each cell converter by the equal current sharing in the steady state. In the case of the high-speed disturbance, the input voltage unbalance among the cell converters or voltage surges appears because of the mismatch of the response speeds of the cell converters.

The transition time which was sufficiently slower than the response speed of all cell converters was achieved by the active gate controlled SiC protection switch. The influences caused by the mismatched cell converters were minimized and the characteristics of all cell converters were uniformed under the controlled smooth transition.

The voltages of 32 V which was higher than 24 V were seen for the remained three converters V_{Ci2}, V_{Ci3}, and V_{Ci4} under the fault tolerant operation. Generally, the input voltages of remained cell converters V_{Cik} ($k = 1, 2, \ldots, N$) rise to $V_{IN}/(N-1)$ in case the single cell converter fails under the fault tolerant operation, although the input cell voltages are V_{IN}/N under the steady state operation. The threshold values for the overvoltage protection V_{OV} and the undervoltage protection V_{UV} have to be designed as the following equations:

$$V_{OV} > \frac{V_{IN}}{N-1}$$
$$V_{UV} < \frac{V_{IN}}{N} - \frac{V_{OV} - V_{IN}/N}{N-1}. \quad (1)$$

In Figure 9, the input voltages of the remained cell converters were 32 V (= 96 V/3) under the fault tolerant operation and the threshold value V_{OV} was set at 35 V. Each cell converter has to be designed taking the above voltage range for the fault tolerant operation into account.

As the number of cell converters N increases, the input voltages of the remained cell converters under the fault tolerant operation approach the voltages under the steady state operation. This means that the OV and the UV protections are activated simply because the influence of the voltage overshoot caused by the fault tolerant operation becomes small.

4.2. Application Effect of Active Gate Controlled SiC Protection Switch for Volume Reduction. The proposed protection circuit removes the current limiting power inductor in the conventional protection circuit. On the other hand, the proposed circuit requires the output inductor of the buck chopper for the active gate control. The inductor volumes for the conventional and the proposed circuits are compared here.

The inductor volume is generally proportion to the stored energy in the inductor. In the conventional protection circuit in Figure 3, the stored energy of the current limiting inductor L_k corresponds to the stored energy in the input capacitor C_{ik}.

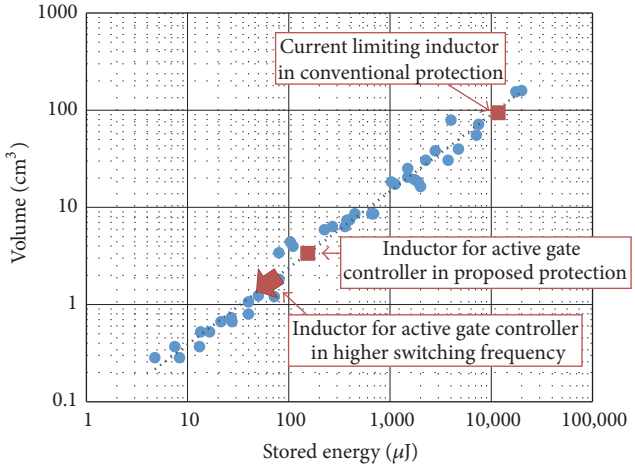

Figure 10: Relationship between inductor volume and stored inductive energy.

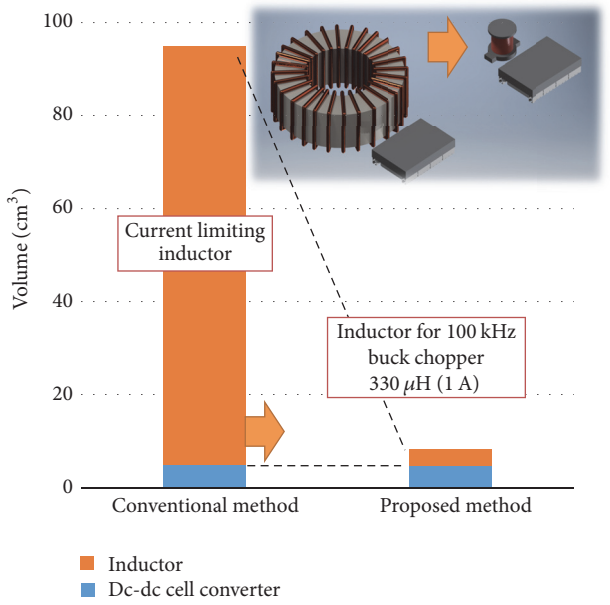

Figure 11: Application effect of active gate controlled SiC power transfer switch to downsize inductor volume.

The volume of the current limiting inductor V_{Lk} is expressed by the following equation:

$$V_{Lk} = f\left(\frac{1}{2}\cdot L_k \cdot i_{Lk}^2\right) = f\left(\frac{1}{2}\cdot C_{ik}\cdot v_{Cik}^2(0)\right). \quad (2)$$

In this paper, the capacitance C_{ik} is 22 μF from Tables 1 and 2. The voltage $v_{Cik}(0)$ means the threshold value to detect the overvoltage and this voltage was set at 35 V as shown in Figure 9. The transferred energy from the capacitor to the inductor was approximately 13.5 mJ.

In the proposed circuit in Figure 4, the inductance of the active gate controller depends on the switching frequency of the buck chopper. The inductor volume V_{Lg} is expressed as follows:

$$V_{Lg} = f\left(\frac{1}{2}\cdot L_g \cdot i_g^2\right). \quad (3)$$

From Table 2, the inductance for the active gate control was 330 μH here. This inductance was designed to suppress the ripple current through the inductor within 10% for the rated gate current i_g of 1 A under 100 kHz switching operation. The rated current of 1 A is enough for the gate drive circuit because the switching speed of the protection switch is not fast. The stored energy of the inductance for the active gate drive circuit was approximately 170 μJ.

Figure 10 shows the relationship between the volume and the stored energy of the commercially available power inductor. The gradient of this graph means the function f in (2) and (3). The inductor volumes for the conventional and the proposed circuits are obtained from this figure. The volume of 90 cm^3 is required for the conventional protection circuit and the volume of 3.5 cm^3 is necessary for the proposed protection circuit. The inductor volume for the active gate controller can be reduced by increasing the switching frequency of the buck chopper.

Figure 11 shows the application effect of the proposed protection circuit to reduce the total volume of the multicell dc-dc converter. The volume of the single cell converter V048F480T006 in Table 2 was 4.8 cm^3 for the rated output power of 300 W. The volume of the current limiting inductor for each cell converter was 90 cm^3 from Figure 10. This means that the power density of the multicell dc-dc converter is determined by the inductor in the case of the conventional protection circuit. In the case of the proposed protection circuit, the volume of the inductor for the active gate driver was 3.5 cm^3 under the switching frequency of 100 kHz. The inductor volume was smaller than the volume of the cell converter, and the proposed circuit has the potential to achieve smaller inductor volume by increasing the switching frequency of the active gate driver. This means that the high power density and the highly reliable multicell dc-dc converter will be developed by using the proposed protection methodology.

5. Conclusions

The SiC protection switch with the active gate control was proposed for the fault tolerant operation of ISOP multicell dc-dc converter. The first laboratory prototype of the protection switch using SiC-MOSFET (1200 V, 80 mΩ from CREE) with the 100 kHz buck chopper was fabricated to confirm the effectiveness of the active gate control. The experiment using four dc-dc cell converters and the SiC protection switch verified the fault tolerant operation without the voltage and the current surges in transient.

The inductor for the active gate control will be downsized by operating the buck chopper under higher switching frequency operation. The proposed approach solves the key issue in the ISOP multicell converter and this contributes to realizing the low carbon society using high power density and highly reliable converters.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

References

[1] T. Ninomiya, Y. Ishizuka, R. Shibahara, and S. Abe, "Energy-saving technology using next-generation power electronics," in *Proceedings of the IEE-Japan (IEEJ) Industry Applications Society Conference*, pp. I15–I20, Chiba, Japan, 2012.

[2] Y. Sugiyama, "Green ICT toward low carbon society," in *Design for Innovative Value Towards a Sustainable Society: Proceedings of EcoDesign 2011: 7th International Symposium on Environmentally Conscious Design and Inverse Manufacturing*, pp. 739–742, Springer, Dordrecht, The Netherlands, 2012.

[3] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1462–1473, 2004.

[4] M. Jaritz, T. Rogg, and J. Biela, "Control of a modular series parallel resonant converter system for a solid state 2.88MW/115-kV long pulse modulator," in *Proceedings of the 17th European Conference on Power Electronics and Applications (EPE '15 ECCE-Europe)*, vol. 99, pp. 1–11, Geneva, Switzerland, September 2015.

[5] L. Wang and X. He, "Input- series and output-parallel connection modular DC-DC converters with interleaved constant duty cycle control strategy," in *Proceedings of the 33rd Annual Conference of the IEEE Industrial Electronics Society (IECON '07)*, pp. 1901–1906, Taipei, Taiwan, November 2007.

[6] C. Martinez, T. Jalakas, D. Vinnikov, A. Lazaro, and A. Barrado, "QZSI DC/DC converters in input-series output-parallel connection for distributed generation," in *Proceedings of the 21st International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM '12)*, pp. 952–957, Sorrento, Italia, June 2012.

[7] J. P. Lee, B. D. Min, T. J. Kim, D. W. Yoo, and J. Y. Yoo, "High efficient interleaved input-series-output-parallel-connected DC/DC converter for photovoltaic power conditioning system," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE '09)*, pp. 327–329, IEEE, San Jose, Calif, USA, September 2009.

[8] Y. Hayashi, "Approach for highly efficient and ultra compact converters in next generation 380 V DC distribution system," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE '12)*, pp. 3803–3810, IEEE, Raleigh, NC, USA, September 2012.

[9] V. Choudhary, E. Ledezma, R. Ayyanar, and R. M. Button, "Fault tolerant circuit topology and control method for input-series and output-parallel modular DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 402–411, 2008.

[10] Y. Hayashi and T. Ninomiya, "Analysis and prototyping of multicellular DC-DC transformer for environmentally friendly data centers," *Journal of Energy and Power Engineering*, vol. 10, no. 5, pp. 313–323, 2016.

[11] L. M. Tolbert, B. Ozpineci, S. K. Islam, and M. S. Chinthavali, "Wide bandgap semiconductors for utility applications," in *Proceedings of the 17th IASTED International Conference on Power and Energy Systems (PES '03)*, pp. 317–321, February 2003.

[12] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2597–2605, 2014.

[13] Z. Wang, X. Shi, L. M. Tolbert, and B. J. Blalock, "Switching performance improvement of IGBT modules using an active gate driver," in *Proceedings of the 28th Annual IEEE Applied Power Electronics Conference and Exposition (APEC '13)*, pp. 1266–1273, IEEE, Long Beach, Calif, USA, March 2013.

[14] K. Miyazaki, S. Abe, M. Tsukuda et al., "General-purpose clocked gate driver (CGD) IC with programmable 63-level drivability to reduce Ic overshoot and switching loss of various power transistors," in *Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC '16)*, pp. 1640–1645, Long Beach, Calif, USA, March 2016.

[15] Y. Lobsiger and J. W. Kolar, "Closed-loop d*i*/d*t* and d*v*/d*t* IGBT gate driver," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3402–3417, 2015.

[16] V. John, B.-S. Suh, and T. A. Lipo, "High-performance active gate drive for high-power IGBT's," *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1108–1117, 1999.