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Research Article

Hybrid Dynamic MCML Style: A High Speed Dynamic MCML Style

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This paper proposes hybrid dynamic current mode logic (H-DyCML) as an alternative to existing dynamic CML (DyCML) style for digital circuit design in mixed-signal applications. H-DyCML introduces complementary pass transistors for implementation of logic functions. This allows reduction in the stacked source-coupled transistor pair levels in comparison to the existing DyCML style. The resulting reduction in transistor pair levels permits significant speed improvement. SPICE simulations using TSMC 180 nm and 90 nm CMOS technology parameters are carried out to verify the functionality and to identify their advantages. Some issues related to the compatibility of the complementary pass transistor logic have been investigated and the appropriate solutions have been proposed. The performance of the proposed H-DyCML gates is compared with the existing DyCML gates. The comparison confirms that proposed H-DyCML gates is faster than the existing DyCML gates.

1. Introduction

There has been tremendous boost on the design and development of portable electronic goods in recent past [1–4]. As the battery life is critical in these systems, there has been a paradigm shift towards low power designs. Though the CMOS logic circuits consume negligible static power, the dynamic power consumption increases sharply as the operating high frequencies are increased [5–8]. The MOS current mode logic (MCML) is a promising alternative to CMOS logic, in both reducing power consumption at high frequencies and providing high performance for mixed-signal applications [9–14]. Due to the presence of static current source, the power consumption of these circuits is high. Therefore, a new logic family called dynamic CML [15, 16] is suggested in literature which used dynamic current source and operate on precharge evaluate method prevailing in dynamic CMOS logic. The multiple input logic realization requires stacking of transistors leading to significant delay.

In this paper, a new method to realize the logic function in DyCML gate for reducing the stacking of transistors is presented. A dynamic logic style employing the complementary pass transistor logic (CPL) for implementing the logic functions is proposed. This new logic style is named hybrid dynamic CML logic and is abbreviated as H-DyCML style. The paper first briefly describes the existing DyCML style and highlights its advantages over the MCML style in Section 2. Thereafter, the architecture of the proposed H-DyCML style is presented and investigated in Section 3. The power consumption of the proposed style is formulated in Section 4. The functionality of the proposed H-DyCML gates and the performance comparison with the existing DyCML gates are carried out in the simulation Section 5. Lastly, the conclusions are drawn in Section 6.

2. Dynamic Current Mode Logic (DyCML) Style [15, 16]

A DyCML gate uses dynamic current source, instead of constant current source employed in conventional CML, and achieves low power consumption. It operates on precharge and evaluate logic wherein in the output node capacitance is first precharged and subsequently evaluated according to the applied inputs. It has a pull-down network (PDN) to realize the logic function, a precharge circuit operating in

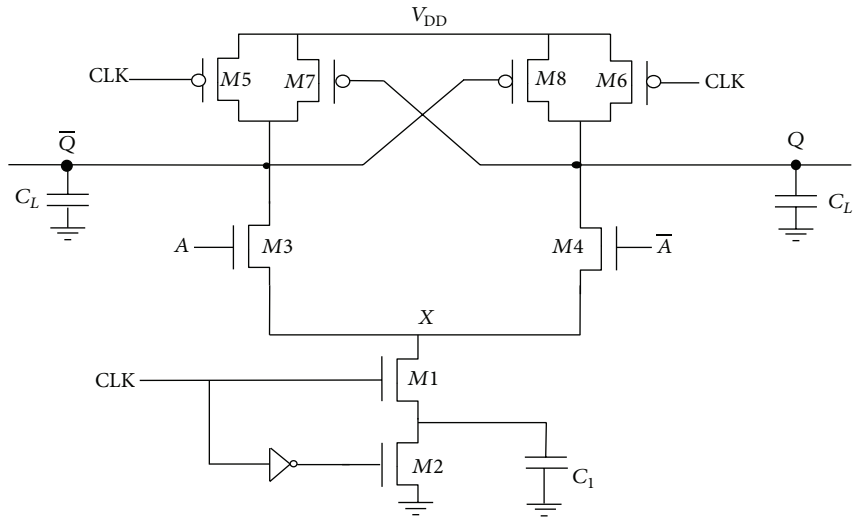

Figure 1: DyCML inverter [15, 16].

the precharge phase, a dynamic current source working in the evaluation phase, and a latch circuit for maintaining the voltage levels at the output.

The schematic of the DyCML inverter ($M1$–$M8$) is shown in Figure 1. In the circuit diagram, the transistors ($M1$, $M2$) and capacitor C_1 form the dynamic current source and the transistors ($M3$, $M4$) constitute the PDN, while the transistors ($M5$, $M6$) and ($M7$, $M8$) make the precharge and the latch circuit, respectively. During the precharge phase, the CLK is low, the transistors $M2$, $M5$, and $M6$ are On, and the transistor $M1$ is Off. Both the output nodes Q and $\overline{Q}$ are precharged to the high voltage level ($V_{OH} = V_{DD}$) through the transistors $M5$ and $M6$, respectively. Also, the capacitor C_1 is discharged to the ground potential via transistor $M2$. In the precharge phase, the differential input A is applied and does not cause any change in the output level as the precharge transistors $M5$, $M6$ are On and the transistor $M1$ is Off. The circuit enters in the evaluation phase for high value of the CLK signal. The transistor $M1$ is On in this phase and output is evaluated according to the input.

The DyCML gates offer significant power saving and are able to achieve smaller delays in comparison to the basic MCML gates. Also DyCML gates inherit the advantageous features such as high performance, noise immunity, and robustness to supply voltage scaling of MCML gates due to the fact that these are derived from the MCML gates [15, 16]. The circuit diagrams for different DyCML gates are shown in Figure 2. It can be observed that the PDN consist of multiple levels of source-coupled transistor pair arranged in accordance with the series-gating approach which adds to the delay of the gate. In this paper, an alternate arrangement to reduce the delay of the DyCML gates is proposed. The new gates are built with an aim of reducing the number of source-coupled transistor pair levels in the PDN. To accomplish this, the complementary pass transistor logic is introduced in DyCML style and nomenclature hybrid dynamic CML (H-DyCML) gates are used for the resulting logic style.

3. Proposed Hybrid Dynamic CML (H-DyCML) Style

The basic architecture of a H-DyCML gate is shown in Figure 3. The precharge, dynamic current source, and the latch circuits are similar to those of the existing DyCML gate. The only difference is in the way of realizing the logic function. The complementary pass transistor logic (CPL) is used to realize a part of functionality while the remaining part is implemented in the PDN. To illustrate the concept, the implementation of two- and three-input XOR gates in H-DyCML style is considered and is shown in Figure 4. In the two-input H-DyCML XOR gate (Figure 4(a)), the CPL implements the XOR functionality and whose output is given as the input to the DyCML inverter. The realization of the three-input XOR gate consists of two levels of stacked source-coupled transistor pair in contrast to the three levels in existing DyCML XOR gate. The input to the lowest level is provided by the CPL logic that realizes the XOR of two inputs and the upper level is then formed by applying the series-gating approach as followed for DyCML gate. The resulting implementation is shown in Figure 4(b). Another implementation of the three-input XOR gate can be obtained by realizing the complete XOR functionality in the CPL network and then connecting its output to the DyCML inverter. This implementation of the three-input XOR with only single level of source coupled transistor is drawn in Figure 4(c).

The operation of a H-DyCML gate in general can be divided into the precharge and the evaluation phase. The operation of the two-input XOR gate is elaborated as an example. In the precharge phase, when the CLK is low, both the output nodes Q and $\overline{Q}$ are precharged to the high voltage level ($V_{OH} = V_{DD}$) through the transistors $M5$ and $M6$, respectively. Also, the output of the complementary pass transistor logic is applied to input A but it does not cause any change in the output level as the precharge transistors

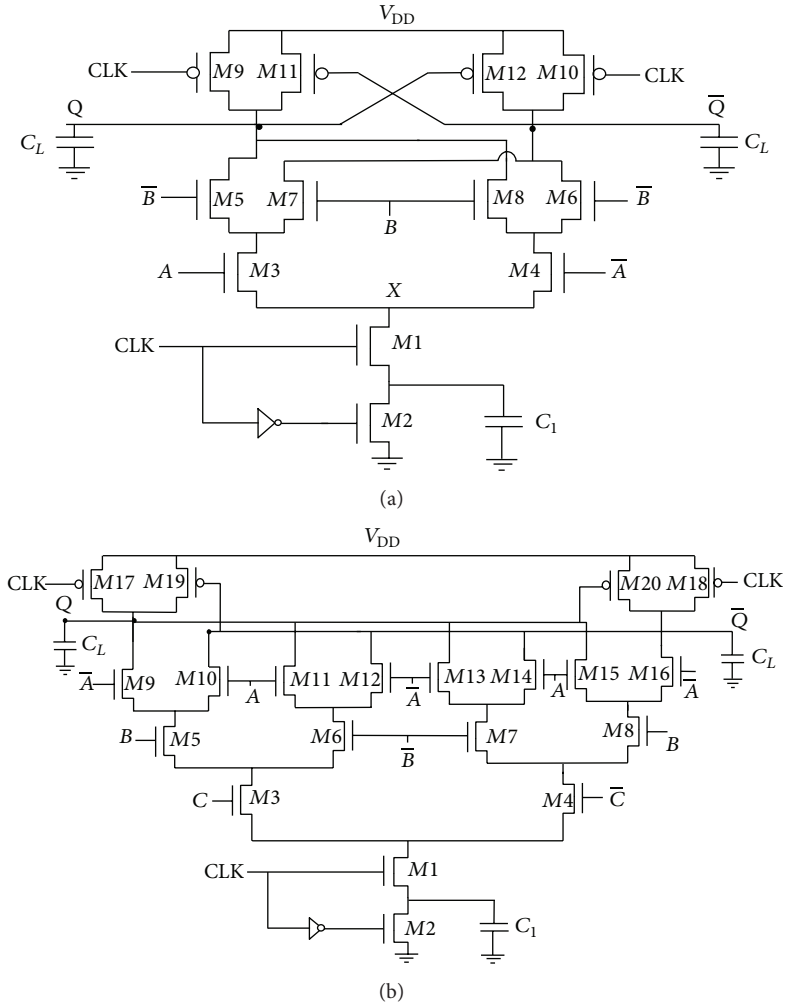

Figure 2: DyCML gate: (a) two-input XOR; (b) three-input XOR.

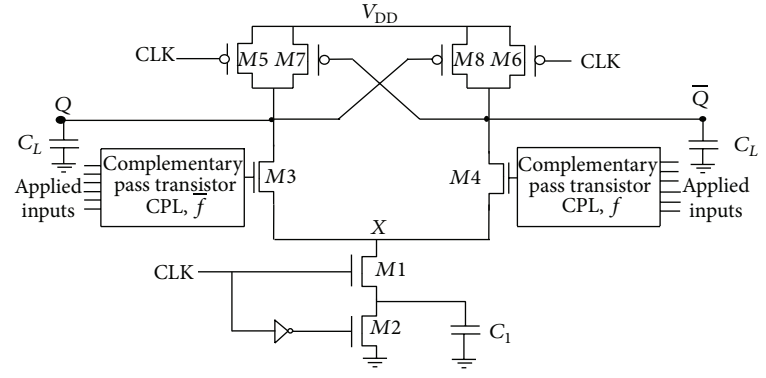

Figure 3: Basic architecture of H-DyCML gate.

$M5$, $M6$ are On and the transistor $M1$ is Off. For high value of the CLK signal, the circuit enters in the evaluation phase and the transistor $M1$ is On. The output of the CPL is now evaluated and is appropriately reflected at the output node. The reduction in the source coupled level reduces the resistance offered by the transistors for charging the capacitor C_1 and in turn reduces the delay of the gate.

It may be noted that the implementation of the logic function through the CPL approach involves the use of NMOS transistors. As already known the maximum voltage obtained from an NMOS transistor is one threshold voltage less than the gate voltage. Therefore, if a high input (V_{DD}) is applied to an NMOS transistor having its gate connected to high potential (V_{DD}) then the output can attain maximum

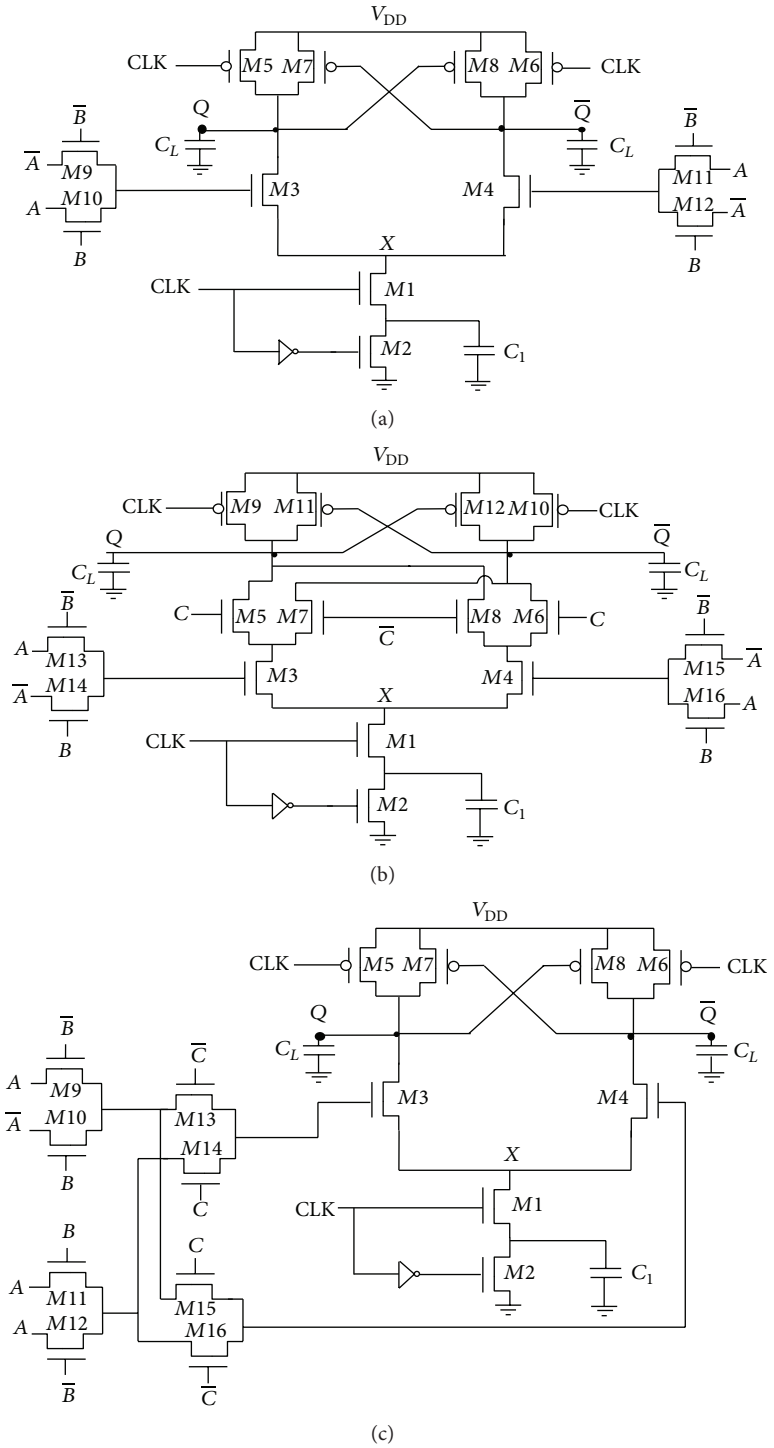

Figure 4: Proposed H-DyCML gates: (a) 2-input XOR gate; (b) 3-input XOR gate with two levels of source-coupled transistor pair in the PDN; (c) 3-input XOR gate with single level of source-coupled transistor pair in the PDN.

voltage (V_{OH}) of $V_{DD} - V_{T,n}$, where $V_{T,n}$ is the threshold voltage of NMOS transistor. This reduction in output voltage may lead to erroneous operation of dynamic gate. So three techniques to address the problem are proposed.

Technique 1: Use of Level Restorer. The maximum voltage obtained from the CPL can be raised by using cross-coupled PMOS transistors operating as level restorer. To illustrate the operation of a level restorer, the CPL implementation of a two-input XOR gate with inputs A and B is considered and is shown in Figure 5. Consider that the input A is high (V_{DD}) and the input B is low ($V_{DD} - V_{SWING}$) where V_{SWING} is the voltage swing of the CML gate. For this input condition, the output of the branch representing XOR functionality (f)

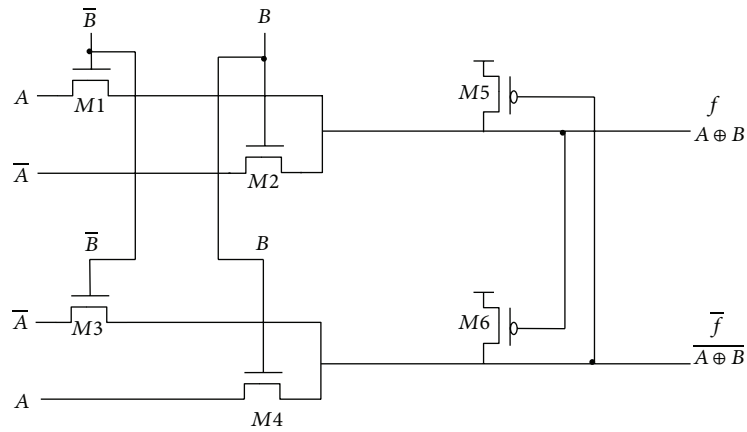

Figure 5: CPL with level restorer.

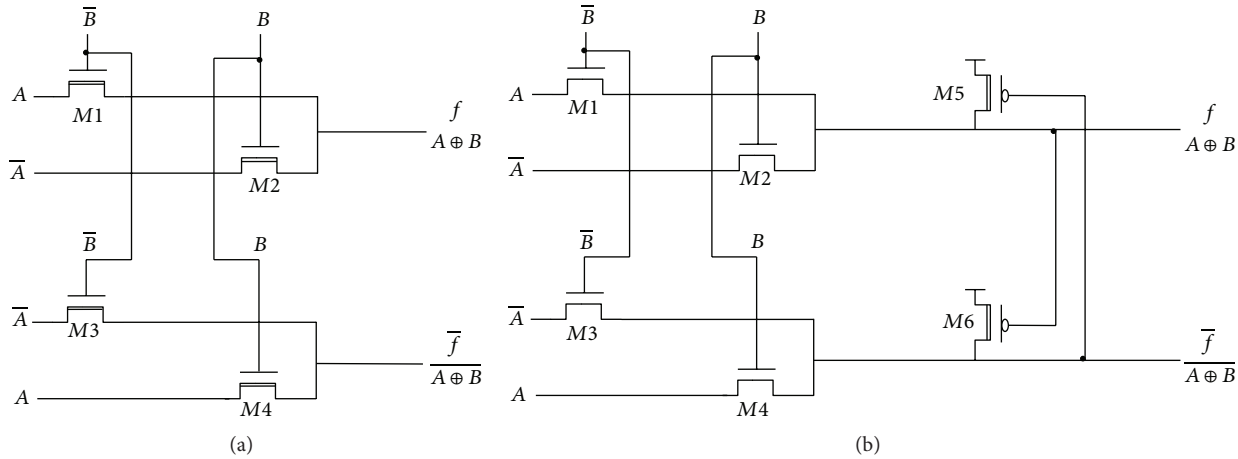

Figure 6: CPL logic with multiple threshold voltage transistor: (a) NMOS transistors; (b) PMOS transistors.

will be high ($V_{DD} - V_{T,n}$) whereas the other branch ($\overline{f}$) is low ($V_{DD} - V_{SWING}$). If the gate-source voltage of the PMOS transistor $M5$ ($V_{SG} = V_{SWING}$) is less than the threshold voltage (V_T), it gets turned On and raises the voltage level of the XOR function (f) to V_{DD}. The other PMOS transistor $M6$ will not conduct and the output of the other branch ($\overline{f}$) will remain low ($V_{DD} - V_{SWING}$).

It may be noted that this technique poses a restriction on the voltage swing V_{SWING} of the gate. This can be explained from the fact that the cross-coupled PMOS transistor $M5$ will be On only if gate-source voltage is less than the threshold voltage (i.e., $V_{SG} < V_T$). In other words, the voltage swing of the gate should be greater than the threshold voltage ($V_{SWING} > V_T$). Therefore for the CML gate having lower voltage swing, this technique is not suitable. Another technique to handle the lower CML gates is presented in the following.

Technique 2: Use of Multiple Threshold Voltage Transistor. The above technique has the limitation on the voltage swing of the CML gate due to the threshold voltage of the transistor. Therefore, this technique suggests the use of lower threshold voltage transistors in the circuit. This can be implemented in two ways either by using lower threshold voltage NMOS transistors in the CPL network or by employing lower threshold voltage PMOS transistors in the level restorer. The same is depicted in Figure 6 for the two-input XOR gate. The transistors with bold lines denote low threshold voltage transistor. Thus, the H-DyCML gates with low voltage swing can also be implemented.

An alternate approach which neither having any limitations on the voltage swing of the gate nor putting any constraint on threshold voltage is also possible and is elaborated further.

Technique 3: Use of Transmission Gates. The drop in the high voltage level at the output of the CPL network can be overcome by realizing the logic function through transmission gates. An implementation of the XOR gate by using transmission gate is shown in Figure 7. Though this technique will increase the number of transistors it does not pose any restrictions on the voltage swing of the H-DyCML gate.

4. Power Consumption of H-DyCML

In the proposed H-DyCML gate, the transistor pairs $M1$ and $M2$ (Figure 3) never turns On simultaneously. As a consequence, a direct path between the power supply

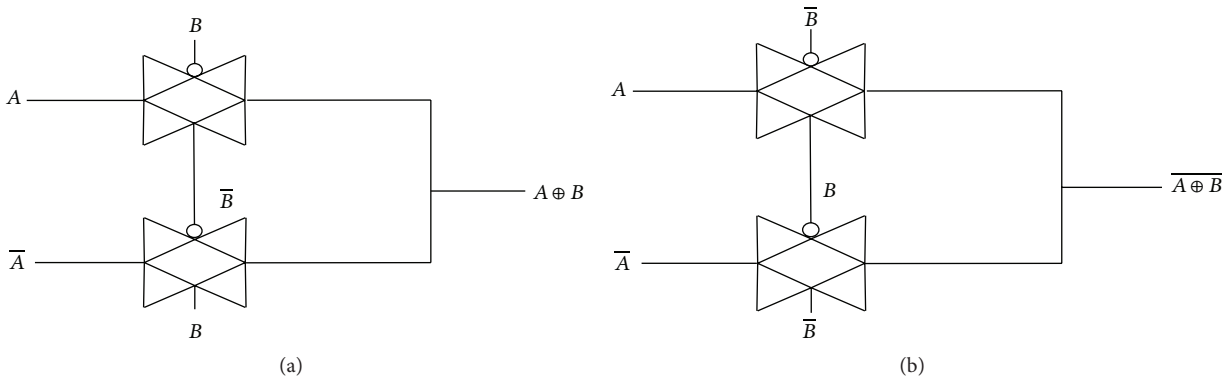

Figure 7: XOR function realization for H-DyCML gate.

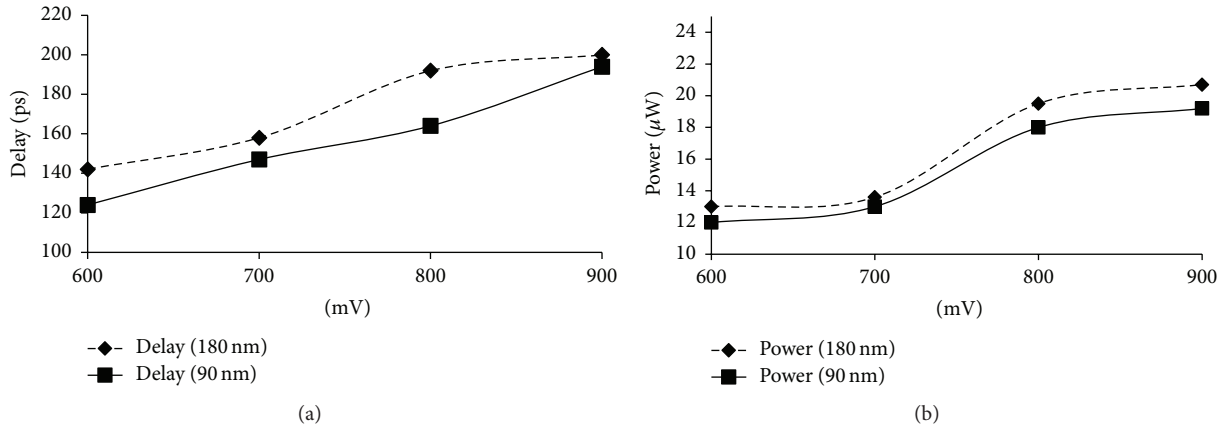

Figure 8: Performance of the two-input H-DyCML XOR gate by varying the voltage swing: (a) delay results: (b) power results.

and the ground is not established resulting in negligible static power consumption. The proposed H-DyCML gate however consumes dynamic power due to the presence of the load capacitors. In general, the dynamic power is given by

$$P_{\text{dyn}} = \alpha C_{\text{OUT}} V_{\text{DD}} V_{\text{SWING}} f_{\text{CLK}}, \quad (1)$$

where C_{OUT} is the total load capacitance at the output node which includes the parasitic capacitances of the transistors and the external load capacitance C_L, f_{CLK} represents the frequency of the CLK signal, V_{DD} is the power supply, and V_{SWING} and α correspond to the voltage swing and switching activity of the circuit, respectively.

In H-DyCML gates, due to the inherent differential nature of the inputs, it may be noted that one of the output nodes will make a high-to-low transition which requires subsequent precharging to V_{DD}. This observation indicates that the power consumption of the H-DyCML gate is data-independent. In other words, irrespective of the differential inputs, in every clock cycle one of the output nodes will be charged. This signifies that, for a H-DyCML gate, the switching activity is unity. Equation (1) reduces to (2) for power consumption of H-DyCML gates as follows:

$$P_{\text{dyn}_{\text{H-DyCML}}} = C_{\text{OUT}} V_{\text{DD}} V_{\text{SWING}} f_{\text{CLK}}. \quad (2)$$

5. Simulation Results

Different H-DyCML gates such as two-input AND, two-input OR, two-input XOR, and three-input XOR are simulated by using 180 nm and 90 nm CMOS technology parameters with a supply voltage of 1.8 V. The three techniques to realize H-DyCML gates are considered. So for the sake of fair comparison all the gates are designed to operate with a voltage swing greater than the threshold voltage of the transistor. A voltage swing of 700 mV is chosen. The other simulation settings are $C_{\text{OUT}} = 40$ fF, $f_{\text{CLK}} = 333$ MHz. The values of performance parameters such as power, delay, and power-delay product are noted and are summarized in Tables 1–5. The theoretical value of power consumption in H-DyCML gate is computed using (2) which is found to be 16.78 μW and is very close to the values reported in Tables 1–5.

It may be noted in Tables 1 and 2 that the maximum delay reduction of 37.87% is observed for the proposed H-DyCML gates in comparison to the existing DyCML gates. Analogously, the H-DyCML two-input and three-input XOR gates show a delay reduction of 48.23% and 49.4%, respectively, as compared to existing DyCML XOR gate counterparts.

To include design choices as per the suggestion, the performance of the proposed H-DyCML gates is investigated through simulations for different voltage swing and aspect

Table 1: Performance comparison of the existing DyCML and the proposed H-DyCML AND gate.

Parameter	Style				
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)		H-DyCML (Technique 3)
			PMOS	NMOS	
Technology node 180 nm					
Delay (ps)	192.31	176.01	167.92	162.13	180.54
Power (μW)	20.31	15.57	15.58	15.02	15.58
PDP (fJ)	3.90	2.69	2.61	2.43	2.81
Technology node 90 nm					
Delay (ps)	180	156	129	164	168
Power (μW)	14.2	13.36	13.1	13.9	13.4
PDP (fJ)	2.55	2.08	1.68	2.27	2.25

Table 2: Performance comparison of the existing DyCML and the proposed H-DyCML OR gate.

Parameter	Style				
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)		H-DyCML (Technique 3)
			PMOS	NMOS	
Technology node 180 nm					
Delay (ps)	236.24	172.28	162.12	219.03	170.25
Power (μW)	32.11	13.762	13.83	13.88	13.94
PDP (fJ)	7.58	2.37	2.24	3.04	2.37
Technology node 90 nm					
Delay (ps)	180	156	129	164	168
Power (μW)	14.2	13.36	13.1	13.9	13.4
PDP (fJ)	2.55	2.08	1.68	2.27	2.25

Table 3: Performance comparison of the existing DyCML and the proposed H-DyCML 2-input XOR gate.

Parameter	Style				
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)		H-DyCML (Technique 3)
			PMOS	NMOS	
Technology node 180 nm					
Delay (ps)	237.93	160.63	160.00	171.31	158.33
Power (μW)	29.28	14.84	14.84	13.23	15.20
PDP (fJ)	6.96	2.37	2.37	2.26	2.4
Technology node 90 nm					
Delay (ps)	201	143	140	145	147
Power (μW)	24	14.8	14.8	14.91	13
PDP (fJ)	4.84	2.11	2.07	2.16	1.91

Table 4: Performance comparison of the existing DyCML and the proposed H-DyCML 3-input XOR gate with two levels of source-coupled transistors in the PDN.

Parameter	Style				
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)		H-DyCML (Technique 3)
			PMOS	NMOS	
Technology node 180 nm					
Delay (ps)	326.39	211.02	180.00	191.31	199.05
Power (μW)	26.54	14.84	14.84	13.23	12.32
PDP (fJ)	8.66	7.35	5.56	5.69	6.37
Technology node 90 nm					
Delay (ps)	226	175	163	169	190
Power (μW)	23	16.2	16.8	18.4	16.7
PDP (fJ)	5.2	2.83	2.73	3.1	3.17

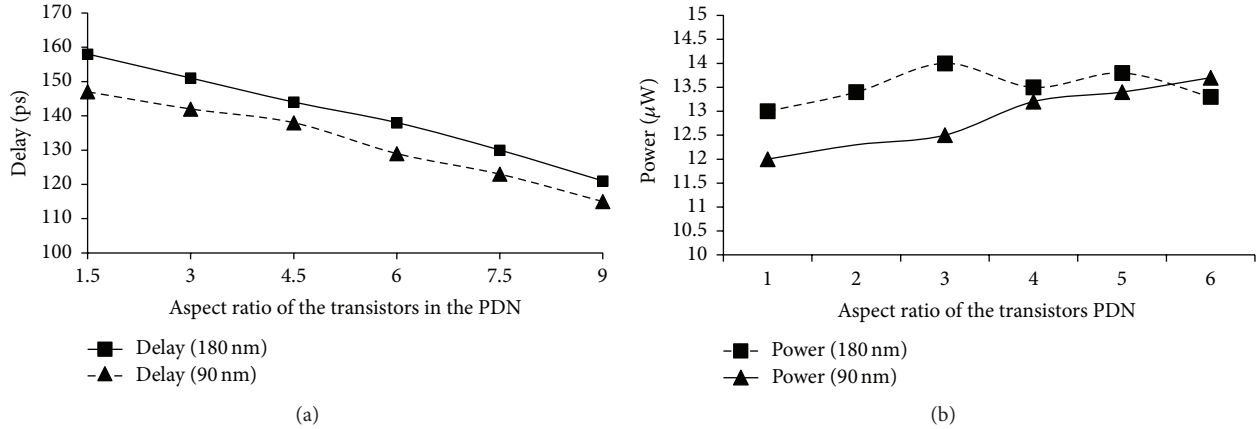

Figure 9: Performance of the two-input H-DyCML XOR gate by varying the aspect ratio of the transistors in the PDN: (a) delay results; (b) power results.

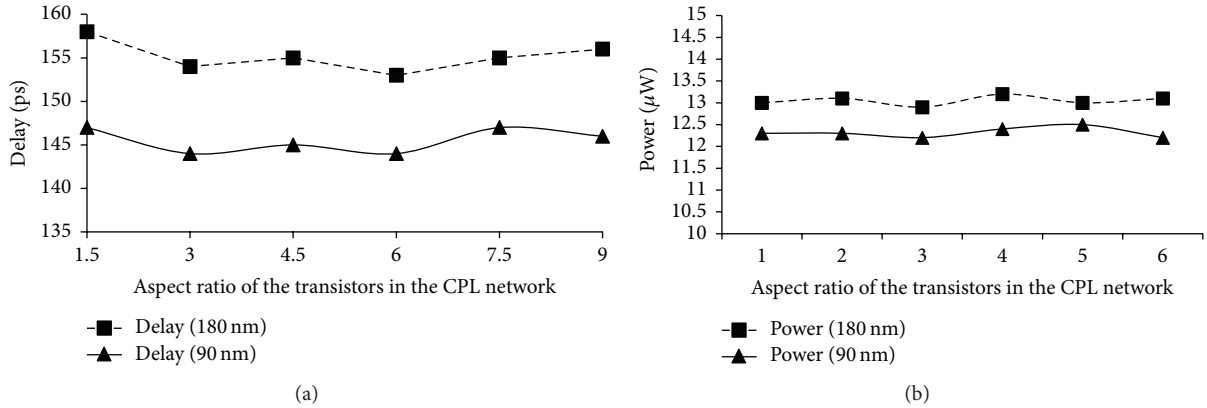

Figure 10: Performance of two-input H-DyCML XOR gate by varying the aspect ratio of the transistors in the CPL network: (a) delay results; (b) power results.

Table 5: Performance comparison of the existing DyCML and the proposed H-DyCML 3-input XOR gate with single level of source-coupled transistors in the PDN.

Parameter	Style				
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)		H-DyCML (Technique 3)
			PMOS	NMOS	
Technology node 180 nm					
Delay (ps)	326.39	166	170	187	193
Power (μW)	26.54	18	17.5	19	17.6
PDP (fJ)	8.66	2.9	2.9	3.5	3.3
Technology node 90 nm					
Delay (ps)	226	125	141	176	187
Power (μW)	23	16.2	16.8	18.4	16.7
PDP (fJ)	5.2	2.0	2.3	3.2	3.1

ratio values. The results have been summarized for a two-input XOR gate based on technique 3 in Figures 8–10. Following are the observations:

(i) In Figure 8, the power consumption increases with the increase in voltage which is supported with the theoretical formulations discussed in Section 4. Also, an increase in voltage swing requires more charge to be transferred from the output load capacitance making a corresponding increase in the delay as indicated in Figure 8.

(ii) Figure 9 shows the dependence of the delay on the aspect ratios of the transistors in the PDN network. There is a decreasing trend in delay with aspect ratio increase. To explain this, the transistors in the PDN

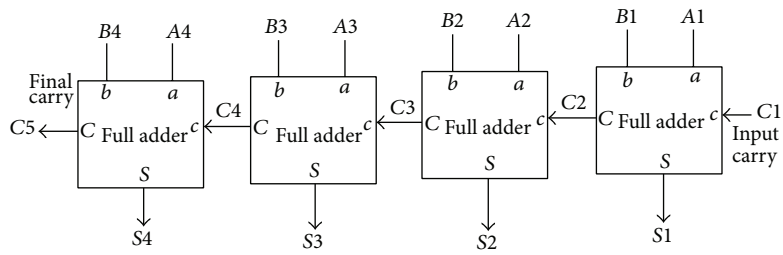

Figure 11: Block diagram of a 4-bit RCA.

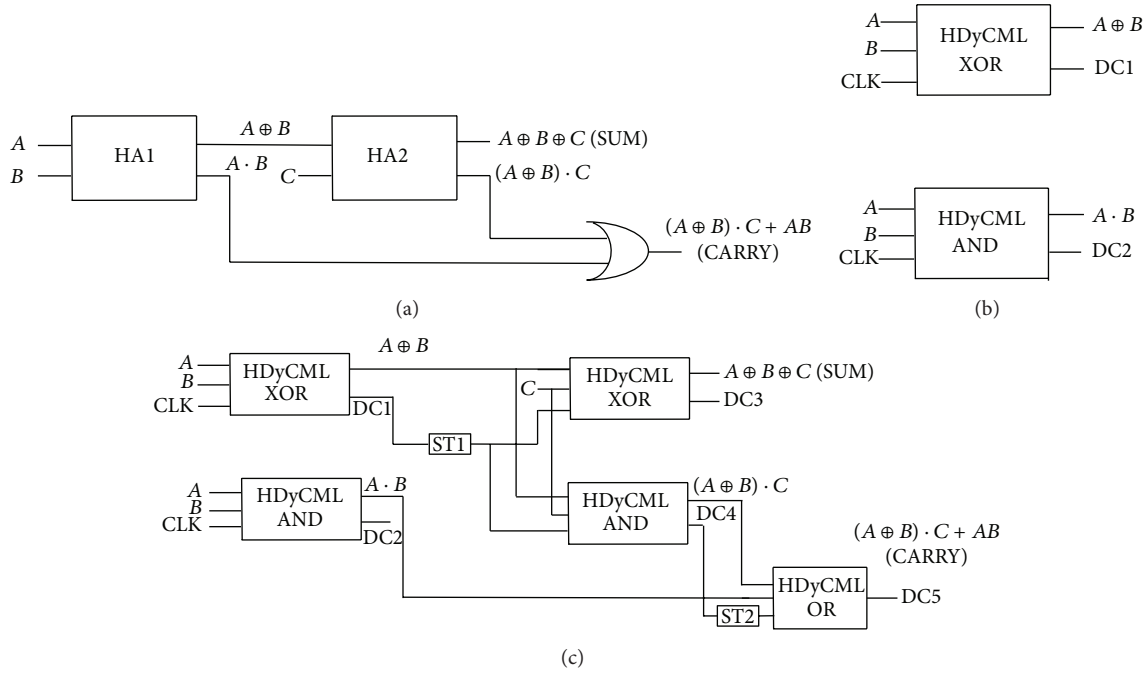

Figure 12: (a) Full adder schematic; (b) H-DyCML half adder schematic; (c) complete schematic of D-HyCML full adder.

can be viewed as resistor. When aspect ratios of transistors in PDN are increased it results in smaller resistance and lower delay values.

(iii) Lastly, the power and the delay of the proposed H-DyCML gate remain almost constant for different values of aspect ratio of the transistors in the CPL network (Figure 10). This is due to the fact that the changes in the CPL network occur in the precharge phase which has no effect in determining the performance of the H-DyCML gate.

In order to present an application of the proposed style, a 4-bit RCA (Figure 11) implementation is considered. The implementation requires cascading of four full adder (FA) circuits wherein the full adder is realized by cascading two half adders (HA) and an OR gate as shown in Figure 12(a). The realization of half adder uses the schematic in Figure 12(b) and its H-DyCML realization is placed in Figure 12(c). The signals DCi ($i = 1, 2$) represent voltage across capacitor C_1 of H-DyCML XOR and AND gates. In dynamic CML style, the direct cascading of various gates is not possible [16]; therefore self-timed buffers (STs) [16] are placed intermittently. The operation of ST is to trigger the evaluation process in subsequent stages upon receiving a completion signal from preceding stage via DC1.

The performance parameters such as power, delay, and PDP are noted for the 4-bit RCA using different techniques and are noted in Table 6. It may be noted that the delay is almost the same for all the proposed topologies which may be attributed to the same number of total cascaded stages used for realization. Further, there is significant reduction in delay and power consumption in comparison to the existing DyCML style. The delay reduces by 63.43% in the proposed H-DyCML based design in comparison to existing DyCML RCA design.

6. Conclusion

In this paper, a new hybrid dynamic current mode logic (H-DyCML) is presented as an alternative to the existing DyCML style. The use of complementary pass transistors in logic function realization is proposed in H-DyCML style. This is done to reduce source-coupled transistor pair levels

Table 6: Performance comparison of the existing DyCML and the proposed H-DyCML 4-bit RCA.

Parameter	Style			
	DyCML	H-DyCML (Technique 1)	H-DyCML (Technique 2)	H-DyCML (Technique 3)
Delay (ps)	967.74	339.57	326.39	357.08
Power (μW)	250.88	130.362	129.52	131.11
PDP (fJ)	242.78	44.354	42.27	46.82

in the PDN of the gate which results in an improvement of delay of the gate. Different gates in H-DyCML style are implemented and simulations are performed to compare their performance with the existing DyCML gates. The TSMC 180 nm and 90 nm CMOS technology parameters are used. The issues related to the compatibility of the complementary pass transistor logic with CML gates are identified and appropriate solutions have been proposed. An application example is also taken to demonstrate the benefit of employing proposed H-DyCML gates over the existing DyCML gates. A maximum improvement of 63.43% was observed in delay by employing proposed H-DyCML gates. Hence, it is confirmed that the proposed H-DyCML gates offer significant speed advantage over the existing DyCML gates.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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