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Research Article

Design and Analysis of Front Side Modular Multilevel Converter for Smart Transformer in 15 kV Arba Minch Distribution Network Using Diverse Controllers and Multicarrier Modulation

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This paper presents design and analysis of a bidirectional medium voltage (MV) front-side converter of smart transformer (ST) for Arba Minch Town distribution system. A modular multilevel converter (MMC) configuration is used in the MV side of the ST. The grid side MV is 15 kV RMS line value and the desired MVDC voltage is 24.5 kV for ensuring bidirectional operation of the converter in the time of grid outage. A half bridge semiconductor power module is used to model the front-side MMC. Based on the MV DC voltage requirement, the number of submodules per phase leg is designed to be four (four in the upper arm and four in the lower arm). Multicarrier modulation techniques such as phase-shifted PWM and level-shifted PWM are used to generate gate signals. The model is developed in MATLAB/Simulink, and its performance with respect to input side voltage harmonics, current harmonics, and output DC voltage value has been tested by carrying out several case studies under different controllers such as proportional integrator(PI), fuzzy inference system (FIS), and adaptive neuro fuzzy inference system (ANFIS) for obtaining reference signal for modulation. Level-shifted PWM is used with PI, FIS, and ANFIS, whereas phase-shifted PWM with a technique of introducing DC bias is used with PI controller alone. From the simulation results, it has been observed that better power system current quality of FS-MMC is obtained for PS-PWM (2.16%) than level-shifted PWM (5.22%). Use of FIS and ANFIS with level shift PWM method slightly brings down the current THD values to 2.98% and 2.72%, respectively (decrease by 2.5%). Also, a maximum output DC voltage of 24650 V is obtained for ANFIS with level shift PWM as compared to values obtained by PI with level shift PWM and PI with phase shift PWM.

1. Introduction

Power electronics-interfaced resources (such as distributed generators and electric vehicle charging stations) can be more widely used in modern electricity distribution grids by using a solid-state transformer-based smart transformer (ST). Due to the fact that smart transformer (ST) being a new and effective mode of infrastructure for electricity grid evolution, this paper presents the ST's basic architecture and typical control schemes in systematic detail and the advanced services that ST can provide to improve the performance of electricity grids in terms of controlling power flow, improving power quality, active damping, and actively contributing to improved distribution [1]. Conventional power distribution systems would be incomplete without classical transformer which was invented by Zipenowsky and his colleagues in 1885 [2]. On the other hand, in 1888, Tesla proposed the use of transformers in an electrical distribution network [3]. Classical transformers play roles of interconnecting the high-voltage and low-voltage grids (galvanic isolation), regulating voltages, and providing the required voltage ratio to allow energy

exchange between the two grids. Although the classical transformer is efficient and reliable, it has many gaps in fulfilling the additional requirements in modern power distribution systems in which many distributed generations are integrated [4, 5]. These gaps are as follows:

(i) The design is characterized by bulky size and weight.
(ii) Environmental concerns happen when leaks of mineral oil occur.
(iii) Voltage drop under loading condition.
(iv) Inability to mitigate flicker.
(v) Sensitivity to harmonics.
(vi) Limited performance under DC-offset load unbalances.
(vii) Inability to convert single-phase service to three-phase for powering certain types of equipment.
(viii) No energy-storage capacity (inability to interface distributed generation sources).
(ix) Propagation of unwanted voltage characteristics (e.g., voltage sags and fault occurrence) from HV grid to LV grid and vice versa.
(x) Losses in classical transformers are relatively high at the average load level: transformers exhibit their maximum efficiency at their nominal load, while distribution transformer average load level is about 30%.

The abovementioned technical gaps of classical transformer are rectified by added features of smart transformer such as modularity, high power density, presence of multiple DC links, and power electronic converters with bidirectional power flow control [4, 5]. William McMurray first proposed the idea of a high-frequency link AC/AC power converter in 1970 [6]. However, J.L. Brooks first proposed the term "solid state transformer" (SST) for naval systems in 1980 as an alternative to the auto-transformer based on an AC/AC buck converter and AC/AC buck-boost converter [7]. There have been significant advances in the control, topologies, protective aspects, power converter topologies, and implementations of STs summarized in this review paper. An attempt is made to include some ST topologies that are not currently included within the reported classification schemes proposed in the literature by introducing a new methodology for classification of STs. This work also includes a lengthy discussion of the design and implementation of medium-frequency transformers [8].

One such technology, termed ST, is the subject of this paper. It is possible to achieve isolation and voltage conversion from one level to another with the help of power electronic devices and a high-frequency transformer in an ST. Using the ST in the distribution system has proven to be beneficial in achieving the smart grid goal. The high-frequency transformer's performance can be significantly impacted by even small changes in operating conditions, as illustrated in an example system [9]. Falcone et al. introduced a useful classification of ST architecture based on the number of power converter stages, from which the appropriate configuration can be selected for a given set of circumstances. Figure 1 shows the four basic topology principles as defined by this classification [10–13].

The three stages with dual DC link ST topology is the most recommended type for distribution system as it contains multiple ports for interfacing medium- and low-voltage DC source, allowing much degree of freedom and added functionalities. The front-side converter of three-stage ST can be a standard voltage source converter (VSC) or modular multilevel converter (MMC) of which MMC is the focus of this research work as it draws more attention because of its easy voltage scalability, modularity, and fault-tolerance functionalities.

Generation of reference phase signals to produce gate signals for converters at different stages of ST is carried out by using proper controller in respective stages of ST. The proportional integral (PI) controller is a popular control strategy used to indirectly control the power being utilized by the system by directly modifying the pulse width modulation (PWM) control signal to the gates of power electronic devices. This controller has a feedback control loop that calculates an error signal by taking the difference between the output of a system, which in this case is the output voltage at the MV DC link, and the set point. The set point is the desired voltage level (24.5 kV) at which the system would operate. Mohammad Ebrahim used a voltage-oriented control strategy having PI controller with abc to dq0 transformation and phase locked loop for the input side converter of ST. He used this control method for generating proper reference signals for modulation purpose [14]. Ansari et al. presented an extensive review of stabilization methods through band width limit and droop control for DC microgrids with constant power loads. The nonlinear characteristic of load side converter of DC microgrid, which acts as constant power loads, creates system instability. The stabilization methods, as discussed by these authors, are grouped as source side, interface, and load side stabilization techniques. Load side stabilization techniques inject power that affects the performance of a load, and hence, source side stabilization technique is more preferable, as it does not affect the load dynamics. In the review paper, it was explained that there is a definite relation between bandwidth of constant power load and system stability is established by converting a cascaded DC-DC converter into a fifth-order system. The same approach extended to modular multilevel converter (MMC) in distribution system that supplies constant power loads with limited band width showed that DC voltage control, circulating, and line current control affect source side impedance while the MMC offers good stability to the entire system [15].

The power electronic building blocks (PEBB) of MMC can be half-bridge IGBT power module or full-bridge IGBT power module. For this project work, a half-IGBT power module is selected as it contains smaller switches and hence has reduced semiconductor losses. Figure 2 shows the switch transitions of half-bridge IGBT power module.

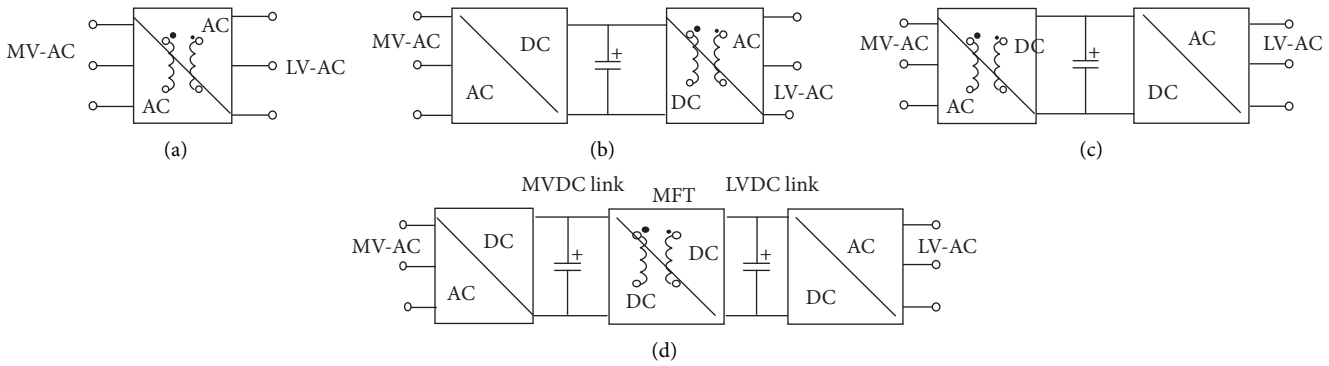

Figure 1: Basic ST topologies. (a) Single stage AC-AC, (b) two stage with MV DC link, (c) two stage with LV DC link, and (d) three stage with dual DC link.

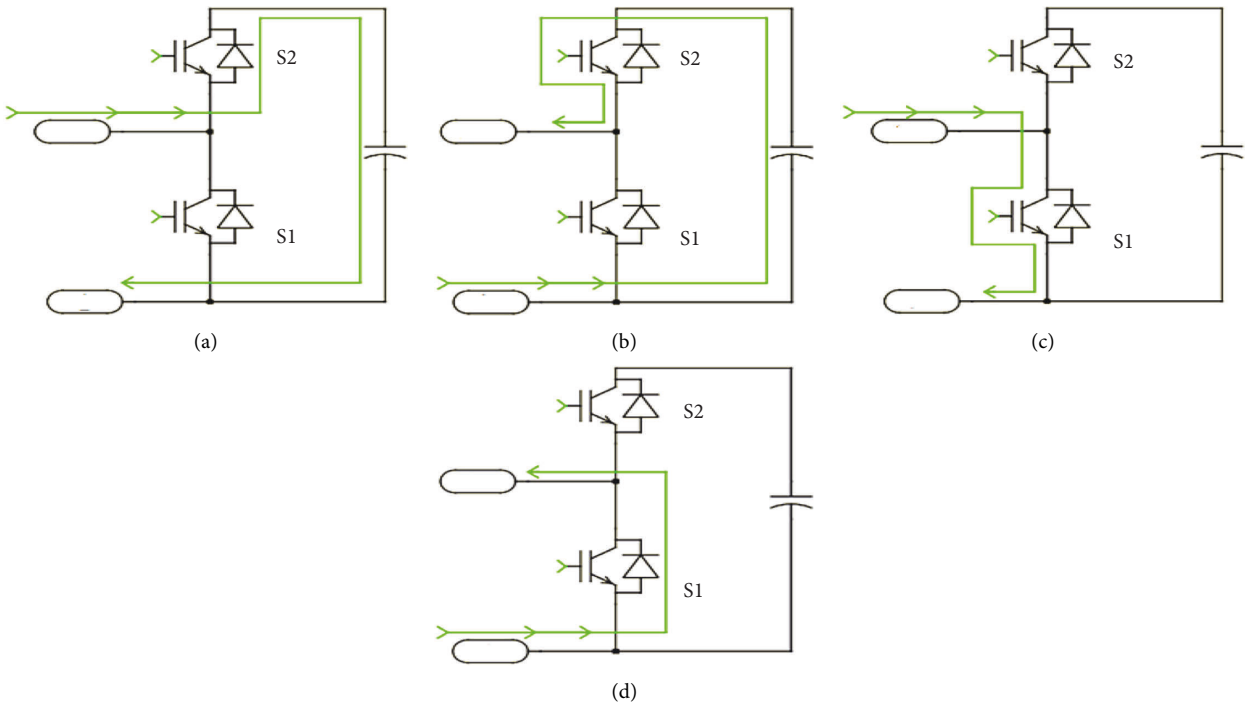

Figure 2: Different operating states of half bridge. (a) State_1, (b) State_2, (c) State_3, and (d) State_4.

1.1. Research Problem Statement. Generation of gating signals to fire semiconductor switches requires comparison of reference AC voltage signals (modulating signals) and carrier signals. Reference signals can be obtained by use of voltage and current measurement technique, abc to dq0 transformation, and PI controllers. Generating reference signals for firing power switches by use of PI controller is subject to fluctuations when the power systems enter into momentary and sustained sag and swell problems. This may cause unnecessary turn ON/OFF of power switches and may cause large current and voltage harmonics in the AC grid side. Use of intelligent controllers such as FIS and ANFIS which can be used with crisp data can replace PI and can give better voltage and current quality. In this research work, front-side modular multilevel converter (FS-MMC) is designed, modeled, and simulated with diverse controllers such as PI FIS and ANFIS and multicarrier PWM modulation techniques to evaluate the level of grid side harmonics and magnitude of DC voltage at converter output side. The rest part of the paper is structured as follows: Section 2 deals with mathematical approaches of MMC. Section 3 discusses about modeling and design of FS-MMC. Section 4 describes about simulation of system with various controllers and modulations. Section 5 deals with results and discussions followed by conclusions at the last section.

2. Mathematical Approach of MMC

An MMC generally contains N number of series connected submodules in one-phase arm, both in upper and lower arms resulting in total of $2N$ submodules in the phase leg (Figure3). Grid side inductance and resistance as well as arm

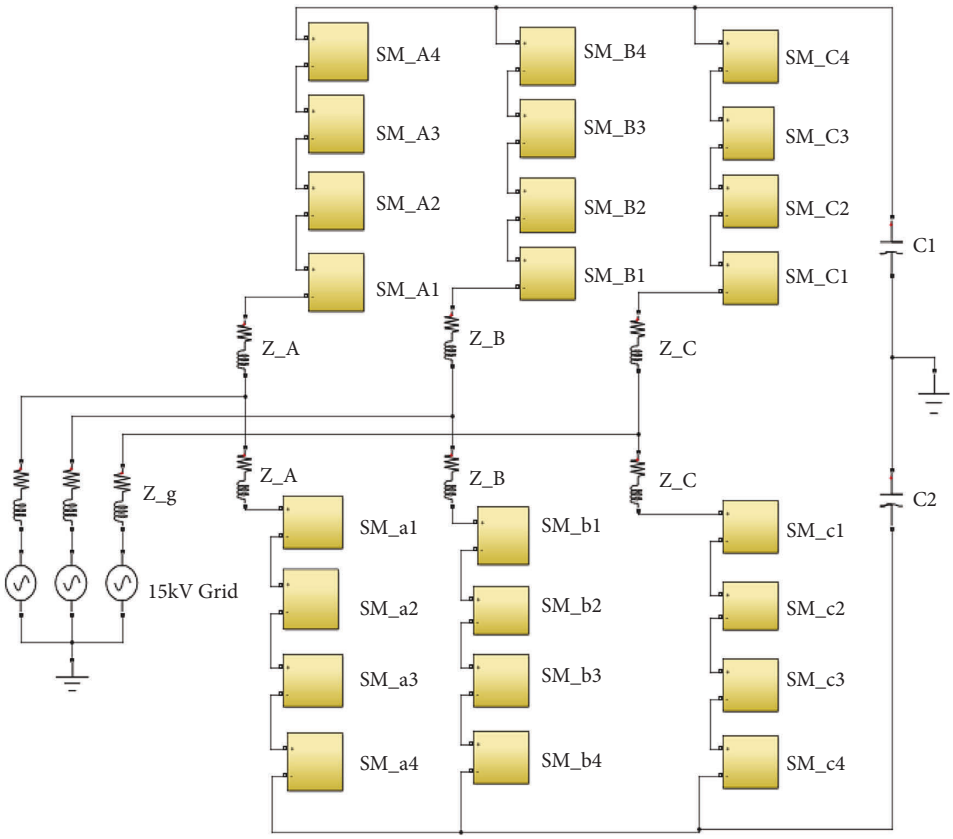

Figure 3: FS_MMC developed in MATLAB/Simulink.

inductance and resistance are used to filter out harmonics and limit phase leg current. Each phase leg works in a way that the total DC link voltage is applied across its terminals. Its equivalent circuit is shown in Figure 4.

In its basic operation, the number of submodules in the phase leg which are in ON state at one instant of time should be equal to N (number of submodules in the arm). Two independent modes of operations are possible in the analysis of phase leg of MMC. These are the common mode operation and differential mode operation as shown in Figure 5 [10].

The voltage (V) and current (I) in common mode operation and differential mode operation are given by use of KVL and KCL as follows:

$$I_{Pa} + I_{na} = I_a. \tag{1}$$

Application of KVL to the upper loop of Figure 5 gives the following voltage equation:

$$\frac{Vd}{2} - V_{mU1} - V_{mU2}V_{mUN} - L\frac{\mathrm{d}i_{pa}(t)}{\mathrm{d}t} - Ri_{pa} - V_a = 0, \tag{2}$$

where $V_{mU1}\ldots\ldots V_{mUN}$ are submodule voltages from first submodule to N^{th} submodule.

In compact form, (2) can be put as follows:

$$\frac{Vd}{2} - \sum_{j}^{N} V_{mUj} - L\frac{\mathrm{d}i_{pa}(t)}{\mathrm{d}t} - Ri_{pa} - V_a = 0. \tag{3}$$

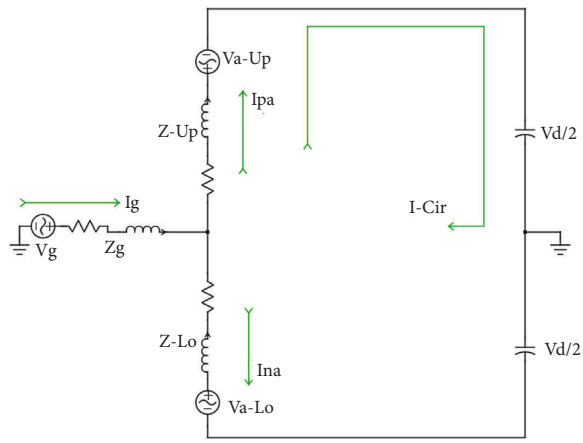

Figure 4: Equivalent circuit of phase arm of MMC.

In the same manner, application of KVL for lower loop gives the following equation:

$$\frac{Vd}{2} - \sum_{j}^{N} V_{mLj} - L\frac{\mathrm{d}i_{na}(t)}{\mathrm{d}t} - Ri_{na} - V_a = 0. \tag{4}$$

Further analysis of (3) and (4) gives the following relation among V_a, submodule voltage, and arm impedance.

$$V_a = \frac{1}{2} - \left[\sum_{j}^{N} V_{mUj} - \sum_{j}^{N} V_{mLj}\right] - \frac{1}{2}\left[L\frac{\mathrm{d}i_{na}(t)}{\mathrm{d}t} - Ri_{na}\right]. \tag{5}$$

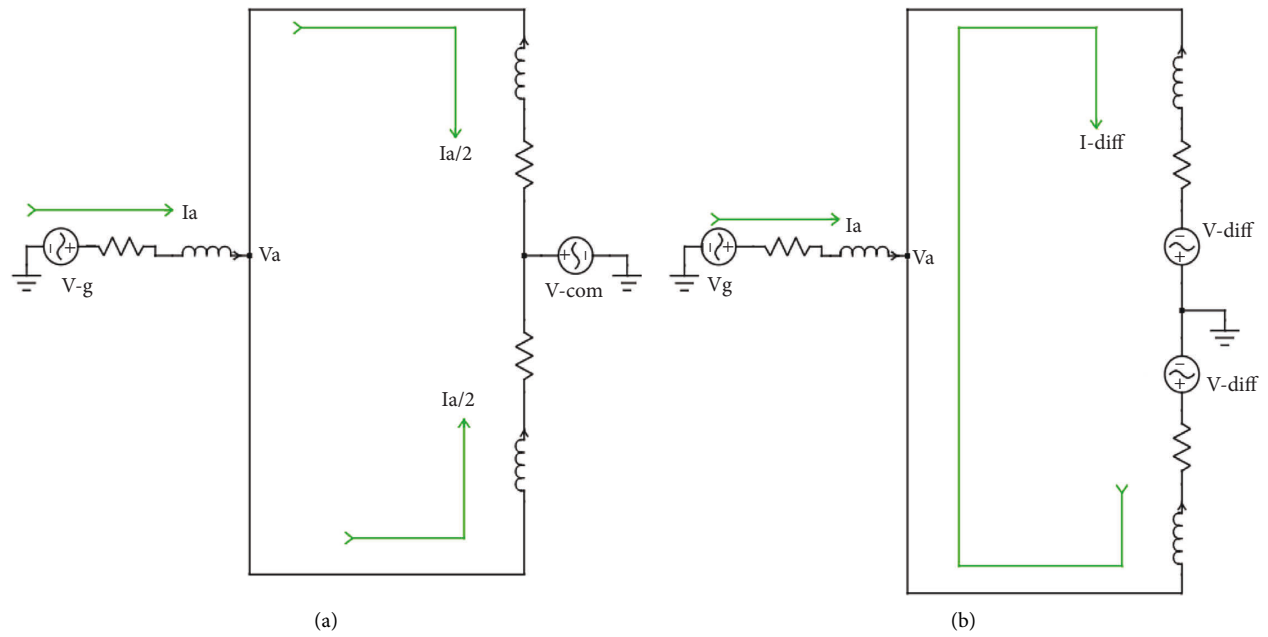

Figure 5: Modes of operation of MMC. (a) Common mode and (b) differential mode.

Inserting (1) into (5) gives the following relation:

$$V_a = \frac{1}{2} - \left[\sum_j^N V_{mUj} - \sum_j^N V_{mLj}\right] - \frac{1}{2}\left[L\frac{\mathrm{d}i_a(t)}{\mathrm{d}t} - Ri_a\right]. \quad (6)$$

Addition of (3) and (4) gives the following relation among DC link voltage, submodule voltage, and arm impedance [5]:

$$V_d - \left[\sum_j^N V_{mUj} - \sum_j^N V_{mLj}\right] = L\frac{\mathrm{d}\left(i_{pa} + i_{na}\right)(t)}{\mathrm{d}t} R\left(i_{pa} + i_{na}\right). \quad (7)$$

For normal power flow (AC grid to DC link), the sum total of upper and lower submodule voltages is greater than DC link voltage, and for reverse power flow mode, the converse is true.

The flow of circulating current (differential current) in the phase legs of MMC is unavoidable because of unbalancing of submodule voltage in the upper and lower arms. The circulating current contains both AC and DC components. The DC component is necessary for energizing the submodules, whereas the AC component needs to be minimized as it increases semiconductor losses. The expression for circulating current (i_{cir}) can be given by the following equation [7]:

$$\begin{aligned} I_{Pa} &= I_{cir} + \frac{I_a}{2}, \\ I_{na} &= I_{cir} - \frac{I_a}{2}, \\ I_{Cir} &= I_{pa} + I_{na}. \end{aligned} \quad (8)$$

To reduce the flow of differential current, submodule capacitor voltage balancing algorithm can be separately used with modulation circuits, or phase-shifted PWM that gives equal conduction time for semiconductor switches can be used.

3. Modeling and Design of Front-Side-MMC of ST

For design and modeling of MMC, the power level to be transferred, the distribution system voltage level, and DC link voltage are needed. Based on power rating of the MMC, the DC link voltage is chosen according to the standard current and voltage ratings of components. The number of submodules per arm (N) is selected based on the quality of the predicted voltage waveform. The submodule capacitance value is chosen so that it should operate at low-voltage ripple [10]. A model of front-side modular multilevel converter (FS_MMC) for interfacing 15 kV distribution system is shown in Figure 3.

As shown in Figure 3, the number of submodules per phase arm is decided by considering the voltage rating of IGBTs, grid side AC voltage, and MV DC link voltage.

As discussed in [6], the expression for MV DC voltage is given by the following equation:

$$V_{dc} \geq \frac{2\sqrt{2}VL - L}{\sqrt{3}}. \quad (9)$$

For a 15 kV AC grid system, the value of V_{dc} equals 24.5 kV. If the IGBTs blocking voltage (V_{CES}) rating is 6.5 kV and the safety factor (η) to be used is 1.1, the number of submodules per phase leg arm (N) is given by equation below:

$$N \geq \frac{V_{dc}}{\eta V_{CES}}. \quad (10)$$

Substitution of the parameter values for V_{dc}, V_{CES}, and η gives the value of number of submodules per phase leg arm to be four (4).

Phase leg arm inductance is used to filter out circulating current and limit arm current in the event of fault. Based on the maximum ripples in the circulating current, the arm

inductance can be given by the expression as discussed in References [16, 17].

$$L_{\text{arm}} \geq 0.25 \frac{U_{C,\text{MAX}}}{N f_C \Delta i_{L,\text{Max}}}, \tag{11}$$

where $U_{C,\text{Max}}$ is the maximum voltage of an SM capacitor, $\Delta i_{L,\text{Max}}$ is the maximum current ripple of the circulating current, N is the number of submodule, and f_C is the switching frequency of each SM.

Submodule capacitance (C_{SM}) as a function apparent power, power factor, average capacitor voltage, acceptable ripple, switching frequency, and modulation index and number of submodule is given as follows [16, 17]:

$$C_{SM} \geq \frac{S}{3NmV_C^2 \varepsilon \omega} \left[1 - \left(\frac{m\text{Cos}\varphi}{2}\right)^2\right]^{2/3}. \tag{12}$$

By assumption of purely sinusoidal arm current and balanced submodule capacitor voltage, reference [18] expresses submodule capacitance as a function of energy difference stored (ΔW_{SM}) over one cycle for acceptable ripple (ε) as follows:

$$C \geq \frac{\Delta W_{SM}}{2\varepsilon V_{C,av}^2}, \tag{13}$$

where $V_{C,av}$ is the average submodule capacitor voltage given by (Vd/N) and ε is the voltage ripple.

4. Simulation with Controllers and Modulations

Table 1 listed the distribution system, converter, and controller parameters. These essential values were used in the Simulink modeling to build the system.

4.1. PI Controller with Level-Shifted PWM. The AC grid side current and voltage wave forms are shown in Figure 6. The total harmonic distortion (THD) of current and voltage for level-shifted modulation technique with PI controller are 5.22 percent and 0.01 percent, respectively, as shown in Figures 7 and 8 in the result section under "A." The RMS voltage is 24170 volts, while the MV DC voltage is 24470 volts. Ripple values can reach a maximum of 1.2%. The DC link voltage rises to its maximum value in less than 0.5 seconds, as shown in Figure 9.

4.2. Result with PI Controller and Phase-Shifted PWM. The wave forms of grid side current and voltage are shown in Figure 10. Current and voltage THD for phase-shifted modulation with PI controller are 2.16 percent and 0.01 percent, respectively, as shown in Figures 11 and 12 in the result section under "B." It is indicated in Figure 13, that the maximum MV DC voltage obtained is 24530 V and its RMS value is 24300 V with a ripple of 0.9%. It is also shown that the rise time to reach maximum DC link voltage is less than 0.2 sec.

4.3. Result with Fuzzy Logic and ANFIS Controller for Level-Shifted PWM. In the generation of the reference voltage signal for generation of gate signals, a fuzzy logic controller can replace a classical PI controller. The classical PI controller is being replaced by a fuzzy logic control with two inputs and one output in this work. The error signal (E) and the change in error signal (CE) between the reference DC voltage and the measured DC voltage are two of the two inputs to the system. When the signal is processed, it generates the desired DC voltage. On the basis of the variable value limit, seven membership functions (MSF) have been developed as big positive (BP), medium positive (MP), small positive (SP), zero (ZE), small negative (SN), medium negative (MN), and big negative (BN). Adaptive-neuro fuzzy inference system (ANFIS) is hybrid of artificial neural network (ANN) and fuzzy logic control, which can better yield a good control response. A one input-one output with seven rules and five layers based ANFIS is used to replace PI in this project. The proposed controller employs the Sugeno fuzzy model with five layers. The first layer (Layer 1) is in charge of mapping the input variable relative to every membership function (MF). It is also in charge of effectively conveying the external crisp signal to the other layers. It has adaptive nodes.

The second layer (Layer 2) either performs the fuzzification process or receives crisp inputs and determines which inputs belong to the fuzzy set's neuron (i). The third hidden layer is a fuzzy rule layer that normalizes the previous layer. The fourth layer is normalization layer used to calculate a normalized firing strength of rules. The last fifth layer performs defuzzification process to produce global output through summation of all inputs that comes to this layer. A hybrid learning rule with 100 iterations and Gaussian membership function are used. The basic ANFIS architecture is given in Figure 14.

To get the output variable value, the input variables are combined in an AND logical operation. A one input-one output with seven rules based ANFIS is used to replace PI in this research work. A Gaussian membership functions are used for input variables, and triangular functions are used for output variable. The required data to design fuzzy inference system (FIS) and adaptive neuro-fuzzy inference system (ANFIS) is obtained from PI controller. The error signal between the desired DC link voltage and the actual DC voltage (e) is fuzzified by big negative (BN), medium negative (MN), small negative (SN), zero (ZE), small positive (SP), medium positive (MP), and big positive as shown in first row in Figure 15. In the same way, the changes in error signal (Δe) are given by BP, MP, SP, ZE, SN, MP, and BP in the first column of Figure 15.

The Arba Minch Town distribution system's smart transformer (ST) front-side converter is a model in this paper. According to this modeling, various modulation/control techniques like FIS/PI/ANFIS have been tested. Table 2 shows the overall effectiveness of the work. ANFIS with the level-shifted PWM has shown better performance than with PI with level shift PWM techniques. The ANFIS

Table 1: Specification of the system.

Parameter	Value
AC grid line voltage (Vg)	15 kV
Grid side inductance (Lg)	10 μH
Grid side resistance (R_g)	0.01 Ω
Submodule arm inductance (L_arm)	12 mH
Submodule arm resistance (R_arm)	0.1 Ω
Submodule arm capacitance ($C_{\_SM}$)	0.1 mF
DC link capacitance ($C_{\_DC\ Link}$)	10 mF
Grid frequency (f_g)	50 Hz
Converter switching frequency (fc)	4 kHz
Converter maximum capacity (S)	50 kVA
No of submodule (SM)	4
PI controller parameters	
Proportional gain (KP)	0.01
Integral gain (KI)	0.00023

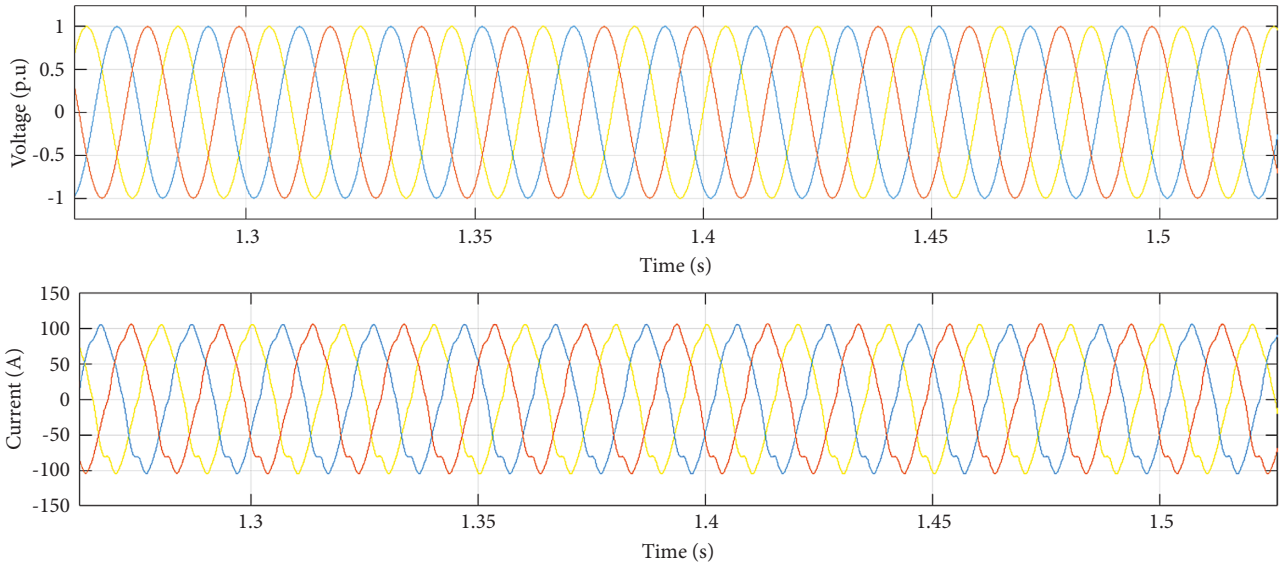

Figure 6: Grid side voltage and current wave forms for PI with level-shifted PWM.

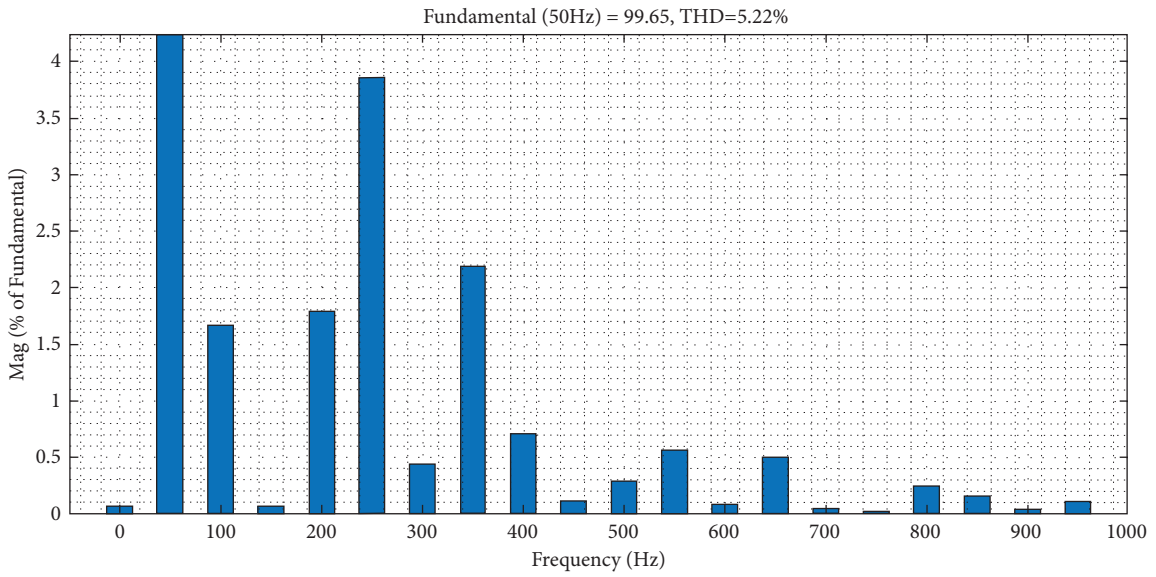

Figure 7: Current THD of AC grid side for PI with level-shifted PWM.

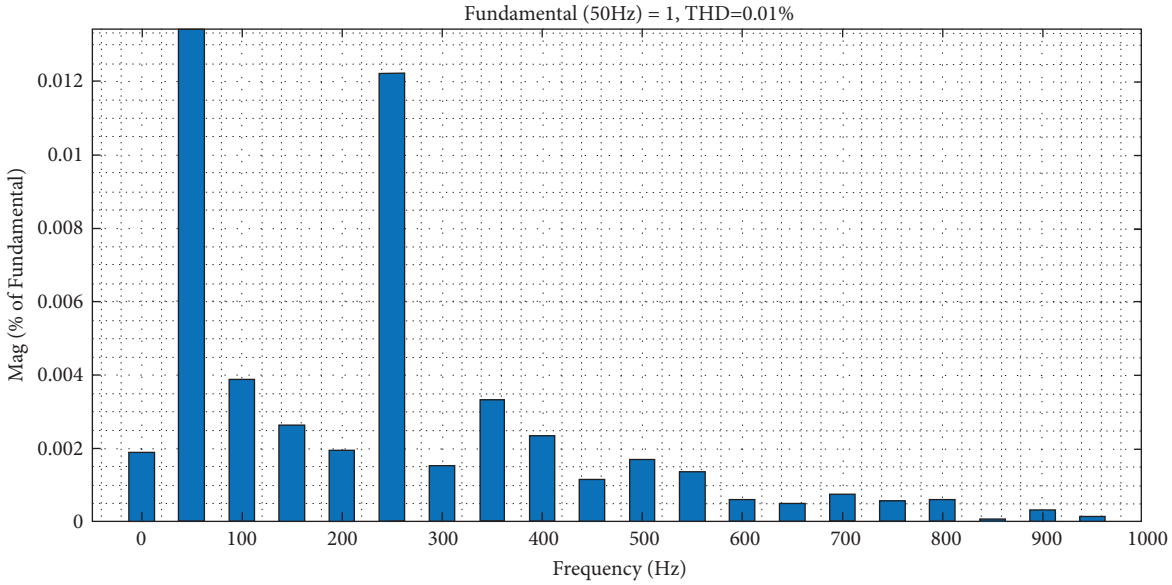

Figure 8: Voltage THD of AC grid side for PI with level-shifted PWM.

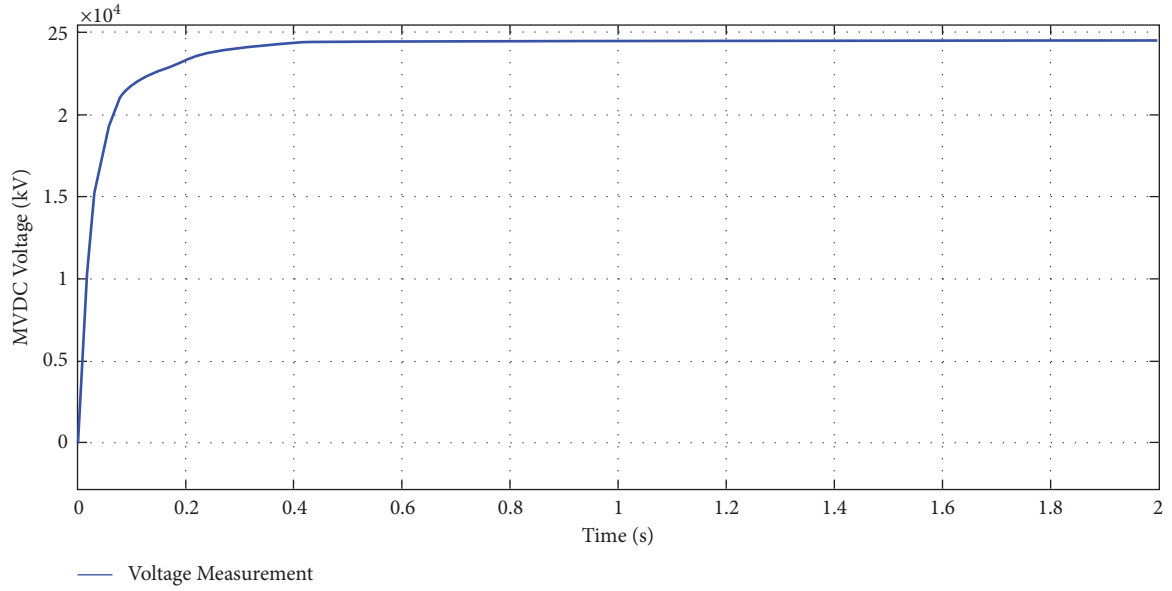

Figure 9: DC link voltage for PI with level-shifted PWM.

current and voltage THD were 2.78% and 0.01%, respectively, at the time of this observation. The rise time is less than 0.3 seconds, and the ripple at level-shifted ANFIS is about 1.3 percent. The overall performance of the analysis for MVDC link voltage is illustrated in Figure 16. The voltage THD value has been within acceptable limit for all controllers and it was around 0.01% as shown in Figure 17. Results in Figures 18 and 19 show that ANFIS with level shift PWM gives a better THD value of current than its FIS counterpart.

5. Results and Discussions

Overall performance comparisons of controllers and modulation techniques were explored in Figure 20. The ANFIS with level-shifted had shown outstanding current quality over other techniques (THDi = 2.78%). Table 2 illustrates ripple values, medium voltage (MV) value, current, and voltage THD of the controllers. The maximum DC voltage obtained in the work was 24650 V. The rise time of the techniques had been almost similar in the

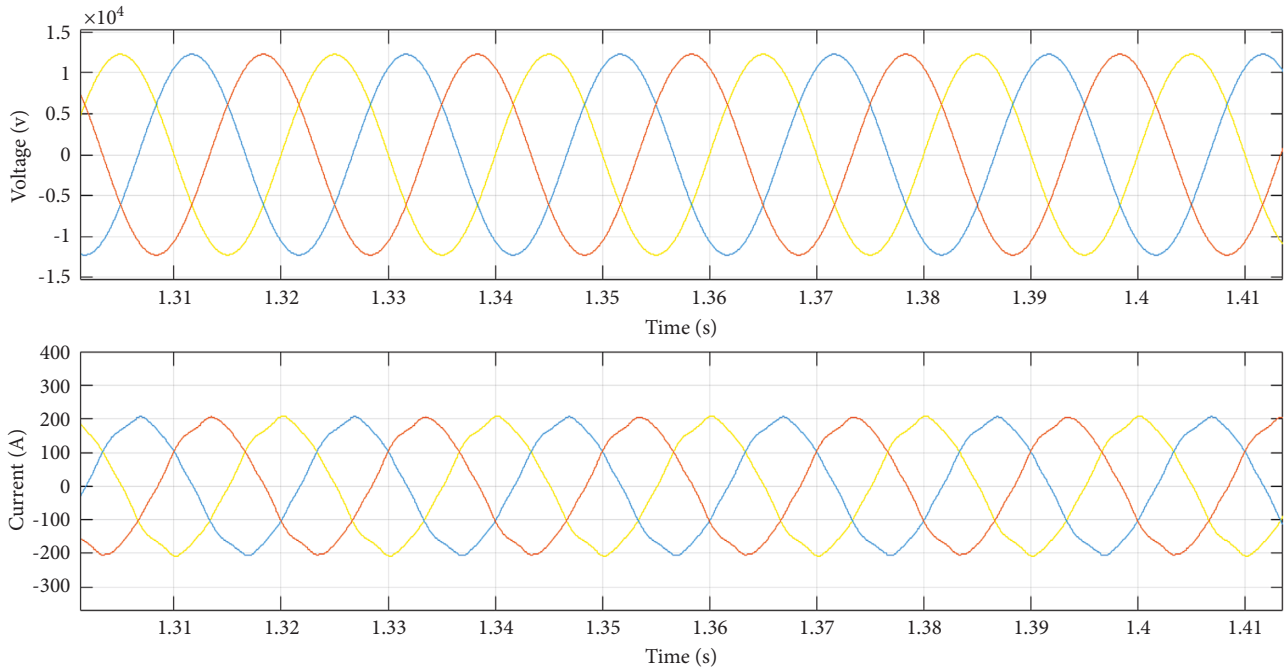

Figure 10: Grid side voltage and current wave form for PI with phase shifted technique.

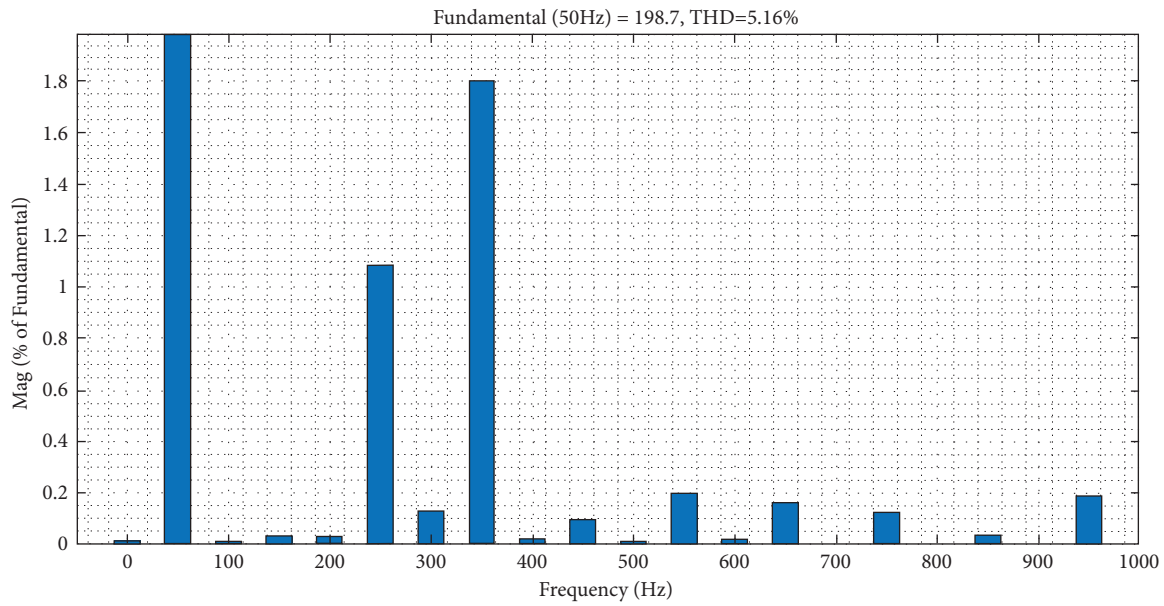

Figure 11: THD for grid side current for PI with phase-shifted technique.

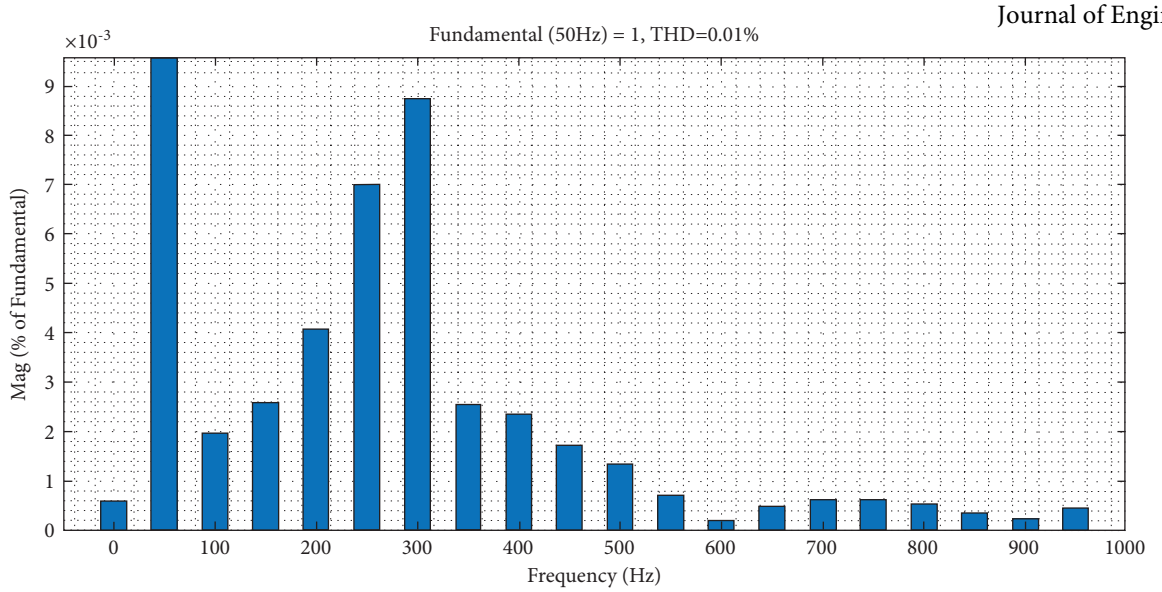

Figure 12: THD for grid side voltage for phase-shifted with PI.

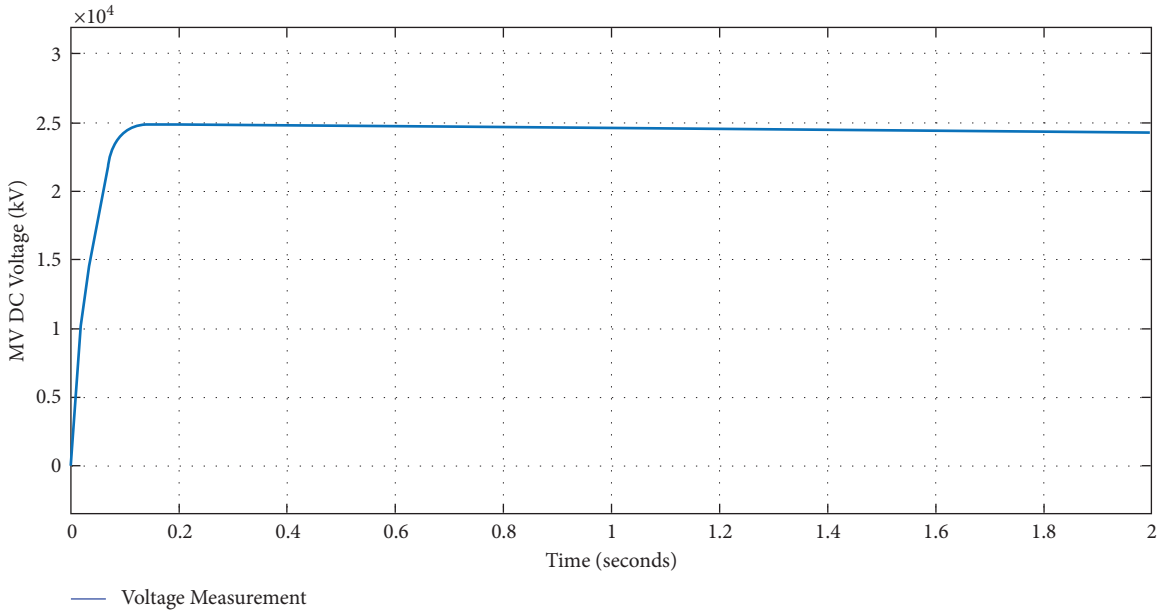

Figure 13: MV DC link voltage wave for PI with phase shift PWM.

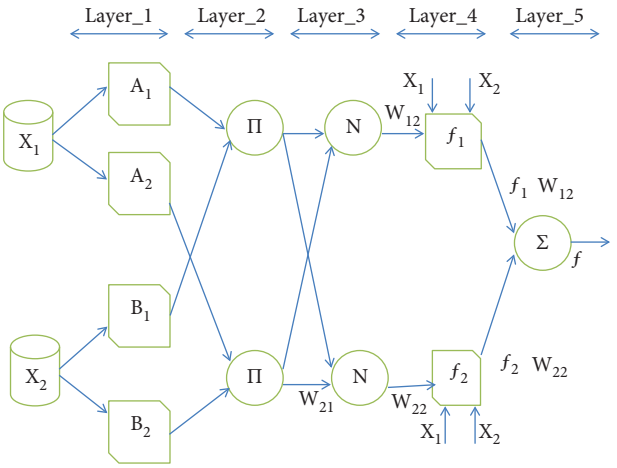

Figure 14: Basic ANFIS architecture.

		⟵ e ⟶						
		BN	MN	SM	ZE	SP	MP	BP
↑ Δe ↓	BP	ZE	SP	MP	BP	BP	BP	BP
	MP	SN	ZE	SP	MP	BP	BP	BP
	SP	MN	SN	ZE	SP	MP	BP	BP
	ZE	BN	MN	SN	ZE	SP	MP	BP
	SN	BN	BN	MN	SN	ZE	SP	MP
	MN	BN	BN	BN	MN	SN	ZE	SP
	BN	BN	BN	BN	BN	MN	SP	ZE

Figure 15: Membership function of ANFIS.

Table 2: Performance comparison of PI, FIS, and ANFIS.

Performance comparison parameter		Modulation and controller			
		PI with level shift	PI with phase shift	FIS with level shift	ANFIS with level shift
THD (current)		5.22%	2.16%	2.92%	2.78%
THD (voltage)		0.01%	0.011%	0.01%	0.01%
MV DC voltage	Ripple	1.2%	0.9%	1.3%	1.3%
	Rise time	<0.3 sec	<0.2 sec	<0.3 sec	<0.3 sec
	Max DC voltage	24470 V	24530 V	24640 V	24650 V

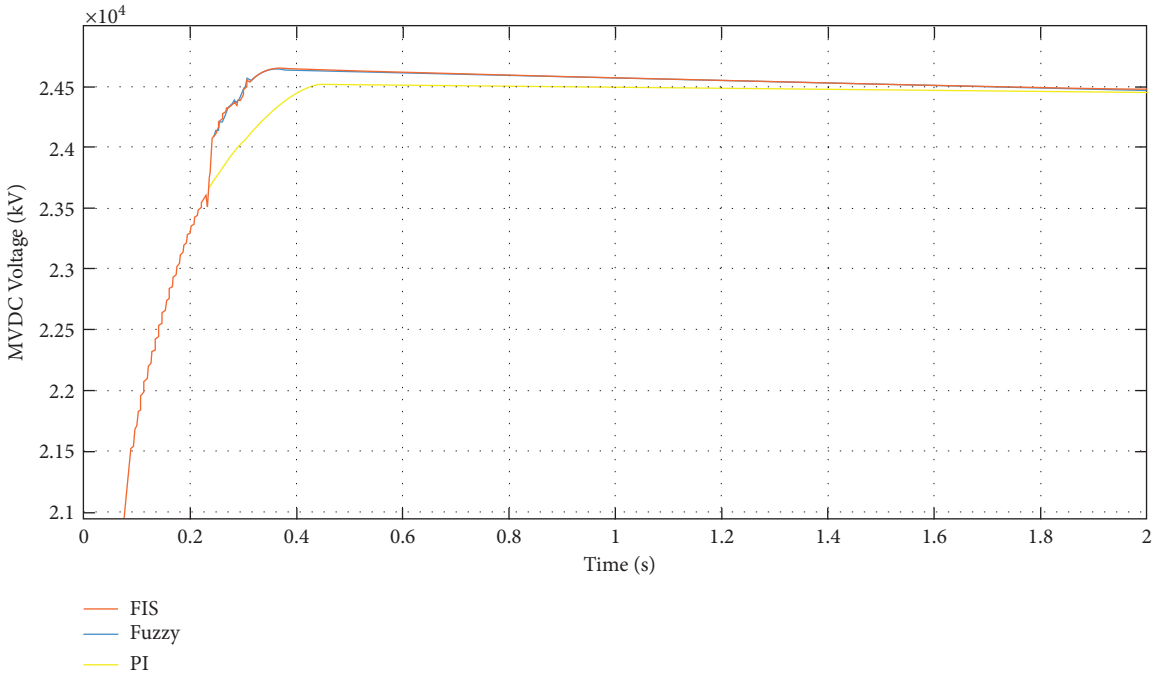

Figure 16: MV DC voltage of FS-MMC with different controllers.

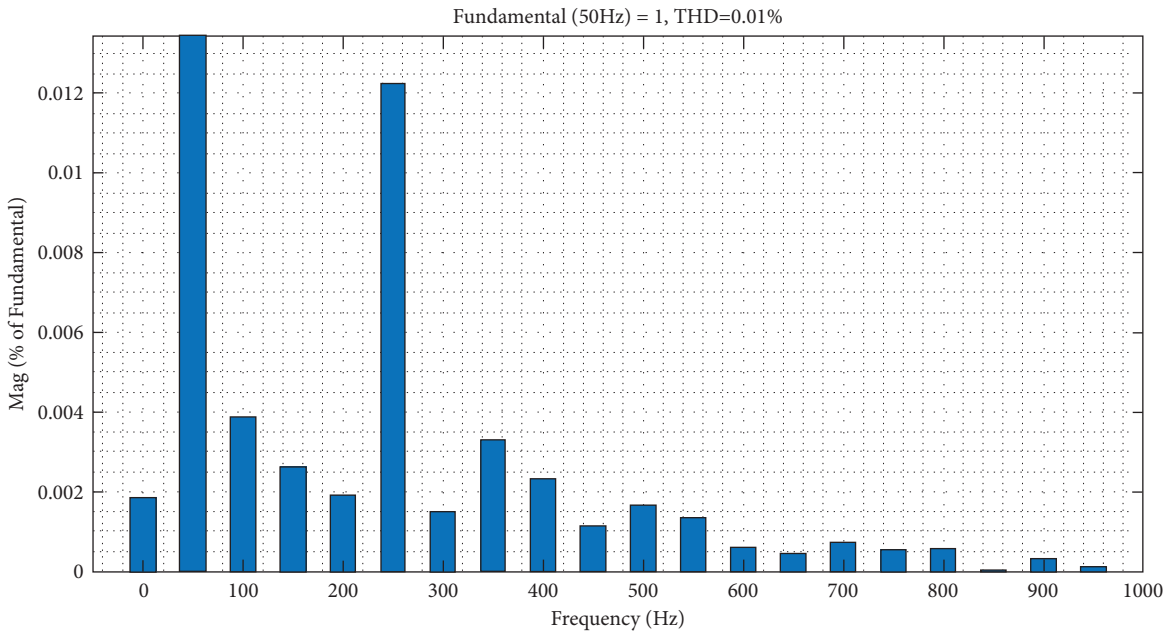

Figure 17: THD (voltage) for FIS and ANFIS with level shift PWM.

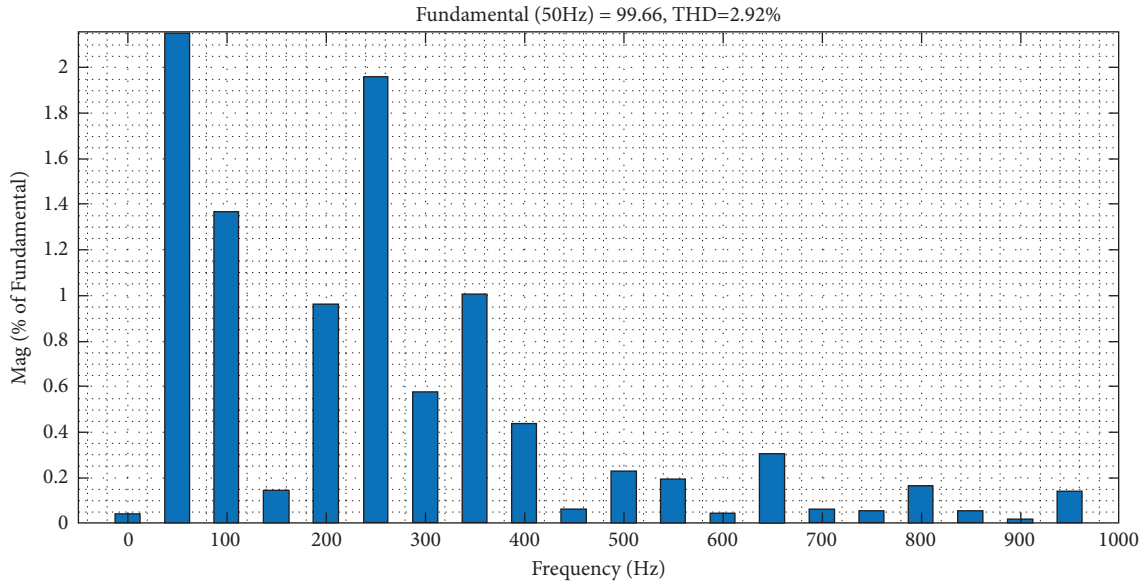

Figure 18: THD (current) for FIS with level shift PWM.

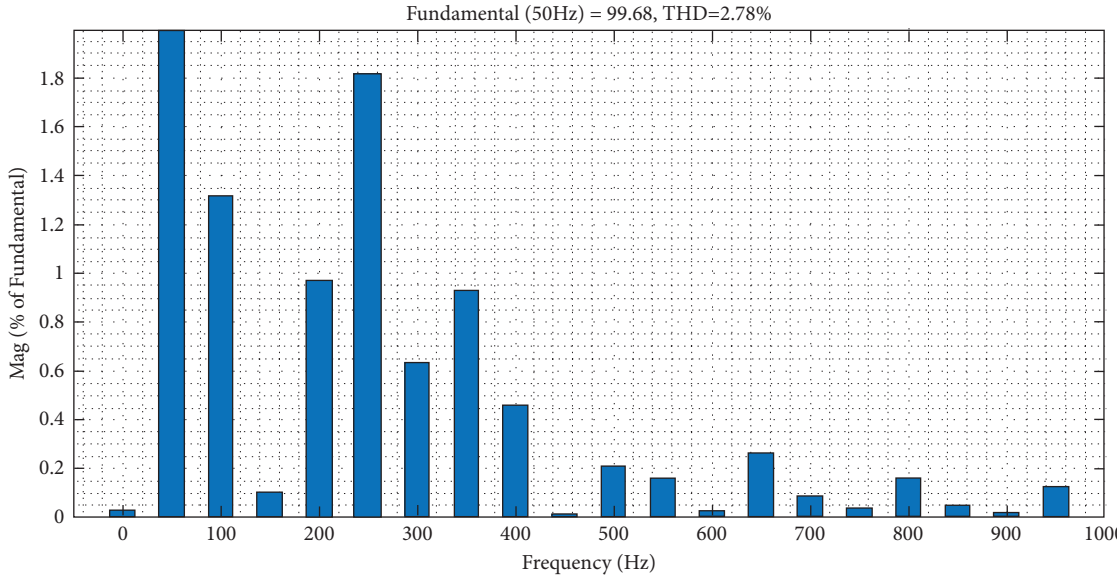

Figure 19: THD (current) for ANFIS with level shift PWM.

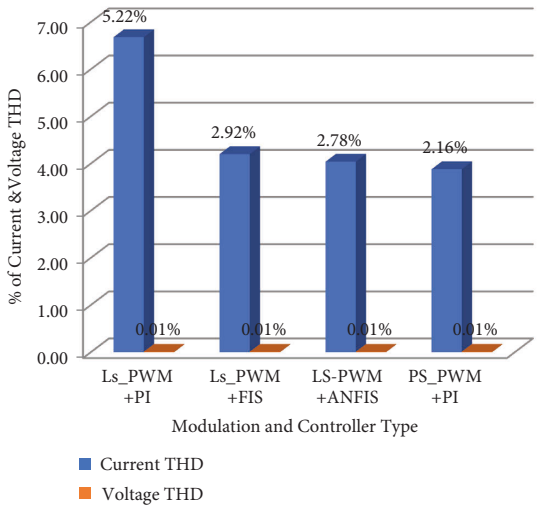

Figure 20: Overall current and voltage THD of controllers with modulations.

results. The ANFIS with level shift has ripple values less than 1.3%.

6. Conclusion

A three-phase modular multilevel front-side converter (FS_MMC) for smart transformer to link 15 kV Arba Minch Town distribution system is designed and analyzed in this paper. The power electronic building block (PEBB) used to model the converter is half-bridge power module of insulated gate bipolar transistors (IGBTs). The required number of submodules used in the system is four (4) taking into consideration the voltage rating of semiconductor switch to be 6.5 kV. Level-shifted PWM with PI, FIS, and ANFIS controllers is used in MATLAB/Simulink simulation platform for comparative performance analysis of voltage and current quality at grid side and DC voltage at output side. PI controller with phase-shifted PWM having DC bias injection to reference signal is used to see the changes in the performance condition of converter in the case of PI with level shift PWM. As shown in Figure 11, PI controller with phase-shifted PWM method gives a better current THD (2.16%) than PI with level-shifted PWM (5.22%).

The THD for grid side voltage for level-shifted PWM is 0.01% and for phase-shifted PWM is also 0.01%, both are within the acceptable limit. Fuzzy inference system (FIS) and adaptive-neuro fuzzy inference system (ANFIS) are used to replace the classical PI controller with level-shifted PWM to see their impact in improving system performance. It was seen from simulation result that the use of FIS and ANFIS with level shift PWM slightly reduces grid side current THD values from 5.22% to 2.92% and 2.783%, respectively. For system performance regarding the DC link output voltage, ANFIS with LS-PWM yields a maximum value of 24650 V, while FIS with LS-PWM yields a value of 24540 V. PI with phase shift yields a maximum DC output value of 24530 V and PI with LS-PWM with yields DC output voltage of 24470 V with respect to reference value of 24.5 kV [19].

Acronyms

ANFIS: Adaptive neuro fuzzy inference system
FS-MMC: Front-side modular multilevel converter
FIS: Fuzzy inference system
IGBT: Insulated gate bipolar transistor
LS-PWM: Level shift pulse width modulation
MV: Medium voltage
MVDC: Medium voltage direct current
MMC: Modular multilevel converter
PEBB: Power electronic building block
PI: Proportional and integral
PS-PWM: Phase shift pulse width modulation

PWM: Pulse width modulation
ST: Smart transformer
VSC: Voltage source converter.

Data Availability

The authors declare that all data used in this work were generated during the course of the work and will be given upon request. Any other source has been appropriately referenced within the manuscript.

Ethical Approval

Authors affirm that the submitted manuscript is ours and original.

Conflicts of Interest

The authors declare that they have no known competing conflicts or personal relationships that could have appeared to influence the work reported in this paper.

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