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Review Article

Design Considerations for Autocalibrations of Wide-Band ΔΣ Fractional-N PLL Synthesizers

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Autocalibration of VCO frequency and loop gain is an essential process in PLL frequency synthesizers. In a wide tuning-range fractional-N PLL frequency synthesizer, high-speed and high-precision automatic calibration is especially important for shortening the lock time and improving the phase noise. This paper reviews the design issues of the PLL auto-calibration and discusses on the limitations of the previous techniques. A very simple and efficient auto-calibration method based on a high-speed frequency-to-digital converter (FDC) is proposed and verified through simulations. The proposed method is highly suited for a very wide-band ΔΣ fractional-N PLL.

1. Introduction

ΔΣ fractional-N RF frequency synthesizer is an essential building block in modern wireless communication systems. Achieving wide frequency tuning range, low phase noise, and fast locking time is challenging especially as the required tuning range becomes wider. If a single tuning curve is used to cover total tuning range, the VCO gain K_{VCO} of an LC VCO needs to be extremely large as illustrated in Figure 1(a). As a result, the phase noise and spur performances will be unacceptably poor. This is why multiple subband tuning curves via a switched capacitor bank are usually needed to cover the wide tuning range as well as keep K_{VCO} low, as shown in Figure 1(b) [1]. In this case, if the total capacitance of the switched capacitor bank varies in linear proportion to the cap bank code n, the K_{VCO} and the sub-band spacing f_{step} will vary in a cubic power of the f_{VCO} variation [2]. For example, K_{VCO} and f_{step} vary eight times if f_{VCO} varies two times. Due to such a wide variation of the VCO tuning characteristics, the PLL's essential performance parameters such as loop gain, lock time, and phase noise vary much, which is usually undesirable. Therefore, a fast and accurate autocalibration is needed for a PLL frequency synthesizer.

Finding a sub-band tuning curve that is the closest to a target frequency is referred to as the VCO frequency calibration. There had been many methods reported in the literature [3–10]. However, they all showed severe speed-resolution limitation. Meanwhile, maintaining the loop gain constant over the entire tuning range is referred to as the loop gain calibration. It is required in order to have a constant loop bandwidth and low phase noise. Previous techniques of this also showed slow calibration time due to the closed loop operation [11, 12].

This paper reviews the previous calibration techniques and examines their limitations. Based on the considerations, a new autocalibration technique based on a high-speed FDC is presented, which is highly suited to a wide tuning range ΔΣ fractional-N synthesizer.

2. Previous Techniques and Design Considerations

2.1. VCO Frequency Calibration. The most critical issue for the VCO frequency calibration is the accuracy and speed, that is, the calibration resolution and time. The calibration time should be fast enough because it will enlarge the total lock time, and the calibration resolution should be at least better than $f_{step}/2$ in order to be able to resolve two adjacent sub-band tuning curves. Note that f_{step} can be easily smaller than f_{REF} in a fractional-N PLL. Thus, the calibration circuit should be able to provide sub-f_{REF}

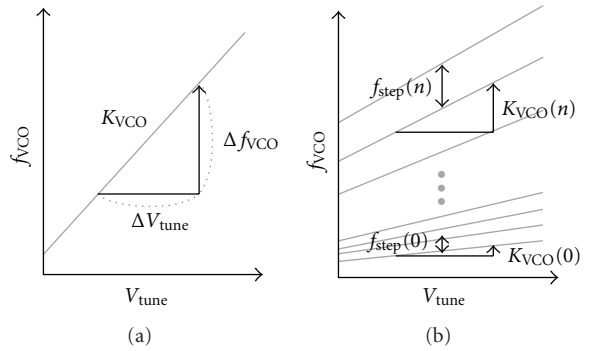

Figure 1: Frequency tuning characteristics in a wide band VCO. (a) Single tuning curve. (b) Multiple tuning curves with $K_{VCO}(n)$ and $f_{step}(n)$ variation.

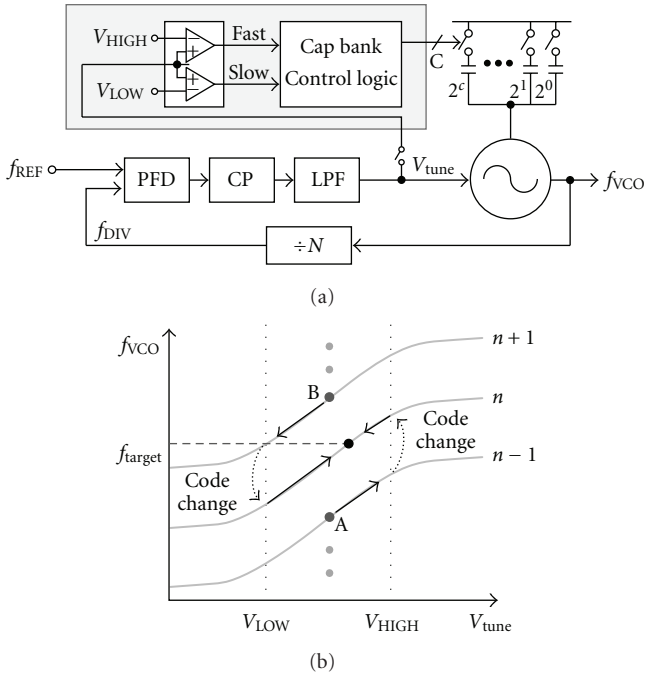

Figure 2: VCO frequency calibration by V_{tune} monitoring. (a) Architecture. (b) Operation principle [4–6].

calibration resolution while the calibration time is as fast as possible.

The tuning voltage monitoring technique as shown in Figure 2(a) was the oldest technique [4–6]. It monitors the VCO tuning voltage V_{tune} to find if it goes out of the predefined range between V_{HIGH} and V_{LOW}. If it goes out of the range, the cap bank code is automatically adjusted. Figure 2(b) illustrates the operation procedure. First, the calibration starts at point A on code $n-1$. Then, V_{tune} goes up toward V_{HIGH} due to the high f_{target}. When V_{tune} exceeds V_{HIGH}, the calibration circuit changes the cap bank code from $n-1$ to n. Then, PLL settles into the lock state with f_{VCO} approaching f_{target}. If the calibration process starts from point B on code $n+1$, similar process is carried out to reach the cap bank code n. This method always maintains the closed-loop lock state during the calibration process. Because of the closed-loop operation, this method usually requires several hundreds of μsec for the calibration, which is the major drawback of this method. This method, however, can be useful when it is used as an auxiliary lock maintaining tool to deal with the unwanted VCO tuning characteristic variation during the normal closed-loop operation of PLL [6].

Next the most popular VCO calibration technique is the "relative" frequency comparison method [7, 8]. The structure is shown in Figure 3(a). It compares the counted values of two clock signals f_{REF} and f_{VFC} during $k \cdot T_{REF}$ counting period. As illustrated in Figure 3(b), f_{VFC} ($= f_{VCO}/M$) is counted during $k \cdot T_{REF}$. Then, the comparator simply compares the two values and generates Fast/Slow flag signal, and then the control logic changes cap bank code accordingly. During the calibration, PLL stays in the open-loop state and V_{tune} is fixed at $V_{DD}/2$. The frequency resolution of this technique is given by $M \cdot f_{REF}/k$. As in the usual implementation, if M is the PLL's total division ratio N, the frequency resolution will be f_{VCO}/k. Thus, k must be higher than N in order to have sub-f_{REF} resolution, and higher k leads to a longer calibration. Thus, the typical calibration time of this method usually reaches several tens of μsec or even hundreds of μsec, which is also a major drawback of this method.

Another very fast but more analog intensive method is the time-to-voltage converter- (TVC-) based "relative" period comparison technique [9, 10]. The schematic structure is shown in Figure 4(a). It compares the voltages V_{C1} and V_{C2} that are proportional to the periods of the two incoming clock signals f_{REF} and f_{VCO}/N (Figure 4(b)). This method is usually very fast and only requires a few μsec or even sub-μsec. But due to the analog circuitry involved in the comparison process, its accuracy can be easily affected by the circuit mismatches and PVT variations. In addition, it is not suitable to a $\Delta\Sigma$ fractional-N PLL. Figure 5 illustrates how the f_{DIV} clock edges can vary when $\Delta\Sigma$ modulator is activated to provide a fractional division ratio $N \cdot f$. Assuming an MASH-111 is used for the $\Delta\Sigma$ modulator, f_{DIV} clock edge can be anywhere between $(N-3) \cdot T_{VCO}$ and $(N+4) \cdot T_{VCO}$ depending on the $\Delta\Sigma$ modulator output values, where T_{VCO} is a VCO signal period in lock state. Therefore, if the TVC-based technique is applied to a $\Delta\Sigma$ fractional-N PLL, a multiple period integration of the TVC output is needed, which will not only make the calibration time slow but also degrade the calibration accuracy.

Another issue in the VCO frequency calibration methods is about the code selection algorithm. Note that the conventional simple binary search process only gives an odd numbered code as a final result [7]. In Figure 6, code 9 would be selected as a final code by the conventional simple binary search process although even-numbered code 10 is the closest to the target frequency f_1. In order to overcome this, an improved method in [10] compares the last two searched codes. But this algorithm will also fail if the closest code is in multiples of 4. This limitation is explained in Figure 6. This method is not a problem for the target frequency f_2, for which the closest code 2 will be selected. But for the target

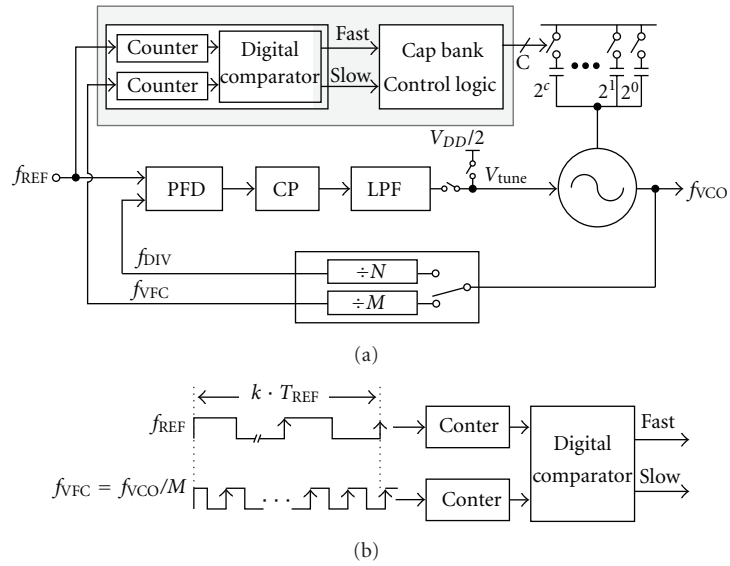

Figure 3: Relative frequency comparison VCO frequency calibration. (a) Architecture. (b) Operation principle [7, 8].

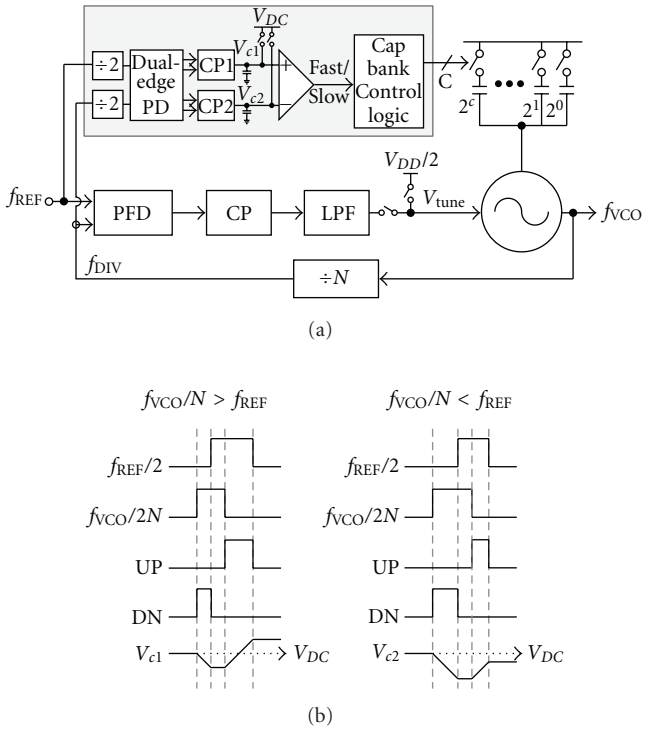

Figure 4: Relative period comparison VCO frequency calibration. (a) Architecture. (b) Operation principle [9, 10].

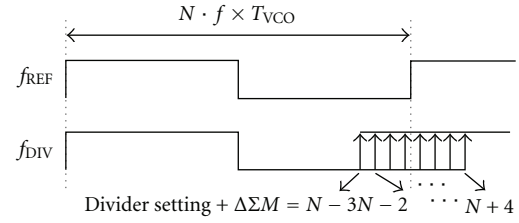

Figure 5: f_{DIV} clock period jittering at the lock state with a $\Delta\Sigma$ modulator activated in a $\Delta\Sigma$ fractional-N PLL.

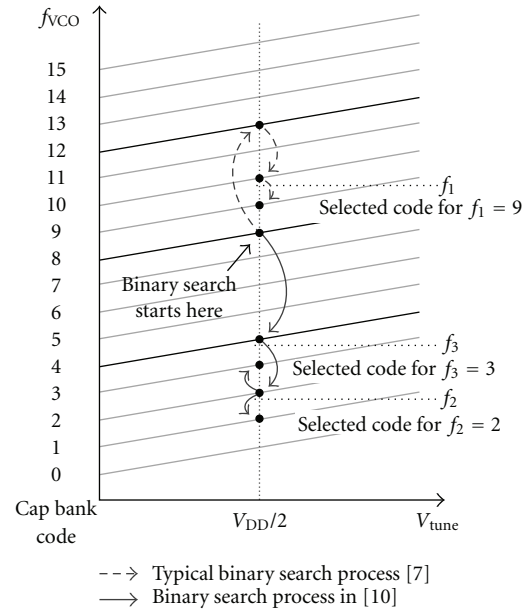

Figure 6: Final code selection of binary search process for various target frequencies in previous techniques. For f_1, typical binary search process is used [7], and improved algorithm in [10] is applied for f_2 and f_3.

frequency f_3, the method in [10] will provide the less optimal code 3 rather than the optimal code 4. Therefore, a truly closest code selection algorithm must be able to store the frequency error for all searched codes during the calibration process and finally produce the closest code to the target frequency.

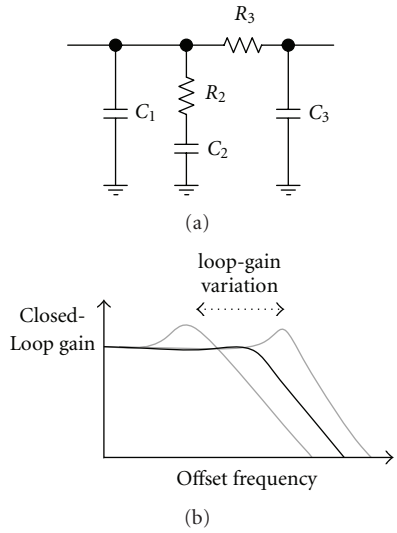

Figure 7: (a) A third-order passive loop filter. (b) Closed-loop gain and bandwidth variation in PLL.

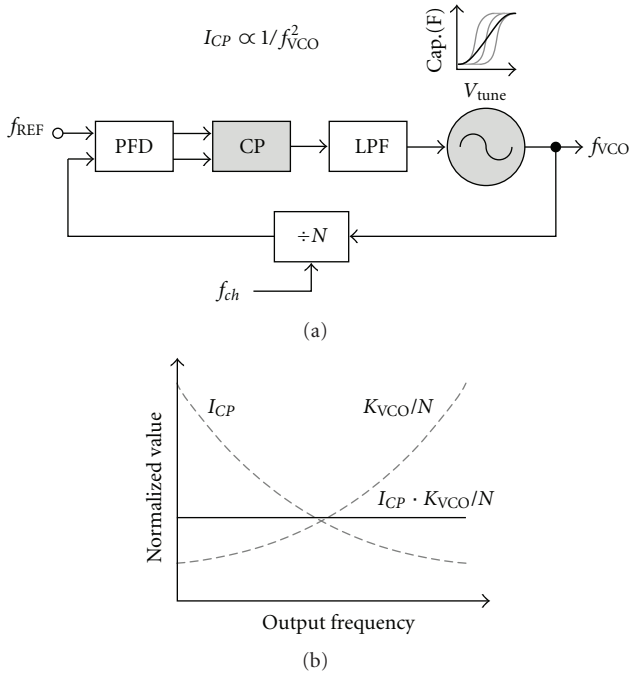

Figure 8: Loop gain compensation by preset pattern of charge pump gain I_{CP}. (a) Architecture. (b) Operation principle [13].

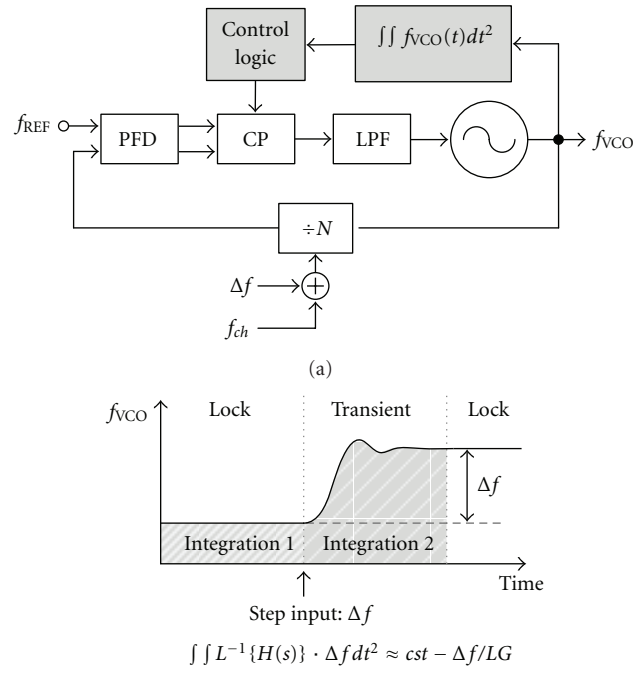

Figure 9: Loop gain calibration by measuring step-response of PLL (a) Architecture. (b) Operation principle [10, 11].

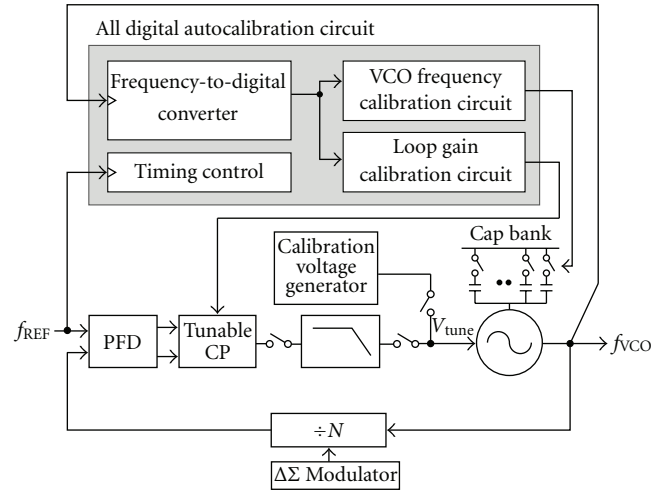

Figure 10: PLL block diagram with the FDC-based autocalibration circuit.

2.2. Loop Gain Calibration. A charge pump PLL generally uses the third-order passive loop filter as shown in Figure 7(a). It is known that the loop gain is proportional to $I_{CP} \cdot K_{VCO} \cdot R_2/N$, the lock time is proportional to $\sqrt{(I_{CP} \cdot K_{VCO} \cdot R_2/N)}$, and the integrated phase noise is inversely proportional to $I_{CP} \cdot K_{VCO} \cdot R_2/N$. Thus, the variation of each parameter will cause significant variation of the PLL closed-loop performances such as the loop gain, the lock time, and the phase noise. Figure 7(b) depicts the loop bandwidth variation due to the loop gain variation. The effect of I_{CP} variation on the loop gain can be minimized by using the same-type on-chip resistor for the loop filter R_2 and the I_{CP} reference voltage generation [15]. The division ratio N is a digital value, so its impact on the loop gain can be precisely predicted and accurately compensated. Meanwhile, the variation of K_{VCO} due to PVT variation cannot be accurately predicted. Therefore, the loop gain calibration circuit must be able to gauge the K_{VCO} variation

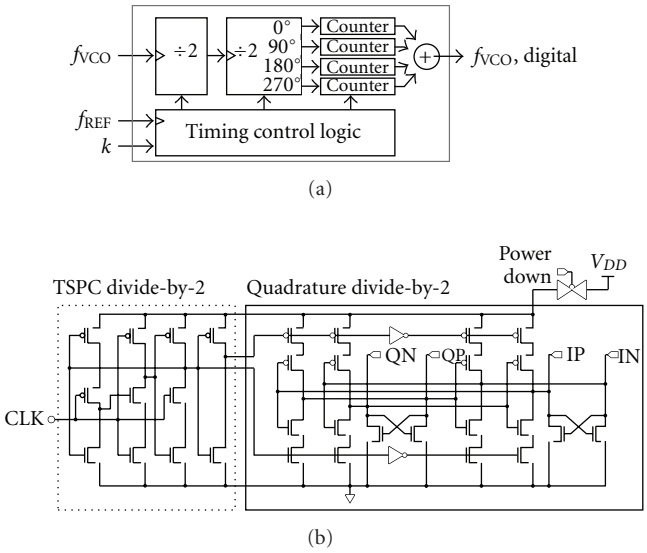

Figure 11: (a) Detail block diagram of the FDC. (b) Circuit schematic of quadrature-phase predivider having division ratio of 4.

accurately, which should be equivalent to the loop gain variation.

Figure 8(a) shows the previous loop gain compensation method [13]. Note that the term "compensation" is used here instead of the preferred "calibration." The basic idea of this compensation is to make the charge pump gain follow a preset way such that it is inversely proportional to $f_{VCO}{}^2$. Figure 8(b) illustrates the operation principle of this compensation. To compensate K_{VCO}/N variation that is proportional to $f_{VCO}{}^2$ in an LC tuned VCO, the charge pump gain is controlled to be inversely proportionally to $f_{VCO}{}^2$. Then, the loop gain that is proportional to $I_{CP} \cdot K_{VCO}/N$ will stay at a constant value, resulting in the constant loop bandwidth. But since this method cannot deal with any unexpected PVT variation of K_{VCO}, its effect would be limited after the chip fabrication.

The limitation of the previous method in [13] comes from the absence of the on-chip gauge of the loop gain. The on-chip measurement of the loop gain and the use of this value for loop gain calibration should be a very effective approach. It is known that PLL's closed-loop time-domain step response is closely related to the PLL's loop bandwidth. Previously, using the time-domain step-response to measure the loop gain and calibrate the charge pump gain was reported [11, 12]. Figure 9(a) shows the block diagram and Figure 9(b) shows the operating procedure. To calibrate loop gain, the two-step integrator integrates the VCO output signal in the locked state. After that, the step input Δf is triggered, and the integrator integrates the PLL's step-response. In [12], only the step-response is integrated to reduce the calibration time. The drawback of this calibration method is a long calibration time, that is almost up to several tens of μsec due to the closed-loop operation. In addition, the accuracy might be affected by the K_{VCO} variation during the transient state. Thus, we need

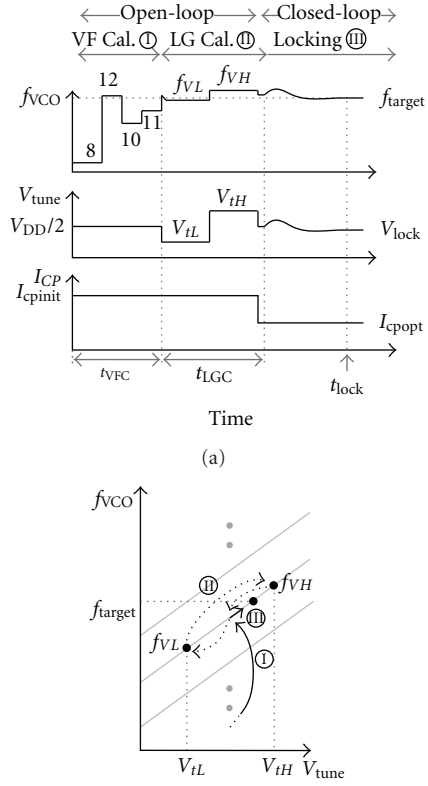

Figure 12: (a) Transitions of f_{VCO}, V_{tune}, and I_{CP} during calibration and locking process. (b) Transition of f_{VCO} during calibration.

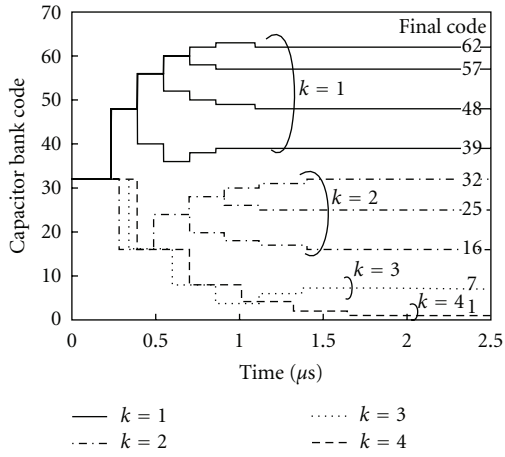

Figure 13: Behavioral simulation result of the VCO frequency calibration with k-value varying from 1 to 4 according to the required resolution.

more accurate and fast on-chip K_{VCO} measurement tool for the loop gain calibration.

2.3. Linearization of VCO Coarse Tuning Characteristics. The variation range of K_{VCO} and f_{step} are known to be

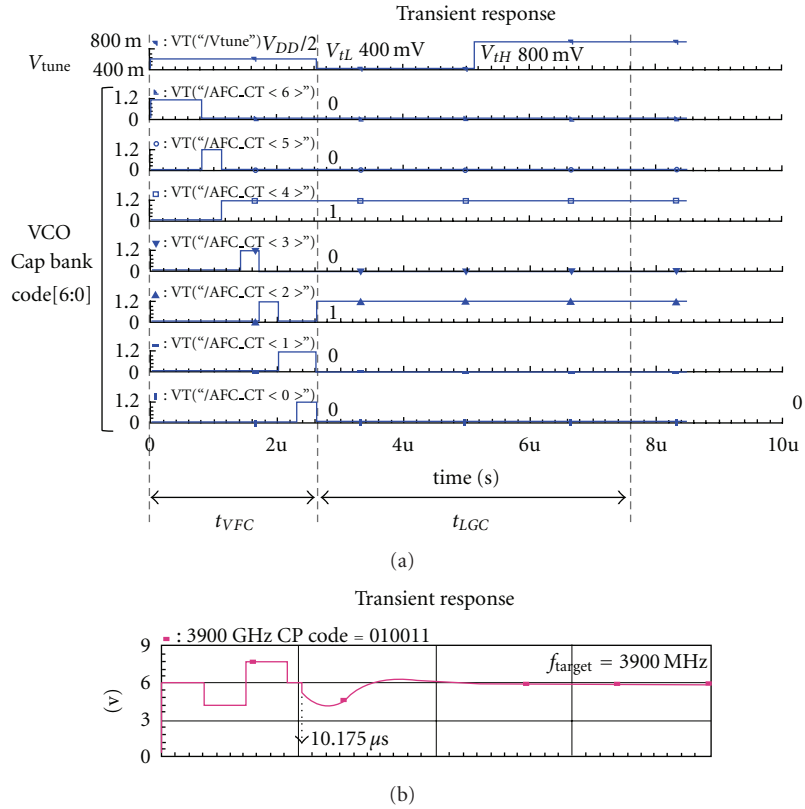

FIGURE 14: Behavioral simulation results for the proposed autocalibration. (a) V_{tune} and VCO cap bank code during autocalibration. (b) V_{tune} for the total locking process for 3900 MHz target frequency.

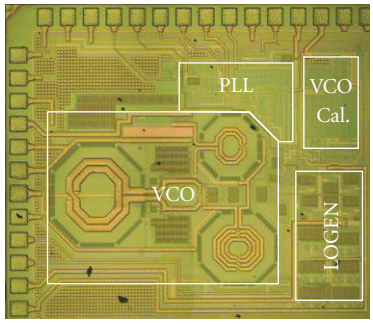

FIGURE 15: Chip micrograph of the ΔΣ fractional-N PLL synthesizer including only the VCO frequency calibration circuit [14].

proportional to the cubic power of the f_{VCO} total tuning range as the following equation:

$$\frac{K_{VCO,max}}{K_{VCO,min}} = \frac{f_{step,max}}{f_{step,min}} = \left(\frac{f_{VCO,max}}{f_{VCO,min}}\right)^3. \quad (1)$$

The large variation of K_{VCO} and f_{step} degrades the speed and accuracy of the loop gain and VCO frequency calibration processes. Therefore, reducing the total variation of K_{VCO} and f_{step} across the entire tuning range is desirable for improving the calibration result. Several studies were reported to reduce the K_{VCO} and f_{step} variation in LC VCO: authors of [16, 17] only addressed the K_{VCO} issue, and authors of [18] proposed a new cap bank structure to reduce the K_{VCO} and f_{step} variations together, but it relied on arbitrary fractional scaling of the capacitance value over the sixteen tuning curves, which made it difficult to apply the method to an even wider tuning range and more tuning curves. Thus, we need more simple and systematic design method of the capacitor bank structure for reducing the K_{VCO} and f_{step} variations across the total tuning range.

3. FDC-Based Autocalibration Technique

The limitations of the previous calibration technique can be overcome by the proposed FDC-based autocalibration technique, which is described in this section. Figure 10 shows the architecture of the fractional-N PLL with the proposed FDC-based all-digital autocalibration scheme. The calibration circuit comprises a high-speed FDC, the VCO frequency calibration circuit, the loop gain calibration circuit and the auxiliary timing control logic, and calibration voltage generator.

The high-speed FDC enables the fast calibration of VCO frequency and loop gain. The FDC operates in the time period of $k \cdot T_{REF}$ to convert the VCO frequency to a digital value with a conversion resolution of f_{REF}/k whereas the conventional technique in Figure 3 requires N times longer time $N \cdot k \cdot T_{REF}$ for acquiring the same

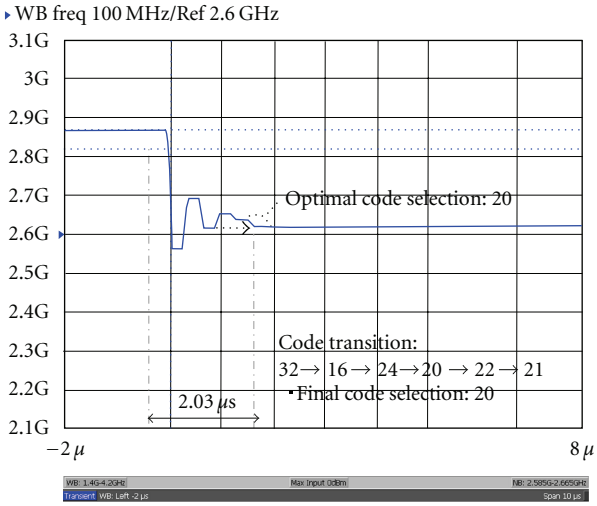

Figure 16: Measured VCO frequency during the VCO frequency calibration.

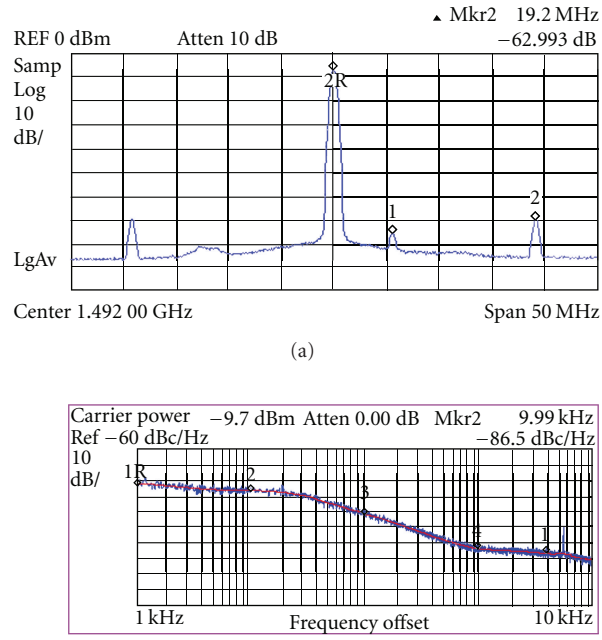

Figure 17: Measured PLL results at 1492 MHz. (a) Output spectrum. (b) Phase noise.

resolution. The detailed block diagram of the FDC is shown in Figure 11(a). The FDC accepts the VCO signal and divides it down to $f_{VCO}/4$ by using a quadrature-phase predivider, which is composed of a true single phase clock (TSPC) divide-by-2 and a quadrature-phase divide-by-2 as shown in Figure 11(b). After the predivider, the subsequent four counters that is connected to each of the quad-phase output signals count the VCO frequency. As a result, each counter can operate at a reduced speed of $f_{VCO}/4$ while the overall frequency resolution is not diminished. Finally the sum of the four counter outputs represents the VCO frequency.

The frequency error is generated by subtracting the target f_{target} digital code from the current f_{VCO} digital code. The resulting sign bit is used as Fast/Slow flag for the binary search process. The absolute value of the frequency error is utilized for the final optimal code selection process to find the final code that has shown the minimum frequency error. The more detailed description of the proposed VCO frequency calibration technique can be found in [14]. After the VCO frequency calibration is completed, the loop gain calibration process begins. It is basically based on the on-chip measurement of K_{VCO}. The FDC extracts two VCO frequencies f_{VH} and f_{VL} at two different tuning voltages V_{tH} and V_{tL}. Then, K_{VCO} is computed digitally. With the computed K_{VCO}, the optimal charge pump gain is generated according to the relation $I_{CP} \sim N/K_{VCO}$. After these two autocalibration processes, the normal PLL locking process begins. Proper selection of V_{tL} and V_{tH} is important in the proposed calibration technique. In the chosen range, the charge pump current must be sufficiently constant for accurate loop gain calibration. At the same time, the VCO sub-band tuning curves must be sufficiently overlapping to ensure V_{tune} to remain in this range after the PLL locking. Considering these aspects, V_{tL} and V_{tH} are chosen to be 0.4 and 0.8 V, respectively, which is 0.4 V off from the 1.2-V supply voltage.

Figure 12(a) shows the calibration procedure by illustrating the waveforms of f_{VCO}, V_{tune}, and I_{CP}, and Figure 12(b) illustrates how the VCO output frequency wanders on the VCO tuning curve plane during the calibration process. Note that this illustration is only for 4-bit cap bank case. In the first VCO frequency calibration mode, the binary search is performed with V_{tune} fixed at $V_{DD}/2$. The final optimal code is fed to VCO at t_{VFC}. In the subsequent loop gain calibration mode, V_{tune} is sequentially switched from V_{tL} to V_{tH} to extract f_{VL} and f_{VH}, and finally producing K_{VCO}. After t_{LGC}, the optimal charge pump code I_{cpopt} is generated to control the loop bandwidth. After the two-step open-loop calibration is completed, the PLL loop is closed and a normal locking process starts.

In order to verify the proposed autocalibration method, various behavioral simulations were performed for a PLL built in a mixed-signal circuit environment including verilog codes and circuit elements. Figure 13 shows a simulation result of the VCO calibration with a 6-bit cap bank. Due to the widely varying sub-band spacing f_{step}, the frequency resolution is adjusted by varying k from 1 to 4. Thus, the calibration time varies from 1.05 to 2.03 μs. Figure 14(a) shows a simulated result of V_{tune} and VCO cap bank code during the full autocalibration process. V_{tune} is fixed at $V_{DD}/2$ during the first VCO frequency calibration, and the final code found is 0010100. At the subsequent loop gain calibration, V_{tune} is switched from 400 to 800 mV. In this time, the FDC extracts two frequencies to calculate K_{VCO}. The simulated loop gain calibration time is 5 μs. Figure 14(b) shows the V_{tune} waveform during the total locking process at the target frequency of 3900 MHz. All of the above

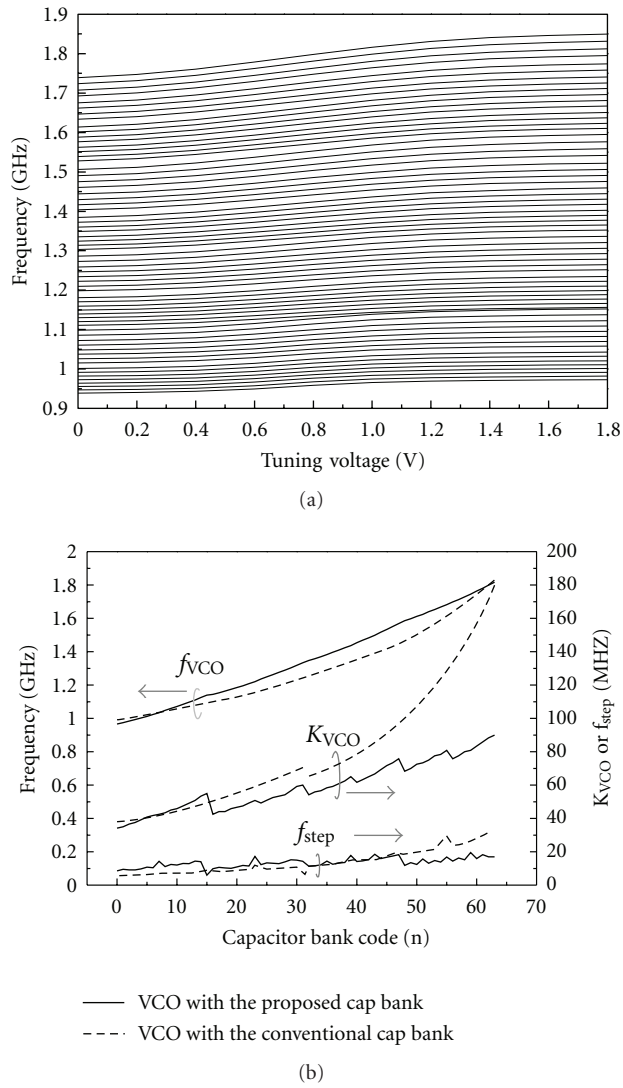

FIGURE 18: Measured VCO tuning characteristics. (a) Frequency tuning curves. (b) VCO output frequency, K_{VCO}, and f_{step} over the 64 tuning curves.

behavioral simulation results prove that the proposed FDC-based autocalibration method works successfully for the VCO frequency and loop gain calibrations.

A prototype chip including only the VCO frequency calibration circuit is fabricated in 0.13-μm CMOS technology [14]. The chip micrograph is shown in Figure 15. The die size including the pad frame is $1.33 \times 1.58\,\text{mm}^2$, and the active area of the VCO calibration circuit is $240 \times 400\,\mu\text{m}^2$. It dissipates 15.8 mA from a 1.2 V supply.

Figure 16 shows the measured f_{VCO} waveform during the VCO frequency calibration process at 2620 MHz. The measured calibration time is 2.03 μs, and the finally selected optimal code is 20, which show successful operation of the proposed optimal code selection algorithm. The PLL output spectrum at the output frequency of 1492 MHz is shown in Figure 17(a). The reference and fractional spurs are −63 and −68 dBc, respectively. The reference spur appears at the reference frequency of 19.2 MHz. Figure 17(b) shows the measured phase noise, which is −102.1 and −124.1 dBc/Hz at 100 kHz and 1 MHz offset, respectively. The in-band phase noise is −86.5 dBc/Hz at 10 kHz offset. And another prototype PLL chip including the full autocalibration capability has been fabricated and planned to be characterized.

The linearized coarse tuning characteristics are obtained by proposing a pseudoexponential capacitor bank structure [2] while the conventional cap bank produces a linear capacitance variation. Figure 18(a) shows the measured frequency tuning characteristics of the VCO with the proposed cap bank. Notice that the 64 sub-band tuning curves are evenly distributed. Figure 18(b) gives the plots for the f_{VCO}, K_{VCO}, and f_{step} over the 64 cap bank codes. For the sake of comparison, the measured results for a test VCO employing a conventional binary-weighted cap bank structure are shown together. It can be observed that the proposed cap bank structure substantially reduce the K_{VCO} variation from 38–180 (473%) to 34–90 (264%) MHz/V, and the f_{step} variation from 5.6–31 (553%) to 6–18 (300%) MHz/code. The results prove that the proposed pseudoexponential cap bank structure effectively linearizes the coarse tuning characteristics and reduces the K_{VCO} and f_{step} variations. It is found to be very instrumental for the autocalibration of a PLL having a wide-tuning range LC VCO.

4. Conclusion

Design considerations for the autocalibration of VCO frequency and loop gain are discussed for wide-band ΔΣ fractional-N PLL synthesizers. To overcome the limitations of the conventional techniques, the FDC-based all-digital autocalibration circuit is proposed. The FDC-based method remarkably shortens calibration time and improves calibration accuracy, and was found to be highly suitable for a wide band ΔΣ fractional-N PLL.

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