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Research Article

Differential Difference Current Conveyor Transconductance Amplifier: A New Analog Building Block for Signal Processing

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A new active building block for analog signal processing, namely, differential difference current conveyor transconductance amplifier (DDCCTA), is presented, and performance is checked through PSPICE simulations which show the usability of the proposed element is up to 201 MHz. The proposed block is implemented using 0.25 μm TSMC CMOS technology. Some of the applications are presented using the proposed DDCCTA, namely, a voltage mode multifunction filter, a current mode universal filter, an oscillator, current and voltage amplifiers, and grounded inductor simulator. The feasibility of DDCCTA and its applications is confirmed via PSPICE simulations.

1. Introduction

The analog integrated circuit design in current mode is receiving increased attention due to some potential performance features like wide bandwidth, less circuit complexity, wide dynamic range, low power consumption, and high operating speed [1]. The current mode approach has emerged as an alternate method besides the traditional voltage mode circuits. The current mode active elements are appropriate to operate with signals in current or voltage or mixed mode and are gaining acceptance as building blocks in high-performance circuit designs. A number of current mode active elements such as operational transconductance amplifier (OTA) [2], current conveyors (CCs) [3–5], differential voltage current conveyor (DVCC) [6], differential difference current conveyor (DDCC) [7], current feedback operational amplifier (CFOA) [8] are available in the literature.

Recently some new analog building blocks, such as current conveyor transconductance amplifier (CCTA) [9, 10], current controlled current conveyor transconductance amplifier (CCCCTA) [11], current difference transconductance amplifier (CDTA) [12], current controlled current difference transconductance amplifier (CCCDTA) [13], differen tial voltage current conveyor transconductance amplifier (DVCCTA) [14], and differential voltage current controlled conveyor transconductance amplifier (DVCCCTA) [15], are reported in the literature. These may be constructed by cascading of current mode building blocks with transconductance amplifier (TA) analog building blocks in monolithic chip for compact implementation of signal processing circuits and systems. It is well known that DDCC has some advantages [7, 16, 17] specially for applications demanding differential and floating inputs, over CCII or CCCII owing to three high input impedance terminals for DDCC compared to one high input impedance terminal for CCII or CCCII. However, DDCC does not have a powerful inbuilt tuning property in contrast to CCCII. The DDCC is more versatile than DVCC as it has an extra high input impedance terminal.

The main intention of this paper is to propose a new active building block, namely, differential difference current conveyor transconductance amplifier (DDCCTA), which has DDCC [7] as input block and is followed by a TA. The DDCCTA has all the good properties of CCTA, CCCCTA, and DVCCTA including the possibility of inbuilt tuning

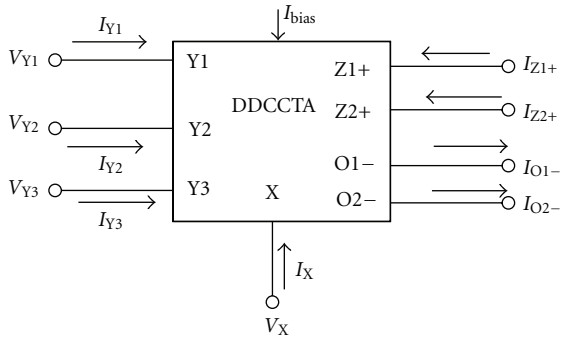

Figure 1: Circuit symbol of the proposed DDCCTA.

of the parameters of the signal processing circuits to be implemented and also all the versatile and special properties of DDCC such as easy implementation of differential and floating input circuits. However, the same may be implemented using separate DDCC and OTA analog building blocks, but it will be more convenient and useful if DDCCTA is implemented in monolithic chip which will result in compact implementation of signal processing circuits and systems. Section 2 deals with the proposed DDCCTA circuit and some of its properties. Section 3 is devoted for some of its applications in developing signal processing circuits such as voltage mode (VM) filter, current mode (CM) filter, oscillator, current and voltage amplifier, and grounded inductor simulator. The functionality of all the proposed circuits has been verified using SPICE simulations. The conclusion is given in Section 4.

2. Proposed DDCCTA

The DDCCTA is based on DDCC [7] and consists of differential amplifier, current mirrors, and TA. The port relationships of the DDCCTA as shown in Figure 1 can be characterized by the following matrix:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_{Z1+} \\ I_{Z2+} \\ I_{01} \\ I_{O2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1+} \\ V_{Z2+} \\ V_{O1-} \\ V_{O2-} \end{bmatrix}, \quad (1)$$

where g_m is transcon/ductance of the DDCCTA.

The CMOS-based internal circuit of DDCCTA in CMOS is depicted in Figure 2. It consists of the circuit of DDCC [7] (transistors M1 to M14) followed by a transconductance amplifier (transistors M15 to M24). The derivation of port relationships is given in Sections 2.1 to 2.3 [13].

2.1. Relationship between Voltages of X Port and Y1, Y2, and Y3 Ports. The voltage at X port may be found by analyzing the differential difference part (comprising of transistors M1 to M10) of the circuit of Figure 2 as follows:

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2} + \beta V_{Y3} + \varepsilon_V, \quad (2)$$

where

$$\beta_1 = \frac{1}{P_1}\left(g_{m3}g_{m6} + \frac{g_{m3}(g_{m4}g_{m5} - g_{m3}g_{m6})}{g_{m3} + g_{m4}}\right),$$

$$\beta_2 = \frac{1}{P_1}\left(g_{m1}g_{m5} + \frac{g_{m1}(g_{m1}g_{m5} - g_{m2}g_{m6})}{g_{m1} + g_{m2}}\right),$$

$$\beta_3 = \frac{1}{P_1}\left(g_{m2}g_{m6} + \frac{g_{m2}(g_{m1}g_{m5} - g_{m2}g_{m6})}{g_{m1} + g_{m2}}\right), \quad (3)$$

$$\varepsilon_V = -\frac{I_B}{P_1}\left(\frac{g_{m1}g_{m5} - g_{m2}g_{m6}}{g_{m1} + g_{m2}} + \frac{g_{m4}g_{m5} - g_{m3}g_{m6}}{g_{m3} + g_{m4}}\right),$$

$$P_1 = g_{m4}g_{m5} - \frac{g_{m4}(g_{m4}g_{m5} - g_{m3}g_{m6})}{g_{m3} + g_{m4}},$$

and I_B represents current through transistor Mi ($i = 7, 8, 10, 12, 14$). With matched transconductances $g_{m1} = g_{m2} = g_{m3} = g_{m4}$ and $g_{m5} = g_{m6}$, V_X is obtained as

$$V_X = V_{Y1} - V_{Y2} + V_{Y3}. \quad (4)$$

2.2. Relationship between Currents at Z1+, Z2+, and X Ports. The analysis of the portion of the circuit comprising of transistors M9 to M14 of the circuit of Figure 2 gives

$$I_{Z1+} = \alpha_1 I_X + \varepsilon_{I1},$$
$$I_{Z2+} = \alpha_2 I_X + \varepsilon_{I2}, \quad (5)$$

where

$$\alpha_1 = \frac{g_{m11}}{g_{m9}}, \qquad \varepsilon_{I1} = \left(1 - \frac{g_{m11}}{g_{m9}}\right) I_B,$$
$$\alpha_2 = \frac{g_{m13}}{g_{m9}}, \qquad \varepsilon_{I2} = \left(1 - \frac{g_{m13}}{g_{m9}}\right) I_B. \quad (6)$$

For matched transconductances $g_{m9} = g_{m11} = g_{m13}$, the port currents are simplified to

$$I_{Z1+} = I_{Z2+} = I_X. \quad (7)$$

2.3. Relation for Currents at O1− and O2− Ports. The proposed DDCCTA contains a transconductor cell comprising of transistors M15 to M24. Assuming gate voltages of transistors M17 and M18 as V_{T1} and V_{T2}, the output currents I_{O1-} and I_{O2-} may be found, respectively, as

$$I_{O1-} = -(\gamma_1 V_{T1} - \gamma_2 V_{T2} + \varepsilon_{T1}),$$
$$I_{O2-} = -(\gamma_3 V_{T1} - \gamma_4\ V_{T2} + \varepsilon_{T2}), \quad (8)$$

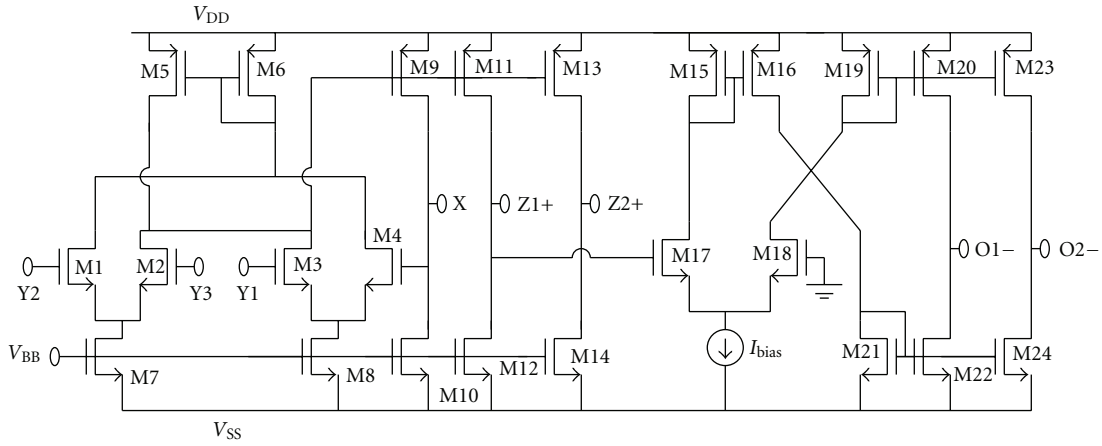

Figure 2: DDCCTA implementation.

where

$$\gamma_1 = g_{m17}\left(\frac{g_{m16}g_{m22}}{g_{m15}g_{m21}} - \frac{1}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m22} - g_{m15}g_{m18}g_{m20}g_{m21}}{g_{m17}+g_{m18}}\right)\right),$$

$$\gamma_2 = g_{m18}\left(\frac{g_{m20}}{g_{m19}} + \frac{1}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m22} - g_{m15}g_{m18}g_{m20}g_{m21}}{g_{m17}+g_{m18}}\right)\right),$$

$$\gamma_3 = g_{m17}\left(\frac{g_{m16}g_{m24}}{g_{m15}g_{m21}} - \frac{1}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m24} - g_{m15}g_{m18}g_{m23}g_{m21}}{g_{m17}+g_{m18}}\right)\right),$$

$$\gamma_4 = g_{m18}\left(\frac{g_{m23}}{g_{m19}} + \frac{1}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m24} - g_{m15}g_{m18}g_{m23}g_{m21}}{g_{m17}+g_{m18}}\right)\right),$$

$$\varepsilon_{T1} = -\frac{I_{\text{Bias}}}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m22} - g_{m15}g_{m18}g_{m20}g_{m21}}{g_{m17}+g_{m18}}\right),$$

$$\varepsilon_{T2} = -\frac{I_{\text{Bias}}}{g_{m15}g_{m19}g_{m21}} \times \left(\frac{g_{m16}g_{m17}g_{m19}g_{m24} - g_{m15}g_{m18}g_{m23}g_{m21}}{g_{m17}+g_{m18}}\right). \quad (9)$$

With $g_{m17} = g_{m18}$, $g_{m21} = g_{m22} = g_{m24}$, $g_{m15} = g_{m16} = g_{m19} = g_{m20} = g_{m23}$, the output currents I_{O1-} and I_{O2-} reduce to

$$I_{O1-} = -(g_{m17}V_{T1} - g_{m18}V_{T2}), \quad (10)$$

$$I_{O2-} = -(g_{m17}V_{T1} - g_{m18}V_{T2}). \quad (11)$$

In the circuit, $V_{T1} = V_{Z1+}$ and $V_{T2} = 0$; hence the output currents are simplified to

$$I_{O1-} = -g_{m17}V_{Z1+}, \qquad I_{O2-} = -g_{m17}V_{Z1+}. \quad (12)$$

The value of g_{m17} is obtained as $\sqrt{2\mu C_{\text{ox}}(W/L)_{17}I_{\text{Bias}}}$ if transistors are biased in strong inversion region and $2I_{\text{Bias}}/V_T$ ($V_T = KT/q$) if transistors are biased in subthreshold region which can be adjusted by bias current I_{Bias}.

2.4. Simulation. To validate the behaviour of the proposed element, PSPICE simulations have been carried out using TSMC 0.25 μm CMOS process model parameters. The supply voltages of $V_{DD} = -V_{SS} = 1.25$ V and $V_{BB} = -0.8$ V are used. The aspect ratio of various transistors for DDCCTA is given in Table 1. The DC transfer characteristics of the proposed DDCCTA from $Y1$, $Y2$, and $Y3$ terminals to X terminal are shown in the Figure 3. It is clear that the voltage at X terminal follows the Y terminal voltages in the range of -200 mV to $+200$ mV. The variation of current at Z1+ and Z2+ terminals with X terminal current from $-100\,\mu$A to $100\,\mu$A is shown in Figure 4. It may be noted that there is deviation for current below $-80\,\mu$A. The variation of the transconductance value by changing I_{Bias} from 0 to 500 μA is depicted in Figure 5. The decreases in transconductance for larger bias currents than 450 μA or so is due to transistors (M_{17}, M_{18}) entering in linear region of operation from saturation region. The maximum transconductance is about 1.6 mS. The other circuit performance parameters of the DDCCTA are summarised in Table 2.

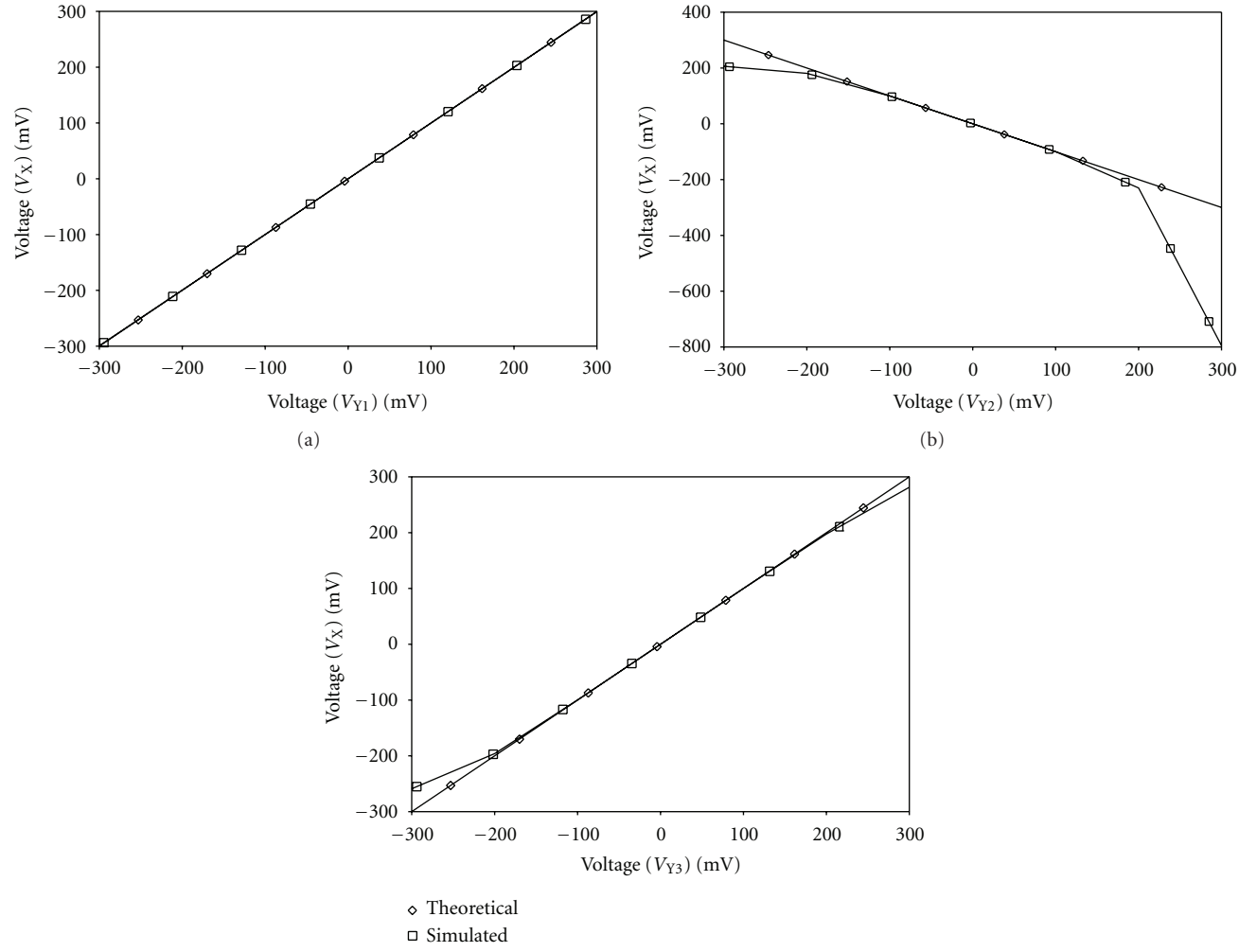

Figure 3: DC transfer characteristic for voltage transfer from (a) $Y1$ port to X port, (b) $Y2$ port to X port, and (c) $Y3$ port to X port.

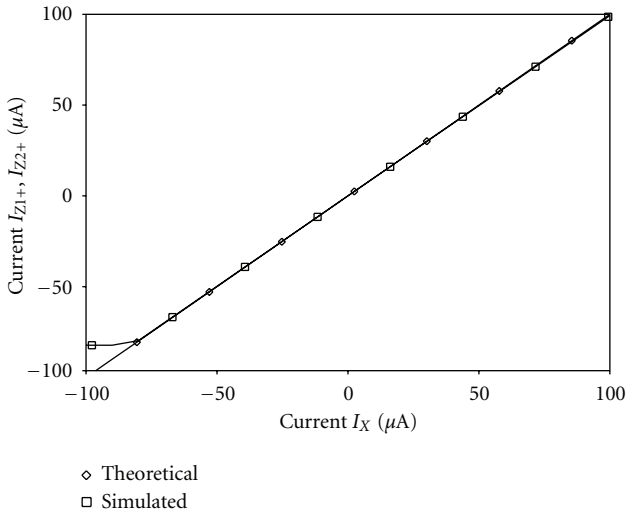

Figure 4: DC transfer characteristic for current transfer from X port to $Z1+$ and $Z2+$ ports.

Table 1: Aspect ratio of various transistors

Transistor	Aspect ratio (W(μm)/L(μm))
M1–M4	10/0.5
M5, M6	5/0.5
M7, M8	27.25/0.5
M9, M11, M13	8.5/0.5
M10, M12, M14	44/0.5
M15, M16, M19–M24	5/0.5
M17, M18	27/0.5

3. Applications

3.1. Multifunction Voltage Mode Filter. In this section a multifunction voltage mode (VM) filter is proposed. It uses a single DDCCTA, two grounded capacitors, and a grounded resistor. The proposed multifunction VM filter is shown in

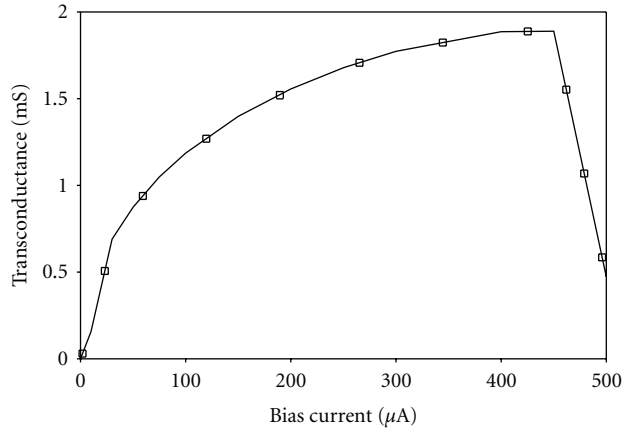

Figure 5: Variation of transconductance with bias current.

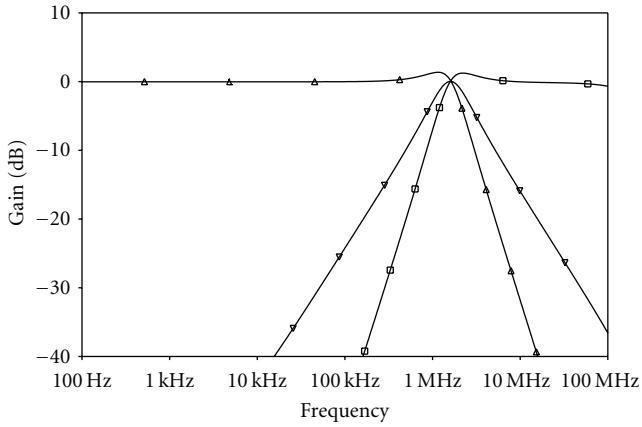

Figure 7: Simulated responses of the proposed voltage mode filter.

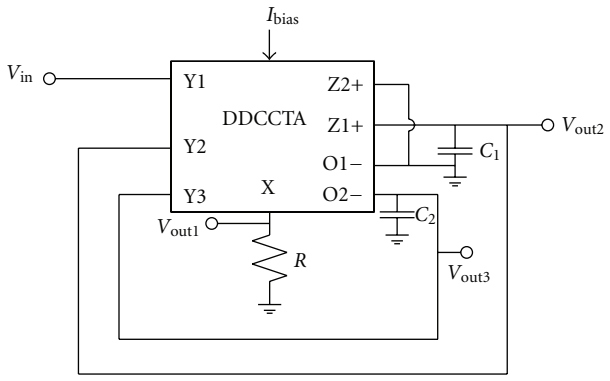

Figure 6: Proposed voltage mode filter.

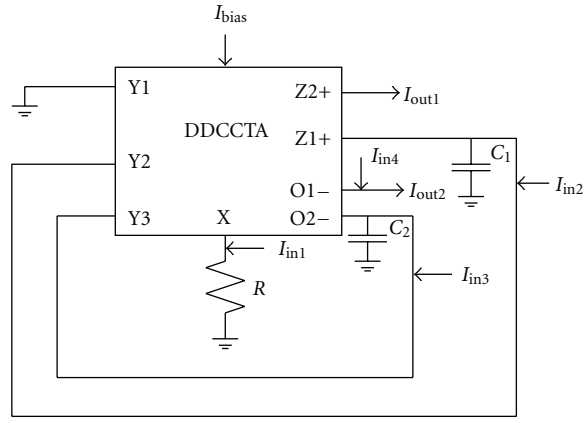

Figure 8: Current mode universal filter.

Table 2: Circuit performance parameters of the DDCCTA.

Power consumption	1.8 mW
Input voltage linear range (voltage inputs)	−200 mV to +200 mV
Input current linear range (current input)	−80 μA to 100 μA
Parasitic at Y ports (R_Y, C_Y)	very high, 20 fF
Parasitic at Z ports (R_Z, C_Z)	218 kΩ, 35 fF
Parasitic at $O-$ ports (R_{O-}, C_{O-})	324 kΩ, 20 fF
−3 dB bandwidth (at $I_{Bias} = 100\,\mu A$)	236 MHz for V_X/V_Y 223 MHz for I_Z/I_x 201 MHz for I_{O-}/V_z
Input bias range for controlling transconductance amplifier	10 nA to 450 μA

Figure 6. The analysis of circuit yields the output voltages at various nodes as

$$\frac{V_{out1}}{V_{in}} = \frac{s^2 C_1 C_2 R}{D(s)},$$
$$\frac{V_{out2}}{V_{in}} = \frac{sC_2}{D(s)}, \tag{13}$$
$$\frac{V_{out3}}{V_{in}} = -\frac{g_m}{D(s)},$$

where

$$D(s) = s^2 C_1 C_2 R + sC_2 + g_m. \tag{14}$$

It may be observed from (13) that high-pass, band-pass, and low-pass responses are available simultaneously at V_{out1}, V_{out2}, and V_{out3}, respectively. Thus, the proposed structure is a single-input-and-three-output voltage mode filter. It may be noted that no component matching constraint is required. The responses are characterized by pole frequency (ω_0), bandwidth (ω_0/Q_0), and quality factor (Q_0) as

$$\omega_0 = \left(\frac{g_m}{RC_1C_2}\right)^{1/2}, \qquad \frac{\omega_0}{Q_0} = \frac{1}{RC_1}, \qquad Q_0 = \left(\frac{g_m RC_1}{C_2}\right)^{1/2}. \tag{15}$$

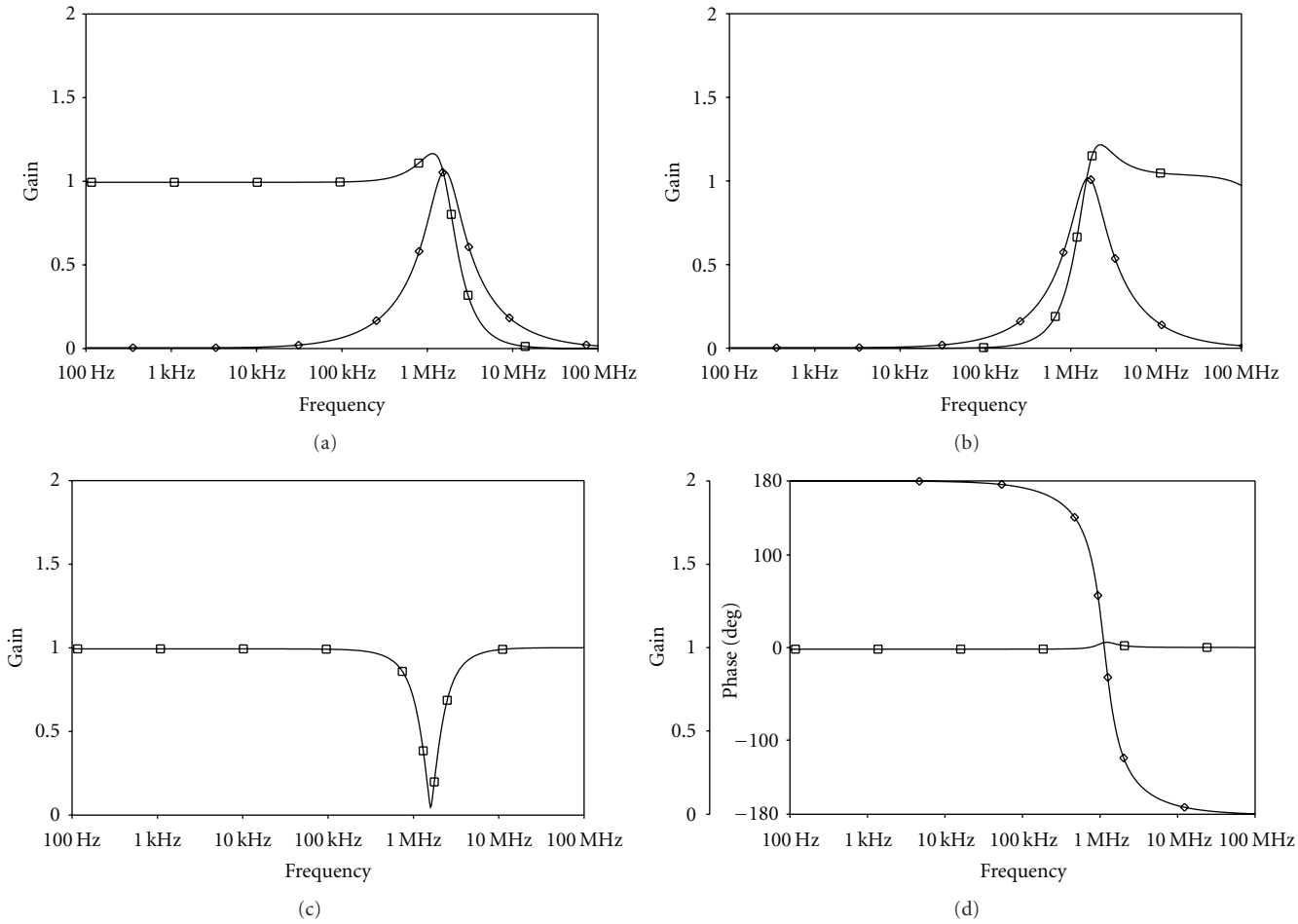

Figure 9: Simulated responses of the proposed current mode universal filter: (a) low pass and band pass; (b) high pass and band pass; (c) notch; (d) all pass.

Table 3: Comparative study of the available similar type of single-active-element-based VM filters.

Reference	Active element used and number of passive components	Grounded passive components	Availability of LP, HP, BP, notch, and AP responses	Number of available simultaneous responses	No inversion of input voltage	No requirement of gain of input signal such as $2V_{in}$ and $3V_{in}$	Tunability	No matching condition
[11]	CCCCTA, 2	No	All	1	No	No	Yes	No
[15]	DVCCCTA, 2	Yes	2	2	Yes	Yes	Yes	Yes
[18]	DBTA, 5	No	LP, HP, BP, Notch	1	Yes	Yes	Yes	No
[19]	DBTA,4	No	All	2	Yes	Yes	Yes	No
Proposed	DDCCTA, 3	Yes	LP, HP, BP	3	Yes	Yes	Yes	Yes

LP: low pass; HP: high pass; BP: band pass; Notch: notch response; AP: all pass.

Equation (15) reveals that for high-pass and band-pass responses the pole frequency (ω_0) and quality factor (Q_0) can be adjusted by g_m, that is, by bias current of DDCCTA, without disturbing ω_0/Q_0. The ω_0 and Q_0 are orthogonally adjustable with simultaneous adjustment of g_m and R such that the product g_mR remains constant and the quotient g_m/R varies and vice versa. The resistance R being a grounded one may easily be implemented as a variable resistance using only two MOS [17]. Equation (15) also indicates that high values of Q-factor will be obtained from moderate values of ratios of passive components, that is, from low component spread [22]. These ratios can be chosen as $g_mR = (C_1/C_2) = Q_0$. Hence, the spread of the component values becomes of the order of $\sqrt{Q_0}$. This feature of the filter related to the component spread allows the realization of high Q_0 values more accurately compared to the topologies where the spread

Table 4: The I_{in1}, I_{in2}, I_{in3}, and I_{in4} values selection for each filter function response.

Filter responses	Inputs				Output
	I_{in1}	I_{in2}	I_{in3}	I_{in4}	
Low pass	0	0	1	0	I_{out2}
Band pass	0	0	1	0	I_{out1}
	1	0	0	0	I_{out2}
	0	1	0	0	I_{out2}
High pass	1	0	0	0	I_{out1}
Notch	0	1	0	1	I_{out2}, $R = 1/g_m$
All pass	0	1	0	1	I_{out2}, $R = 1/g_m$

Table 5: Comparative study of the available similar type of single-active-element-based CM filters.

Reference	Active element used and number of passive components	Grounded passive components	Availability of LB, HP, BP, notch, and AP responses	No requirement of current inversion	No requirement of gain of input signal such as $2I_{in}$ and $3I_{in}$	Output current at high impedance	Tunability	Simple/no matching condition
[11]	CCCCTA, 2	Yes	Yes	Yes	No	Yes	Yes	Yes
[13]	CCCDTA, 2	Yes	Yes	No	Yes	No	Yes	Yes
[20]	CCCDTA, 2	Yes	Yes	Yes	No	Yes	Yes	Yes
[21]	CCCCTA, 2	Yes	No	Yes	Yes	No	Yes	Yes
Proposed	DVCCTA, 3	Yes	Yes	Yes	Yes	Yes	Yes	Yes

LP: low pass; HP: high pass; BP: band pass; Notch: notch response; AP: all pass.

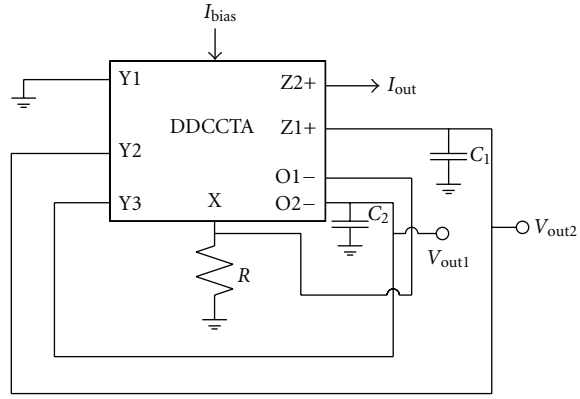

Figure 10: Proposed Oscillator.

of passive components becomes Q_0 or Q_0^2. It can also be easily evaluated to show that the sensitivities of pole ω_0 and pole Q_0 are within unity in magnitude. Thus, the proposed structures, can be classified as insensitive.

A detailed study of the available similar type of single-active-element-based (such as CCCTA, DBTA, and DVCCCTA) voltage mode filters and the proposed one is given in Table 3. It reveals that the topology [18, 19] uses excessive number of passive components whereas the proposed topology uses one extra passive component, namely, resistor (R) than [11, 15]. The proposed topology also provides the availability of a maximum number of simultaneous responses. Structures [11, 18, 19] use floating passive components and also use matching condition. Topology [11] needs input signal V_{in}, $-V_{in}$, and $-2V_{in}$; hence there is requirement of additional circuits. Thus, it reveals that although the proposed topology realizes only LP, HP, and BP responses, it has two or more advantages over the other available topologies [11, 15, 18, 19].

To verify the functionality of the proposed single-DDCCTA-based voltage mode filter, SPICE simulations have been carried out using TSMC 0.25 μm CMOS process model parameters and supply voltages of $V_{DD} = -V_{SS} = 1.25$ V and $V_{BB} = -0.8$ V. The filter is designed for a pole frequency of $f_0 = 1.59$ MHz, $Q = 1$, the component values are found to be $C_1 = C_2 = 100$ pF, $R = 1$ kΩ, and bias current of DVCCTA equals 100 μA. Figure 7 shows the simulation results for high-pass (V_{out1}), band-pass (V_{out2}), and low-pass (V_{out3}) filter responses which are available simultaneously.

3.2. MISO Current Mode Universal Filter. A multiple-input single-output (MISO) universal current mode (CM) filter is proposed in this section which is obtained by grounding voltage input in Figure 6 and exciting it with current inputs as shown in Figure 8. It employs a single DDCCTA, two grounded capacitors, and a grounded resistor. Analysis of this circuit gives the output current as

$$I_{out1} = \frac{-s^2C_1C_2RI_{in1} - (sC_2 + g_m)I_{in2} + sC_1I_{in3}}{D(s)},$$
$$I_{out2} = \frac{(I_{in1} - I_{in2})sC_2Rg_m + g_mI_{in3} + D(s)I_{in4}}{D(s)}, \quad (16)$$

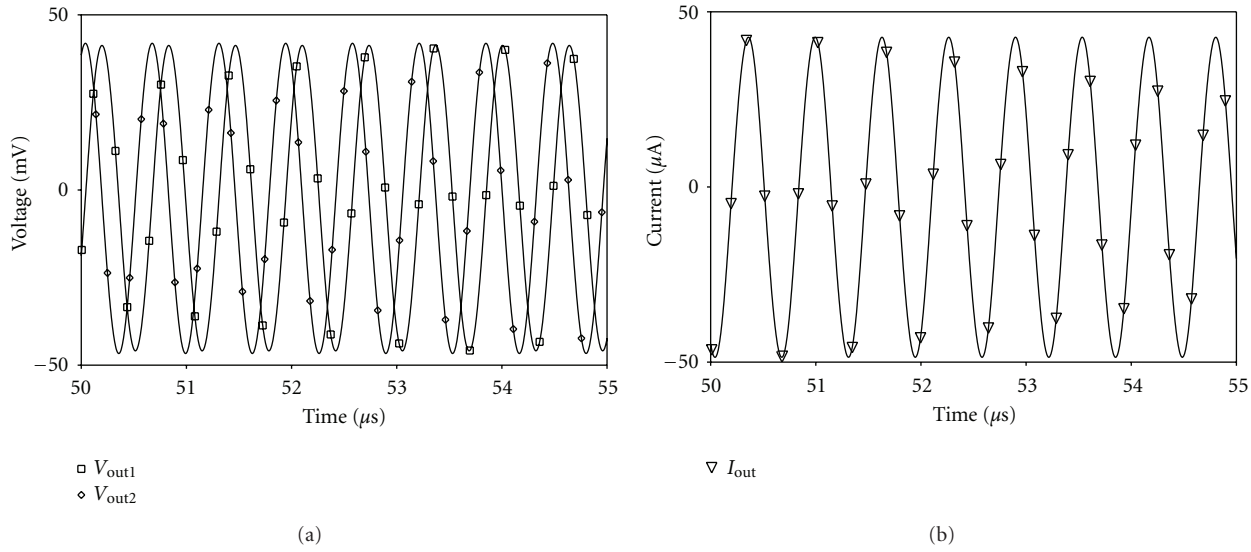

FIGURE 11: Outputs of the proposed oscillator: (a) quadrature output voltages at V_{out1} and V_{out2}; (b) current oscillation at I_{out}.

where

$$D(s) = s^2C_1C_2R + sC_2 + g_m. \quad (17)$$

Table 4 shows the availability of each filter response and the corresponding selection of input currents I_{in1}, I_{in2}, I_{in3}, and I_{in4}. Thus, the proposed structure is a four-input-single-output current mode filter. It may be noted that there is no component matching constraint for obtaining any filter response. The filter parameters are the same as given in (15). The grounded resistance (R) may easily be implemented as variable one using only two MOS [17] for full electronic control of filter parameters. The ω_0, Q_0, and ω_0/Q_0 can be orthogonally adjusted for low-pass, high-pass, and band-pass responses the way discussed in Section 3.1.

A detailed study of the available similar type of active-element-based (such as CCCCTA, CCCDTA, and CCCCTA) CM filters and the proposed one is given in Table 5. It reveals that although the proposed structure needs one extra resistor, the reported structures [11, 13, 20, 21] suffer from one or more features. In addition some active elements are required to sense current in [13, 21]. Thus, structures in [11, 13, 20, 21] will require some extra circuits to compensate the shortcomings in their features in comparison to the proposed one.

The proposed universal MISO current mode filter is validated through SPICE simulations. The circuit of Figure 8 for a pole frequency of $f_0 = 1.59$ MHz, $Q = 1$ has been designed with the component values of $C_1 = C_2 = 100$ pF, $R = 1$ kΩ, and bias current of DDCCTA equal to 100 μA. Figure 9(a) shows the simulation results for band pass (I_{out1}) and low pass (I_{out2}) filter responses which are available simultaneously for $I_{in} = I_{in3}$, $I_{in1} = I_{in2} = I_{in4} = 0$. Figure 9(b) shows the simulation results for band pass (I_{out2}) and high-pass (I_{out1}) filter responses which are available simultaneously for $I_{in} = I_{in1}$, $I_{in2} = I_{in3} = I_{in4} = 0$. Notch and all pass responses are shown in Figures 9(c) and 9(d)

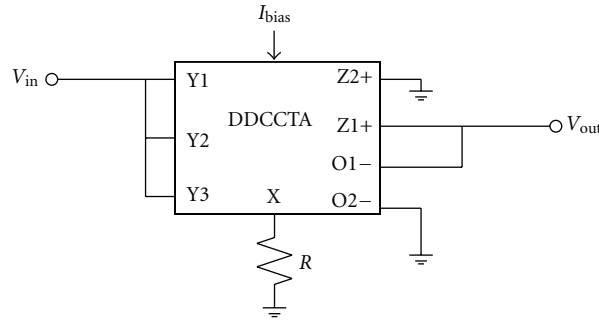

FIGURE 12: Voltage amplifier.

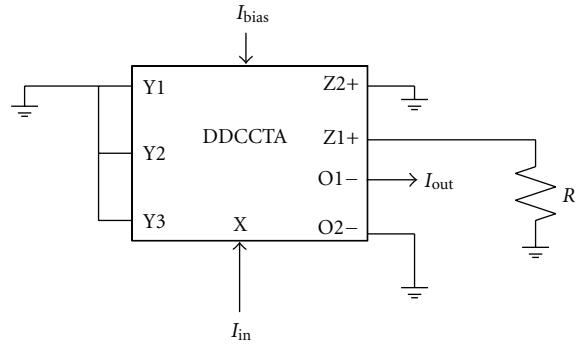

FIGURE 13: Current amplifier.

with $I_{in} = I_{in2} = I_{in4}$, $I_{in1} = I_{in3} = 0$ and $R = 1$ kΩ and 2 kΩ, respectively.

3.3. Oscillator. The current mode filter of Figure 8 may be used as oscillator when output I_{out2} is connected to I_{in1} as

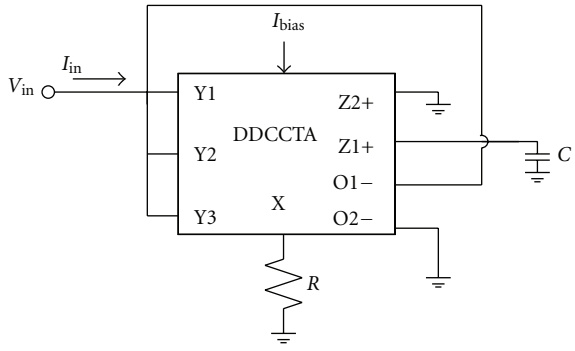

Figure 14: Grounded inductor simulator.

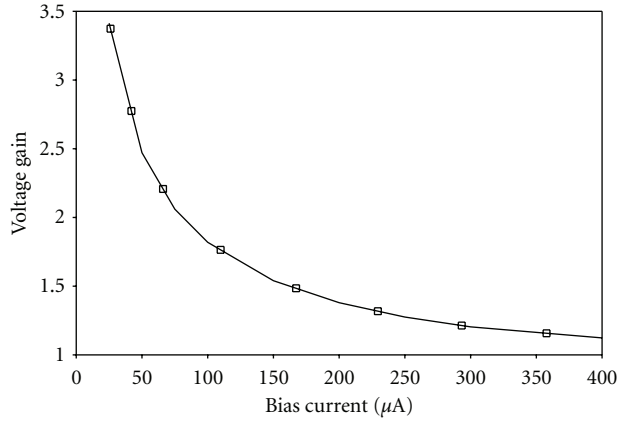

Figure 15: Voltage gain.

shown in Figure 10. The analysis of the circuit of Figure 10 gives the following characteristic equation:

$$s^2C_1C_2R + sC_2(Rg_m - 1) + g_m = 0. \tag{18}$$

The condition and frequency of oscillation may be computed as

$$\begin{aligned} \text{CO: } & g_m = \frac{1}{R}, \\ \text{FO: } & \omega_0 = \sqrt{\frac{g_m}{RC_1C_2}}. \end{aligned} \tag{19}$$

The oscillations are available at outputs V_{out1} and V_{out2}, and they are related as

$$V_{out1} = -\frac{g_m}{sC_2}V_{out2}. \tag{20}$$

Thus, these voltages exhibit quadrature relationship. The current oscillations are also available at high output impedance at I_{out}.

To verify the proposed circuit, an oscillator was designed for 1.59 MHz with $C_1 = C_2 = 100$ pF, $R = 1$ kΩ, and bias current of 100 μA. The simulated current and quadrature voltage waveforms are shown in Figure 11 for which the total harmonic distortion is 1.28%.

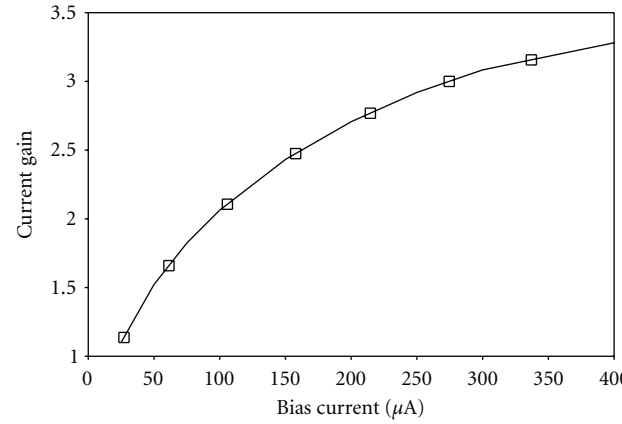

Figure 16: Current gain.

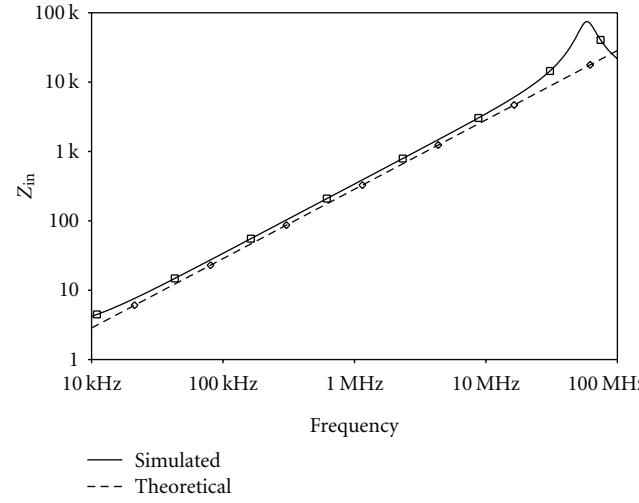

Figure 17: Frequency response of grounded inductor.

3.4. Voltage Amplifier, Current Amplifier, and Grounded Inductor. The proposed DDCCTA may also be configured for voltage and current amplifiers and grounded inductor simulator as shown in Figures 12, 13, and 14, respectively. The transfer functions may be expressed as follows:

(i) voltage amplifier:

$$\frac{V_{out}}{V_{in}} = \frac{1}{Rg_m}, \tag{21}$$

(ii) current amplifier:

$$\frac{I_{out}}{I_{in}} = Rg_m, \tag{22}$$

(iii) grounded inductor simulator:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sCR}{g_m}. \tag{23}$$

It may be noted that the gain of amplifiers and inductance can be adjusted by g_m, that is, by varying bias current of DDCCTA.

To verify the proposed amplifiers, the simulations have been carried out for $R = 0.5\,\text{k}\Omega$ ($2\,\text{k}\Omega$) for voltage (current) amplifier and bias current of $25\,\mu$A to $400\,\mu$A. The results are depicted in Figures 15 and 16. The inductor simulator is also validated through simulation with $R = 0.5\,\text{K}\Omega$, $C = 100\,\text{pF}$, and bias current of $90\,\mu$A. Figure 17 shows the simulated and theoretical results and there is close agreement between the two.

4. Conclusion

A new analog building block, namely, DDCCTA, is presented and some of its properties are discussed. It is found that the proposed DDCCTA is useful up to about 201 MHz. As applications of the proposed DDCCTA, VM multifunction filter, CM universal filter, quadrature oscillator, voltage and current amplifiers, and grounded inductor simulator topology are presented. The resistor being grounded may easily be implemented as a variable one using only two MOS [17]. The simulation results verify the theory.

References

[1] G. Ferri and N. C. Guerrini, *Low-Voltage Low-Power CMOS Current Conveyors*, Kluwer Academic, London, UK, 2003.

[2] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial," *IEEE Circuits and Devices Magazine*, vol. 1, no. 2, pp. 20–23, 1985.

[3] A. S. Sedra and K. C. Smith, "A second generation current conveyor its application," *IEEE Transactions on Circuit Theory*, vol. 17, no. 1, pp. 132–134, 1970.

[4] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "High frequency applications based on a new current controlled conveyor," *IEEE Transactions on Circuit and Systems I*, vol. 43, pp. 82–91, 1996.

[5] I. A. Awad and A. M. Soliman, "Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications," *International Journal of Electronics*, vol. 86, no. 4, pp. 413–432, 1999.

[6] H. O. Elwan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications," *IEE Proceedings—Circuits Devices Systems*, vol. 144, pp. 195–200.

[7] W. Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential difference current conveyor and their applications," *IEE Proceedings—Circuits Devices Systems*, vol. 143, pp. 91–96, 1996.

[8] C. Toumazou and A. Payne, "Current feedback opamp: a blessing in disguise?" *IEEE Circuits and Devices Magazine*, vol. 10, pp. 43–47, 1994.

[9] R. Prokop and V. Musil, "CCTA-a new modern circuit block and its internal realization," in *Proceedings of the International Conference on Electronic Devices and Systems, (IMAPSCZ '05)*, pp. 89–93, Brno, Czech Republic, 2005.

[10] W. Jaikla, P. Silapan, C. Chanapromma, and M. Siripruchyanun, "Practical implementation of CCTA based on commercial CCII and OTA," in *Proceedings of the International Symposium on Intelligent Signal Processing and Communication Systems, (ISPACS '08)*, pp. 1–4, Bangkok, Thailand, February 2009.

[11] M. Siripruchyanun and W. Jaikla, "Current controlled current conveyor transconductance amplifier (CCCCTA): a building block for analog signal processing," *Electrical Engineering*, vol. 90, no. 6, pp. 443–453, 2008.

[12] D. Biolek, "CDTA—building block for current-mode analog signal processing," in *Proceedings of the European Conference on Circuit Theory and Design, (ECCTD '03)*, pp. 397–400, Krak ów, Poland, September 2003.

[13] M. Siripruchyanun and W. Jaikla, "CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing," *International Journal of Electronics and Communications*, vol. 62, no. 4, pp. 277–287, 2008.

[14] A. Jantakun, N. Pisutthipong, and M. Siripruchyanun, "A synthesis of temperature insensitive/electronically controllable floating simulators based on DV-CCTAs," in *Proceedings of the 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, (ECTI-CON '09)*, pp. 560–563, Pattaya, Chonburi, Thailand, May 2009.

[15] W. Jaikla, M. Siripruchyanun, and A. Lahiri, "Resistorless dual-mode quadrature sinusoidal oscillator using a single active building block," *Microelectronics Journal*, vol. 42, no. 1, pp. 135–140, 2010.

[16] H. P. Chen, "Versatile universal voltage-mode filter employing DDCCs," *International Journal of Electronics and Communications*, vol. 63, no. 1, pp. 78–82, 2009.

[17] H. P. Chen, "High-input impedance voltage-mode multifunction filter with four grounded components and only two plus-type DDCCs," *Active and Passive Electronic Components*, vol. 2010, Article ID 362516, 5 pages, 2010.

[18] N. Herencsar, K. Vrba, J. Koton, and I. Lattenberg, "The conception of differential-input buffered and transconductance amplifier (DBTA) and its application," *IEICE Electronics Express*, vol. 6, no. 6, pp. 329–334, 2009.

[19] N. Herencsár, J. Koton, K. Vrba, and I. Lattenberg, "New voltage-mode universal filter and sinusoidal oscillator using only single DBTA," *International Journal of Electronics*, vol. 97, no. 4, pp. 365–379, 2010.

[20] M. Siripruchyanun and W. Jaikla, "Electronically controllable current-mode universal biquad filter using single DO-CCCDTA," *Circuits, Systems, and Signal Processing*, vol. 27, no. 1, pp. 113–122, 2008.

[21] S. Mangkalakeeree, D. Duangmalai, and M. Siripruchyanun, "Current-mode KHN filter using single CCCCTA," in *Proceedings of the 7th PSU Engineering Conference*, pp. 306–309, Hat-Yai, Thailand, May 2009.

[22] S. I. Liu, "High input impedance filters with low component spread using current-feedback amplifiers," *Electronics Letters*, vol. 31, no. 13, pp. 1042–1043, 1995.