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Research Article

A 3.9 μs Settling-Time Fractional Spread-Spectrum Clock Generator Using a Dual-Charge-Pump Control Technique for Serial-ATA Applications

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A low-jitter fractional spread-spectrum clock generator (SSCG) utilizing a fast-settling dual-charge-pump (CP) technique is developed for serial-advanced technology attachment (SATA) applications. The dual-CP architecture reduces a design area to 60% by shrinking an effective capacitance of a loop filter. Moreover, the settling-time is reduced by 4 μs to charge a current to the capacitor by only main-CP in initial period in settling-time. The SSCG is fabricated in a 0.13 μm CMOS and achieves settling time of 3.91 μs faster than 8.11 μs of a conventional SSCG. The random jitter and total jitter at 250 cycles at 1.5 GHz are less than 3.2 and 10.7 psrms, respectively. The triangular modulation signal frequency is 31.5 kHz and the modulation deviation is from −5000 ppm to 0 ppm at 1.5 GHz. The EMI reduction is 10.0 dB. The design area and power consumption are 300 × 700 μm and 18 mW, respectively.

1. Introduction

Serial Advanced Technology Attachment (SATA) is widely used as a low-cost, high-speed interface for external storage devices like HDDs and optical disc drives (ODDs) such as blu-ray discs, DVDs, and CDs. However, electromagnetic interference (EMI) is a particular problem with SATA devices [1]. One approach to reducing the EMI is to apply a spread-spectrum clock generator (SSCG) to a SATA-PHY.

Figure 1 shows a common block diagram of the SATA-PHY. It consists of a parallel-to-serial converter (P/S), a spread-spectrum clock generator (SSCG), a driver (DRV), a receiver (RCV), a clock and data recovery (CDR) circuit, and a serial-to-parallel converter (S/P). The SSCG generates a transmission clock signal (F_{VCO}). The P/S converts a transmission parallel data (TD) into a transmission serial data by using the F_{VCO}. This transmission serial data is transmitted by the DRV. The F_{VCO} frequency should be modulated to reduce the EMI in accordance with the SATA specification [1]. A received serial data is inputted to the CDR via the RCV. The CDR generates the recovery data (DATA) and recovery clock (CLK) from the received data. The serial-to-parallel converter (S/P) converts from the DATA to the received parallel data (RD) by using the CLK. In this SATA-PHY, the SSCG is applied a fractional SSCG because of a large EMI reduction [2–18]. The fractional SSCG should be narrow loop bandwidth because the quantized noise originated from a ΣΔ modulator is removed. Therefore, the fractional SSCG essentially has large design area and long settling-time. There were some approaches to reduce design area in previous works [15, 17, 18]. However, those could not consist with shrinking design area, shorting settling-time, and reducing EMI and jitter. Therefore, we introduced a capacitance multiplication technique to the fractional SSCG and then we proposed fast-settling technique by controlling the CP.

Figure 2 depicts the states defined by the SATA specification and the SATA-PHY power consumption [1]. In a sync state, a communication is successfully established between a host and a device. In the sync state, the SATA-PHY operates the SSCG. The slumber state is a standby state. The SATA-PHY can stop the SSCG because allowed wake-up period

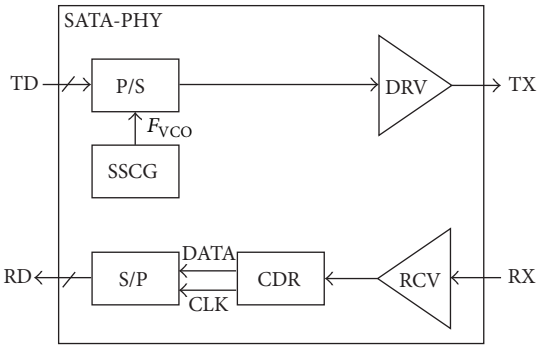


Figure 1: Block diagram of SATA-PHY.

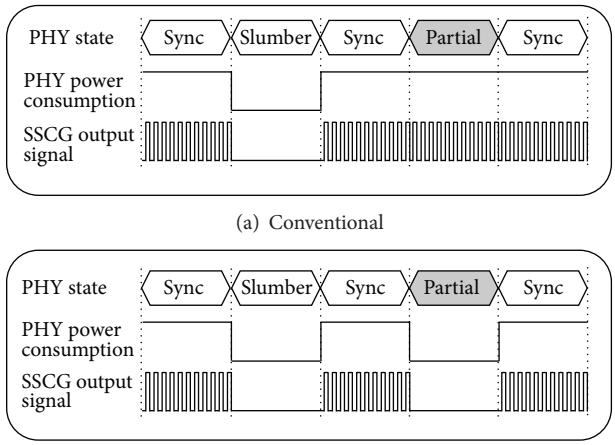


Figure 2: Proposed low power SATA-PHY operation.

from slumber to sync is a long period. The partial state is also a standby state. However, allowed wake-up period from partial to sync is a short period of less than 10 μs. Thus, it cannot stop the SSCG because the settling time of the SSCG is longer than 10 μs as shown in Figure 2(a). The SATA-PHY is set to the partial state many times in HDD and ODD applications. If the SSCG can achieve a settling time less than 10 μs, the SATA-PHY can stop the SSCG in partial state as shown in Figure 2(b). This is attractive for portable applications because of saving power. To achieve this operation, the SSCG has to have a settling time of less than about 4 μs, taking the wake-up time of the other blocks into consideration. This stringent settling time requirement is far shorter than that of a conventional SSCG.

Figure 3 shows a block diagram of a conventional SSCG based on a fractional PLL [3, 4, 6, 10–20]. It consists of a phase frequency detector (PFD), a charge pump (CP), a 3rd order loop filter (LF), a voltage controlled oscillator (VCO), a multimodulus divider (MMD), a programmable counter (PGC), a ΣΔ modulator (ΣΔ), and a wave generator (WG). The WG is a logic circuit and generates a triangular wave as a spread-spectrum modulation. The ΣΔ modulates the triangular signal and then generates divide ratio (N) that the average of the N is modulated by the triangular wave.

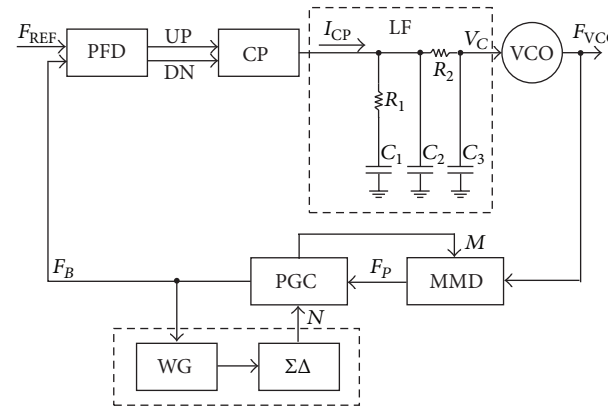


Figure 3: Conventional SSCG block diagram.

The F_{VCO} frequency is thus modulated by the triangular wave. This SSCG can reduce EMI more substantially than other SSCGs because the linearity of the modulation can be obtained accurately by utilizing the logic circuits [2–7].

This SSCG has two main jitter sources. One is a VCO jitter originating from the thermal and flicker noise of the MOS transistors. The other is a ΣΔ modulator jitter originating from the quantization noise of the ΣΔ modulator. The SSCG output jitter is the sum of these two jitters. To remove the quantization noise that is high-pass characteristics, the loop bandwidth should be designed narrow. Thus, the settling-time is necessarily longer and the design area is large.

Several approaches have been presented for reducing the design area. The high-resolution fractional divider technique shifts the modulator quantization noise to the higher frequency side and so it achieves wider bandwidth [5]. However, it is difficult to reduce the EMI by much because spurious jitter originating from the high-resolution fractional divider remains in the modulation bandwidth. All-digital SSCGs have been presented as a means of substantially reducing design area [17, 18]. However, their output jitter is still large because their digitally controlled ring oscillators generate large jitter and it is difficult to operate them accurately if there are PVT variations. The capacitance multiplication technique has been presented to reduce the design area as an approach in which the operation is based on that of a conventional SSCG [2, 7, 20]. However, the settling time is necessarily long because the loop bandwidth is set to be narrow.

To achieve a low-cost SATA-PHY suitable for portable applications, the design area, settling-time, power consumption, jitter, and EMI must all be reduced at the same time. To consummate these aggressive demands, we have proposed the dual-CP SSCG architecture with fast-settling CP control technique.

The rest of the paper is organized as follows. Section 2 describes the overall dual-CP SSCG architecture in detail. Section 3 presents the fast-settling CP control technique we have developed to achieve short settling time. Section 4 describes a CP circuit design to achieve a dual-CP architecture that is robust against PVT variations. Section 5 describes the VCO with high-frequency limiter. Section 6 presents

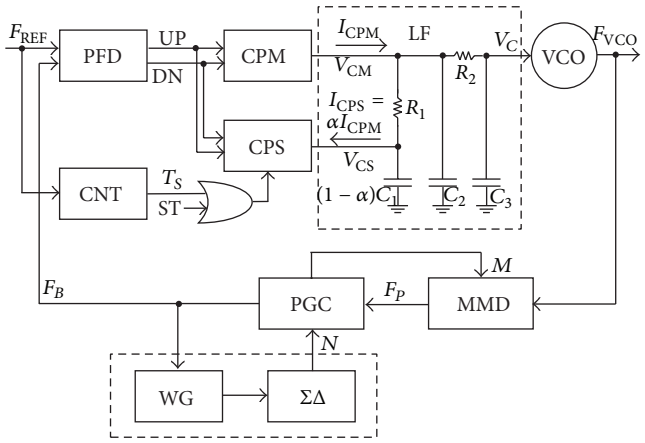


Figure 4: Block diagram of the proposed dual-CP SSCG with fast-settling CP control technique.

measurement results for evaluation purposes, and Section 7 concludes with a short summary of the key points.

2. Overall Dual-CP Architecture

Figure 4 shows our dual-CP SSCG architecture with fast-settling CP control technique to reduce the design area, settling time, power consumption, jitter, and EMI all at the same time. It includes a conventional SSCG, an additional CP (CPS), and a counter (CNT). A third-order ΣΔ modulator and a third-order low-pass loop filter are applied to reduce the ΣΔ modulator jitter. The PFD compares a phase of the reference clock signal (F_{REF}) with that of the feedback clock signal (F_B) and then generates up and down signals (UP, DN). Two CPs, a main CP (CPM) and an auxiliary CP (CPS), are applied to fulfill the need for high capacitance via the use of a capacitance multiplier. When the UP is generated by the PFD, the CPM charges the C_1 by the current (I_{CPM}), and the CPS discharges the C_1 by the current (I_{CPS}). In this architecture, the open loop transfer function of the main CP (CPM) path ($F_{CPM}(s)$) is given by

$$F_{CPM}(s) = \left(I_{CPM}\left(C_1R_1\right)s + 1\right) \cdot \left(s^3 + \left(\frac{1}{C_3R_2} + \frac{1}{C_1R_1} + \frac{1}{C_2R_1} + \frac{1}{C_2R_2}\right)s^2 + \left(\frac{C_1 + C_2 + C_3}{C_1C_2C_3R_1R_2}\right)s\right)^{-1}. \quad (1)$$

The open loop transfer function of the auxiliary CP (CPS) path ($F_{CPS}(s)$) is given by

$$F_{CPS}(s) = I_{CPS} \cdot \left(s^3 + \left(\frac{1}{C_3R_2} + \frac{1}{C_1R_1} + \frac{1}{C_2R_1} + \frac{1}{C_2R_2}\right)s^2 + \left(\frac{C_1 + C_2 + C_3}{C_1C_2C_3R_1R_2}\right)s\right)^{-1}. \quad (2)$$

If the $I_{CPM} = \alpha * I_{CPS}$ and α is less than 1, the open loop transfer function from the PFD to the VCO control voltage (V_C) is given by

$$F(s) = \left(I_{CPM}\left(C_1R_1\right)s + I_{CPM}\left(1-\alpha\right)\right) \cdot \left(s^3 + \left(\frac{1}{C_3R_2} + \frac{1}{C_1R_1} + \frac{1}{C_2R_1} + \frac{1}{C_2R_2}\right)s^2 + \left(\frac{C_1 + C_2 + C_3}{C_1C_2C_3R_1R_2}\right)s\right)^{-1}. \quad (3)$$

The zero of the open loop transfer function is given by

$$Fu = \frac{(1-\alpha)}{C_1R_1}. \quad (4)$$

On the other hand, that of the conventional one is given by

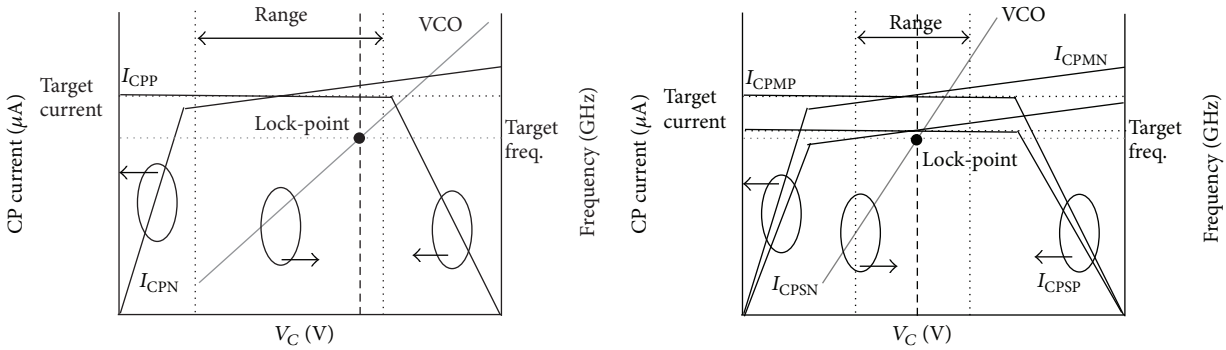
$$Fu = \frac{1}{C_1R_1}. \quad (5)$$

Our dual-CP technique, therefore, results in C_1 being $(1-\alpha)$ times smaller than that of the conventional one.

There is a key design point in this dual-CP architecture. Figure 5 shows the difference in the CP and VCO characteristics for a conventional SSCG and proposed dual-CP SSCG. The locking range, which means the V_C range at which the charge current (I_{CPP}) is almost the same as the discharge current (I_{CPN}), is wide because the SSCG loop has a tolerance for the current difference "$I_{CPP} - I_{CPN}$" in the conventional SSCG, as shown in Figure 5(a). The SSCG does not have to lock out of the lock range, which means that the CP current difference between the I_{CPP} and the I_{CPN} is large. However, in this case, the jitter originating from CP current difference becomes large. Thus, the SSCG output jitter becomes larger. Therefore, to meet the SATA jitter specification, the SSCG should lock into the lock range. In a conventional SSCG, the locking-point can thus be designed at a higher voltage area to reduce the VCO jitter because the low VCO sensitivity (K_V) brings about in the low VCO jitter.

In proposed dual-CP SSCG, the jitter originating from CP is more sensitive than that of the conventional one. Thus, the lock range becomes narrower as shown in Figure 5(b). This is because the SSCG loop is affected by the current differences "$I_{CPMP} - I_{CPSN}$" and "$I_{CPMN} - I_{CPSP}$". This means that it is important for the current difference to have a sufficient tolerance for PVT variations. The narrow lock range makes it possible to design the VCO sensitivity (K_V) to be higher than that of the conventional one.

Figure 6 shows a typical example of the open loop transfer function. As aspect of the EMI, the loop bandwidth should be designed wider because harmonic elements of the modulation triangle signal that fundamental frequency is 31.5 kHz can pass through the loop bandwidth. In our previous work, the 15th harmonics of the triangular signal should be passed in order to obtain the large EMI reduction [3]. However, as aspect of the jitter, as the loop bandwidth is wider, the jitter originated from ΣΔ modulator quantized



(a) Conventional SSCG (b) Proposed dual-CP SSCG

Figure 5: The explanation of CP current characteristics and VCO frequency current characteristics of the conventional SSCG (a) and the proposed dual-CP SSCG (b).

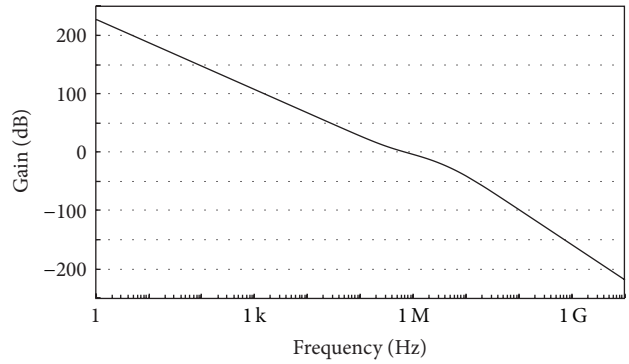


Figure 6: SSCG open loop frequency characteristics.

noise is larger. And the jitter originated from the VCO phase noise is larger as the loop bandwidth is narrower. Therefore, the loop bandwidth is designed at about 650 kHz. This is wide enough to meet the jitter specification and reduce the EMI, but this structure cannot achieve a settling-time of less than 4 μs. Such a settling-time is achieved by utilizing the CP control technique we describe in Section 3. It is important for the SSCG to have a sufficient tolerance for CP current variation due to PVT variation.

Figure 7 shows the effects of the CP current variation on the loop design. The current difference "$I_{CPM} - I_{CPS}$" affects the phase margin very little as shown in Figure 7(a). Even if the current difference varies −50%, the effect on the phase margin is less than 5% as shown in Figure 7(a). On the other hand, the current "I_{CPM}" or "I_{CPS}" has a huge influence impact on the loop bandwidth. Even if the different current varies −50%, the phase margin is affected at less than 50% as shown in Figures 7(b) and 7(c). The CP should be designed such that the variation of the current difference should remain less than about ±40%, taking the jitter specification into consideration. The main CP current (I_{CPM}) and auxiliary CP current (I_{CPS}) have a huge impact on the loop bandwidth and phase margin. The variation of the I_{CPM} and I_{CPS} should be designed at less than ±20%, taking the jitter specification and loop stability into consideration. A CP design that is robust against PVT variation is presented in Section 4.

3. Fast-Settling CP Control Technique

We have developed a fast-setting CP control technique. Figure 8 shows the concept of proposed fast-settling CP control technique. In the conventional SSCG, the settling-time is long because the large C_1 is charged by the small CP current as shown in Figure 8(a) [7]. As shown in Figure 8(a), in this SSCG, a charging speed (Δ_{CONV}) that means a slope in the settling period is given by

$$\Delta_{conv} = \frac{(1-\alpha)\, I_{CPM}}{C_1}. \tag{6}$$

In our dual-CP SSCG architecture, the C_1 is smaller than that of the conventional one. Thus, in the dual-CP SSCG, if a charged current is same, the charging speed is faster than that of the conventional one. In the dual-CP SSCG, the differential charge current is small; however, the I_{CPM} is larger than the charge current of the conventional SSCG. Thus, the charging speed can be faster if the only CPM charges the C_1. As shown in Figure 8(b), in this case, the charging speed (Δ_{PROP}) is given by

$$\Delta_{PROP} = \frac{I_{CPM}}{C_1}. \tag{7}$$

The charging speed (Δ_{PROP}) achieved with our technique is $1/(1-\alpha)$ times faster than the conventional one. In this

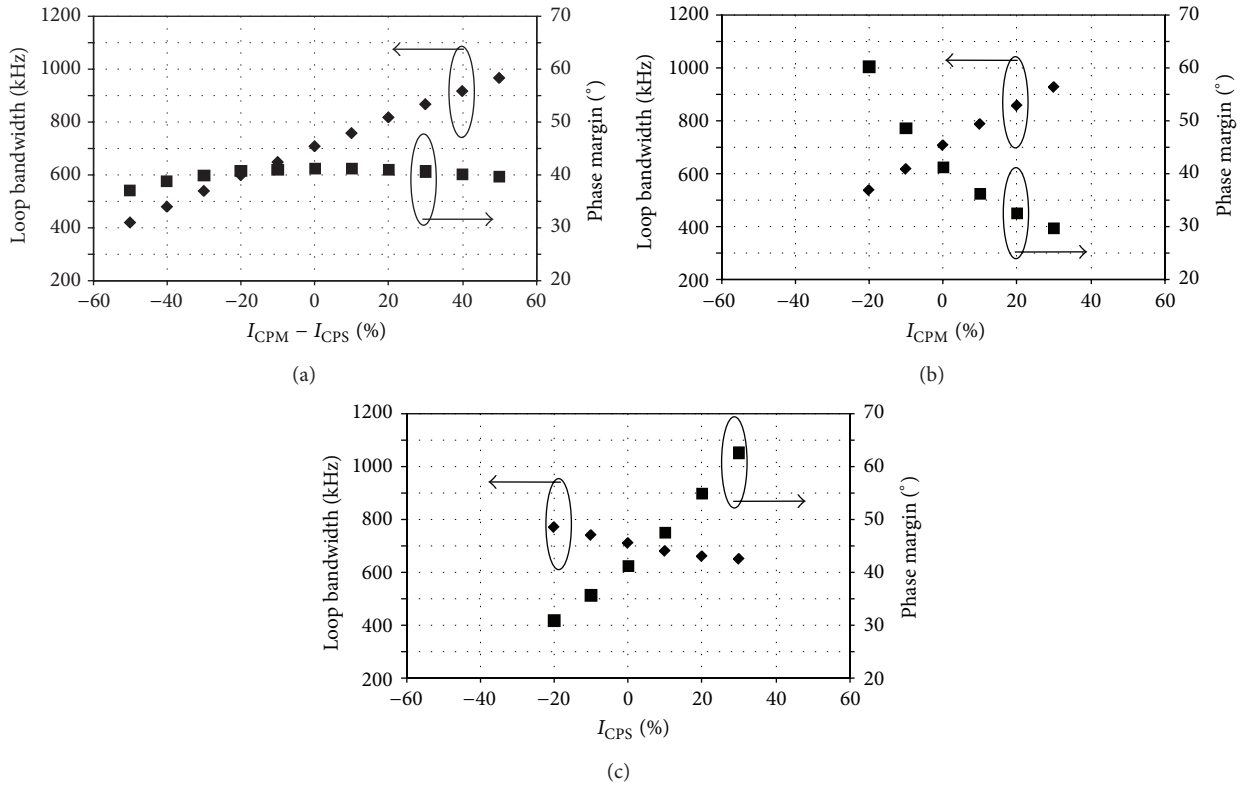


FIGURE 7: The effect of the loop bandwidth and phase margin due to CP parameters. (a) The effect by different current ($I_{CPM} - I_{CPS}$). (b) The effect by CPM (I_{CPM}). (c) The effect by CPS (I_{CPS}).

case, the CPS activates in the middle of the settling period. If the CPS activates at early in the settling period, the effect of the boosting charge by the CPM is weak. On the other hand, if the CPS activates at late in the settling period, a large overshoot may occur because the operation is unstable and settling period is prolonged rather than shortened. Moreover, the MMD cannot operate due to the overshoot and then the SSCG falls into a malfunction as shown in Figure 8(b). To overcome this trade-off, the VCO with high frequency limiter is applied to the SSCG as shown in Figure 8(c) [3]. When the CPS is activated, the overshoot occurs. However, the F_{VCO} frequency cannot be more than 2.2 GHz, which is the MMD maximum operating frequency by the high frequency limiter. Therefore, even if the overshoot occurs, the SSCG can be locked. To reduce the settling period, the CPS activation time is as long as possible. However, the settling period becomes longer due to large dumping if the CPS is activated after cross-over 1.5 GHz of the SSCG output signal. Thus, the CPS should be activated before cross-over 1.5 GHz of the SSCG output signal. Moreover, even if the CPS is activated right before cross-over 1.5 GHz, the large dumping might occur in the case that the phase difference between the reference clock and the feedback clock becomes large. It is difficult to control the phase difference at the CPS activation point. Thus, the CPS should activate relative less than cross over 1.5 GHz to have a margin of the lock period of the phase difference. In our proposed SSCG, the CPS activation time is set to 1 μs to reduce settling period when the SSCG achieves the settling period of less than 4 μs. As shown in Figure 4, the CPS is controlled by the CNT. The CNT is the counter that makes the CPS activation time by counting the F_{REF}. As shown in Figure 8, the SSCG is activated when the standby signal (T_S) is set to low. At this time, the CPS is not activated because the T_S is set to high. After a certain period that is made by the CNT, the T_S is set to low and the CPS activates.

Figure 9 shows the behavior simulation results for the settling time. This simulation is not designed for a settling time of less than 4 μs but designed to verify the fast settling period by using the CPS control. The conventional dual-CP SSCG achieves a settling time of less than about 22 μs in this simulation. On the other hand, when only the CPM operates, the overshoot occurs and the operation is unstable. When we apply our CP control technique to this SSCG so that the CPS is activated at 3 μs, the settling behavior is the same as that when only the CPM is activated before 3 μs. After the CPS is activated at 3 μs, the settling behavior deviates from that when only the CPM is activated and then directed to the target frequency slowly. After small overshoot occurs, the SSCG becomes locked at 18 μs. In this case, our technique enables the settling time to be shortened to about 4 μs, which is almost the same as the period during which the CPS is stopped. As the CPS is stopped for as long a time as possible, the settling time can be shortened. However, this technique has little effect when the CPS is activated after the overshoot occurs. Moreover, large overshoot may occur due to a small damping factor and the settling time may be longer than that

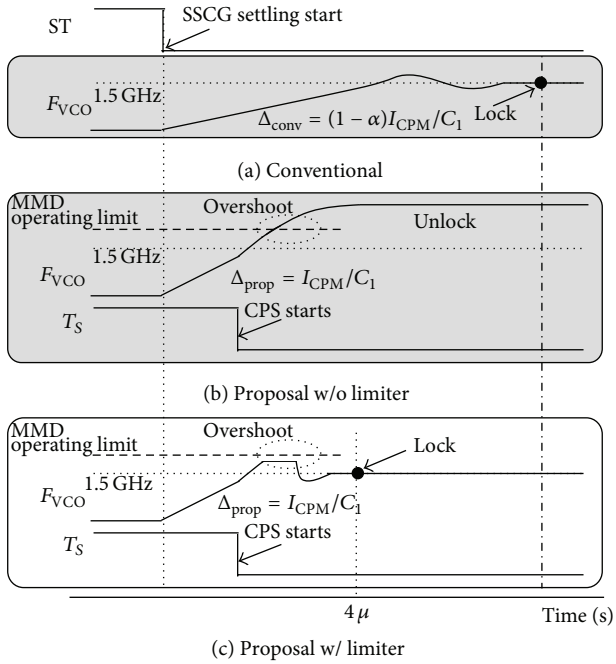


Figure 8: Explanation of proposed fast-lock dual-CP SSCG settling operation of the conventional SSCG (a) and the proposed dual-CP controlled technique without VCO high frequency limiter (b) and with limiter (c).

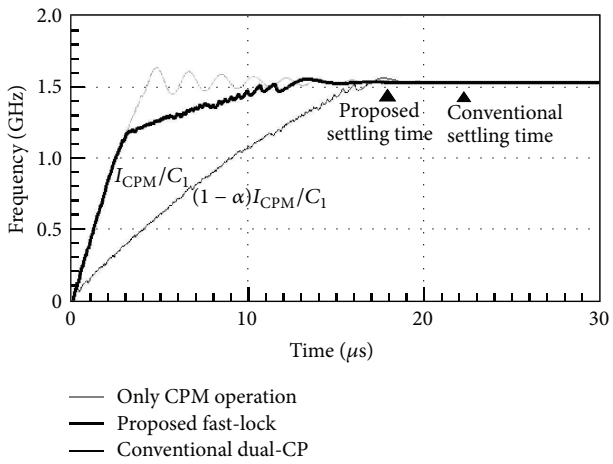


Figure 9: Simulation results of the conventional and proposed settling time.

without our technique's function when the CPS is activated just before the overshoot appears. Therefore, the timing is set such that the CPS is activated just before the overshoot occurs. This timing is made by counter that counts F_{REF}. In our design, the CPS is activated at about 1.0 μs, taking the CP current and filter capacitance into consideration.

4. Dual-CP Circuit Design

Figure 10 shows a circuit diagram of the CPM and the CPS. The PFD output signals (UP, UPB, DN, and DNB) are connected to the gate of the switch MOSs (M8, M21, M9, M10, M16, M15, M17, and M18). The VB is connected to the band-gap reference (BGR) and the reference current (I_{CP}) is generated as M1 drain current. The main CP current (I_{CPMP} and I_{CPMN}) and the auxiliary CP current (I_{CPSP} and I_{CPSN}) are generated from the I_{CP} by utilizing the current mirror and are given by

$$\frac{I_{CPMP}}{I_{CP}} = \frac{W_{M5}}{W_{M3}}, \qquad \frac{I_{CPMN}}{I_{CP}} = \frac{W_{M7}}{W_{M6}},$$
$$\frac{I_{CPSP}}{I_{CP}} = \frac{W_{M13}}{W_{M3}}, \qquad \frac{I_{CPSN}}{I_{CP}} = \frac{W_{<14}}{W_{M6}}. \tag{8}$$

The transistor width is described as W_{MN}, where N is the transistor number. Thus, the CP current ratio (α) is given by

$$\alpha = \frac{I_{CPSP}}{I_{CPMP}} = \frac{W_{M13}}{W_{M5}} = \frac{I_{CPSN}}{I_{CPMN}} = \frac{W_{M14}}{W_{M7}}. \tag{9}$$

Figure 11 shows the simulation results for the CPM and CPS charge/discharge characteristics. The simulation conditions are that the process, voltage, and temperature are typical, 1.35 V, and −40°C, respectively. The horizontal axis is the control voltage (V_C) and the vertical axis is the CP current. PMOS currents (I_{CPMP} and I_{CPSP}) appear as absolute values in the Figure. In our work, the CPM current (I_{CPMP} and I_{CPMN}) and CPS current (I_{CPSP} and I_{CPSN}) are designed at 44 μA and 32 μA, respectively. Therefore, the designed current difference value is 12 μA and α is 76%. In general, a PMOS transistor has accurate saturation characteristics and a narrow saturation region and an NMOS transistor has inaccurate saturation characteristics and a wide saturation region. In this work,

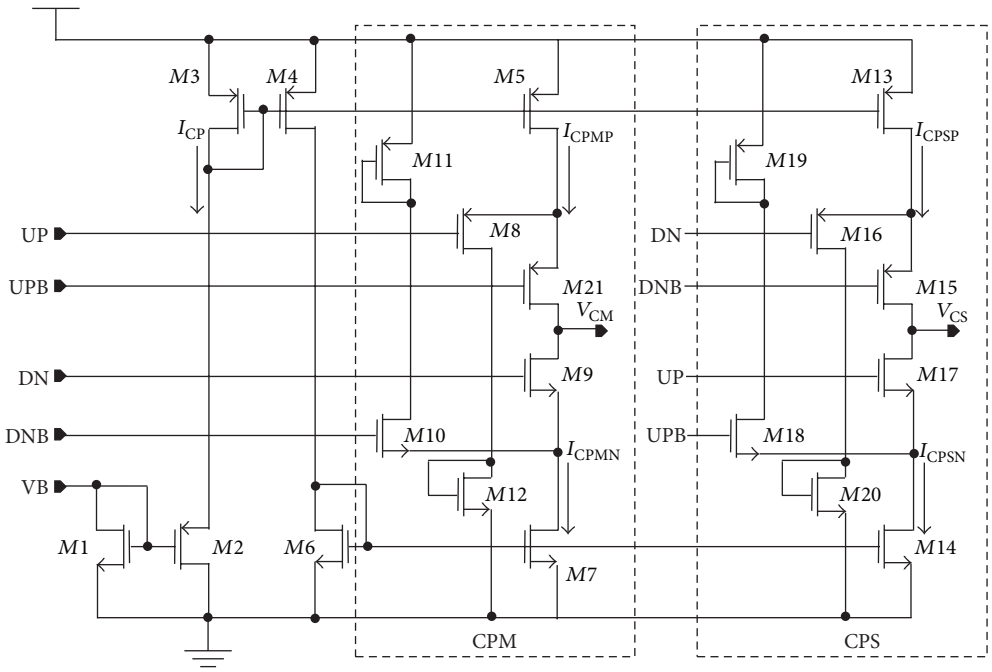
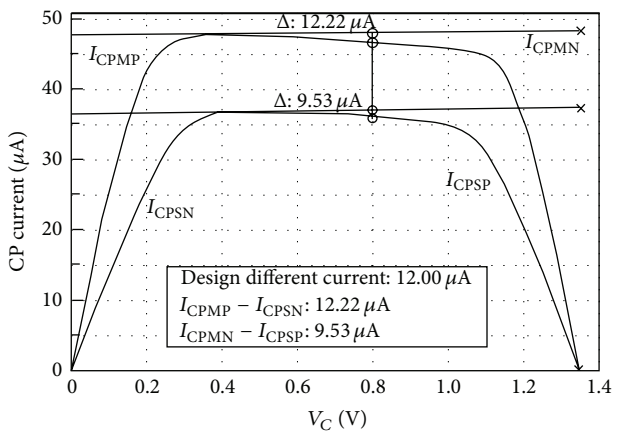


Figure 10: Circuit diagram of CP. The CP consists of the CPM and the CPS.



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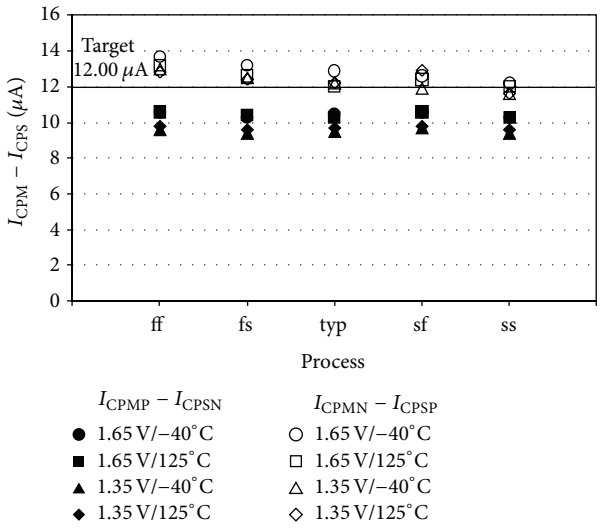


Figure 12: Simulation result of different CP current ($I_{CPMP} - I_{CPSN}$, $I_{CPMN} - I_{CPSP}$). Design target current is that I_{CPM} (I_{CPMP} and I_{CPMN}) and I_{CPS} (I_{CPSP} and I_{CPSN}) are 44 mA and 32 mA, respectively.

these problems are resolved merely by using a simple circuit design because other solutions, such as using an OpAmp or other additional circuits, increase design area and power consumption. The main reason for the difference between the design targets and simulation results is the channel length modulation. The NMOS length is designed to be long to decrease the effects of channel length modulation. Figure 12 shows the simulation results for the current difference between the main CP and the auxiliary CP. Since the main CP current and the auxiliary CP current are designed at 44 μA and 32 μA, respectively, the design target for the current difference is 12 μA. As shown in Figure 12, the variation of the current difference is designed at less than ±20%.

And then, this CP has offset between charge current and discharge current. This offset causes jitter. There are some techniques to overcome the offset. However, these techniques cause large power. In our SSCG, the main jitter sources are VCO and ΣΔ modulator and jitter is designed sufficiently even if the CP has offset. Therefore, the CP circuit as shown in Figure 10 is applied to prefer the power to the jitter.

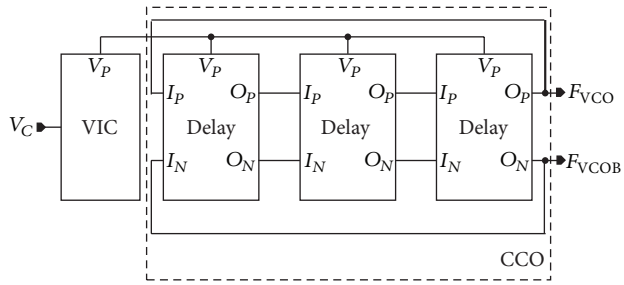


Figure 13: VCO block diagram [3].

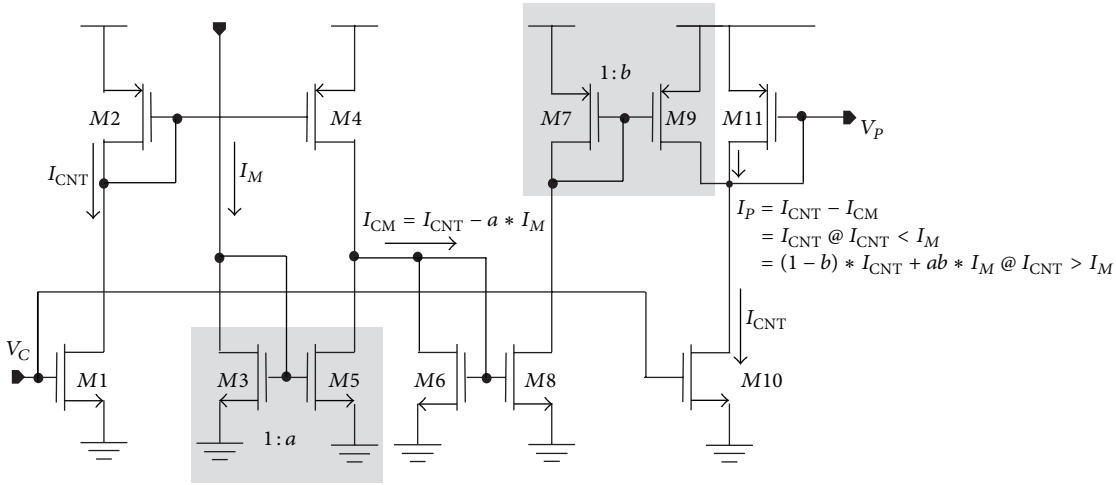


Figure 14: VIC circuit diagram [3].

5. VCO with High Frequency Limiter

The MMD can operate at less than 2.2 GHz under the worst condition. If the SSCG output signal frequency exceeds 2.2 GHz in the settling period due to the dual-CP control technique, the SSCG falls into an unlocked state. To prevent this malfunction, a VCO with a high frequency limiter is applied as shown in Figure 13 [3]. This VCO consists of a voltage-current converter (VIC) and a current-controlled oscillator (CCO) as shown in Figures 14 and 15. Figure 16 shows the explanation of the VCO with the high frequency limiter. The VIC converts a control voltage (V_C) to a control current (I_P). The VIC performs a high current limiter. The CCO generates output clock signals (F_{VCO} and F_{VCOB}) where the frequency is controlled by the I_P. Therefore, this VCO can perform the high frequency limiter. In the VIC, $M1$ converts the V_C to an I_{CNT}. An I_{CM} that is calculated as $I_{CNT} - I_M$ is generated at $M4$ drain node. The I_P that is a $M11$ drain current is calculated as $I_{CNT} - I_{CM}$. When the I_{CNT} smaller than the I_M, the I_P is the I_{CNT} because the I_{CM} is zero. On the other hand, when the I_{CNT} larger than the I_M, the I_P is calculated as $(1 - b) * I_{CNT} + ab * I_M$ that is nearly $ab * I_M$. The a and b are current mirror ratios of $M3 : M5$ and $M7 : M9$, respectively. The I_P is expected constant current against the V_C. However, if the I_{CNT} that is the $M1$ drain current is different from the I_{CNT} that is $M10$ drain current, the I_P may not be constant. The I_{CNT} that is $M10$ drain current is likely to be smaller than one of the $M1$ because the $M10$ has heavier loads that are the $M9$ and $M11$ than the $M1$. In this case, the I_P characteristics have negative slope against the V_C. These negative characteristics cause that SSCG falls into the unlock state because the SSCG loop may be positive feedback. To prevent from this malfunction, the current mirror ratio between the $M7$ and $M9$ is $1 : b$ in order that the I_P characteristics have positive slope against the V_C when the I_{CNT} is larger than I_M.

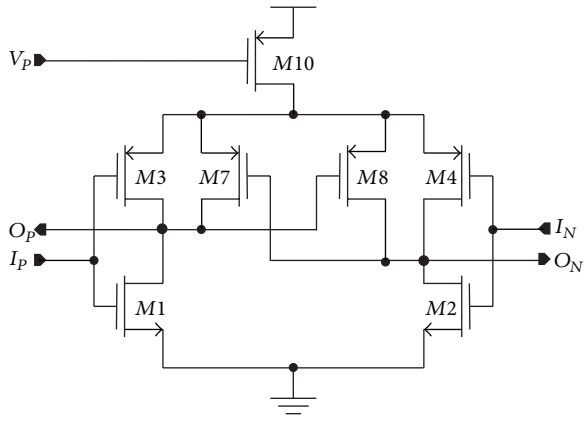
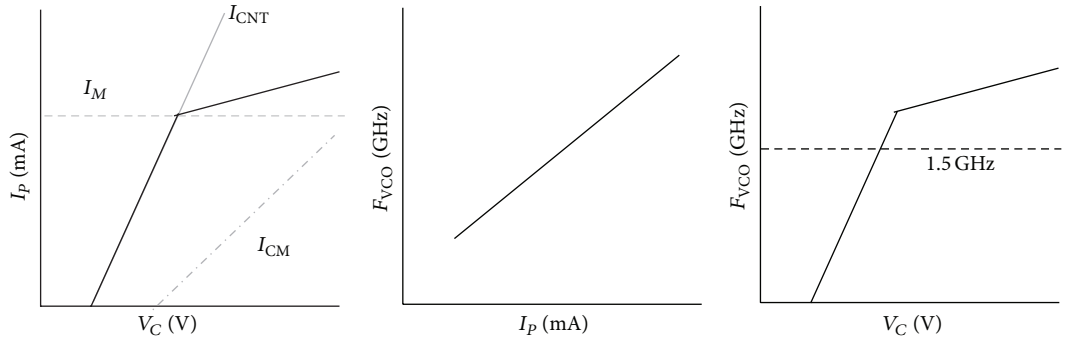


Figure 15: Delay cell circuit diagram [3].



(a) VIC (b) CCO (c) VCO

Figure 16: Explanation of the VCO with high frequency limiter [3].

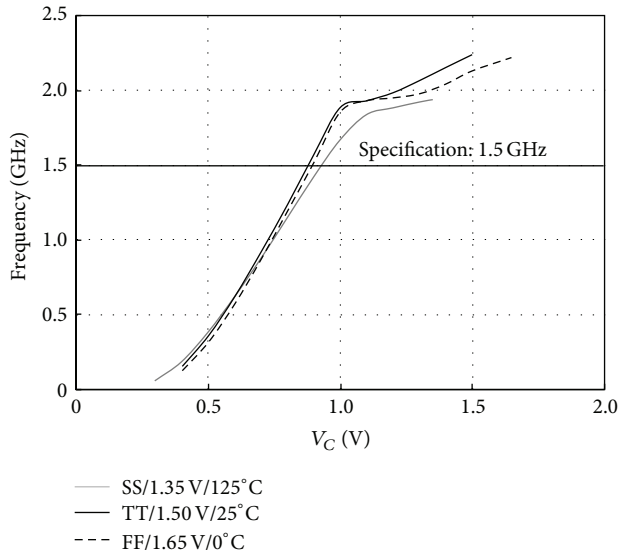


Figure 17: Postlayout simulation result of VCO frequency-voltage characteristics.

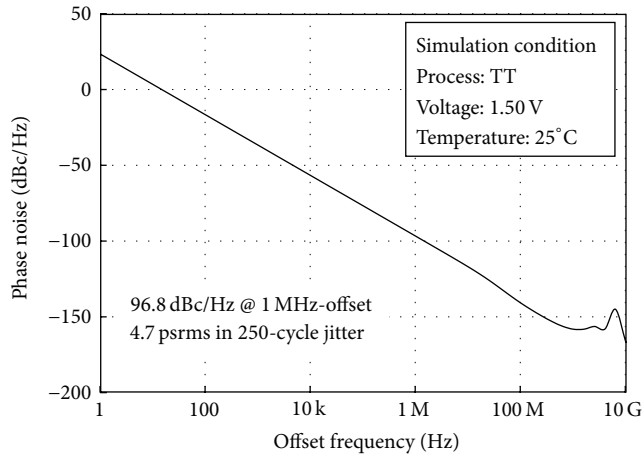


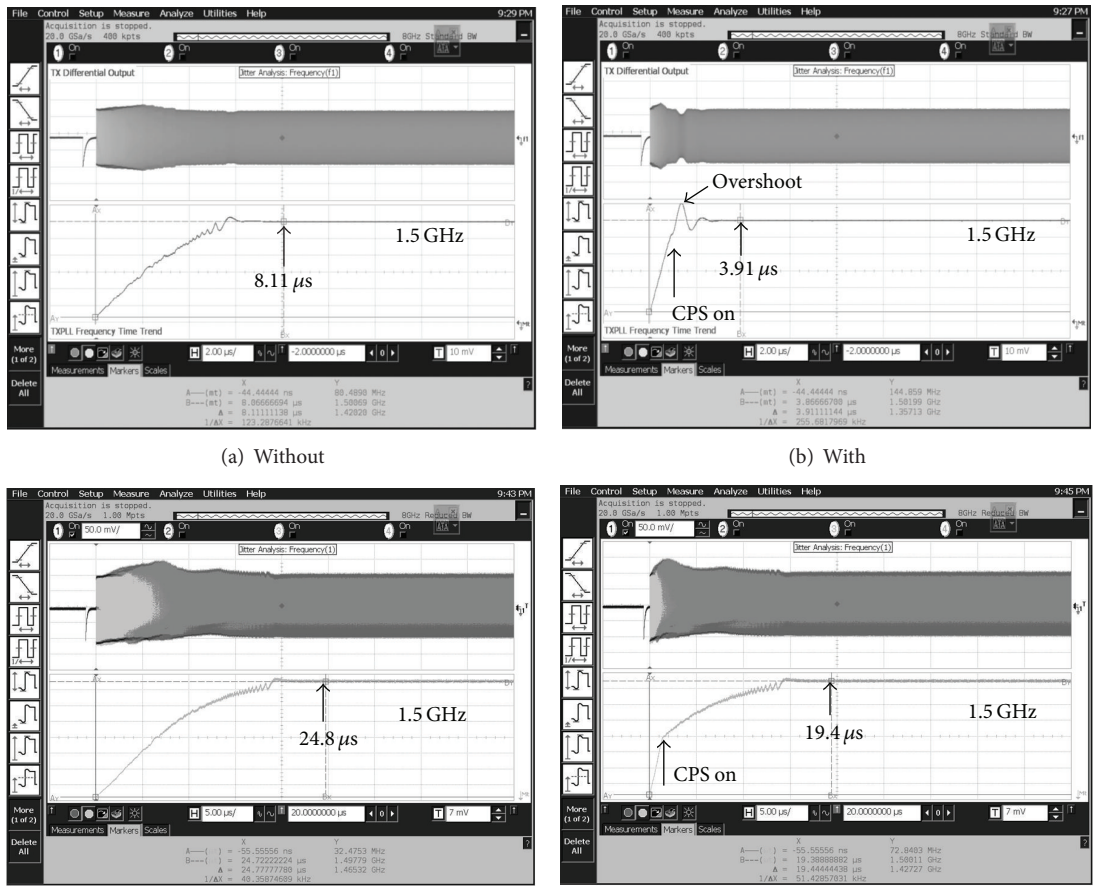
Figure 18: Postlayout simulation result of VCO phase noise characteristics.

Figure 17 shows the postlayout simulation results for the VCO frequency-voltage characteristics. As shown in Figure 11, the locking-point should be set at the range from 0.5 V to 0.8 V because the current differences ($I_{CPMP} - I_{CPSN}$ and $I_{CPMN} - I_{CPSP}$) are nearly equal to the design targets. The maximum frequency of the VCO output signal should be set at less than 2.2 GHz under the worst condition. As shown in Figure 17, the VCO oscillates at 1.5 GHz at about 0.8 V and the maximum frequency is less than 1.9 GHz under the worst condition.

Figure 18 shows the VCO phase noise characteristics in TT condition. The phase noise at 1 MHz offset frequency is 96.8 dBc/Hz. The jitter in 250-cycle is 4.7 psrms. Main jitter sources are thermal noise of the $M10$ and $M11$ in the VIC in Figure 14.

6. Measurement Result

We fabricated our SSCG using a 0.13 μm CMOS process. Figure 19 shows the settling-time results with and without the fast-settling dual-CP control technique. The sample is SS. In Figure 19, there are four results. Figures 19(a) and 19(b) show the fast settling-time setup of the SSCG without and with the proposed control. Figure 19(b) shows 4 μs settling-time by using proposed control technique. On the other hand, Figures 19(c) and 19(d) show the same setup as Figure 9 without and with proposed control to demonstrate the silicon results of the settling-time same as the simulation results as shown in Figure 9. The measurement condition is 1.35 V/125°C. In Figures 19(a) and 19(b), without proposed control technique, the settling-time was 8.11 μs as shown in Figure 19(a). With it, the settling-time was 3.91 μs, as shown in Figure 19(b), which is less than 4 μs. The CPS began operating at about 1.0 μs. Soon after, an overshoot appeared and the SSCG output signal frequency became nearly 2.2 GHz. However, the VCO with its high-frequency limiter prevented it from exceeding 2.2 GHz and leading to malfunctions. In Figures 19(c) and 19(d) that are shown to compare between simulation results in Figure 9 and silicon results in Figure 19. Without proposed control technique, measurement and simulation results are 24.8 μs and 22.5 μs, respectively. With control technique, measurement and simulation results are 19.4 μs and 18.2 μs, respectively. In the



(a) Without (b) With

(c) Without (d) With

Figure 19: Measurement result of the proposed SSCG settling-period. The sample is SS. Measurement condition is 1.35 V/125°C. Without proposed fast-lock dual-CP function (a), settling-period could be less than 8.11 ms. With function (b), settling-period could be less than 3.91 μs. (c) and (d) are same PLL parameter as Figure 9. Without function (c), measurement and simulation settling period are 24.8 μs and 22.5 μs, respectively. With function (d), measurement and simulation settling period are 19.4 μs and 18.2 μs, respectively.

settling-time, measurement results are similar to simulation results.

Figure 20 shows the measurement results for the SSCG output signal frequency. The signal was modulated by a triangular wave whose frequency was 31.5 kHz. The modulation deviation of the 1.5 GHz output signal was from +50 ppm to −4259 ppm, which met the SATA specification of from +350 ppm to −5000 ppm.

Figure 21 shows the measurement results of SSCG output signal spectrum. The EMI reduction was 10.0 dB with the SSC.

Figure 22 shows the measurement results for RJ and TJ under various conditions; the results met the SATA specification for all PVT variations. The RJ was less than 3.2 psrms. The domain jitter source was the VCO. The CP jitter due to the current mismatch of the dual-CP was far smaller than the VCO jitter.

Figure 23 shows the measurement result of the VCO frequency-voltage characteristics in worst condition. The 1.5 GHz locking frequency was achieved at 1.0 V. The maximum frequency is less than 2.2 GHz.

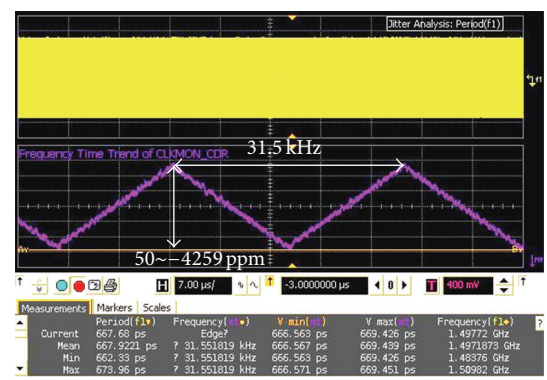
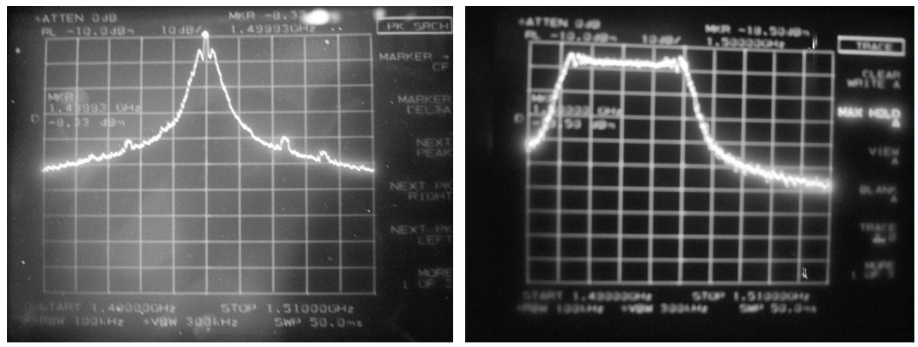


Figure 20: Measurement result of the output signal frequency modulated by triangular signal. Modulation frequency is 31.5 kHz and modulation deviation is from +50~−4259 ppm at 1.5 GHz.

Figure 24 shows the measurement results for the CP current. The CP currents were measured by using an output pin between the CP and the LF. When the I_{CPMP} was measured, the CPM was enabled and the CPS was disabled,



w/o SSC w/ SSC

Figure 21: Measurement results of the SSCG output signal spectrum with and without SSC.

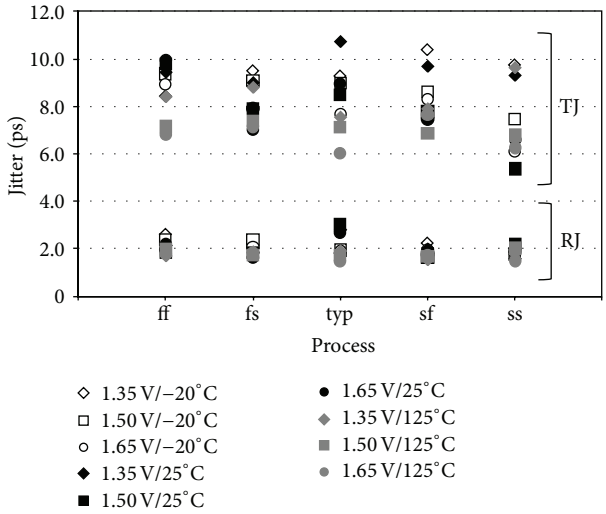


Figure 22: Measurement result of output signal jitter of RJ and TJ.

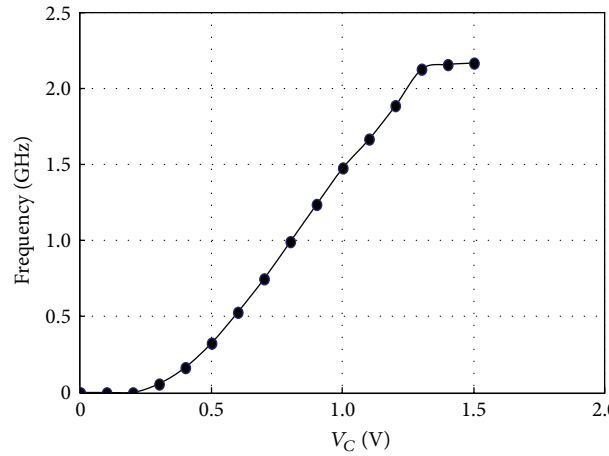


Figure 23: Measurement result of VCO frequency-voltage characteristics in worst condition (SS/1.35 V/125°C).

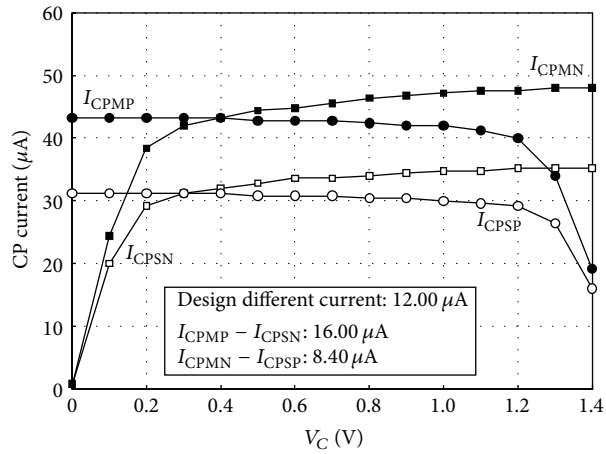


Figure 24: Measurement result of CP current.

and then the UP and the DN were set to high and low, respectively. The CPM currents (I_{CPMP} and I_{CPMN}) and CPS current (I_{CPSP} and I_{CPSN}) were designed at 44 μA and 32 μA, respectively. The NMOS currents (I_{CPMN} and I_{CPSN}) did not have accurate saturation characteristics due to channel length modulation.

Figure 25 shows the measurement results for the current difference between the CPM and CPS under various conditions. The design target for the current difference was 12.0 μA. The variation of the current difference was less than ±30%. Under the "ff" and "fs" conditions, the variation was larger than under the other conditions. This was because the channel length modulation caused the ratio of the current mirror consisting of PMOSs to deviate from the ideal ratio.

Our SSCG generated an output signal with a frequency of 1.5 GHz, which meets the SATA specification. As summarized in Table 1, its EMI was reduced by 10.0 dB, its power consumption was 18 mW, and its settling-time was less than 4 μs; the latter had been unachievable with previous SSCGs that applied to the SATA specifications [2–6].

Figure 26 shows a chip microphotograph. The design area was 300 × 700 μm. The 3.91 μs locking-time was faster than the other previous works. The proposed SSCG can make the SATA-PHY reduce the power in the partial state because the SSCG can be disabled. For portable devices, a battery lifetime

Table 1: Comparison table.

Item	Unit	[3]	[5]	[2]	[4]	This work
Output frequency	GHz	1.5	1.5	1.5	1.5	1.5
Random jitter @ 250 cycles	Ps rms	<3.3	—	5	3.2	<3.2
Total jitter @ 250 cycles	ps rms	<3.6	—	—	16.8	<10.7
EMI reduction	dB	10.0	8.2	—	9.8	10.0
Locking-time	μs	30	4.2	50	6.3	3.91
Technology	μm	0.13	0.13	0.18	0.18	0.13
Power	mW	30	12	27	77	18
Area	mm^2	0.3570	0.1120	0.2112	0.3100	0.2100

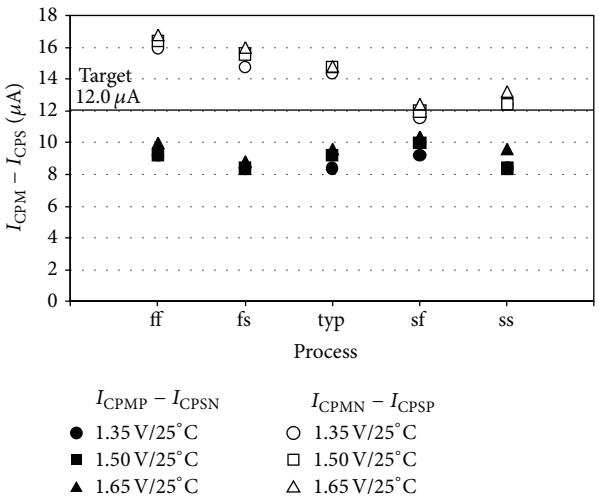


Figure 25: Measurement result of different CP current.

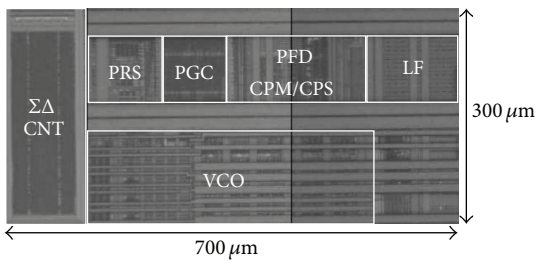


Figure 26: Test chip microphotograph.

is critical issue. Our proposed low power SATA-PHY can be one of the solutions to overcome the battery issue.

7. Conclusion

A fast-settling spread-spectrum clock generator (SSCG) for Serial Advanced Technology Attachment (SATA) application has been developed. The SSCG's settling time is shortened through the use of a charge-pump (CP) control technique. A prototype of our SSCG achieved 3.91 μs settling-time, 300 × 700 μm design area, 18 mW power consumption, 3.2 psrms random jitter, and 10.0 dB EMI reduction. A SATA-PHY with our SSCG consumes less power in the partial state in SATA applications because it can stop the SSCG. This makes it well suited for portable applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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