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Research Article

New Application's Approach to Unified Power Quality Conditioners for Mitigation of Surge Voltages

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This paper outlines a new approach for the compensation of power systems presented through the use of a unified power quality conditioner (UPQC) which compensates impulsive and oscillatory electromagnetic transients. The newly proposed control technique involves a dual analysis of the UPQC where the parallel compensator is modelled as a sinusoidal controlled voltage source, while the series compensator is modelled as a sinusoidal controlled current source, opposed to the traditional approach where the parallel and series compensators are modelled as current and voltage nonsinusoidal sources, respectively. Also a new compensation algorithm is proposed through the application of the theory of generalized reactive power; this is then compared with the theory of active and reactive instantaneous power, or *pq* theory. The results are presented by means of simulations in MATLAB-Simulink®.

1. Introduction

Currently, one of the main problems with power quality is the increase of electronic devices, which require a high level of waveform voltage quality to operate properly at both residential and industrial levels [1]. These electronic devices are mainly responsible for the deterioration of the power quality acting as nonlinear loads [2].

The capacitor-switching transients, or CST, constitute the most common cause of surge voltage, followed only for lightning in most systems [3]. These transients cause misoperation or faults in devices at both residential and industrial levels; therefore, this problem of power quality has recently gained more attention due to devices that use solid state electronics and are more sensitive to surges than their predecessors [4].

Custom power devices or CPDs used in distribution systems can control power quality problems such as voltage and current harmonics, poor power factor, unbalance at the source, load imbalance, and flicker [5, 6]. The most common CPDs are parallel compensators for current and power factor correction [7, 8] and the series compensators to compensate harmonic voltage, sag, swell, and flicker. One of the most efficient CPDs consists of parallel and series compensators with a common DC bus, which is called *unified power quality conditioner* or UPQC [1, 9, 10]. This combination allows the simultaneous compensation in the source current side via the parallel compensator and the load voltage side with the series compensator, thus isolating the system of power quality problems generated from the load and the load of problems from the source.

CPDs reference signals generation has been a major research problem. To date, generating reference signals for the compensation of most power quality problems has been widely studied; however, there is no compensation model for voltage surges through CPD. This is because the traditional model of compensation and estimation algorithms requires that the CPD generate a highly distorted wave and wide frequency range. Therefore, the focus on mitigating the transient has been focused on the *surge protective devices* (SPD) or limiter type switch as gas tubes, MOVs (Metal Oxide Varistors), and avalanche junction semiconductor devices [11].

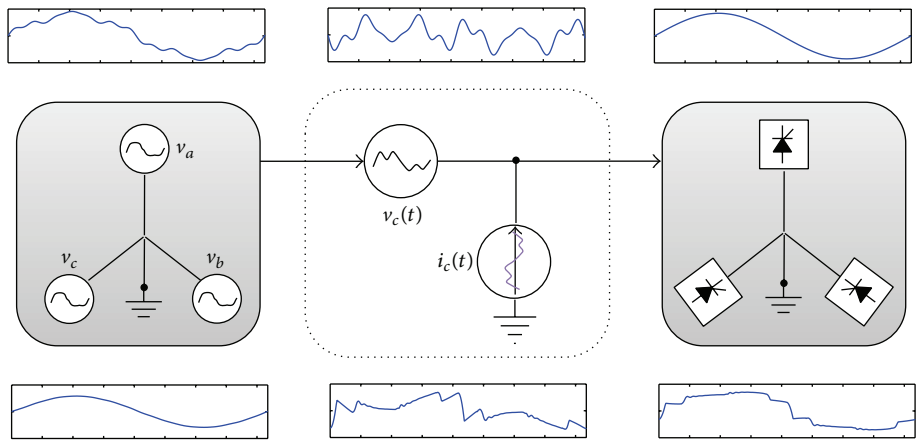

Figure 1: Classical scheme of compensation with the UPQC.

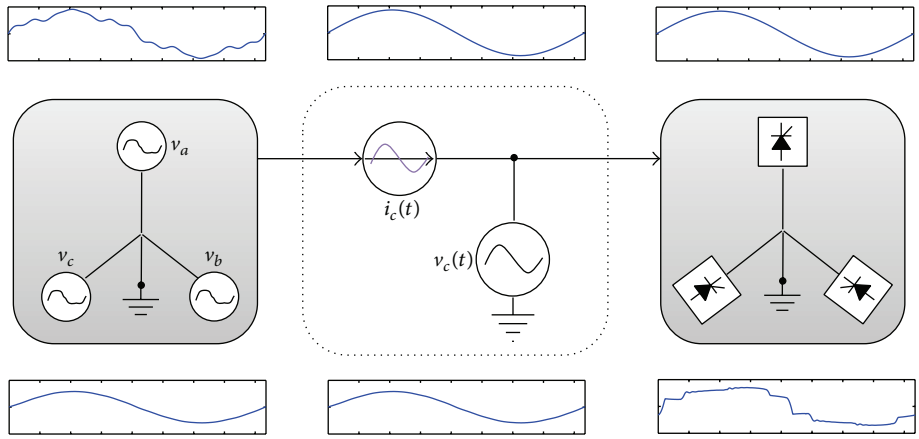

Figure 2: Dual scheme of compensation with the UPQC.

The main objective of this research is to develop a control technique and an algorithm for generating a reference signal that permits us to extend the use of CPD to compensate voltage surge.

In order to validate the proposed schematics, a power system compensation was undertaken in a test circuit by means of a simulation. It compensates low power factor, voltage and current harmonics, and oscillatory transient in voltage with a UPQC in dual topology.

2. Unified Power Quality Conditioner (UPQC)

2.1. Principle of Operation. The UPQC is composed of two power inverters in voltage source configuration VSI, connected back-to-back to a single DC bus. Each inverter acts like a controlled voltage and current sources.

In the classic model of compensation, the series compensator was modelled like a voltage controlled source that compensates the power quality problems in the voltage waveform. On the other hand, the parallel compensator acts like a current controlled source that removes the quality problems generated by the load current [9, 10]. This classical model of compensation is shown in Figure 1.

In [12–14], a new scheme of compensation is proposed for the UPQC, where the functions of the series and parallel compensators are invested, so that the series compensator acts like a sinusoidal current source that isolates the source from the power quality issues of the current in the load side. The parallel compensator functions like a sinusoidal voltage source that guarantees that the load is fed with a pure sinusoidal and sag-swell free voltage waveform. This model of compensation is called *dual* scheme of the UPQC and is illustrated in Figure 2.

The main advantage of the dual UPQC is that the waveforms that are needed to compensate the system are purely sinusoidal.

The general circuit of an electric power system with a UPQC is shown in Figure 3. The UPQC is composed of two three-leg VSI power inverters. The DC bus is composed of two capacitors with the middle point connected to GND; this configuration is called *three-leg split capacitor inverter* or *TLSC inverter*. The source has an impedance, R_{rd} and L_{rd}, in each phase.

The load is a nonlinear full controlled AC/CC converter that generates harmonic currents and a low power factor.

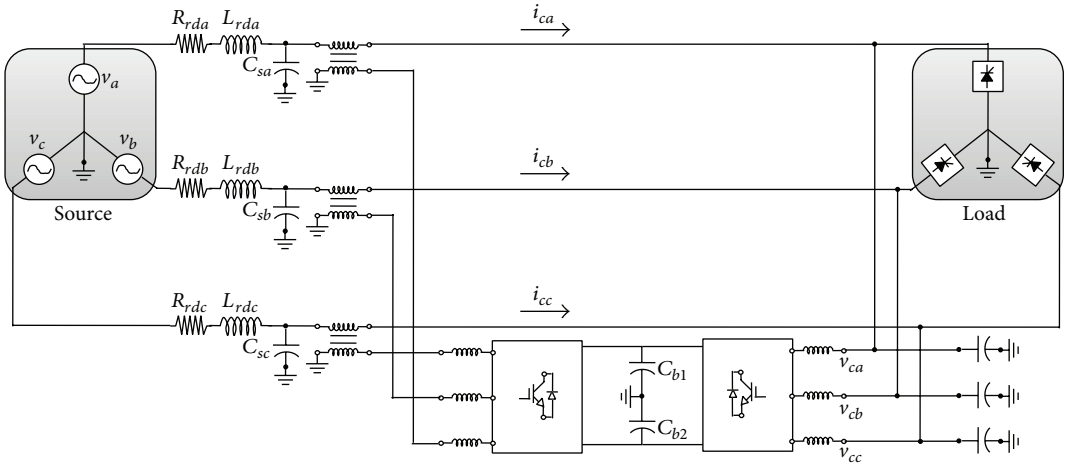

Figure 3: Circuit scheme of the UPQC.

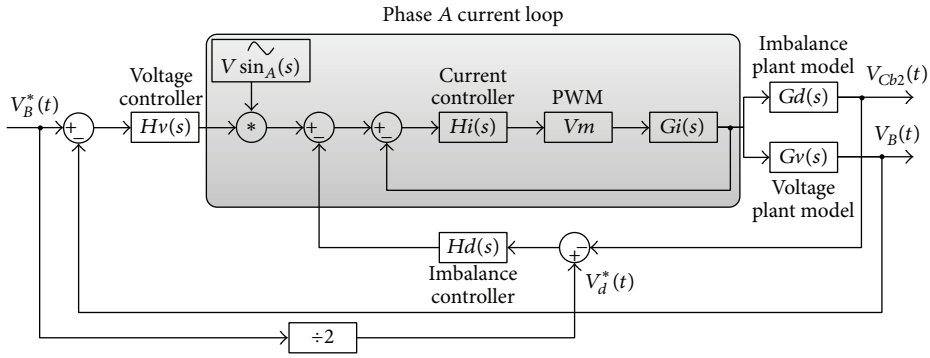

Figure 4: Block diagram of the UPQC control loops.

2.2. Control Scheme. The loop control for the UPQC is necessary to guarantee that the inverters generate efficiently the reference signals. The split capacitor structure has the main advantage that it allows us to make an uncoupled analysis of each phase of the series and parallel inverters.

The series compensator control is composed of four control loops. Since the dual model of compensation, the current control scheme proposed in this document is illustrated in Figure 4. The more internal control loop is the sinusoidal current controller of the source; it guarantees that the source current is sinusoidal and in phase with the voltage waveform. The intermediate loop is the imbalance control of the DC bus capacitors voltage, this controller must keep the same voltage in both capacitors, and this control loop acts like a DC current reference that charges or discharges the capacitors according to the difference in the value of the voltage between them.

Finally, the outer control loop in Figure 4 is the DC bus voltage control loop; this control keeps the voltage in the DC terminals of the inverters in a reference value, so that the UPQC can correct the power quality problems in the source and the load and has enough power to compensate sags and swells.

The space state model of the source's current loop is derived from the average model of the left-side inverter [15], so that the one per-phase circuit, referring to the primary of the coupled transformer, can be simplified in the circuit of Figure 5. Equation (1) is the space state model of the circuit:

$$\begin{bmatrix} V_B D(s) \\ 0 \end{bmatrix} = \begin{bmatrix} R_p + sL_{eq\_p} + Z_m & Z_m \\ Z_m & sL_{eq\_s} + R_{eq\_s} + Z_m \end{bmatrix} * \begin{bmatrix} I_{cs\_p}(s) \\ I_{cs\_s}(s) \end{bmatrix}. \quad (1)$$

The parallel compensator control loop has the main objective of providing the load with pure three-phase sinusoidal waveforms, balanced and with nominal value voltage. It has a unique control loop.

Every controller is designed in frequency with the methodology presented in [14]; then the transfer functions are discretized to be compensated with PID classical control schemes.

3. Generalized Reactive Power Theory Applied to Dual UPQC

In 2007 the generalized reactive power formulation applied to poly-phase systems was presented [16, 17]; this was defined later in 2010 as *instantaneous power tensor theory* [18, 19]. This

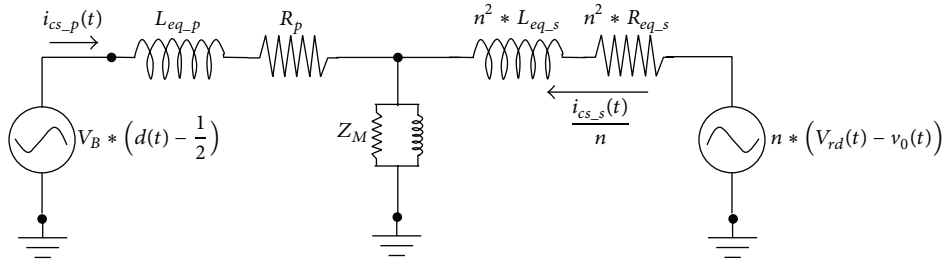

Figure 5: Simplified averaged circuit of the series inverter.

formulation is based on the interpretation of the instantaneous voltage and current vectors like first-order tensors to define the components of power from operations with *dyadic* or *tensorial* product.

From the instantaneous vectors of voltage and current, $\vec{u} = \mathbf{u} = [u_1 \ u_2 \ \cdots \ u_4]$ and $\vec{i} = \mathbf{i} = [i_1 \ i_2 \ \cdots \ u_4]$, in [16, 17] the active instantaneous power $p(t)$ and the imaginary instantaneous power $q(t)$ are defined according to (2) and (3), respectively:

$$p(t) = \vec{u} \bullet \vec{i}, \tag{2}$$

$$q(t) = \vec{i}(t) \wedge \vec{u}(t). \tag{3}$$

In the previous equations ((2) and (3)), $\bullet$ and $\wedge$ operators denote the *dot* and the *outer product*, respectively. The outer product is an antisymmetrization of the *dyadic* or *tensorial product* which is denoted by the $\otimes$ operator, so that (3) can be rewritten like

$$q(t) = \vec{i}(t) \wedge \vec{u}(t) = \left(\vec{i} \otimes \vec{u}\right) - \left(\vec{u} \otimes \vec{i}\right). \tag{4}$$

Furthermore, the active component of the current is defined in

$$\vec{i}_p = \frac{p(t)}{\vec{u}^T \vec{u}} \vec{u} = \frac{(u_1 i_1 + u_2 i_2 + \cdots + u_n i_n)}{\vec{u} \bullet \vec{u}} \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{bmatrix}. \tag{5}$$

The total current demanded by the load is defined in

$$\begin{aligned} \vec{i} &= \frac{\left(\vec{i} \otimes \vec{u}\right)}{\vec{u} \bullet \vec{u}} \vec{u} = \frac{\left[\left(\vec{u} \otimes \vec{i}\right) + \left(\vec{i} \otimes \vec{u}\right) - \left(\vec{u} \otimes \vec{i}\right)\right]}{\vec{u} \bullet \vec{u}} \vec{u} \\ &= \frac{\left(\vec{u} \otimes \vec{i}\right)}{\vec{u} \bullet \vec{u}} \vec{u} + \frac{\left[\left(\vec{i} \otimes \vec{u}\right) - \left(\vec{u} \otimes \vec{i}\right)\right]}{\vec{u} \bullet \vec{u}} \vec{u} \\ &= \frac{\left(\vec{u} \otimes \vec{i}\right)}{\vec{u} \bullet \vec{u}} \vec{u} + \frac{\left(\vec{i} \wedge \vec{u}\right)}{\vec{u} \bullet \vec{u}} \vec{u} = \frac{p(t)}{\vec{u} \bullet \vec{u}} \vec{u} + \frac{q(t)}{\vec{u} \bullet \vec{u}} \vec{u}. \end{aligned} \tag{6}$$

Finally, the result is that the current can be decomposed in two components, an active component and a reactive or imaginary component like

$$\vec{i} = \vec{i}_p + \vec{i}_q. \tag{7}$$

From this formulation, the estimation of the reference to parallel compensators of current named *perfect harmonic cancellation* or *PHC* is given by

$$\vec{i}_{\text{ref}} = \vec{i} - \vec{i}^{+}_{p\_f}, \tag{8}$$

where $\vec{i}^{+}_{p\_f}$ is the instantaneous vector of direct sequence and fundamental frequency current, given by

$$\vec{i}^{+}_{p\_f} = \frac{\text{tr}\left(\overline{\wp}_{ij}\right)}{(1/T)\int_T \left(\vec{v}^{+}_f \cdot \vec{v}^{+}_f\right)} \vec{v}^{+}_f. \tag{9}$$

Equation (9) is current reference for the UPQC in dual topology because it is at fundamental frequency, positive sequence, and in phase with the fundamental component of the voltage. However, $\vec{v}^{+}_f$, called *direct sequence and fundamental frequency voltage vector* [18], is calculated by using the Fortescue transformation and the decomposing in Fourier series of a periodical waveform that is inadequate to compensate sags and swells because the decomposition of the expression in these events has shown $k \in \mathbb{R}$ factor in the amplitude of the voltage reference, and the current reference $\vec{i}^{+}_{p\_f}$ will be affected as in

$$\vec{i}^{+}_{p\_f} = k \frac{\text{tr}\left(\overline{\wp}_{ij}\right)}{(1/T)\int_T \left(\vec{v}^{+}_f \cdot \vec{v}^{+}_f\right)} \vec{v}^{+}_f. \tag{10}$$

As regards the aforementioned drawback, it is necessary to reconsider the calculation of $\vec{v}^{+}_f$. That is why we propose the use of $\vec{v}^{+}_{f\_u}$: that is, the *positive sequence and fundamental frequency unit voltage vector*. To extract this vector we use a phase locked loop in a synchronous reference frame *SRF-PLL* and a unit vector template generator *UVTG* [20] to obtain the three-phase sinusoidal signals in unitary amplitude and later getting

$$\begin{aligned} v^{+}_{f\_u\_a} &= \sqrt{2} V_{\text{RMS\_ref}} \sin\left(\widehat{\theta}\right), \\ v^{+}_{f\_u\_b} &= \sqrt{2} V_{\text{RMS\_ref}} \sin\left(\widehat{\theta} - 120\right), \\ v^{+}_{f\_u\_c} &= \sqrt{2} V_{\text{RMS\_ref}} \sin\left(\widehat{\theta} + 120\right). \end{aligned} \tag{11}$$

In (11), $V_{\text{RMS\_ref}}$ is the nominal voltage value of the load. The scheme to obtain θ is shown in Figure 6.

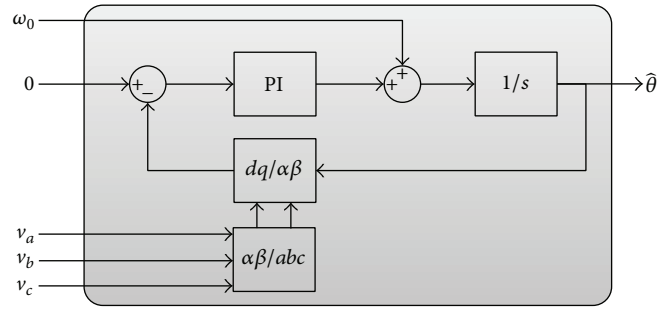

Figure 6: SRF-PLL scheme.

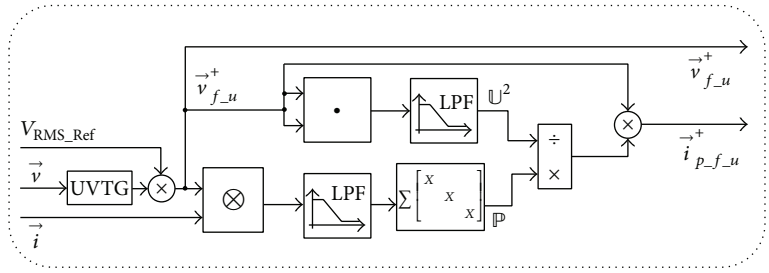

Figure 7: Reference signals generator scheme for the iUPQC with SRF-PLL and UVTG.

The expressions in (11) are the voltage reference signals for the *iUPQC*. With (11), (10) can be formulated like in

$$\vec{i}^{+}_{p\_f\_u} = \frac{\mathbb{P}}{\mathbb{U}^2}\vec{v}^{+}_{f\_u}, \tag{12}$$

where $\mathbb{U}$ is the average norm of the *positive sequence and fundamental frequency unit voltage vector* and $\mathbb{P}$ is the average active power to fundamental voltage that is provided in

$$\mathbb{P} = \vec{v}^{+}_{f\_u} \bullet \vec{i}. \tag{13}$$

The vector $\vec{i}^{+}_{p\_f\_u}$ has the three-phase current reference signals for the unified power quality conditioner; thus, the algorithm for the reference estimation in voltage and current in the *iUPQC* is fully developed in the scheme of Figure 7.

4. Simulation and Results

The simulated iUPQC is composed of a DC bus with split capacitor; the switching pulses are generated by PID discrete controllers compared with 20 kHz triangular signals. The series and parallel compensators have the function of compensating current in the source and voltage in the load, respectively (dual compensation). In addition, by means of the series compensator the DC bus voltage and the DC capacitors imbalance of voltage are controlled. The complete scheme implemented in MATLAB-Simulink is presented in Figure 8.

4.1. Simulation System Parameters

(i) *Source*. 115 V_{RMS}, 60 Hz. The harmonic pollution parameters are in Table 1. The source impedance is $R_{rd} = 0.04\,\Omega$ and $L_{rd} = 107\,\mu$H. In addition, in the voltage source occurs an oscillatory surge voltage or transient in 4.16 ms.

Table 1: Harmonic distortion in the voltage source per phase.

	$v_{f_{RMS}}$	$v_{5th_{RMS}}$	$v_{7th_{RMS}}$	$v_{11th_{RMS}}$	$v_{13th_{RMS}}$
v_a	115 V	15 V	0 V	5.7 V	5.7 V
v_b	115 V	15 V	15 V	0 V	5.7 V
v_c	108 V	12 V	12 V	5.4 V	0 V

(ii) *Load*. Composed of a fully controlled thyristors rectified bridge, with 40° phase angle, the impedance in DC side is a parallel RC load in series with an inductor; the values are $R = 75\,\Omega$, $C = 10\,\mu$F, and $L = 100$ mH.

(iii) *Series Inverter*. The series compensator is connected by means of $L = 20$ mH reactors and 1 kVA single-phase transformers with $n = 1$. The open circuit and short circuit parameters were measured. At source side a $C_s = 100\,\mu$F capacitor per phase is placed to mitigate the high frequency of the inverter.

(iv) *Parallel Inverter*. This is connected by $L_p = 650$ mH reactors and a high frequency RC filter with a capacitor of $C = 10\,\mu$F.

(v) *DC Bus*. These are two series capacitors with the middle point ground connected: each one is of 6 mF for a total capacitance of 3 mF.

4.2. Results. In Figure 9 results of compensation in the source current are shown. The series compensator enables us to follow the reference of the algorithm in the generalized reactive

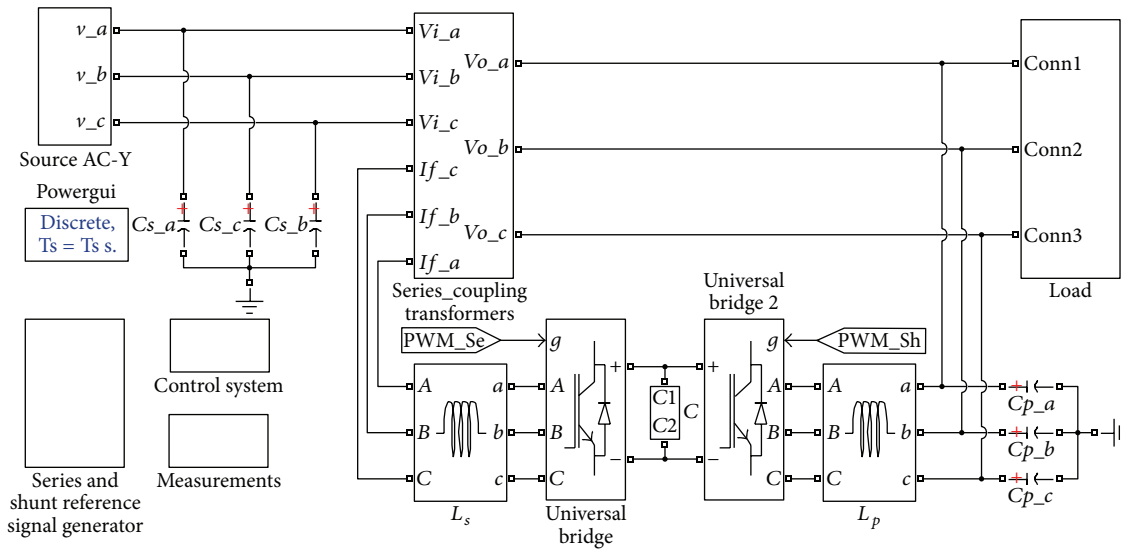

Figure 8: MATLAB-Simulink simulation algorithm.

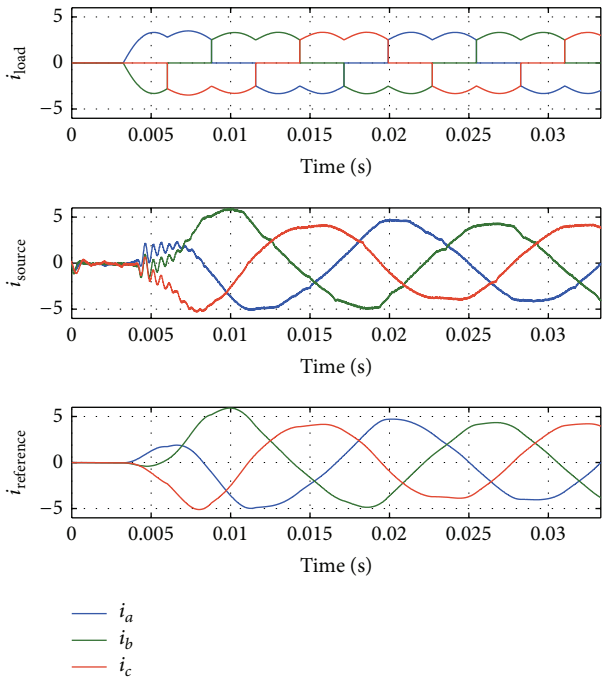

Figure 9: Current waveforms before and after compensation and reference signals.

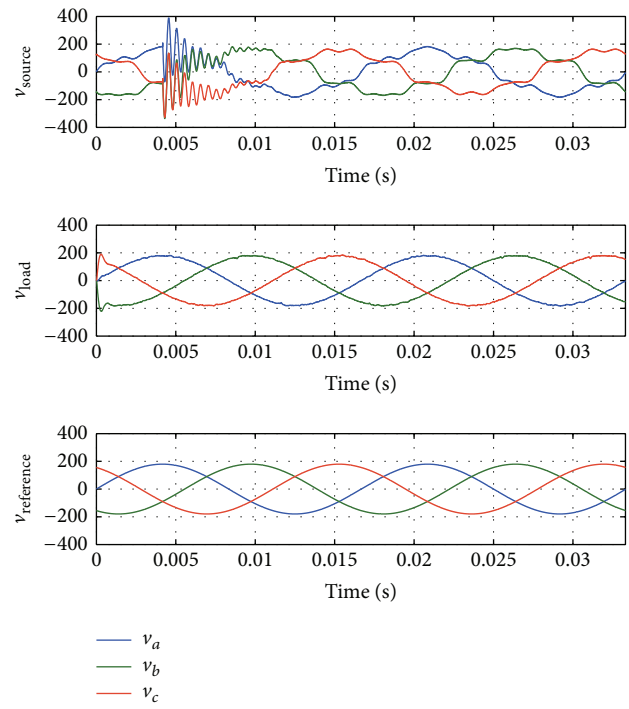

Figure 10: Voltage waveforms before and after compensation and reference signals.

power theory frame. Figure 10 shows the results of compensating the load voltage. In the three phases of the source system a surge voltage is generated (voltage corresponding to nonsynchronous closing in a capacitor bank [21]), but these do not affect the load by the action of the iUPQC. In the source current (Figure 9), we show that at the same time of surge voltage there is an oscillation; this is because of the interaction of the surge with the source impedance Z_{rd}.

The frequency results of compensation are summarized in Table 2. The per-phase harmonic distortion index was evaluated during and after the voltage surge for voltage and for the current before and after compensation THD.

Finally, in Figure 11 we show the comparison of the current signal reference estimation in a particular load case using the generalized reactive power theory with the proposed algorithm and the same reference estimation results of [12] derived with the instantaneous reactive power theory or *pq* theory.

Table 2: Per-phase THD values before and after compensation.

	THD before compensation with surge voltage	THD before compensation without surge voltage	THD after compensation
v_a	40.39%	14.96%	1.24%
v_b	41.88%	19.29%	1.10%
v_c	42.32%	16.51%	1.08%
i_a	NA	30.36%	3.45%
i_b	NA	30.26%	4.46%
i_c	NA	30.33%	3.43%

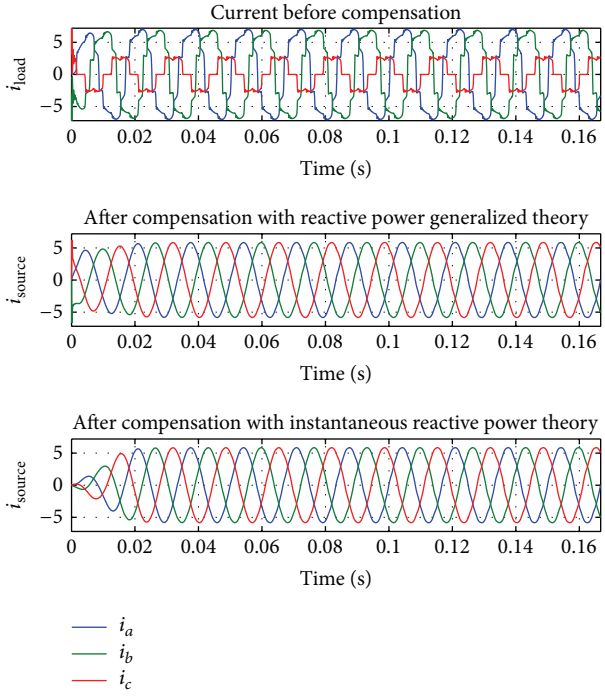

Figure 11: Current waveforms for a particular load and signal reference estimated with two different algorithms. Comparison of the proposed algorithm and [12] algorithm.

5. Conclusions

In this paper, we propose a new reference signal algorithm to estimate the references for a UPQC in dual topology using the generalized reactive power theory, and inverting the functioning of the compensators to work like sinusoidal voltage dependent source and sinusoidal current dependent source. This is called the dual of the traditional concept where the dependent sources are highly distorted. The results of the simulations show that the UPQC with the proposed algorithm is able to compensate highly distorted and imbalanced source currents with the series compensator, and at the same time it can compensate sag, swell, unbalance, and voltage harmonics with the parallel compensator. The proposed control approach for the UPQC has improvements in its functioning by the addition of the capability to compensate oscillatory transients and source voltage. Finally, the proposed algorithm is compared with the algorithm to estimate signals references by means of the instantaneous reactive power theory showing that the new one has a faster response in transients, therefore reaching the steady state in less time than the previously proposed algorithm.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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