Hindawi Publishing Corporation
Journal of Electrical and Computer Engineering
Volume 2016, Article ID 8202581, 9 pages
http://dx.doi.org/10.1155/2016/8202581

Research Article

A Low Noise, Low Power Phase-Locked Loop, Using Optimization Methods

Noushin Ghaderi, Hamid Reza Erfani-jazi, and Mehdi Mohseni-Mirabadi

Faculty of Engineering, Shahrekord University, Shahrekord 8818634141, Iran

Correspondence should be addressed to Noushin Ghaderi; ghaderi.nooshin@eng.sku.ac.ir

Received 6 April 2016; Accepted 17 August 2016

Academic Editor: M. Jamal Deen

A divider-less, low power, and low jitter phase-locked loop (PLL) is presented in this paper. An extra simple open loop phase frequency detector (PFD) is proposed which reduces the power consumption and increases the overall speed. A novel bulk driven Wilson charge pump circuit, whose performance is enhanced by some optimization algorithms, is also introduced to get high output swing and high current matching. The designed PLL is utilized in a 0.18 μm CMOS process with a 1.8 V power supply. It has a wide locking range frequency of 500 MHz to 5 GHz. In addition, through the use of a dead-zone-less PFD and a divider-less PLL, the overall jitter is decreased significantly.

1. Introduction

The role of a phase-locked loop or a delay-locked loop (DLL) is to generate a clock signal which is usually a multiple of a reference clock and is synchronized with the reference clock in phase. They are extensively utilized in many applications including clock data recovery systems and frequency synthesis circuits.

One of the most important components of the PLL and DLL, which is often considered as the bottleneck, is the phase frequency detector (PFD). The limited speed of this block is the main limiting factor in the data rate of the PLL. In high frequencies, the PFDs cannot follow the phase differences between reference and feedback clocks. Therefore, a frequency divider circuit is often inserted before the PFD block in the feedback path of the PLL. It means that the input clock frequency of the PFD is reduced. However, by adding the divider circuit, the overall jitter of the PLL will extremely increase. Thus, by designing a high frequency PFD, the divider circuit will be omitted and the noise behavior of the PLL will be improved [1].

Another important component of the PLL is charge pump circuit. It converts the output signal of PFD into an accurate amount of current. In practice, there are some nonidealities in the charge pump circuit. Reference spurs and phase offset are due to the current mismatch while the variations of the PLL loop bandwidth are caused by the variations of the output current amplitude. If the current matching and control voltage range of a charge pump circuit increase simultaneously, then the locking range frequency of the PLL will increase considerably.

In this paper a wide dynamic output voltage range, high impedance, and low power charge pump based on a novel bulk driven Wilson current mirror is presented. Some optimization algorithms are employed to improve the efficiency of the circuit.

2. Proposed PFD

The PFDs detect a phase error signal which is passed through a loop filter to control the delay of a controllable delay line. Therefore, in addition to determination of accuracy, a PD plays a key role in the speed and efficiency of PLL's performance.

A closed loop is the general structure used in the PFD because it is simple, easy to implement, and immune to the dead-zone problem. Because of the feedback path, however,

it has a limited speed which confines its usage in high speed circuits. Furthermore, some rising edges can be missed in the detection when the edges are overlapped with the reset signal [2]. Till now many circuits have been suggested to make the feedback path faster [3–6]; however the feedback path still remains in all of them which causes a reduction in the speed.

Authors in [7] proposed an open loop PD to achieve a high speed performance, without the issue of the reset signal. However, the PFD circuit tends to dissipate crowbar current when both input signals are high. It means that the circuit has some extra average DC power consumption.

The proposed circuit with a very simple structure solves the above problem. Furthermore, the proposed circuit solves the dead-zone and missing edge problems completely.

The task of a PD circuit is to compare the rising edge of two inputs (A and B in Figure 1) and generate a signal which is set to a high value with the rising edge of the first input and then is reset to a low value with the rising edge of the second one.

Figures 1(a) and 1(b) show the proposed PD, for Up and Down paths, which indicate two symmetrical and very simple circuits for Up and Down signals. The waveforms of the PD are shown in Figures 1(c) and 1(d). In Figure 1(c), A leads B. If initially $A = 0$ and $V(C_1) = V_{\text{dd}}$, then a rising transition on A leads to charge the output capacitor through C_1. Therefore, the Up output node will be set to the high value. The Up node stays in this state until rising transition on B. On the other hand, at the Down circuit with A at the high value, the $M6$ transistor will be on, keeping the down output at the low value. After the rising transition on B, $M5$ will turn on, causing the C_2 capacitor to discharge to the ground. Therefore, when A returns to the low value and $M6$ turns off, Down output will remain at zero value. The circuits operate in the opposite manner when A lags B (Figure 1(d)).

As can be observed, the above circuit is extremely simple and fast. Furthermore, due to the use of only three transistors in each path, the power consumption is considerably low. But the proposed PD still suffers from the following problems.

The first problem is as follows: Since the parasitic capacitance of C_1 node is smaller than the parasitic capacitance of the output node, the output node will not be charged through this node completely. Adding an additional capacitor to the C_1 node will add some problems such as extra chip area and longer rise and fall time.

The second problem is its dead-zone problem. This problem may occur when the inputs have a very small phase difference. Therefore, the output pulse may not find enough time to turn on the charge pump switches. To overcome the above two problems, the proposed PD is modified as shown in Figure 2, in which A_d and B_d are delayed waveforms of A and B signals. The ideal waveforms of two outputs are also shown in this figure.

Circuit performance is as follows: by delaying A and B signals on gates of $M1$, $M4$, and $M3$, the zero value of "up" signal will occur a few seconds later. As a result, a high level of "up" signal will become wider than the real amount and the phase difference will be shown more extensive than the actual value. This amount of broadness must be equal to the precharging time (T_{chp}) of the internal parasitic capacitances.

In Figure 2(c), A leads B. As can be seen, just after the rising transition on A, A signal will be set to the high value while A_d, which is the delayed waveform of A signal, still remains at the low value. Therefore, $M1$ and $M2$ turn on and the Up output will be set to the high value. In the same way, just after the rising transition on B, $M5$ and $M6$ turn on, consequently setting the Down output to the high value. With rising transition on B_d, both of the Up and Down outputs return to the low value. The circuits operate in the opposite manner when A lags B as shown in Figure 2(d).

According to [19], the time which is taken by the signal to change from low (high) value to 70% (30%) of high (low) value of logic states is called the gate rise time (or fall time). In this circuit, rise time and fall time make T_{chp}.

The sum of output rise time and fall time is calculated to estimate the maximum operational frequency of the proposed PFD.

$$
\begin{aligned}
t_{\text{rise(fall)}} &= 1.2\tau_{\text{rise(fall)}},\\
\tau_{\text{rise(fall)}} &= R_{\text{eq}_{\text{rise(fall)}}} C_L\\
R_{\text{eqrise}} &= r_{o1} + r_{o2},\\
R_{\text{eqfall}} &= r_{o3} + r_{o4}\\
C_L &= C_{db2} + C_{db3} + \frac{C_{dg2}C_{\text{Not}}}{C_{dg2} + C_{\text{Not}}} + \frac{C_{dg3}C_{\text{delay}}}{C_{dg3} + C_{\text{delay}}}\\
T_{\text{chp}} &= T_{\text{rise}} + T_{\text{fall}},
\end{aligned}
\tag{1}
$$

where τ is considered as time constant, R_{eq} is the equivalent resistant of the charging or discharging path at the output node (UP or DN), C_L is the output equivalent capacitance, C_{delay} is the delay gate, and C_{Not} is the Not gate equivalent capacitances.

By calculating the above equations, T_{chp} is obtained as 48.33 ps. Figure 3 shows that the dead zone is compensated by delay gates through the Not gate and precharging time.

$$T_{\text{chp}} = T_{\text{delay}} - T_{\text{Not}}. \tag{2}$$

T_{Not} and T_{delay} are delay times caused by Not gate and delay gate, respectively. The values of T_{delay} and T_{Not} are obtained as 64.43 ps and 16.1 ps, respectively. It means that the dead zone is entirely removed.

It is evident that the delay time in Figure 3 cannot exceed the value of 3/4 of the clock pulse width. Therefore, the minimum value of pulse width is 85.9 ps. As a result, the maximum frequency of the proposed PFD is obtained as 5.82 GHz.

The proposed PD is simulated in 0.18 μm CMOS technology by HSPICE software using level 49 parameters. The results are drawn in Figure 4 using MATLAB software. The figure shows the difference between average values of Up and Down signals versus the phase difference of two inputs at six different frequencies, 1–100 MHz, 1 GHz, 3 GHz, 4 GHz, and 5 GHz. Since the nonlinearity of the characteristic at the high frequency happens at large phase differences, where the polarity is more important than the magnitude, this

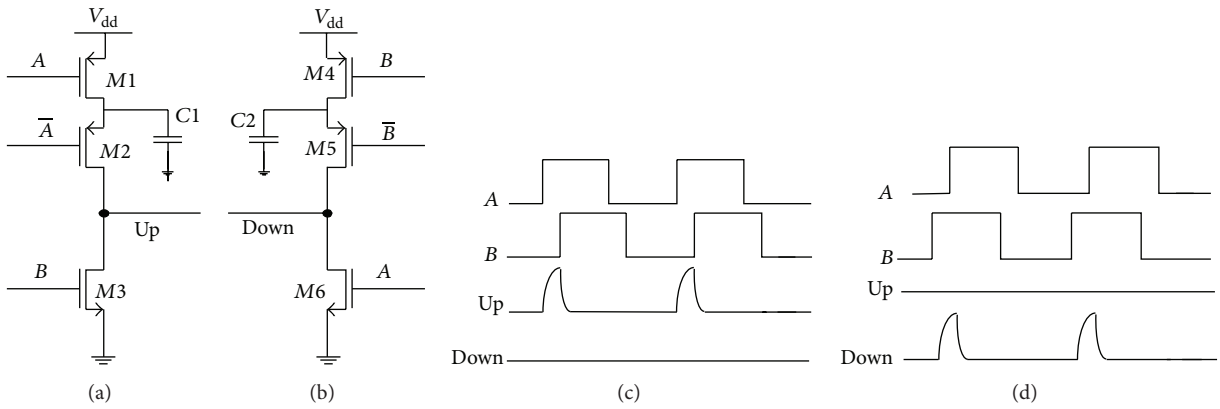

Figure 1: Proposed PD: (a) Up path. (b) Down path. (c) The waveforms of the PD when A leads B; (d) when A lags B.

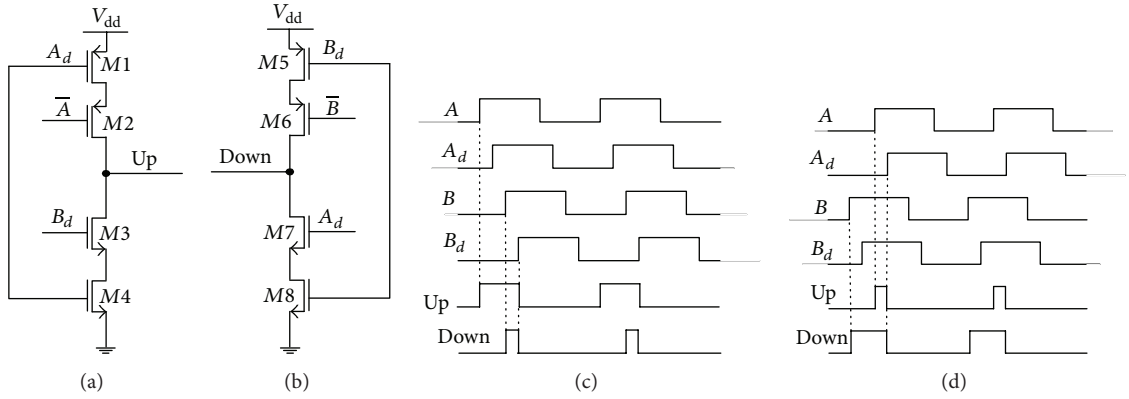

Figure 2: Modified PD: (a) Up path. (b) Down path. (c) The ideal waveforms of the modified PD when A leads B; (d) when A lags B.

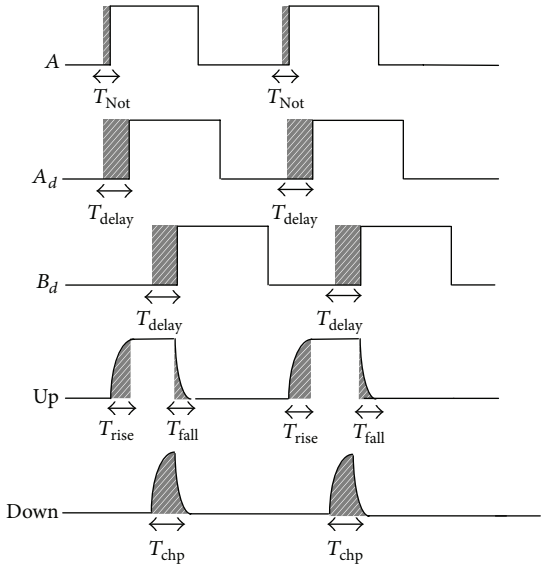

Figure 3: The realistic waveforms of the modified PD.

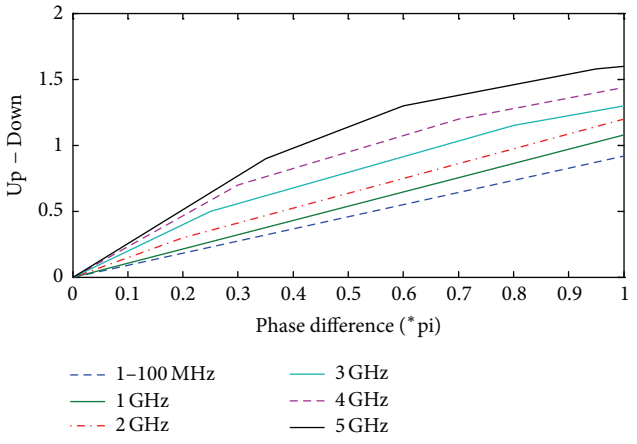

Figure 4: Difference between average values of Up and Down signals versus the phase difference of two inputs.

nonlinearity can be ignored. The diagram should be linear in small phase differences to minimize the locking time jitter of the PLL. The region around zero phase difference shows the accuracy of the PFD even at 5 GHz frequency. The power consumption of the proposed PD at 5 GHz frequency is about 0.3 mW. Table 1 summarizes these results and presents a performance comparison among this work and others.

Table 1: Performance comparison of the proposed phase detector.

Performance parameter	[3]	[8]	[9]	[10]	This work
CMOS tech	0.13 μm	0.35 μm	0.18 μm	0.13 μm	0.18 μm
Supply	1.2 v	3.3 v	1.8 v	1.2 v	1.8 v
Max freq. (GHz)	2.94	0.1	1	2.1	5 GHz
Dead-zone	NA	NA	Free	NA	Free
Power cons. (mW)	0.496 @ 128 MHz	NA	NA	NA	0.3
Structure	Closed	Open	Closed	Open	Open

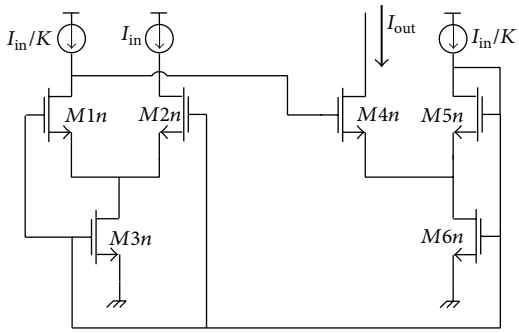

Figure 5: Proposed high swing Wilson current mirror.

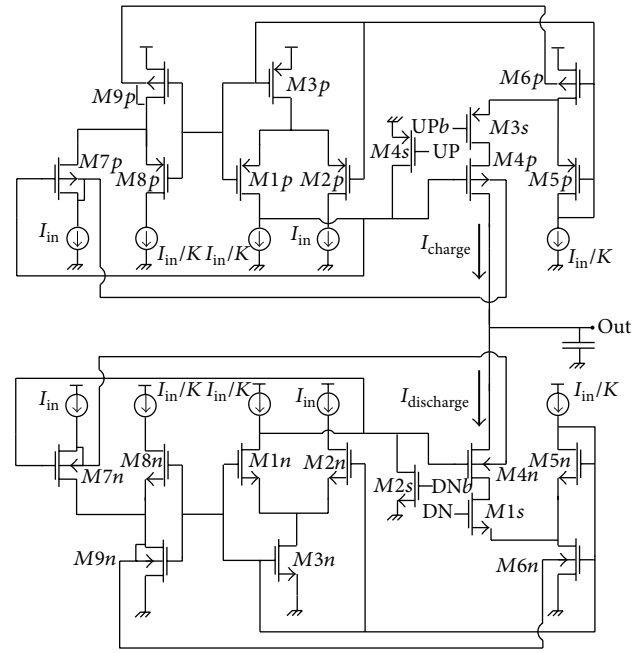

Figure 6: Proposed charge pump circuit.

3. Proposed Charge Pump Circuit

One of the most important components of the PLL is the charge pump circuit. An adaptive body bias charge pump circuit is proposed in [11]. In this circuit a number of resistances are used to compensate current variation. However, multiple parameters, such as temperature and fabrication, change the value of these resistances and are not reliable. The charge pump presented in [12] has used a compensation method to reach a high output swing. However the circuit structure is complicated. Moreover, in this circuit the power supply and hence the power consumption are placed high to achieve a high output swing. In order to increase the output voltage swing of the charge pump, in [13] a bulk driven method in a cascade structure has been used. However, using a cascade structure sets limitation to output swing.

A novel bulk driven, low voltage charge pump for high performance PLLs is proposed in this paper. This charge pump is designed based on Wilson current mirror by a novel bulk driven method. Output resistance and output swing are increased simultaneously.

The charge pump circuits must be designed to have a high output swing. However, there are some limitations in output swing, especially when transistors are placed in cascade form, to obtain the high output impedance. To overcome the above problem, bulk driven technique is employed in the proposed circuit. The proposed charge pump circuit is designed based on Figure 5. This circuit is a modified version of a super-Wilson current mirror [20]. As can be seen, the diode connection transistor of an ordinary circuit is replaced with a cascade one. Therefore, the loop gain is increased by a factor of $g_{m1n}r_{o1n}r_{o3n}$.

The proposed charge pump circuit is indicated in Figure 6. In this circuit $M1$s and $M3$s which are controlled by DN and UPb, respectively, act as charge pump switches. $M2$s and $M4$s are working for faster and better switching. When these MOSFETs turned on, the gate's capacitor of $M4n$ or $M4p$ will be discharged and turn off faster.

In the proposed circuit $M7n(p)$–$M9n(p)$ are used to connect the bulk terminals of $M4n(p)$ and $M6n(p)$ to a higher voltage in comparison with the circuit of Figure 5. It means that the source-bulk voltage (V_{SB}) is decreased. Therefore, according to (3), the threshold voltage (V_T) is reduced too. Equations (4) and (5) indicate that, by decreasing V_T, g_m and g_{mb} are increased and r_o is decreased.

$$V_T = V_{T0} + \gamma\left(\sqrt{\varphi_F + V_{SB}} - \sqrt{\varphi_F}\right), \tag{3}$$

$$g_m = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right),$$
$$g_{mb} = g_m\frac{\gamma}{2\sqrt{\varphi_F + V_{SB}}}, \tag{4}$$

$$r_o = \frac{2}{\mu C_{ox}\,(W/L)\,(V_{GS} - V_T)^2}. \quad (5)$$

In (6), by increasing g_{mM4n} and g_{mbM4n} and decreasing r_{oM4n} and r_{oM6n}, the output voltage swing is extremely increased.

$$\begin{aligned} V_{\text{out min}} &= V_{\text{DS}_{M4n}\,(\text{sat})} + V_{\text{DS}_{M6n}\,(\text{sat})} \\ V_{\text{DS}M4n} &= \left[I_{\text{discharge}} - \left(g_{mM4n} + g_{mbM4n}\right) V_{gs4}\right] r_{oM4n}, \\ V_{\text{DS}M6n} &= I_{\text{discharge}} r_{oM6n}. \end{aligned} \quad (6)$$

Output resistance is equal to

$$\begin{aligned} R_{\text{out}} \approx {} & \left[\left(g_{m1n} + g_{mb1n}\right) r_{o1n} r_{o3n} \left(g_{m4n} + g_{mb4n}\right) r_{o4}\right] \\ & \cdot \left\| \left[\left(g_{m1p} + g_{mb1p}\right) r_{o1p} r_{o3p} \left(g_{m4p} + g_{mb4p}\right) r_{o4p}\right]. \end{aligned} \quad (7)$$

One of the most important issues in bulk driven circuits is nonideal behavior of the MOSFETs due to their channel formations. The operation of the bulk driven MOSFET is similar to a Junction Field Effect Transistor (JFET). Because of nonlinear mathematical equations of the MOSFETs at low voltages, analysis of the circuit becomes complicated. For solving this problem, designers have compensated these nonidealities by choosing the aspect ratios of MOSFETs by trial and error (T&E) method [21]. Using of this method has been the only solution so far. In this paper in addition to T&E, MATLAB software is used to apply two methods of optimization algorithms to find the optimum aspect ratios. The main purpose is equalizing the charge and discharge current in a wide output voltage range to achieve the highest output current matching.

4. Tuning by Particle Swarm Optimization and Genetic Algorithm

In this paper, in addition to T&E, MATLAB software is used to apply two methods of optimization algorithms to find the optimum aspect ratios. The main purpose is to equalize the charge and discharge current in a wide output voltage range to achieve the highest output current matching.

To optimize the aspect ratios of *M*4*n*–*M*9*n* and *M*4*p*–*M*9*p* and choose the best values, Particle Swarm Optimization (PSO) and Genetic Algorithm (GA) are used.

4.1. Particle Swarm Optimization. Particle Swarm Optimization (PSO) was introduced in 1995 by Kennedy and Eberhart [22]. In PSO algorithm, a random population of points is generated. Each point represents a member of the population. In PSO algorithm, there is no sudden jump or confusion; each point is a solution. Considering X and V as particle position and velocity, respectively, the position of nth particle in a space with m dime is represented with $X_n = [X_{n1}, X_{n2}, \ldots, X_{nm}]$.

The position of each particle is changed at the next stage and it reaches a new position. The best position of nth particle which corresponds to the lowest cost function for that particle is saved in P_{best_n}. In addition, P_{best} of all particles are compared and the position of particle which has the lowest cost function is saved in G_{best}. The next vector of each particle depends on its position and its distance to its P_{best} and its distance to G_{best}. The relations of particles movements are as follows:

$$\begin{aligned} V_{nm}^{i+1} &= w \times V_{nm}^{i} + C_1 \times \text{rand}\,() \times \left(P_{\text{best}_{nm}} - X_{nm}^{i}\right) \\ &\quad + C_2 \times \text{rand}\,() \times \left(G_{\text{best}} - X_{nm}^{i}\right), \\ X_{nm}^{i+1} &= X_{nm}^{i} + CV_{nm}^{i+1}, \\ \left|V_{nm}^{i+1}\right| &\le V_{\max}, \end{aligned} \quad (8)$$

where $V_{\max}$ indicates a parameter that prevents going out of suitable search space which causes the solution to be in acceptable region; C_1 and C_2 are constants which represent the speed of learning or pulling to P_{best} and G_{best}, and the weighing function w is given by

$$w = w_{\max} - \frac{w_{\max} - w_{\min}}{\text{iter}_{\max}} \times \text{iter}, \quad (9)$$

where $w_{\min}$ and $w_{\max}$ indicate the minimum and maximum weighing functions and iter denotes the number of iterations.

In order to optimize the parameters of the controller by PSO, the following cost function is used:

$$\text{PSO} = \int_0^{t_1} |e\,(t)|\,dt = \int_0^{t_1} \left|i_{\text{discharge}} - i_{\text{charge}}\right| dt, \quad (10)$$

where t_1 is the final time of simulation, e is the error signal, and t_s is the settling time of the system.

4.2. Genetic Algorithm. Genetic Algorithm is a search-based optimization method [23]. This algorithm has been proposed by John Holland (1962). In the algorithm, he has benefited from two principles of selection and reproduction in the nature. Genetic Algorithm can be considered as an oriented random optimization method which gradually moves towards optimal point.

Unlike other common optimization models in which only one point is used in each stage of optimization process, in Genetic Algorithm, a group of points are used.

If our optimization target function is as

$$F = f\,(x_1, x_2, \ldots, x_n), \quad (11)$$

then, the objective is to find the value of x_i in such a way that F function has the minimum value. In Genetic Algorithm, at the first stage, a set of chromosomes are randomly created (random strings from x_1 to x_n). These x_i refer to genes. Putting each of these chromosomes in target function, the value of F function is obtained. The first generation concludes through appropriate scoring to these values. The first generation is called parents generation.

The process of creating offspring (children) in the next generations follows the following three general principles:

(a) Crossover

(b) Elite

(c) Mutation.

Table 2: Aspect ratio values of MOSFETs at different methods.

	$M4n$	$M5n$	$M6n$	$M4p$	$M5p$	$M6p$
PSO	107	328	169	91	718	268
GA	287	344	261	137	662	363
T&E	43	327	111	53	795	222

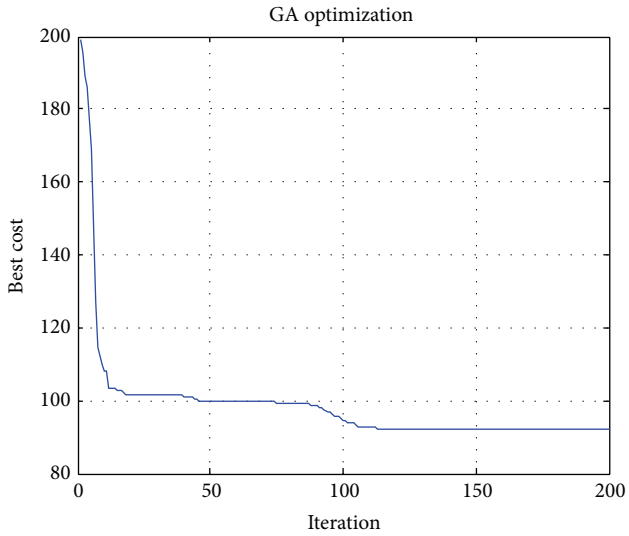

Figure 7: Convergence objective function for Genetic Algorithm.

After the second generation and after creating offspring with ratios determined by selection algorithms, new generation children are selected. Putting these children into target function and scoring them, then, the algorithm is reiterated until the algorithm meets the ending criteria (such as the number of generation and time), causing the algorithm to be stopped.

4.3. Results Optimization. In this study, the values of transistors aspect ratio are optimized using the following considerations.

It should be noted that aspect ratios of $M4n(p)$ equal $M7n(p)$, $M5n(p)$ equal $M8n(p)$, and $M6n(p)$ equal $M9n(p)$. The aspect ratios of the MOSFETs should be positive.

In the present study, the number of the algorithm iterations is the stopping criterion. Both PSO and GA are simulated using the following two sets of parameters:

(a) parameters iteration = 100 and population = 30,

(b) parameters iteration = 200 and population = 50.

The results pertained to the target function optimization of (10) have been shown in Figures 7 and 8. The respective figures, in fact, indicate cost function improvement for the increase in the number of iterations.

The results of T&E and optimal value factor's aspect ratios are presented in Table 2.

To verify the efficiency of the proposed circuit, it is simulated under the power supply of 1.8 V in 180 nm CMOS technology using Hspice. Input current is set to 20 μA. Figure 9 shows the charge and discharge output currents of

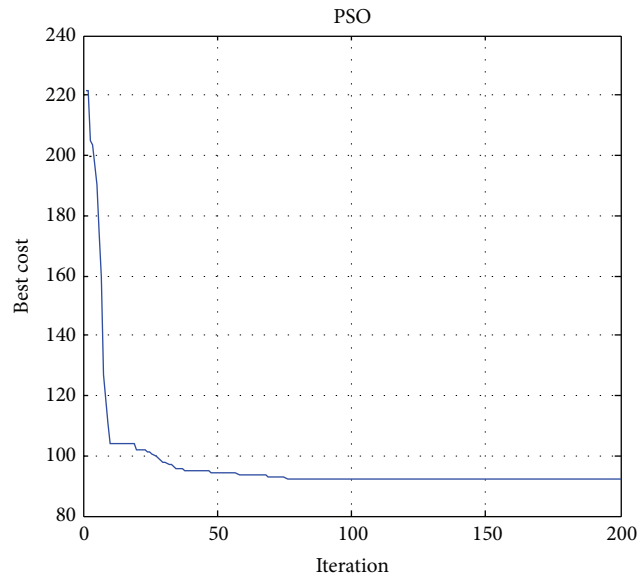

Figure 8: Convergence objective function for Particle Swarm Optimization.

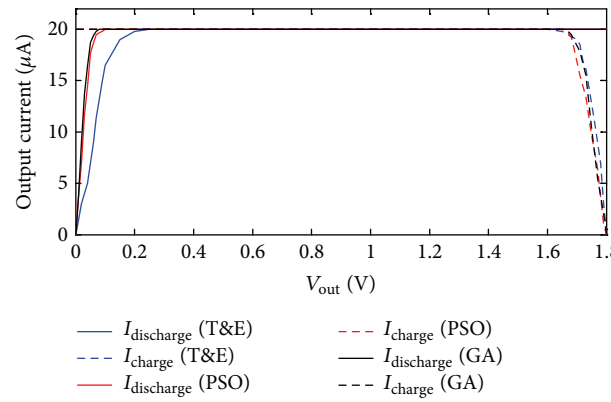

Figure 9: Matching characteristic of the proposed charge pump.

the proposed charge pump which are obtained from T&E, PSO, and GA methods as the output voltage is swept from 0 to 1.8 V. As can be seen, the output dynamic voltage ranges of output current matching are 0.25–1.6 V, 0.1–1.65 V, and 0.08–1.65 V for T&E, PSO, and GA, respectively. According to these results, the GA method makes a better performance to this charge pump. Therefore, the aspect ratios which are presented by the GA are chosen for applying to the proposed charge pump. Current mismatch is less than 1% of nominal output current (I_{charge} or $I_{discharge}$) over the output range of these methods.

In the usual bulk driven current mirror, the gate terminals are tied to V_{dd} [24]. However, in these circuits, the output current cannot track the input current in a specified range [13]. Figure 10 shows the variations of output current versus input current in the proposed circuit. As can be seen, the output current can track the input current in a wide input current range. The overall power consumption of the proposed charge pump circuit is around 160 μW. Table 3

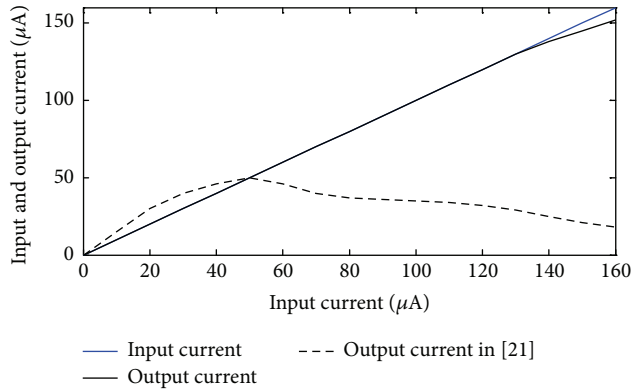

Figure 10: Input and output current transfer characteristics.

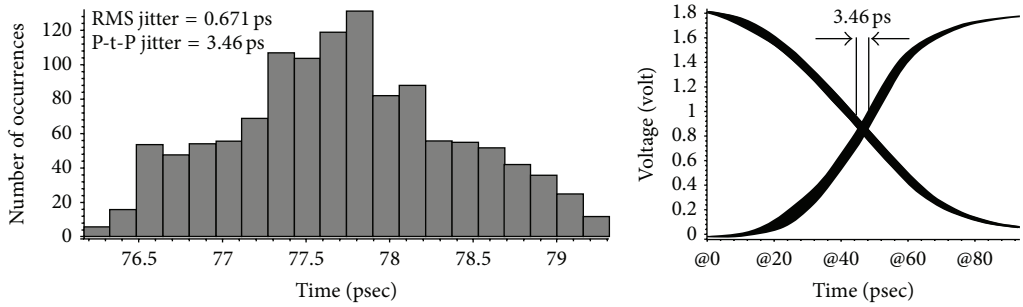

Figure 11: (a) Output jitter histogram at 3 GHz. (b) Output jitter eye diagram at 3 GHz.

Table 3: Performance comparison of the proposed charge pump.

	[11]	[12]	[13]	This work
CMOS tech (nm)	130	180	180	180
Power supply (V)	1.2	3	1.8	1.8
Voltage swing (V)	0.2–1	0.2–2.7	0.3–1.58	0.08–1.66
Swing/V_{dd}	66%	83.3%	71%	88%
Current mismatch	0.9%	2.1%	1%	1%
Power consumption (μW)	30	NA	395	160

summarizes the performance of the proposed charge pump and compares them with recent publications. As can be observed, the proposed circuit has an excellent voltage swing per V_{dd}, while its power consumption is reasonable.

5. Simulation Results of Proposed PLL

The PLL is designed using the proposed PFD and charge pump circuits. Furthermore, it employs a two-stage voltage controlled ring oscillator [18]. This PLL has a wide locking range from 500 MHz to 5 GHz.

Jitter histogram and eye diagram at 3 GHz operating frequency are depicted in Figure 11, which shows around 0.671 ps and 3.46 ps RMS and peak-to-peak jitters, respectively.

Figure 12 shows the output spectrum simulated at 3 GHz. The simulation result shows a reference spur of −72 dBm with a 1.85 GHz frequency offset. The phase noise of the PLL at the locking frequency in different frequency offsets is presented in Figure 13. The output phase noise is −117.6 dBc/Hz at a 1 MHz frequency offset. The total power consumption is about 11.5 mW. The figure of merit of the proposed PLL according to (12) [25] is −198.47 dBc/Hz.

$$\mathrm{FOM} = L\{\Delta f\} - 20\log\left\{\frac{f_0}{\Delta f} \times \frac{\mathrm{FTR}}{10}\right\} + 10\log\left\{\frac{P_{\mathrm{diss}}}{1\,\mathrm{mW}}\right\}, \tag{12}$$

where $L\{\Delta f\}$ is phase noise, Δf is certain frequency offset, f_0 is center frequency, P_{diss} is the power dissipation, and FTR is tuning range of oscillation frequency.

Table 4 summarizes these results and presents a performance comparison of this work with some recent papers. The proposed PLL achieves lowest FOM_T by using a fast PFD circuit and omitting the divider circuit.

6. Conclusion

A very simple, low power, high speed, and open loop phase detector is proposed which operates in a wide frequency range from 1 MHz to 5 GHz. Due to the extra simplicity of the circuit, the power consumption is very low and is about 0.3 mW at the highest operational frequency. The dead-zone and missing edge problems are solved completely in

Table 4: A performance comparison of proposed circuit with some recent papers.

Performance parameter	[14]	[15]	[16]	[17]	[18]	[7]	This work
CMOS tech (nm)	65	65	65	65	90	180	180
Supply voltage (v)	1	1.2	1.2	1	1.2	1.8	1.8
VCO	Ring	Ring	LC	Ring	Ring	Ring	Ring
Ref. frequency (GHz)	0.645	0.64	104	1.6	0.01	5	3
Locking range (GHz)	0.485–1.011	0.25–1.06	103.05–104.58	NA	3.5–7.1	2.5–7.3	0.5–5
Ref. spur (dBm)	NA	−54.8	−63.8	−47	−64.8	−66.8	−72
Phase noise @ 1 MHz offset (dBc/Hz)	−110.8	−88.6	−80.41	−88	−105	−108.2	−117.6
RMS jitter (ps)	NA	9.6	2.44	4.82	3.8	0.88	0.671
P-t-P jitter (ps)	NA	52.2	18	38	NA	3.21	3.46
Power (mW)	10	1.2	63	0.99	29.64	13.4	11.5
FOM @ 1 MHz offset (dBc/Hz)	−157	NA	−162.57	NA	NA	−190.55	−198.47

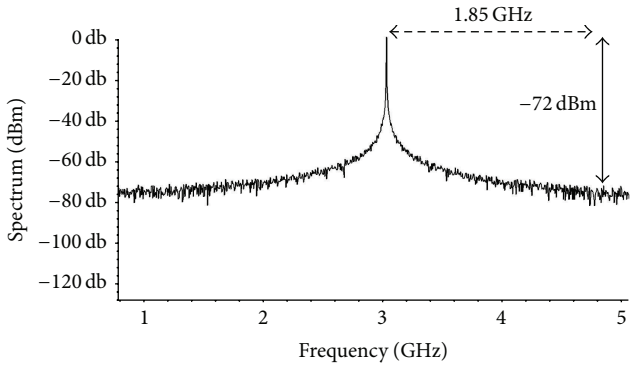

Figure 12: Output spectrum of the VCO.

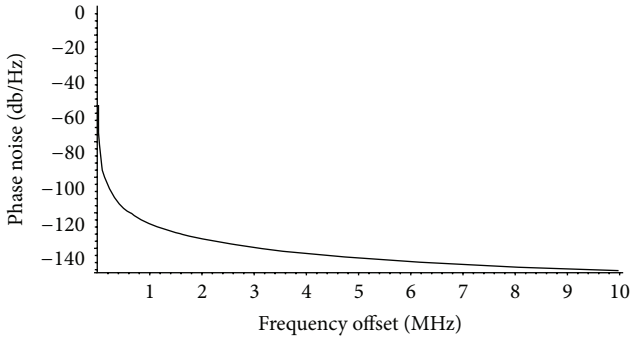

Figure 13: Simulated phase noise at 3 GHz for different frequency offsets.

the proposed architecture. A high output impedance, low power, and single-ended charge pump based on a bulk driven Wilson current mirror, with excellent output current matching, is also introduced in this paper. The proposed charge pump aspect ratios parameter was optimized by PSO and GA. Therefore, the dynamic voltage range was increased significantly which is obtained about 88% of power supply. The current mismatch between charge and discharge current is less than 1% of nominal output current. Therefore, through the use of a dead-zone-less PFD and a divider-less PLL, the overall jitter is decreased significantly. However, since a single ended charge pump architecture has a higher substrate and supply noise coupling, a differential charge pump circuit can be considered as a future work. Moreover, the operating frequency range can be increased by tracking the self-oscillation frequencies of the voltage-controlled oscillator (V_{CO}) and the frequency divider. The rms and peak-to-peak jitters of this PLL at 3 GHz are 0.671 and 3.46 ps, respectively.

Competing Interests

The authors declare that they have no competing interests.

References

[1] R. Prakash, S. Akhtar, and P. T. Balsara, "Phase noise reduction in high speed frequency divider," in *Proceedings of the IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software (DCAS '06)*, pp. 83–86, IEEE, Richardson, Tex, USA, October 2006.

[2] K. Park and I. C. Park, "Fast frequency acquisition phase frequency detectors with prediction-based edge blocking," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '09)*, pp. 1891–1894, IEEE, Taipei, Taiwan, May 2009.

[3] W.-H. Chen, M. E. Inerowicz, and B. Jung, "Phase frequency detector with minimal blind zone for fast frequency acquisition," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 12, pp. 936–940, 2010.

[4] N. M. H. Ismail and M. Othman, "CMOS phase frequency detector for high speed applications," in *Proceedings of the 21th International Conference on Microelectronics (ICM '09)*, pp. 201–204, IEEE, Marrakech, Morocco, December 2009.

[5] R. Y. Chen and W.-Y. Chen, "A high-speed fast-acquisition CMOS phase/frequency detector for MB-OFDM UWB," *IEEE Transactions on Consumer Electronics*, vol. 53, no. 1, pp. 23–26, 2007.

[6] L.-K. Soh and Y.-F. K. Edwin, "An adjustable reset pulse phase frequency detector for phase locked loop," in *Proceedings of the 1st Asia Symposium on Quality Electronic Design (ASQED '09)*, pp. 343–346, IEEE, Kuala Lumpur, Malaysia, July 2009.

[7] H. R. Erfani-Jazi and N. Ghaderi, "A divider-less, high speed and wide locking range phase locked loop," *AEU—International Journal of Electronics and Communications*, vol. 69, no. 4, pp. 722–729, 2015.

[8] S. Kazeminia, K. Hadidi, and A. Khoei, "A low jitter 110 MHz 16-phase delay locked loop based on a simple and sensitive phase detector," in *Proceedings of the 2013 21st Iranian Conference on Electrical Engineering (ICEE '13)*, pp. 1–5, IEEE, Mashhad, Iran, May 2013.

[9] A. C. Kailuke, P. Agrawal, and R. V. Kshirsagar, "Design of phase frequency detector and charge pump for low voltage high frequency PLL," in *Proceedings of the International Conference on Electronic Systems, Signal Processing and Computing Technologies (ICESC '14)*, pp. 74–78, IEEE, Nagpur, India, January 2014.

[10] D. Cai, H. Fu, J. Ren et al., "A 2.1-GHz PLL with −80dBc/−74dBc reference spur based on aperture-phase detector and phase-to-analog converter," in *Proceedings of the IEEE Asian Solid State Circuits Conference (A-SSCC '11)*, pp. 141–144, Jeju, South Korea, November 2011.

[11] P. Liu, P. Sun, J. Jung, and D. Heo, "PLL charge pump with adaptive body-bias compensation for minimum current variation," *Electronics Letters*, vol. 48, no. 1, pp. 16–18, 2012.

[12] N. Joram, R. Wolf, and F. Ellinger, "High swing PLL charge pump with current mismatch reduction," *Electronics Letters*, vol. 50, no. 9, pp. 661–663, 2014.

[13] H. R. E. Jazi and N. Ghaderi, "A novel bulk driven charge pump for low power, low voltage applications," *IEICE Electronics Express*, vol. 11, no. 2, Article ID 20130934, 2014.

[14] J.-M. Kim, S. Kim, I.-Y. Lee, S.-K. Han, and S.-G. Lee, "A low-noise four-stage voltage-controlled ring oscillator in deep-submicrometer CMOS technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 2, pp. 71–75, 2013.

[15] I.-T. Lee, Y.-T. Tsai, and S.-I. Liu, "A leakage-current-recycling phase-locked loop in 65–nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2693–2700, 2012.

[16] K.-H. Tsai and S.-I. Liu, "A 104-GHZ phase-locked loop using a vco at second pole frequency," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 1, pp. 80–88, 2012.

[17] K.-C. Choi, S.-G. Kim, S.-W. Lee, B.-C. Lee, and W.-Y. Choi, "A 990-μW 1.6-GHz PLL based on a novel supply-regulated active-loop-filter VCO," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 6, pp. 311–315, 2013.

[18] S. Min, T. Copani, S. Kiaei, and B. Bakkaloglu, "A 90-nm CMOS 5-GHz ring-oscillator pll with delay-discriminator-based active phase-noise cancellation," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1151–1160, 2013.

[19] K. Martin, *Digital Integrated Circuit Design*, Oxford University Press, New York, NY, USA, 2000.

[20] B. A. Minch, "Low-voltage Wilson current mirrors in CMOS," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '07)*, pp. 2220–2223, IEEE, New Orleans, La, USA, May 2007.

[21] B. Aggarwal, M. Gupta, and A. K. Gupta, "Analysis of low voltage bulk-driven self-biased high swing cascode current mirror," *Microelectronics Journal*, vol. 44, no. 3, pp. 225–235, 2013.

[22] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proceedings of the IEEE International Conference on Neural Networks*, pp. 1942–1948, Perth, Australia, November-December 1995.

[23] K. F. Man, K. S. Tang, and S. Kwong, "Genetic algorithms: concepts and applications," *IEEE Transactions on Industrial Electronics*, vol. 43, no. 5, pp. 519–534, 1996.

[24] Z. Zhu, J. Mo, and Y. Yang, "A low voltage bulk-driving PMOS cascode current mirror," in *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT '08)*, pp. 2008–2011, IEEE, Beijing, China, October 2008.

[25] J. Kim, J.-O. Plouchart, N. Zamdmer et al., "A 44 GHz differentially tuned VCO with 4 GHz tuning range in 0.12 μm SOI CMOS," in *Proceedings of the 2005 IEEE International Solid-State Circuits Conference (ISSCC '05)*, pp. 416–607, IEEE, San Francisco, Calif, USA, February 2005.