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Research Article

A ± 1.55ppm Stable FBAR Reference Clock with Oven-Controlled Temperature Compensation

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We present an oven-controlled FBAR oscillator that achieves a frequency stability of +/-1.55ppm from -5°C to 85°C. The highly integrated system includes a 0.64mm^2 FBAR chip with integrated heater and sensor resistors and a 3 mm^2 CMOS chip with the control electronics. The oscillator achieves an Allen deviation of 4ppb enabled by a temperature-to-digital converter (TDC) with a 150uK resolution. It corresponds to a 1.68JK^2 FOM. The heater consumes a power of 14mW at -5°C and the oscillator consumes only 0.25mW. The ovenized oscillator meets the stringent frequency stability requirements (2 ppm) of GPS applications.

1. Introduction

Low power and low noise radio frequency (RF) references are essential for applications such as low power wireless systems, high performance Analog to Digital Converters (ADC), and high speed serial data links [1]. Table 1 shows the frequency stability demanded by a few common applications. Several highly miniaturized MEMS and FBAR based oscillators have been proposed in the literature [1–9] but achieving a low power and highly integrated frequency reference with frequency stability better than 2ppm has been elusive so far. This work presents the first fully integrated oven-controlled FBAR oscillator with a frequency stability of ±1.5ppm. An energy-efficient serpentine heater and sensor are integrated in a single FBAR chip which is wire-bonded to a CMOS chip with the oscillator and oven control circuitry. The ovenized system operates over a temperature range of -10 to 85°C and consumes a maximum of 14mW power. A novel transformer coupled Colpitts oscillator is used to achieve lower power consumption (250uW) as well as the lower close-in phase noise performance (217 FoM) compared to conventional Pierce and Colpitts oscillators [7]. Thus, the long-term and short-term stabilities of this work are sufficient for the most stringent wireless standards.

The overall description of the temperature compensation system is shown at Section 2. The following subsections explain more details about each block and their measurement results.

The experiment results of the entire system with performance comparison are presented at Section 3 and the conclusion follows.

2. Oven-Controlled Temperature Compensation System

Figure 1 shows the proposed oven-controlled temperature compensation system with FBAR die containing heater and sensor fabricated directly on the resonator (top and bottom side of the resonator). A sensor resistor integrated with the resonator is used at the front-end of the temperature-to-digital converter (TDC) modified for the low power supply (750mV) based on an architecture proposed in [8]. The resistor variation is proportional to the temperature and detected by the TDC. The digital integrator compares TDC output with the target temperature, and accumulates the difference until the temperature of the die is equal to the target temperature. The integrator output is used for controlling the current-steering DAC and adjusts the amount of current

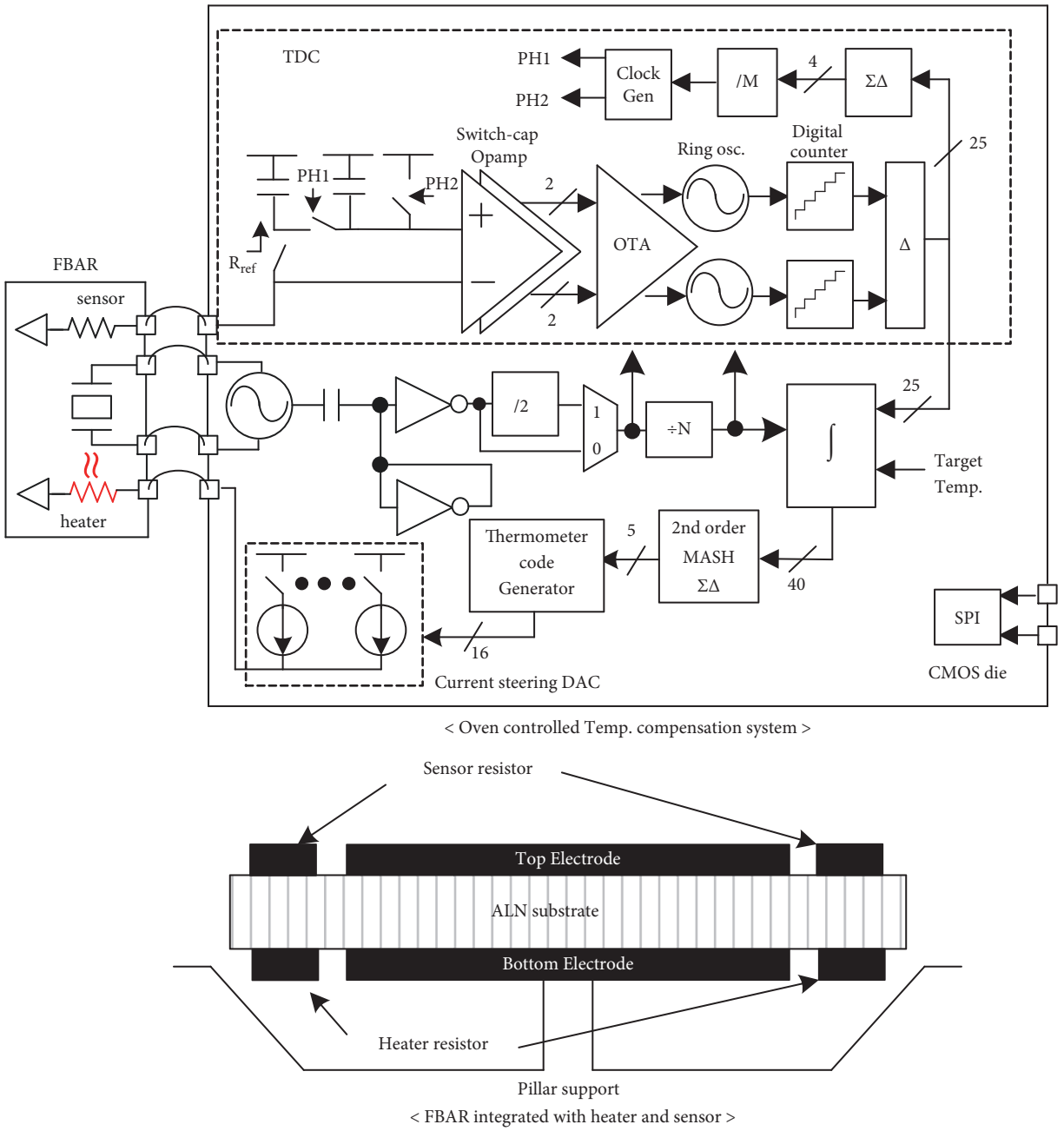


Figure 1: Block diagram of the oven-controlled temperature compensation system with FBAR die. This figure is reproduced from J. Koo et al. (2017) (under the Creative Commons Attribution License/public domain).

flowing through the heater as shown in Figure 1. Due to this closed loop system, it is possible to maintain the temperature of the resonator chip in real time without any calibration at the beginning.

2.1. Temperature-to-Digital Converter. Figure 2 shows the detail block diagram of the TDC. It utilizes the voltage division between the switch capacitor resistance (R_{ref}) and the off-chip sensor resistor in FBAR. The sensor resistance variation changes the bias current of the ring oscillator, and hence the frequency of its output. In order to sample the frequency of the ring oscillator outputs, digital counters are inserted to transform the frequency information into a digital value. This digital information controls the frequency of the

Table 1: Long-term frequency stability requirement.

Application	Frequency stability (ppm)
USB 3.0 Controller	±300
Wi-Fi	±20
WLAN	±20
Bluetooth	±20
GPS	±2

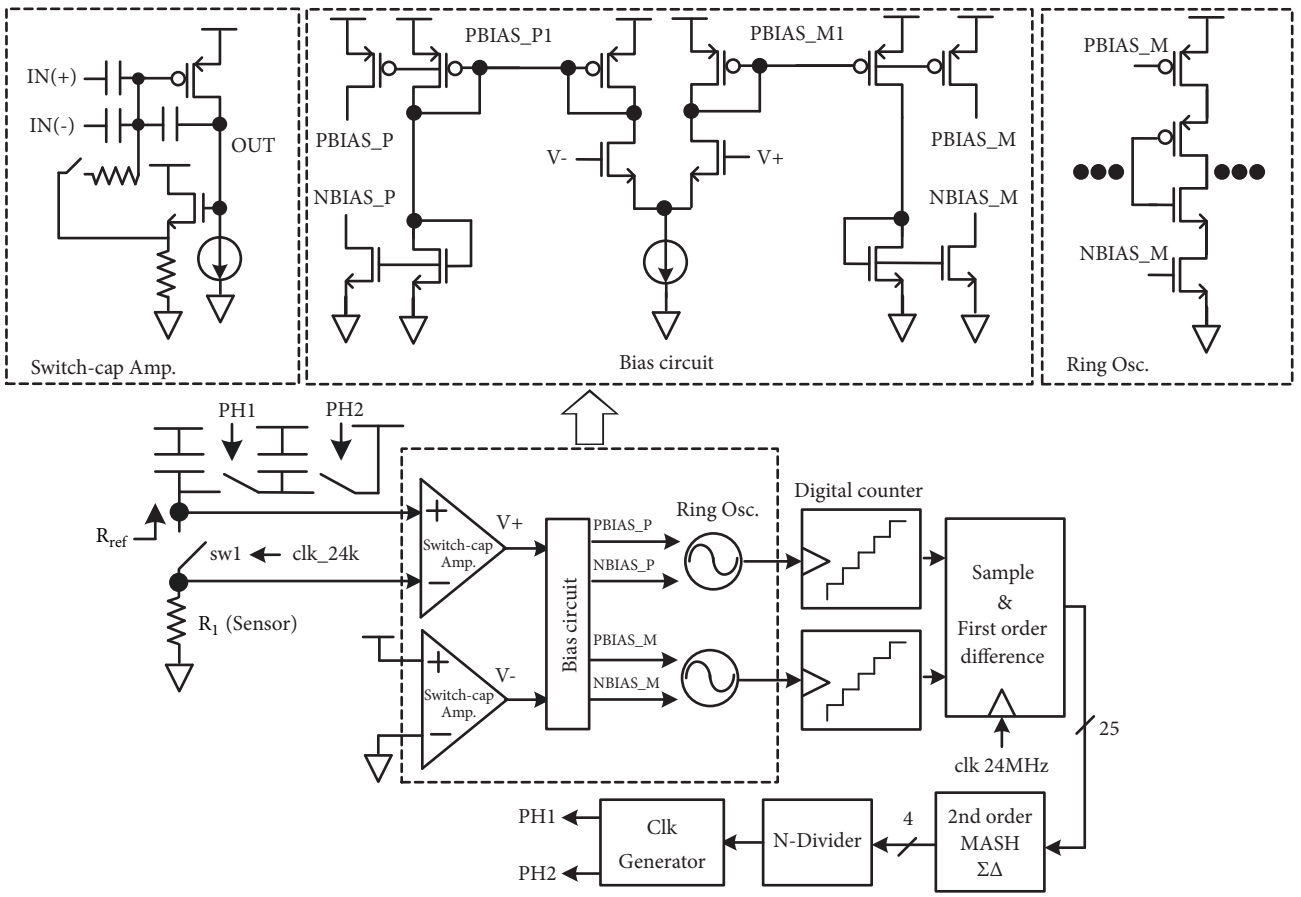
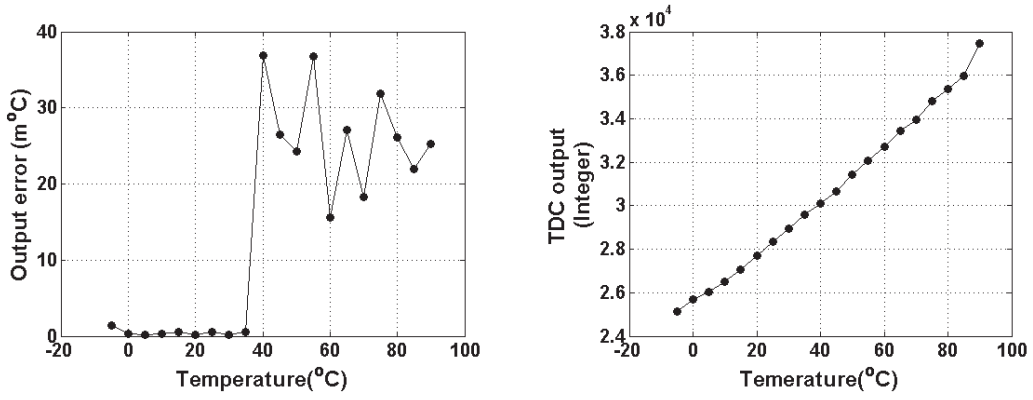


Figure 2: Block diagram of the TDC. This figure is reproduced from J. Koo (2016) (under the Creative Commons Attribution License/public domain).



(a) (b)

Figure 3: Measurement results for (a) TDC linearity and (b) output error.

two clocks (PH1 and PH2). The impedance of the switch capacitor (R_{ref}) is then tuned based on the frequencies of two clocks to make the node between R_{ref} and sensor resistor equal to Vdd/2. According to the linearity test of the TDC when the temperature changes from -5 to 90°C, a resolution of 150uK can be measured as shown in Figure 3(a), sufficient to achieve an Allan deviation of 4ppb. This corresponds to a Figure of Merit (Fom) of 1.68pJK^2 when sampling at 24kHz. Figure 3(b) represents the output error of the TDC under the temperature change. It has less than 1m°C error when the

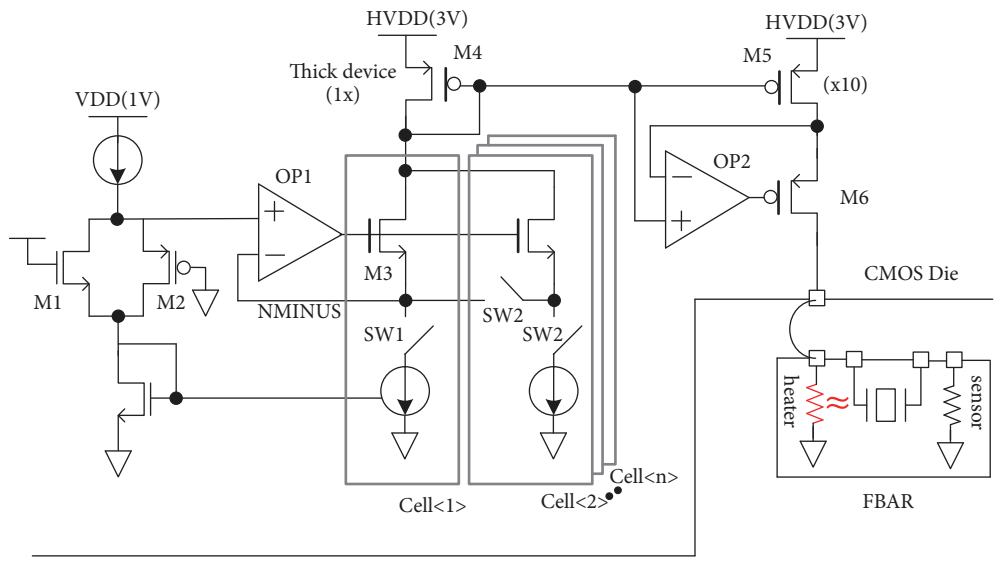


Figure 4: Block diagram of the current-steering DAC. This figure is reproduced from J. Koo (2016) (under the Creative Commons Attribution License/public domain).

temperature is less than 40°C. Although it increases up to 40m°C error at high temperature, it is small enough to make the frequency accuracy less than 2ppm.

2.2. Current-Steering DAC. Another key component in the oven-controlled temperature compensation system is a current-steering DAC. It controls the amount of current flowing through the heater. Figure 4 shows the detail block diagram. The output stage is directly connected to the heater through wire bonding. The DAC uses 17 unit current sources. The DAC is thermometric encoded to ensure linearity. When the current sources are turned on sequentially, the voltage of M4 drain changes as the output impedance of the turned-on current sources decreases. It degrades the INL and DNL errors. Therefore, Op-amp (OP1) and thick devices such as M3 are used to fix the output voltage of the current sources. This results in high output impedance leading to low DNL and INL errors.

Similarly, another Op-amp (OP2) and M6 device are used to decrease the voltage mismatch between drains of M4 and M5.

Figure 5 shows the measurement result of the DAC. The shift registers are programmed to sweep the input data manually, and the corresponding output currents flowing to the heater are monitored. Figure 5(a) shows how the output current changes according to the input value. For the comparison purpose, the ideal simulation result is also plotted in the same chart, showing a close match between ideal and measured results.

The accuracy of the DAC output can be also seen by INL and DNL plot as shown in Figure 5(b). The maximum errors are ±0.15 LSB.

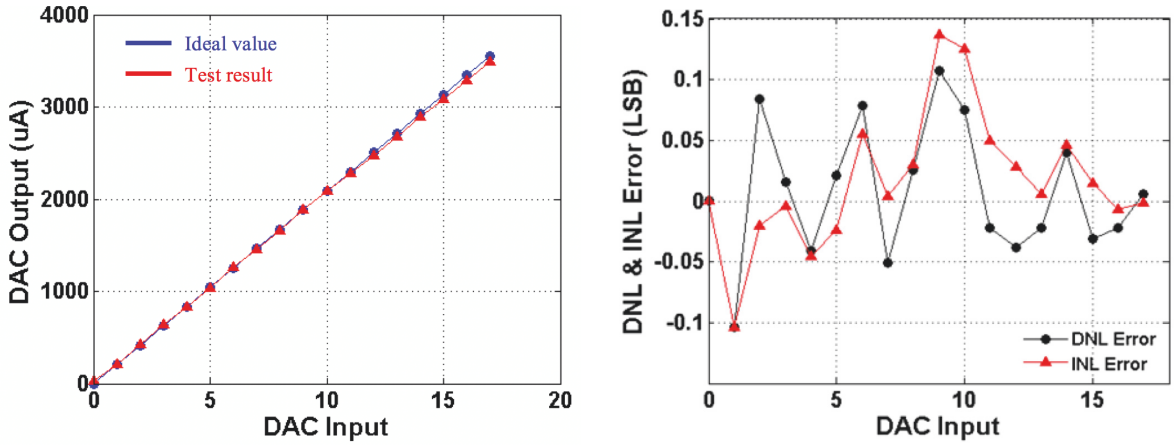
2.3. Transformer Coupled Colpitts Oscillator. Transformer coupled Colpitts oscillator is used to generate the reference clock as shown in Figure 6 [7]. It removes the current source of the conventional Colpitts oscillator to reduce the close-in offset phase noise which is the short-term frequency fluctuation and decrease the power consumption. But the current source is necessary for the Colpitts to obtain enough loop gain to start oscillation. So, the transformer and cross coupled capacitor (C_f) are used to compensate the decreased loop gain. The planar structure for the transformer design is chosen to maximize the Q of the inductors. The inductance ratio between primary and secondary inductors is 2:1 to double the loop gain and its output amplitude. Since the output amplitude is increased, it leads to the lower phase noise at far-out offset frequency (> 1MHz) as well. The critical transconductance needed for oscillation is derived by the equation below.

$$g_m = \frac{1}{R_p}\frac{2C_2 + 2C_1}{3C_2 + C_1}\frac{L_S}{L_S + M} \approx \frac{1}{R_p}\frac{2}{3}\frac{L_S}{L_S + M} \quad (1)$$

The critical transconductance is smaller compared to that of conventional Colpitts oscillator ($g_m = (1/R_p)(1 + C_1/C_2)$) [9] resulting in lower power consumption. Figure 7 shows the spectrum of the oscillator output measured through an open collector buffer. The operating frequency is 750MHz with -20dBm amplitude. Though the oscillator starts up with a -40dBm tone with power consumption of only 200uW, phase noise measurement becomes challenging when the output power is < -20dBm.

3. Measurement Result

Figure 8 represents the test results of the oven-controlled temperature compensation system. It shows the frequency variation of the oscillator over the temperature. The overall frequency variation is 300ppm when the temperature changes from -5 to 90°C and when the temperature compensation is off as shown by the blue graph. With the compensation on, the system can be programmed to set the target temperature.



(a) (b)

Figure 5: Measurement result of (a) the DAC output currents according to input value and (b) INL and DNL error.

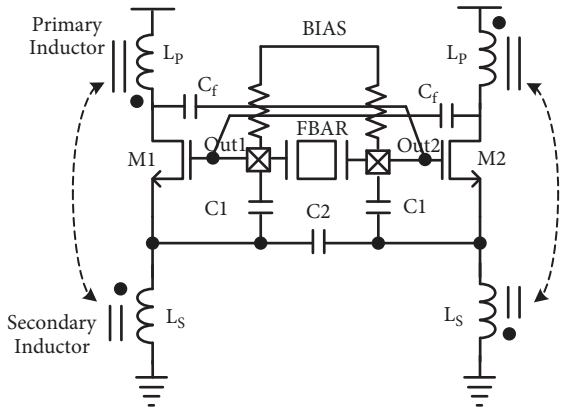


Figure 6: Block diagram of the transformer coupled Colpitts oscillator. This figure is reproduced from J. Koo (2016) (under the Creative Commons Attribution License/public domain).

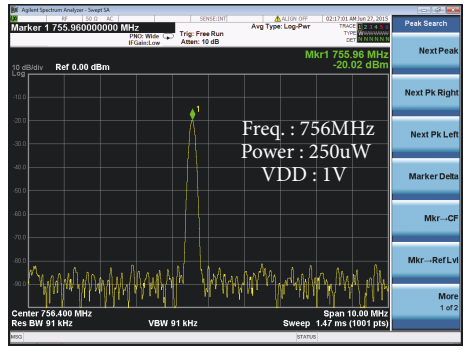


Figure 7: Spectrum analyzer test result of the oscillator.

For example, when the target is set to 80°C, the frequency of the oscillator remains the same, while the temperature varies below 80°C. But, when the temperature increases above its target value, frequency is unlocked. That is because there is no way to cool down as there is only heater inside the resonator chip. Figure 9 shows much detail result. When the target temperature is set to 80°C, the overall frequency variation is decreased down to ±1.55ppm.

Figure 10 shows how the DAC output current changes according to the resonator temperature at each target set. For example, when the target is 80°C and the temperature is -5°C, the maximum current is needed to heat up the FBAR resonator to high temperature (80°C) leading to 14mW power consumption. But, the current from DAC decreases when the temperature of the FBAR increases and gets close to target temperature. When the temperature of resonator reaches to the target, DAC generates no current because there is no need to heat.

4. Conclusion

The IC is fabricated by 65nm CMOS process and occupies an area of 3mm^2. Figure 11 shows the die photo. FBAR resonator is located right below the main chip and connected to the oscillator to minimize parasitic resistance and inductance. As shown in the photo, a transformer which is the largest component of the oscillator takes an area of 900 um x 400 um. Sensor and heater inside FBAR chip are connected to TDC and DAC output, respectively, through the test board and wire bonding.

This work is the first fully integrated oven-controlled temperature compensation system with high resolution TDC (0.15mK), high precision current-steering DAC, and low power transformer coupled Colpitts oscillator used for reference clock. Heater based systems have had an issue for implementing on-chip integration before [6]. In addition, this technique avoids having to do multiple temperature calibrations because of feedback loop characteristic. This is important for low cost, high volume manufacturing of high frequency precision oscillators. Table 2 also shows that higher TDC resolution contributes to obtaining low Allan deviation (4ppb).

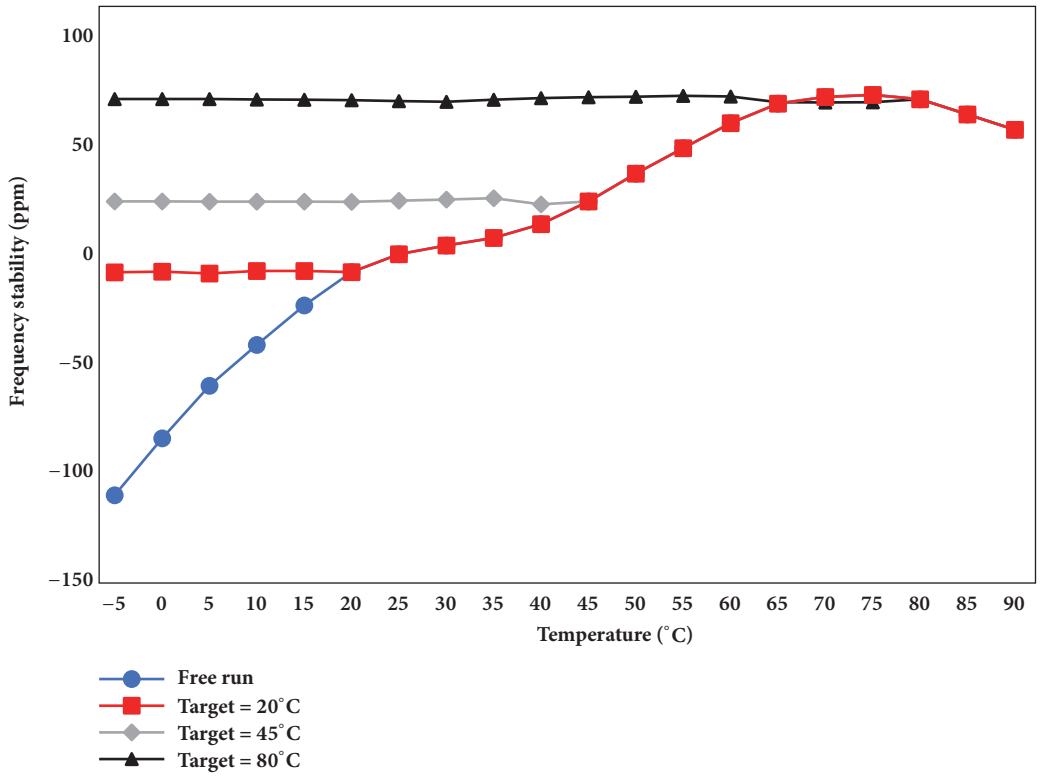


Figure 8: Measurement results of the frequency stability with target temperatures (20°C, 45°C, and 80°C). This figure is reproduced from J. Koo et al. (2017) (under the Creative Commons Attribution License/public domain).

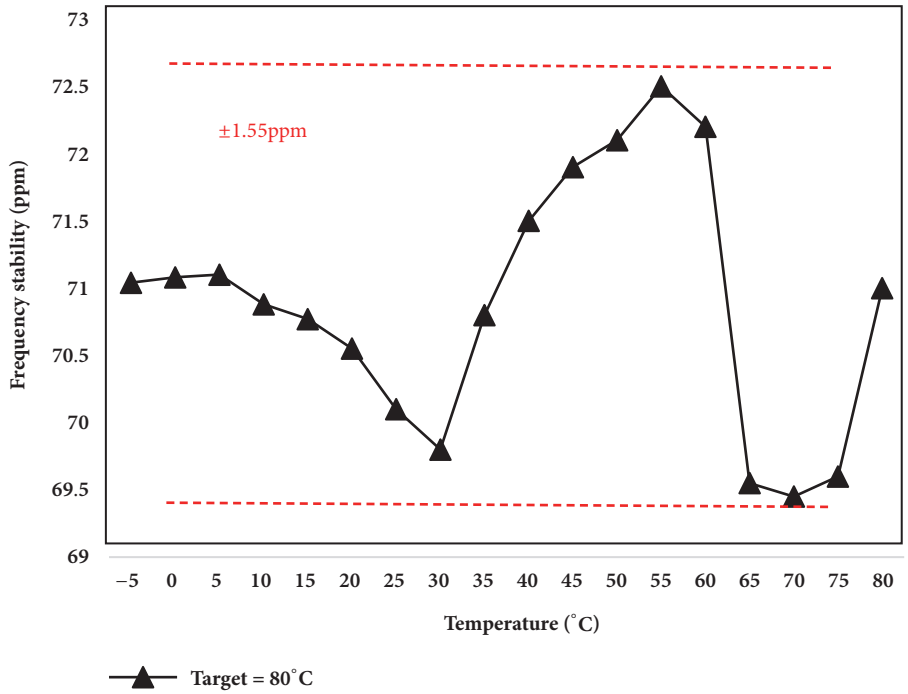


Figure 9: Detail frequency variation when the target temperature is 80°C.

Table 2: Comparison chart.

Performance comparison				
	[6]	[8]	[10]	**This work**
Frequency	582MHz	1-330MHz	750MHz	**750MHz**
VDD(V)	3	3.3	0.75	**0.9(TDC)/3(DAC)**
Power consumption of Osc./System	NA	9.24mW/108mW(FracN PLL)	0.45mW/1,1mW	**0.25mW/2.9mW**
Heater Power(Max)	9mW	NA	NA	**14mW**
Size (mm x mm)	25x25	2.02x1.89	1.6x0.9(CMOS) 0.8x0.8(FBAR)	**1.5x2(CMOS)** **0.8x0.8(FBAR)**
Temperature range(°C)	-45 to 85	-45 to 85	0 to 90	**-10 to 90**
Stability(ppm)	2	±0.5	±3	**±1.55**
Allen deviation@0.1s(ppb)	NA	5	8	**4**
Temp. resolution	NA	0.1	1.2	**0.15**
No. of Trim	NA	12	4	**2**
Tech.	GaAs P-HEMT	0.18um	65nm	**65nm**

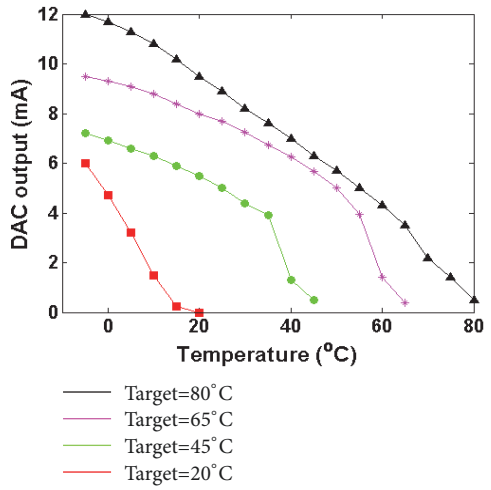


Figure 10: Measurement results of the DAC output according to temperature change at each target.

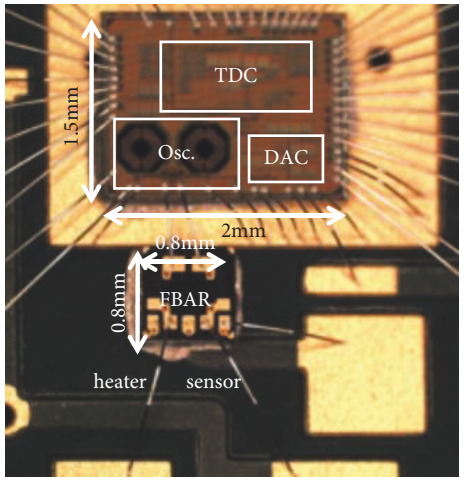


Figure 11: Die photo.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Disclosure

Jabeom Koo is now with Intel Corporation, Hillsboro, OR 97124, USA (e-mail: Jabeom@gmail.com).

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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