Research Article

Design and Implementation of Nanotechnology QCA Geometric Greedy Router

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This paper presents an optimized geometric greedy router (GGR) based on quantum dot cellular automata (QCA) technology. The proposed structure of GGR is based on a spanning tree of the network. This type of communication does not require an IP address. It uses only local information and can be used in many communication devices. In this paper, we first describe the principal components of the router and then we present their QCA architecture. The QCA technology is the most likely alternative to replace conventional circuits (CMOS) due to their very low power consumption and high processing speed. To consider integration with other complex circuit, we have utilized QCA clock-phase-based technique for the proposed design architecture. The results obtained using the QCA designer tool exhibit the superiority of the presented architecture over the existing designs. The proposed structure shows a reduction of 30% reduction in occupied space. The power dissipation rate of the proposed design is analyzed by QCAPro tool to approve its reliability.

1. Introduction

The complementary metal oxide semiconductor (CMOS) technology has many defects, such as short channel effect and high power consumption; it cannot, therefore, continue to follow Morrie's law by increasing the number of devices per chip [1]. It creates the need for nanoscale devices, with high-performance rates and low power consumption. These recent nanoscale devices have the potential to enable progressions in different domains such as industrial, biomedical, and military fields. For these types of applications, classical communication networks, such as IP routing, are not suitable. In fact, these types of applications are very greedy for size, energy, and memory consumption [2]. The design of a geometric greedy router using the quantum dot cellular automata (QCA) can present an alternative to resolve these problems.

The quantum dot cellular automata (QCA) technology is one of the important emerging nanotechnologies that have attracted much researcher's attention in recent years. Such advantages led researchers to develop several projects detailing the construction of QCA circuits. In the recent

years, several circuits such as address [3, 4], sequential circuits [2, 5], switching circuits [6, 7], reversible logic circuit [8, 9], and memories [10, 11] have been designed. On the contrary, to cope with the challenge of IOT, big data domains and the need to achieve data rates of up to multiple gigabits per second require the use of more efficient routing algorithms to avoid network bottlenecks. In the greedy routing method, the main aim is to achieve another routing process by having each participant store only a partial knowledge based on the network.

In the recent years, different studies of geometric greedy router have been proposed [12].

This routing method requires very efficient electronic support. In this paper, we present an optimized architecture of geometric greedy router based on QCA technology.

The paper is organized as follows. Section 2 presents the basic concept of QCA. Section 3 explains briefly the technique of the tree-based greedy routing. Section 4 covers the proposed architectures of the QCA geometric greedy router. Section 4 presents the simulation results of the proposed work along with discussion. Power dissipation analysis is carried out in Section 5. We conclude the paper with Section 6.

2. Preface to Quantum Dot Cellular Automata

The basic QCA cell is illustrated in Figure 1. The QCA cell can be considered as a square including four quantum dots which are occupied by a pair of electrons. The cell comprises four quantum dots and two mobile electrons which are able to confine electric charges. These electrons tend to locate themselves and arranged diagonally in the cell. The repulsive force between two electrons pushes them as far as possible. There are two polarization states, which present logic “0” and “1,” as shown in Figure 1 [13].

In QCA technology, the polarization of adjacent cells is performed by coulomb interaction, as shown in Figure 2(b). Polarization (P) is defined as the following expression:

$$\text{Polarization}(p) = \frac{(P1 + P3) - (P2 + P4)}{(P1 - P2 + P3 + P4)}. \quad (1)$$

The polarization of the electrons in the quantum dots are presented as $P1$, $P2$, $P3$, and $P4$ (Figure 2(a)). Equation (1) presents the value of polarization of QCA cell. If an electron is present, $P_i = 1$, otherwise it is equal 0.

Inverter and majority gates are the essential logic element in the QCA circuits which are realized by some QCA cells, as shown in Figure 3 [13]. The majority gate can be used to generate an “AND” or an “OR” logic, by putting one of the inputs as “0” and “1,” respectively.

The QCA clocking system synchronization is used for controlling the potential barriers between the adjacent quantum dots. The QCA clocking system consists of four phases, as illustrated in Figure 4. The phases are switch, hold, release, and relax [14]. The barriers are raised during the switch phase, and a cell is influenced by the polarization of its adjacent cells. The barriers are high in the hold phase, and the polarization of the cell is retained. During the release phase, the barriers are lowered, and the cell loses the polarity. During the relaxing phase, the cell is nonpolarized.

In QCA, there are two different forms of crossover: coplanar and multilayer crossovers (Figure 5(a) and 5(b)). While multilayer crossover requires at least three layers for implementation, coplanar crossover uses only one layer. Multilayer QCA circuits consume much less area as compared to coplanar circuits.

3. Greedy Router

In geometric routing, a rather simple stateless distributed algorithm routes messages from node to node along a source-destination path, based only on position information (node coordinates). Only local information needs to be stored in each network node. A greedy routing algorithm forwards every packet to the node in the one-hop neighborhood, which lies closest to the final destination. In GR, virtual coordinates are assigned to each of the nodes of a network. The coordinate distribution is based on other ad hoc network protocols or sensors, such as greedy perimeter stateless routing (GPSR) [15]. In [16], the authors have proposed the use of virtual coordinates in NoGeo routing, the creation of the virtual coordinate assignment protocol (VCAP), and the use of conformal maps to find the

coordinates [17]. In GR, a greedy technique is used. As the next hop, the neighbor node with the shortest distance to the destination node is selected.

The problem with geometric greedy routing occurs when a packet is in the case that the distance between the current node and the destination is smaller than the distance between its neighbors and the destination. The solution for this problem can be based on the face routing method [18] or using a greedy embedding method [19]. The embedding method can be done using multiple dimensions in Euclidean space [20, 21] or using multiple trees [22, 23] to improve routing performance. In our work, we used the method proposed in [24]. This method starts with the creation of a spanning tree and the adoption of a set of coordinates to each node of the network. Figure 6 presents this step. It consists of

- (i) The creation of spanning tree (Figure 6(a))
- (ii) Assignment of a number (from 1 to n) for the children of each node (Figure 6(b))
- (iii) Give numbers to the children of each node (from 1 to n)
- (iv) Assign (0, ..., 0) to the root node
- (v) A number previously is given to each child, replacing the first zero of their coordinates (Figure 6(c))

The tree depth presents the number of coordinates will be attributed to the nodes. The number of bits allocated to represent the coordinates in the router implementation is proportional to the number of children of the node. During the process, several steps must be established. When the router structure is created, the embedding tree has already been established and each generated node is aware of the coordinate set (CS) of its neighbors; the node forward the received packet to the neighbor which has the smallest possible distance to the destination. The processes are repeated until the packet reaches its final destination. Algorithm 1 presents the following steps.

The distance between nodes is computed according to the number of hops that must travel in the tree through the nodes, taking into consideration the common ancestors of neighbor nodes and the number of nonzero coordinates in each set.

4. Architecture of the QCA Geometric Greedy Router

Figure 7 shows the block diagram of the geometric greedy router.

Two tasks must be accomplished in the distance calculator module. The first task is based on the distance calculator algorithm (Algorithm 1). The model of the first part of the distance calculator is depicted in Figure 8. The second task is reserved for the destination node and the distance comparator determination.

The architecture of the greedy router is composed of several logic gates such as OR, XOR, NAND, and multiplexer. The optimized QCA layouts of these logic modules are presented in Figure 9.

FIGURE 1: Schematics of the basic QCA cells.

FIGURE 2: Propagation of binary information.

FIGURE 3: Realization of logical OR and AND gates.

FIGURE 4: QCA clock phases.

FIGURE 5: Signal crossover schemes: (a) coplanar crossing; (b) multilayer crossing.

FIGURE 6: (a) Network topology. (b) Spanning tree and children numbering. (c) Coordinate set of each node given.

- (1) **Begin;**
- (2) **while** packet is not at the destination **do**
- (3) **for each** neighbor of present node **do**
- (4) find the first pair of different coordinates, comparing bit by bit, between neighbor and destination node; from there, count the number of nonzero coordinates from both CS **to** encounter distance;
- (5) **end**
- (6) **compare** found distances;
- (7) **forward** packet to node with smallest distance to destination;
- (8) **end**

ALGORITHM 1: Forwarding a packet to its destination.

FIGURE 7: Geometric greedy router [25].

FIGURE 8: Circuit diagram of the distance calculator.

FIGURE 9: Basic logic gates of distance calculator module: (a) XOR; (b) 2:1 Mux; (c) And; (d) Or.

FIGURE 10: QCA architecture of the distance calculator module (DCM).

FIGURE 13: QCA architecture of the counter module (CM).

FIGURE 14: Comparator circuit.

counters, the results will be used by the comparator. The output will present the destination node for the packet.

The QCA architecture of the entire greed router is illustrated in Figure 17. The figure presents the inputs and outputs of the system.

5. Result and Discussion

The comparison between the proposed used logic gates and the existing architectures is given in Tables 1–3. In these tables, the complexity is given by the number of the required cells and the area is given by μm^2 .

The proposed QCA distance calculator layout is composed by 96 cells and occupied a surface of $0.313 \mu\text{m}^2$. In [38], the authors have proposed a circuit composed by 154 cells and occupied a surface of $0.461 \mu\text{m}^2$.

Half Adder presents the basic elements of the counter module. For implementing the half adder in QCA technology, we have used one two-input XOR gate and one two-input AND gate.

Figure 12 shows the proposed layout of the QCA Half Adder circuit and the simulation result. Table 3 shows a comparison between the proposed Half Adder with the previous works. Half Adder circuit has lower computational complexity and better performances compared to existing ones.

The countercircuit is composed by ten Half Adder circuits and two AND logic gates. It occupies a surface of $1.73 \mu\text{m}^2$. The proposed circuits are simulated using QCADesigner tool version 2.0.3 [40]. This allows users to do a custom layout and also verify QCA design by simulation. A nominal cell size of 18 nm by 18 nm is assumed. The

FIGURE 15: QCA architecture of the comparator (CMP).

FIGURE 16: Block diagram of the greed router.

FIGURE 17: Block diagram of the greed router.

TABLE 1: Comparison results of the used 2-input digital "XOR" gate.

XOR structure	Cell count	Surface (μm^2)	Crossover
[26]	60	0.08	Coplanar (rotated cells)
[27]	29	0.03	Not required
[28]	28	0.02	Coplanar
[29]	12	0.0116	Not required
[30]	13	0.01	Not required
[31]	10	0.008	Not required
Used	9	0.008	Not required

TABLE 2: Comparative result of 2:1 multiplexer.

2:1 mux	Cell count	Surface (μm^2)	Crossover
[32]	26	0.02	Coplanar
[33]	29	0.02	Coplanar
[34]	28	0.02	Coplanar
[35]	12	0.02	Coplanar
[36]	13	0.01	Coplanar
[37]	12	0.02	Without
Used	9	0.0076	Without

TABLE 3: Comparative result of Half Adder.

Half Adder	Cell count	Surface (μm^2)
[39]	77	0.08
[40]	62	0.08
Proposed	25	0.025

TABLE 4: Simulation parameters.

Parameter	Value
Cell size	18 nm* 18 nm
Dot	5 nm
Cell separation	2 nm
Simulation engine	Bistable approximation/coherence vector
Radius of effect	65 nm
Number of samples	12800
Convergence tolerance	0.001000
Temperature	1.000000
Relative permittivity	12.900000
Clock high	$9.800000e - 022$
Clock low	$3.800000e - 023$
Clock shiftcty	0.000000
Clock amplitude factor layer	2.000000
Separation	11.500000
Maximum iterations per sample	100
Relaxation time	$1.000000e - 015$

propagation delays from cell to cell required a maximum cell count in a clock zone.

The minimum separation between two different signal wires is width of two cells. We have used multilayer crossovers for wire crossings essentially depending on the complexity of the circuit. The essential QCA parameters are presented in Table 4.

6. Conclusion

In this paper, an optimized design of nanotechnology geometric greedy router architecture in the QCA technology was proposed. The GGR presents the principal components of the router, and this work presents an essential step in the building of QCA circuits for low power in digital nano-communications systems. Our main focus is to propose a prototype of a very low-power GGR module optimized in terms of cell count and area. Results of simulation are shown by QCADesigner version 2.0.3. An interesting future work could be to develop several applications based on this GGR module.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request

Conflicts of Interest

The authors have no conflicts of interest.

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