

Research Article

High-Fidelity and High-Efficiency Digital Class-D Audio Power Amplifier

Cong Wei,¹ Jianhan Wu,¹ Rongshan Wei ,¹ and Minghua He²

¹College of Physics and Information Engineering, Fuzhou University, Fuzhou, China

²Fujian Medical University, Fuzhou, China

Correspondence should be addressed to Rongshan Wei; wrs08@fzu.edu.cn

Received 28 January 2021; Revised 24 March 2021; Accepted 1 April 2021; Published 14 April 2021

Academic Editor: Jit S. Mandeep

Copyright © 2021 Cong Wei et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This study presents a high-fidelity and high-efficiency digital class-D audio power amplifier (CDA), which consists of digital and analog modules. To realize a compatible digital input, a fully digital audio digital-to-analog converter (DAC) is implemented on MATLAB and Xilinx System Generator, which consists of a 16x interpolation filter, a fourth-order four-bit quantized delta-sigma ($\Delta\Sigma$) modulator, and a uniform-sampling pulse width modulator. The CDA utilizes the closed-loop negative feedback and loop-filtering technologies to minimize distortion. The audio DAC, which is based on a field-programmable gate array, consumes 0.128 W and uses 7100 LUTs, which achieves 11.2% of the resource utilization rate. The analog module is fabricated in a 0.18 μm BCD technology. The postlayout simulation results show that the CDA delivers an output power of 1 W with 93.3% efficiency to a 4 Ω speaker and achieves 0.0138% of the total harmonic distortion (THD) with a transient noise for a 1 kHz input sinusoidal test tone and 3.6 V supply. The output power reaches up to 2.73 W for 1% THD (with transient noise). The proposed amplifier occupies an active area of 1 mm^2 .

1. Introduction

Following the rapid development in artificial intelligence Internet of Things, smart speaker and TWS headset based on class-D audio power amplifiers (CDAs) have become the most popular portable audio products. Simultaneously, with the continuous development in digital-storage technology, audio signals have mainly become digital audio signals. The traditional CDAs usually introduce a digital-to-analog converter (DAC) to convert the digital audio signals into analog audio signals and then perform power amplification. This solution not only increases the complexity of the system and is not conducive to transplantation but also requires a high-precision DAC. In addition, intrinsic quantization noise is introduced to reduce the system performance. Figure 1 shows the new CDA structure proposed in the 1990s for compatibility with a digital audio interface [1], which has gradually become a research hotspot in recent years.

The modulation techniques of CDAs can be divided into uniform-sampling pulse width modulation (UPWM) [2–4],

pulse-density modulation (PDM) [5–7], click modulation [8, 9], and zero-position coding with separated baseband [10, 11]. The CDAs comprise several main topologies. The open-loop architecture requires a precise carrier signal to achieve low distortion [12]. The closed-loop architecture does not require a similar precise carrier because the CDA loop gain suppresses the carrier distortion [13]. Moreover, some CDAs generally comprise a single-bit quantizer, but ensuring stability over all modulation indexes requires high controller power [14, 15]. Multibit quantizers can improve the stability of delta-sigma ($\Delta\Sigma$) modulators although they nevertheless entail high quiescent power and considerable complexity [16]. To overcome these drawbacks, we propose a CDA with a closed-loop negative feedback and loop-filtering technologies to improve the total harmonic distortion (THD) and suppress the noise introduced by the power supply. Furthermore, the $\Delta\Sigma$ modulator is implemented using digital circuits.

This paper is organized as follows. Section 2 describes the design of the proposed architecture. The digital module is presented in Section 3. Section 4 shows the implementation

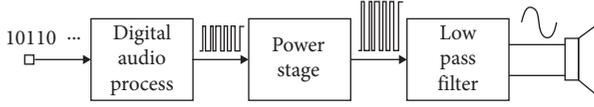


FIGURE 1: Class-D audio power amplifier block diagram.

of the analog module. The postlayout simulation results are provided in Section 5. Finally, the paper is concluded in section 6.

2. Design of the Proposed Class-D Architecture

Figure 2 shows the block diagram of the proposed class-D architecture, which mainly consists of a digital module (called audio DAC) and an analog module. The audio DAC comprises an interpolation filter, a $\Delta\Sigma$ modulator, and a UPWM. The analog module includes the closed-loop negative feedback, loop filter, and output-power stage.

The input digital audio signal is modulated by the $\Delta\Sigma$ modulator to achieve the expected signal-to-noise ratio (SNR). The output bitstream and sampled and held carrier signals are used to realize UPWM in the digital domain. The output UPWM signal drives the analog circuit.

The interpolation filter, $\Delta\Sigma$ modulator, and UPWM are realized using a digital module for compatibility with a digital audio input. Oversampling and noise-shaping technologies of the $\Delta\Sigma$ modulator are used to ensure the system SNR. The loop filter, output-power stage, and closed-loop negative feedback are realized by the analog module. The closed-loop negative feedback technology is used to effectively suppress the power-supply noise and system non-linearity and to ensure high fidelity of the output audio signal. The maximum swing of the audio output voltage can be doubled using the bridge-tied load configuration, which consequently quadruples the output power [17].

3. Implementation of the Digital Module

3.1. Interpolation Filter. To realize sufficient SNR, the interpolation filter oversamples the input digital audio signal by interpolation and evenly distributes the quantization noise in the whole frequency domain of the signal. It prepares for noise shaping in the later stage of the $\Delta\Sigma$ modulator [18].

The conventional interpolation filter generally adopts half-band and comb filters [19]. Although the comb filter structure is relatively simple, its filtering ability is limited. Thus, some compensation technologies should be employed to improve it. Figure 3 shows the block diagram of a 16x interpolation filter for the proposed CDA. Three half-band filters and an inverse sinc filter are cascaded to complete the 16x interpolation of the input digital audio signal.

In a high-performance audio DAC, the passband ripple usually ranges from 0.001 to 0.0001 dB. Therefore, in the interpolation process, the maximum allowable passband ripple of the interpolation filter must be 0.001 dB, and the stopband attenuation should exceed 100 dB. Considering the quantization effect of a finite word length, the distortion of the interpolation filter must be less than 1 dB [20].

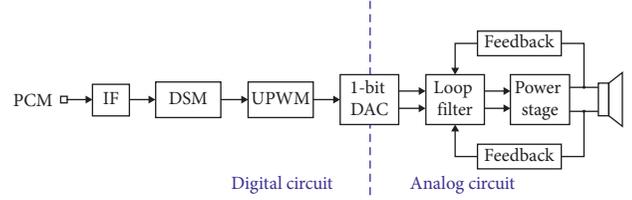


FIGURE 2: Block diagram of the proposed class-D amplifier.

Figure 4 shows the output spectrum of the 16x interpolation filter with $V_{in} = 1.4V_{pp}$ at input signal frequency $f_{in} = 1$ kHz. The SNR reaches up to 99.92 dB.

3.2. $\Delta\Sigma$ Modulator. The conventional $\Delta\Sigma$ modulator generally comprises a single-bit quantizer to simplify the design. However, if the power transistor is directly driven by the output bitstream signal of the single-bit quantizer, the frequency of the modulated switching signal [21] will be too high and will vary with the input signal, resulting in the reduction in the power efficiency. Therefore, the quantizer in the CDAs is usually considered to be multibit quantizers. However, the quantizer bits should not be very high because the system clock will be too fast to increase the system power consumption, and implementing the system becomes difficult. The SNR of the $\Delta\Sigma$ modulator is calculated as

$$SNR \approx 6.02N + 10 \log \left[\frac{3}{2} \frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}} \right], \quad (1)$$

where n is the number of quantizer bits, OSR is the oversampling rate of the input signal, and L is the order of the $\Delta\Sigma$ modulator.

Equation (1) shows that the maximum SNR of the $\Delta\Sigma$ modulator increases with the order of the $\Delta\Sigma$ modulator, the oversampling rate of the input signal, and the number of bits of the quantizer [22]. However, a higher number of quantizer bits or a higher modulator order is required for a low oversampling rate. A higher oversampling rate can greatly reduce the requirements of the modulator and quantizer. In addition to the increase in the system frequency and power consumption, the output pulse signal frequency also exponentially increases. Therefore, in this study, the oversampling rate is set to 16, the order of modulator is set to 4, and the number of bits of the quantizer is set to 4.

High-order $\Delta\Sigma$ modulators usually have two structures: single-loop and multistage noise-shaping (MASH) structures [23, 24]. Although the $\Delta\Sigma$ modulator realized by MASH can achieve high precision, it also needs to achieve addition for the output of hardware resources. Hence, a $\Delta\Sigma$ modulator that adopts a CIFF single-loop high-order structure is shown in Figure 5. In this architecture, only the first-stage integrator receives the feedback signal from the output, which reduces the requirements for the subsequent integrators as well as the hardware resources consumed by the $\Delta\Sigma$ modulator.

In this design, DSM uses Xilinx System Generator tool to complete the design. The software platform uses Xilinx Vivado and MATLAB. The hardware platform uses Artix-7

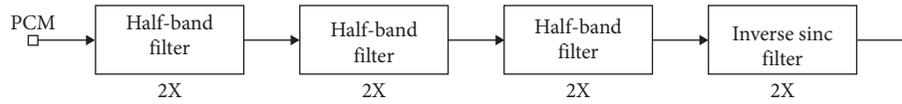
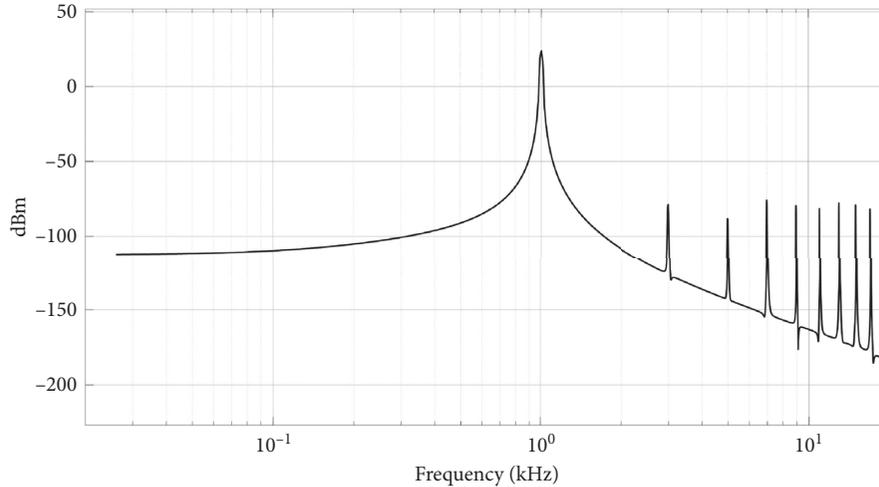


FIGURE 3: Block diagram of the 16x interpolation filter.



RBW = 19.51 Hz, sample rate = 768 kHz

FIGURE 4: Output spectrum of the 16x interpolation filter.

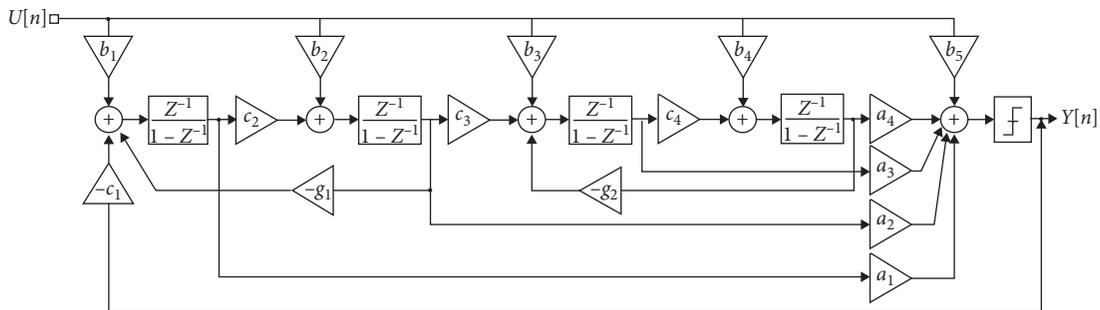


FIGURE 5: $\Delta\Sigma$ modulator with a cascade of integrator feedforward (CIFF) structure.

MIA701 development board. The development board integrates a wealth of hardware resources to meet the digital design requirements of audio digital-to-analog converters.

The $\Delta\Sigma$ modulator is implemented in an all-digital manner. Therefore, the influence of nonideal factors does not need to be considered, such as the operational amplifier in the analog $\Delta\Sigma$ modulator. The output spectrum of the $\Delta\Sigma$ modulator filter with $V_{in} = 1.4V_{pp}$ at input signal frequency $f_{in} = 1\text{ kHz}$ is shown in Figure 6. The SNR reaches up to 112 dB.

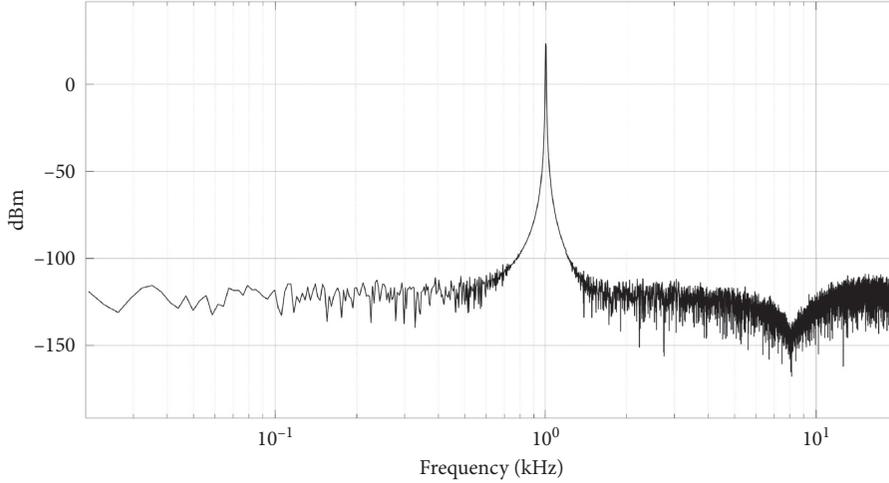
3.3. *UPWM*. The common modulation techniques of CDAs are the UPWM and PDM. Compared with the PDM, UPWM offers the advantages of simple circuit, lower switching frequency, and higher system efficiency.

The UPWM modulator is a direct modulator that converts the digital signal into a switching signal. According

to the different carrier signals, UPWM can be divided into the following: leading-edge UPWM, trailing-edge UPWM, symmetric double-edge UPWM (SDEUPWM), and asymmetric double-edge UPWM. The SDEUPWM has a lower harmonic distortion and higher SNR than the others [25]. In the proposed CDA, the SDEUPWM principle is shown in Figure 7. The output signal of the $\Delta\Sigma$ modulator is compared with the carrier signal to generate a UPWM wave.

4. Implementation of the Analog Module

4.1. *Loop Filter*. The loop filter can reduce the harmonic distortion of the feedback loop using the noise-shaping technology. The frequency-response curve of the Butterworth filter is relatively flat in the passband without fluctuations and gradually decreases to zero in the stopband. Hence, a Butterworth loop filter is designed in this study. The transfer function of the Butterworth loop filter is given by



RBW = 4.39 Hz, sample rate = 768 kHz

FIGURE 6: Output spectrum of the $\Delta\Sigma$ modulator.

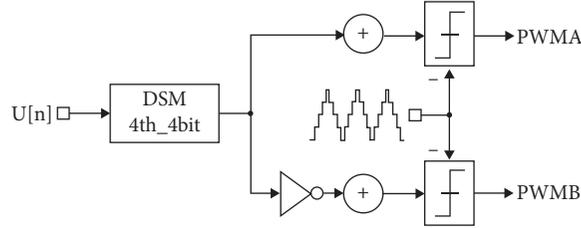


FIGURE 7: Block diagram of the SDEUPWM.

$$H_{\text{NTF}}(s) = \frac{s^n}{s^n + a_1 w_c s^{n-1} + \dots + a_{n-1} w_c^{n-1} s + w_c^n} \quad (2)$$

where n is the order of the filter, w_c is the cutoff frequency of the filter (-3 dB point frequency), and $(n = 1 \sim n - 1)$ is the filter coefficient. Therefore, the open-loop transfer function of the system can be expressed as

$$\begin{aligned} H_{\text{open}}(s) &= H_{\text{loop}}(s)G_{\text{PWM}}(s) \\ &= \frac{a_1 w_c s^{n-1} + \dots + a_{n-1} w_c^{n-1} s + w_c^n}{s^n}, \end{aligned} \quad (3)$$

where

$$H_{\text{loop}}(s) = \frac{s^{n-1} + \dots + (a_{n-1} w_c^{n-2}/a_1)s + (w_c^{n-1}/a_1)}{s^n}, \quad (4)$$

$$G_{\text{PWM}}(s) = a_1 w_c.$$

Figure 8 shows the output spectrum with different orders with $V_{\text{in}} = 1.4V_{\text{pp}}$ at input signal frequency $f_{\text{in}} = 1$ kHz and carrier signal frequency $f_{\text{car}} = 768$ kHz. In the audio band, the noise-suppression effect of the Butterworth loop filter increases with the order, but the increasing trend gradually slows down. By considering the effect of the loop filter on the in-band noise suppression and the complexity of the circuit design, the order is considered as a second order.

In this study, the loop filter of the proposed CDA adopts a second-order integrator architecture, as shown in Figure 9. It consists of two cascaded Miller integrators. Figure 10 shows that the OTA is a two-stage amplifier with a Miller compensation. Because the flicker noise of PMOS is lower than that of NMOS, the differential input pair of the amplifier adopts a P-type MOS transistor, which can reduce the influence of the circuit noise. To reduce the noise and maintain the linearity of the integrator, the DC gain of the two-stage amplifier must be greater than 80 dB, and the -3 dB bandwidth must be greater than 100 Hz. The transfer function of the two-stage operational amplifier is expressed as

$$\frac{V_{\text{OUT}}(s)}{V_{\text{id}}(s)} = \frac{A_{\text{DC}}[1 - (s/p_z)]}{(1 + (s/p_1))(1 + (s/p_2))(1 + (s/p_3))}, \quad (5)$$

where V_{id} is the input differential signal, A_{DC} is the open-loop gain of the amplifier, and p_z , p_1 , p_2 , and p_3 are the zero point, main pole, second pole, and third pole, respectively.

Therefore, the DC gain of the two-stage amplifier reaches up to 86 dB, the -3 dB bandwidth is 200 Hz, the unity-gain bandwidth is 12 MHz, and the phase margin is approximately 80° .

4.2. Rail-to-Rail Differential Comparator. The comparator compares the output of the first- and second-stage integrators to generate a PWM waveform to drive the power

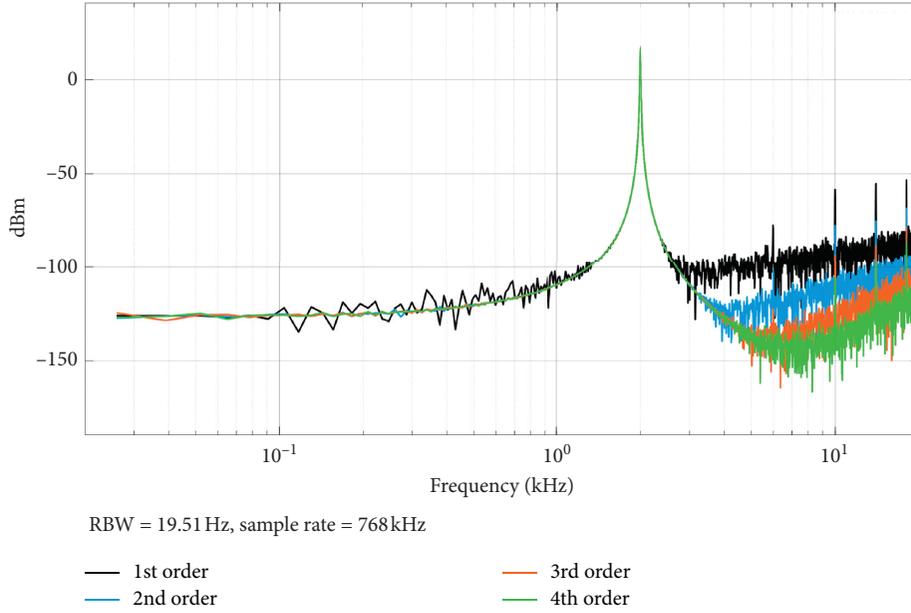


FIGURE 8: Output FFT with different orders at $f_{car} = 768$ kHz.

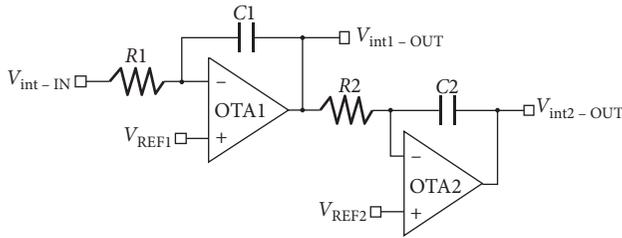


FIGURE 9: Circuit diagram of the second-order integrator.

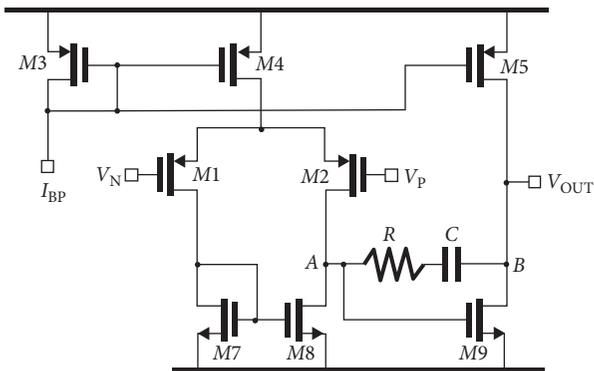


FIGURE 10: Circuit diagram of the two-stage operational amplifier.

transistor. Figure 11 shows the circuit of the rail-to-rail differential comparator, which consists of a preamplifier and a single-stage open-loop comparator.

To ensure that the comparator has sufficient accuracy, the preamplifier employs a folded cascade structure to achieve a high DC gain. Moreover, to achieve a wide swing input range, the input stage of the operational amplifier employs a rail-to-rail input structure using NMOS and PMOS in parallel to reduce the distortion. Figure 11 shows

that $M5-M9$ are current-mirror structures, which provide the bias current required for normal operation of the circuit. The load is composed of $M10-M15$, $R1$, and $R2$. In addition, $R1$ and $R2$ form a common-mode feedback circuit.

The single-stage open-loop comparator consists of a single-stage OTA and two-stage buffers. $M16-M19$ are composed of a simple OTA to realize the function of converting the differential output to a single output. The two-stage buffer plays an isolation role and improves the driving ability of the circuit.

4.3. Output-Power Stage. The power transistor of CDAs can be considered as equivalent to a switch. In reality, the power transistor is not an ideal switch when it turns on, and the influence of the on-resistance should be considered. When current flows through the on-resistance, it generates heat loss, which is called conduction loss. On the other hand, when the PWM signal drives the power transistor to turn it on or off, the gate capacitance is charged and discharged, resulting in a switching loss.

Figure 12 shows the equivalent diagram of the power transistor [26]. G , S , D , and B represent the gate, source, drain, and substrate of the power transistor, respectively. R_{on} is the equivalent on-resistance. The parasitic capacitance mainly includes gate-drain capacitance C_{GD} , gate-source capacitance C_{GS} , and the junction capacitances (C_{SB} , C_{DB} , and C_{GB}).

The on-resistance of the power transistor can be expressed as

$$R_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH})}, \quad (6)$$

where L and W are the gate length and gate width of the power transistor, respectively, μ is the carrier mobility, and

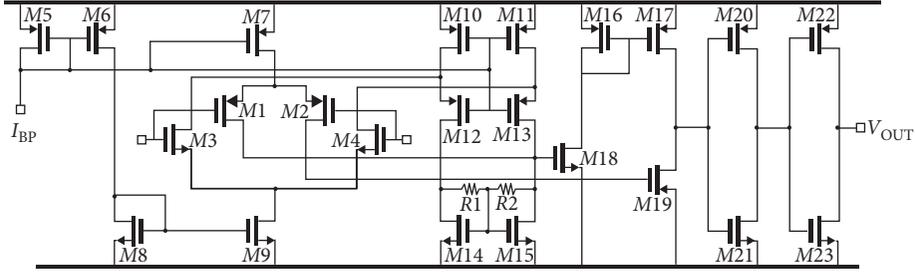


FIGURE 11: Rail-to-rail differential comparator.

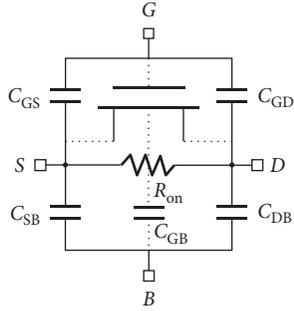


FIGURE 12: Equivalent diagram of the power transistor.

C_{ox} is the unit gate capacitance. Therefore, conduction loss P_{con} of the power transistor can be expressed as

$$P_{con} = I_{rms}^2 R_{on}, \quad (7)$$

where I_{rms} is the effective value of the current that flows through the power transistor. P_{con} is proportional to L and inversely proportional to W .

Total gate capacitance C_G of the power transistor can be expressed as

$$C_G = C_{ox}WL + 2C_{ox}x_dW, \quad (8)$$

where x_d is the transverse diffusion length. Thus, switching loss P_{sw} can be expressed as

$$P_{sw} = C_G V_{DD}^2 f_{sw}, \quad (9)$$

where f_{sw} and V_{DD} are the frequency and amplitude of the PWM signal, respectively. P_{sw} is proportional to W and L .

To achieve an optimal trade-off between the conduction and switching losses, the dimensions of the PMOS power transistor are $W = 1200 \mu\text{m}$ and $L = 0.18 \mu\text{m}$, and those of the NMOS power transistor are $W = 400 \mu\text{m}$ and $L = 0.18 \mu\text{m}$. Moreover, Figure 13 shows the gate-driving circuit. It consists of a nonoverlap configuration and an inverter-chain driving circuit to reduce the short-circuit current and parasitic gate capacitance of the power transistor [27].

4.4. Closed-Loop Negative Feedback. There are two major types of architecture for closed-loop negative feedback. The first one is the single-loop and the second is the multiloop. A major drawback of the multiloop architecture is that precise matching of the analog and digital signal processing paths is required to avoid large errors caused by integrator gain

coefficient variations [28]. To reduce the noise and non-linearity of the system, the proposed CDA adopts a second-order single-feedback loop structure [29, 30]. Figure 14 shows the closed-loop negative feedback structure of the proposed CDA; R_{FB} denotes the feedback resistor.

Figure 14(b) shows that the loop gain of the closed-loop system is calculated as

$$H(s) = H_{int1}(s)G_{PWM}(s)H_2(s)[1 - H_{int2}(s)]. \quad (10)$$

The transfer function of the closed-loop system is given by

$$V_{OUT}(s) = STF(s)V_{IN}(s) + NTF(s)V_N(s), \quad (11)$$

where

$$STF(s) = \frac{H_1(s)H_{int1}(s)G_{PWM}(s)[1 - H_{int2}(s)]}{1 + H_{int1}(s)G_{PWM}(s)H_2(s)[1 - H_{int2}(s)]}, \quad (12)$$

$$NTF(s) = \frac{1}{1 + H_{int1}(s)G_{PWM}(s)H_2(s)[1 - H_{int2}(s)]}. \quad (13)$$

The THD and PSRR of the closed-loop system are expressed as

$$THD = \frac{\sqrt{\sum_{n \neq 1}^{\infty} [V_N(s)]^2}}{STF(s)V_{IN}(s)[1 + H(s)]} \times 100\%, \quad (14)$$

$$PSRR = 20 \log \left[\frac{V_{OUT}(s)}{V_N(s)} \right] = -20 \log [1 + H(s)]. \quad (15)$$

Owing to the closed-loop negative feedback technology, equation (13) indicates that the noise function of the closed-loop system exhibits high-pass characteristics. The noise-shaping technology can be realized by reasonably setting the loop gain of the system. Equation (14) indicates that the THD of the closed-loop system also decreases with the increase in the loop gain, which greatly improves the system performance. Equation (15) illustrates that the PSRR of the closed-loop system also becomes more negative as the loop gain increases, and the ability to suppress the power-supply noise becomes stronger. Because of the voltage negative feedback effect, the output impedance of the closed-loop system is reduced and is independent of the load. During the stabilization of the output impedance, it reduces the voltage division by the output impedance; thus, more power can be

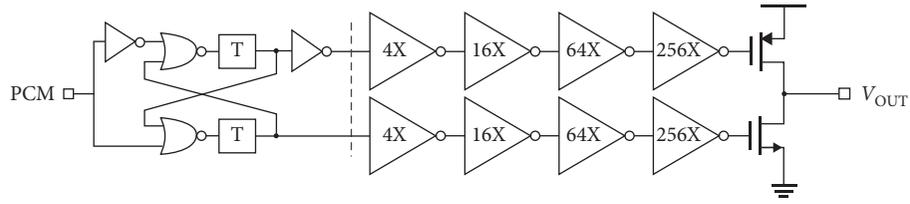
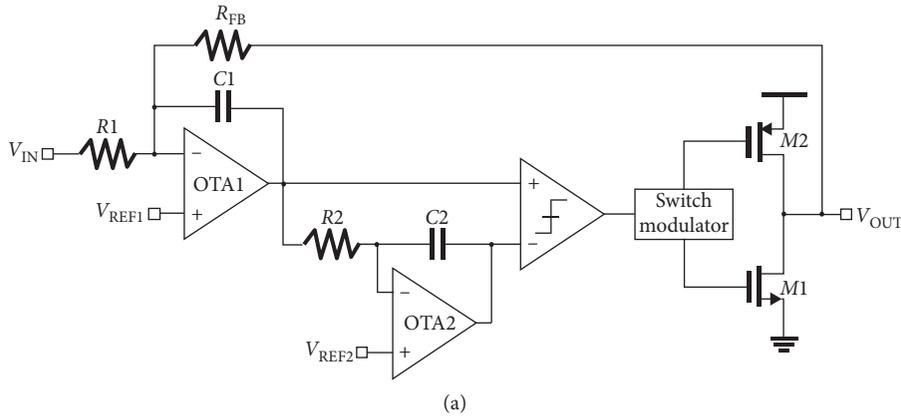
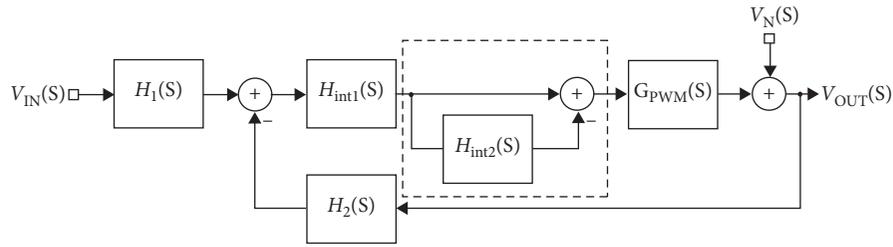


FIGURE 13: Gate-driving circuit.



(a)



(b)

FIGURE 14: (a) Circuit diagram of the second-order closed-loop negative feedback. (b) Small-signal equivalent model.

obtained from the load, and the system efficiency is improved.

5. Simulation Results

The proposed CDA consists of digital and analog modules. The digital module is implemented on the field-programmable gate array (FPGA). Figure 15 shows the resource utilization and power-consumption distribution of the audio DAC. It consumes 0.128 W and uses 7100 LUTs, thus achieving 11.2% of the resource utilization rate.

The analog module of the proposed CDA is designed and fabricated in the 0.18 μm BCD technology. The main circuit uses a 3.6 V power supply, and the output-power stage uses a 5 V power supply. Figure 16 shows the layout photograph of the proposed CDA. The active chip area is approximately 1 mm^2 .

Figure 17 shows the efficiency performance of the proposed CDA at a load of 4 Ω and an audio input frequency of 1 kHz. When the output power is lower, the efficiency is dominated by the system load. With the increase in the output power, the efficiency also gradually increases and tends to become flat. Figure 18 shows the THD performance of the proposed CDA at a load of 4 Ω and an audio input frequency of 1 kHz with a transient noise. The optimal THD (with transient noise) is less than 0.01%. Table 1 lists the summary of the CDA performance and its comparison with the state-of-the-art CDAs. Compared with the digital [31] and analog [32] CDAs, the proposed CDA presents a significant advantage of higher output power for 1%THD + N. It achieves lower THD + N compared with the analog [17, 33] and digital [34] CDAs. Furthermore, it achieves higher efficiency than the others. In summary, the proposed CDA demonstrates good performance.

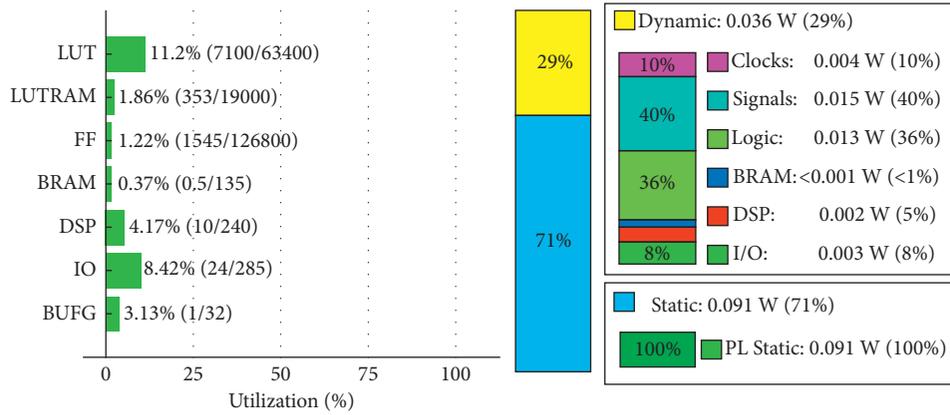


FIGURE 15: Resource utilization and power-consumption distribution in the field-programmable gate array (FPGA).

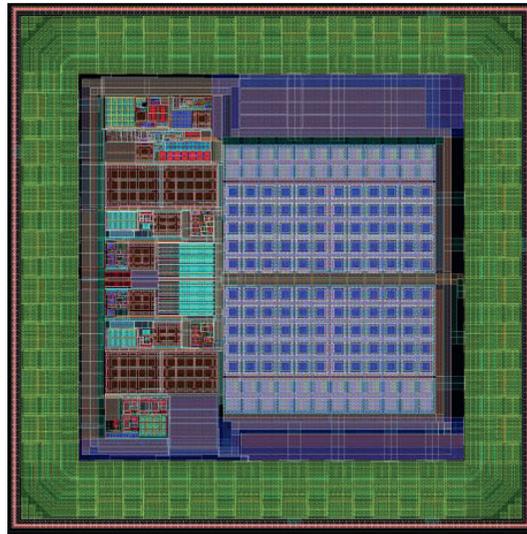


FIGURE 16: Layout photography of the proposed CDA.

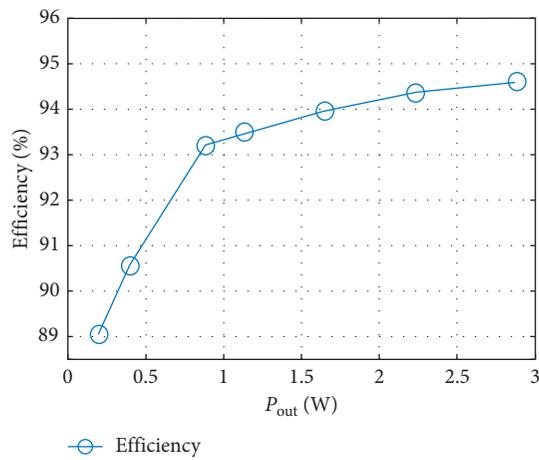


FIGURE 17: Efficiency versus output power at a 4Ω load.

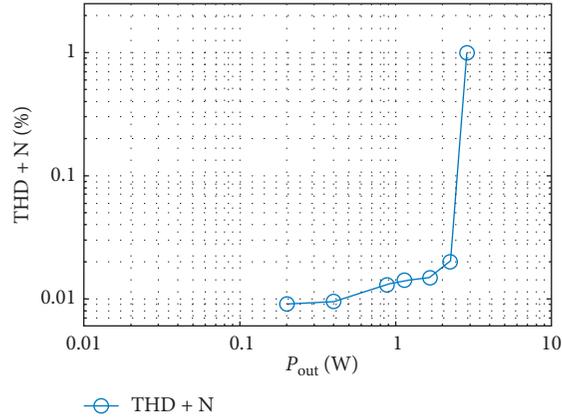
FIGURE 18: THD versus output power at a 4 Ω load with transient noise.

TABLE 1: The comparison with literature.

| Parameter | [17] | [31] | [32] | [33] | [34] | This work ¹ |
|-----------------------------|------------------------|-------------------------|------------------------|------------|-------------------------|------------------------|
| Process | 0.5 μm CMOS | 0.14 μm CMOS | 0.7 μm CMOS | 45 nm CMOS | 0.14 μm CMOS | 0.18 μm BCD |
| Power supply (V) | 2.5 | 3.7, 5.0 | 5.0 | 4.8 | 3.7 | 3.6, 5.0 |
| Modulator architecture | RWDM | $\Delta\Sigma$ + DPWM | HM | NBDDM | $\Delta\Sigma$ + DPWM | $\Delta\Sigma$ + UPWM |
| Input type | Analog | Digital | Analog | Analog | Digital | Digital |
| Output load (Ω) | 8 | 8 | 8 | 8 | 4 | 4 |
| Efficiency (%) | 88~92 | 92 | 84.5 | 90 | 90 | 93.3 |
| THD + N (%) | 0.5 | 0.01 | 0.003 | 0.1 | 0.03 | 0.0138 |
| Output power @ THD + N = 1% | — | 1 | 1.4 | — | 2.7 | 2.73 |
| Area (mm^2) | 0.59 | — | 6 | 0.54 | 1.59 | 1 |

¹Postlayout simulation results with transient noise. RWDM: rectangular wave delta modulator; HM: hysteretic modulator; NBDDM: natural sampled-BD-double-sided modulator.

6. Conclusion

A high-fidelity and high-efficiency CDA has been proposed, which consists of digital and analog modules. To achieve compatible digital input, the audio DAC is implemented using digital circuits. The CDA employs the closed-loop negative feedback and loop-filtering technologies to reduce distortion. The analog module is fabricated in a 0.18 μm BCD technology. The simulation results show that it achieves 0.0138% THD (with transient noise) and 93.3% efficiency for a 1 kHz input sinusoidal test tone and 4 Ω load. The output power reaches up to 2.73 W for 1% THD (with transient noise).

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

This work has been supported by the Natural Science Foundation of Fujian Province, China (Grant no. 2018J01803).

References

- [1] J. Klugbauerheilmeier, "A sigma-delta power amplifier for digital input signals," in *Proceedings of the 102nd Audio Engineering Society Convention*, pp. 1–9, Munich, Germany, March 1997.
- [2] A. Grosso, E. Botti, F. Stefani, and M. Ghioni, "A 250 W audio amplifier with straightforward digital input-PWM output conversion," in *Proceedings of the 27th European Solid-State Circuits Conference*, pp. 225–228, Villach, Austria, September 2001.
- [3] M. Teplechuk, T. Gribben, and C. Amadi, "Filterless integrated class-D audio amplifier achieving 0.0012% THD+N and 96dB PSRR when supplying 1.2W," in *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 240–242, San Francisco, CA, USA, February 2011.
- [4] A. Nagari, E. Allier, F. Amiard, V. Binet, and C. Fraise, "An 8 Ω 2.5 W 1%-THD 104 dB(A)-Dynamic-Range class-D audio amplifier with ultra-low EMI system and current sensing for speaker protection," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3068–3080, 2012.
- [5] T. Ido, S. Ishizuka, L. Risbo, F. Aoyagi, and T. Hamasaki, "A digital input controller for audio class-D amplifiers with 100W 0.004% THD+N and 113dB DR," in *Proceedings of 2006 IEEE International Solid State Circuits Conference-Digest Of Technical Papers*, pp. 1366–1375, San Francisco, CA, USA, February 2006.
- [6] C. Trehan and K. S. Chao, "A high efficiency sigma-delta based direct digital amplifier," in *Proceedings of 2008 51st Midwest Symposium on Circuits and Systems*, pp. 378–381, Knoxville, TN, USA, August 2008.

- [7] R. McKenzie, X. Li, M. Snelgrove, and W. Ng, "A digital class D audio amplifier with pulse density modulation and distortion suppression feedback loop," in *Proceedings of the 143rd Audio Engineering Society Convention*, p. 9859, New York, NY, USA, October 2017.
- [8] K. P. Sozański, "A digital click modulator for a class-D audio power amplifier," *Signal Processing Algorithms, Architectures, Arrangements, and Applications SPA 2009*, vol. 51, pp. 121–126, 2009.
- [9] L. Stefanazzi, F. Chierchie, E. E. Paolini, and A. R. Oliva, "Low distortion switching amplifier with discrete-time click modulation," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3511–3518, 2014.
- [10] W. Mathis and O. Schnick, "A high performance open loop all-digital class-D audio power amplifier using zero positioning coding (ZePoC)," in *Proceedings of the 120th Audio Engineering Society Convention*, p. 6695, Paris, France, May 2006.
- [11] M. Streitenberger and W. Mathis, "A novel coding topology for digital class-D audio power amplifiers with very low pulse-repetition rate," in *Proceedings of the 28th European Solid-State Circuits Conference*, pp. 515–518, Florence, Italy, September 2002.
- [12] M.-T. Tan, H. C. Chua, B. H. Gwee, and J. S. Chang, "An investigation on the parameters affecting total harmonic distortion in class D amplifiers," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'00)*, pp. 193–196, Geneva, Switzerland, May 2000.
- [13] W. Shu and J. S. Chang, "THD of closed-loop analog PWM class-D amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1769–1777, 2008.
- [14] E. Gaalaas, B. Y. Liu, and N. Nishimura, "Integrated stereo delta-sigma class D amplifier," in *Proceedings of ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference*, pp. 120–588, San Francisco, CA, USA, March 2005.
- [15] C.-W. Lin, Y.-P. Lee, and W.-T. Chen, "A 1.5 bit 5th order CT/DT delta sigma class D amplifier with power efficiency improvement," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'08)*, pp. 280–283, Seattle, WA, USA, May 2008.
- [16] J. Torres, A. Colli-Menchi, M. A. Rojas-Gonzalez, and E. Sanchez-Sinencio, "A low-power high-PSRR clock-free current-controlled class-D audio amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1553–1561, 2011.
- [17] S. C. Li, V. C.-C. Lin, K. Nandhasri, and J. Ngarmnil, "New high-efficiency 2.5 V/0.45 W RWDM class-D audio amplifier for portable consumer electronics," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 9, pp. 1767–1774, 2005.
- [18] H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer, "A low-power stereo 16-bit CMOS D/A converter for digital audio," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1290–1297, 1988.
- [19] X. Yao, L. Liu, D. Li, L. Chen, and Z. Wang, "A 90dB DR audio delta-sigma DAC with headphone driver for hearing aid," in *Proceedings of the 3rd International Congress on Image and Signal Processing*, pp. 2890–2893, Yantai, China, October 2010.
- [20] H. T. Jøsok, *Realization of Sigma-Delta DAC for Audio Application on FPGA*, Norwegian University of Science and Technology, Trondheim, Norway, 2017.
- [21] S. An, S. Xia, Y. Ma et al., "A low power sigma-delta modulator with hybrid architecture," *Sensors*, vol. 20, no. 18, p. 5309, 2020.
- [22] P. M. Aziz, H. V. Sorensen, and J. van der Spiegel, "An overview of sigma-delta converters," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61–84, 1996.
- [23] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, and R. P. Martins, "A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH $\Delta\Sigma$ modulator with multirate opamp sharing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 10, pp. 2641–2654, 2017.
- [24] M. Sadollahi and G. C. Temes, "A 10-MHz BW 77.9 dB SNDR DT MASH $\Delta\Sigma$ ADC with NC-VCO-based quantizer and OPAMP sharing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3384–3392, 2019.
- [25] Z. Song and D. V. Sarwate, "The frequency spectrum of pulse width modulated signals," *Signal Processing*, vol. 83, no. 10, pp. 2227–2258, 2003.
- [26] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd edition, McGraw-Hill Education: 2 Penn Plaza, New York, NY, USA, 2001.
- [27] J. S. Chang, M.-T. Meng-Tong Tan, Z.-H. Zhihong Cheng, and Y.-C. Yit-Chow Tong, "Analysis and design of power efficient class D amplifier output stages," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 47, no. 6, pp. 897–902, 2000.
- [28] V. Kledrowetz, L. Fucik, R. Prokop, and J. Háze, "A 1 V 92 dB SNDR 10 kHz bandwidth second-order asynchronous delta-sigma modulator for biomedical signal processing," *Sensors*, vol. 20, no. 15, p. 4137, 2020.
- [29] T. Ge, J. S. Chang, and W. Shu, "Modeling and analysis of PSRR in analog PWM class D amplifiers," in *Proceedings of the IEEE International Symposium On Circuits and Systems (ISCAS'06)*, p. 4, Island of Kos, Greece, May 2006.
- [30] C. K. Lam, M. T. Tan, S. M. Cox, and K. S. Yeo, "Class-D amplifier power stage with PWM feedback loop," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3870–3881, 2013.
- [31] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 5, pp. 992–1002, 2010.
- [32] J. Lu and R. Gharpurey, "Design and analysis of a self-oscillating class D audio amplifier employing a hysteretic comparator," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2336–2349, 2011.
- [33] S. Samala, V. Mishra, and K. C. Chakravarthi, "45nm CMOS 8 Ω Class-D audio driver with 79% efficiency and 100dB SNR," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 86–87, San Francisco, CA, USA, February 2010.
- [34] L. Dooper and M. Berkhout, "A 3.4 W digital-in class-D audio amplifier in 0.14 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1524–1534, 2012.