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Research Article

Modified Space Vector Modulation for Cascaded H-Bridge Multilevel Inverter with Open-Circuit Power Cells

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In this research, a new space vector modulation control algorithm is proposed to increase the reliability of the cascaded H-bridge multilevel inverters in case of faulty situations, where one or several power cells do not function. Methods to detect faults ensure finding open-circuit module exactly, which is fast and easy to program. By giving a detailed analysis of the impact of the faulty power cells, optimal redundant level states are chosen such that highest possible output voltage can be achieved, while the balance of the three-phase line-to-line voltage is maintained and common-mode voltage is reduced. The proposed algorithm is generalized so that it can be applied to H-bridge inverters of any level. The validity of the method is verified by numerical simulations and experiment results with an 11-level cascaded H-bridge inverter.

1. Introduction

Multilevel inverters are increasingly popular in industrial factory, which operate with high-voltage system [1, 2]. Three typical multilevel structures are Neutral Point Clamped (NPC) inverter [3, 4], Flying Capacitor (FC) inverter [5, 6], and Cascaded H-Bridge Multilevel Inverter (CHB-MLI) [7, 8]. Figure 1 depicts general structure of CHB-MLI. This topology can increase the output voltage range by adding more modules, so that it can be easier to maintain and control the output voltage effectively. However, CHB-MLI requires isolated voltage sources for each module.

While expanding level of CHB-MLI, the number of semiconductors increases, belonging with larger possibilities of the faulty power cells. In order to keep the system operating consistently, the accurate fault diagnosis, configurations of CHB-MLI, and algorithm for faulty conditions should be done.

Short-circuit and open-circuit problems are typical faults on power cells. This paper will focus on handling open-circuit faults. There are many researches about detecting the open-circuit location on multilevel inverter. With CHB-MLI structure, in [9], the output average voltages of each cell are used for detecting open-circuit location, requiring output sensors on all of cells, and result in cost increment. However, this method is only available under ideal conditions, when the input voltage of each cell is constant during operation, so it is difficult to use it in experiment. In [10], the fault phase is identified by THD of output voltage; then the load current is used for detecting the fault switch. Nevertheless, measuring and calculating THD immediately require precision measurement circuits and high-processing-speed MCU, and the load current varies depending on the load, so it can only be analyzed precisely when the parameters of the system are constant. In [11], open-circuit and short-circuit problems can be detected by using neural network. Output voltage of each phase is measured and analyzed by DWT to sample data for neural network. The number of samples needed will increase rapidly as level of CHB-MLI increases, and it requires bigger volume of computation. With NPC structure, in [12], voltage of input capacitor and the direction of the current are used for identifying fault location. This method provides accurate results with short processing time, but the selection of the detection threshold of current is still complex, depends on parameters and states of the system, and is greatly affected by the noise. In [13], neural network is used for MMC structure, not only requires a large amount of sample data but also needs information of 53 parameters of

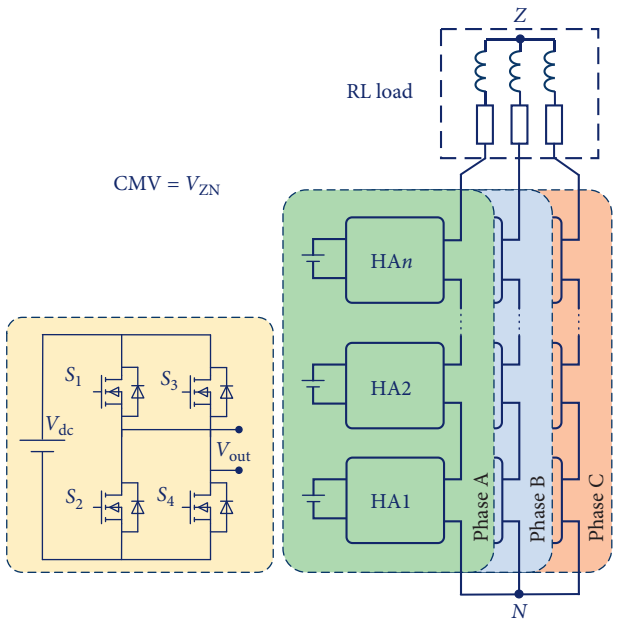


Figure 1: Cascaded H-bridge multilevel inverter.

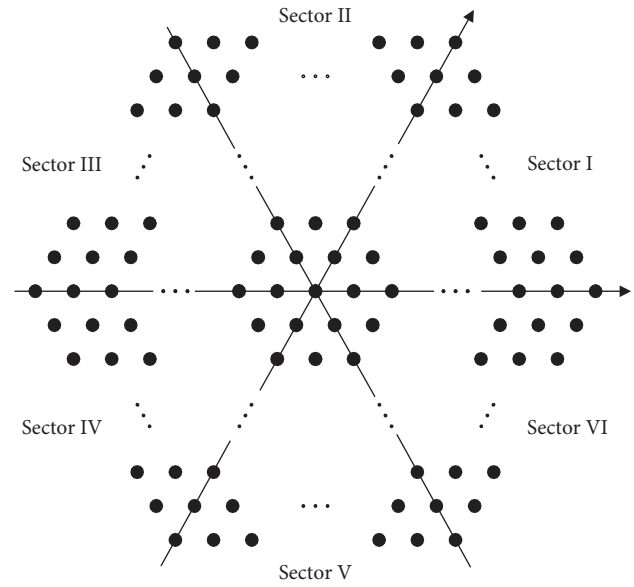


Figure 2: Space vector of CHB-MLI.

the system, and results in significant number of sensors and high capability of computation MCU. This paper proposes open-circuit detecting method for CHB-MLI topology, based on comparison of output voltage of each phase and corresponding control signal. When the difference exceeds the given threshold, cell is considered faulty and is removed from the system. This method allows detecting faults in any cells and multiple cells at the same time, and the cells are independently diagnosed.

Conventional methods are using an auxiliary module [14] and result in larger size of the converter and fundamental phase shift compensation PWM [15]; however, this comes with a large amount of computation. This paper proposes a new method, which applies space vector modulation (SVM) to operate in open-circuit conditions. Based on the characteristics of SVM, vector state has many level states, and we can choose unfaulty state to modulate vector when faults appear. SVM algorithm in case of faulty situations is generalized and can be applied to multilevel inverter with any number of levels. Common-mode voltage (CMV) has impacts on system operation, especially with motor drives [16]. For decades, passive filters [17, 18] and active filters [19] have been proposed to reduce the impact of CMVs. However, these methods cause the volume and the control of the equipment to increase significantly. Using the advantages of SVM, appropriate state will be chosen to achieve minimum CMV while operating effectively in faulty conditions. RL load will be used to evaluate the behaviours of system.

2. Operating System in Faulty Conditions

2.1. Open-Circuit Power Cells. Open-circuit issue is the most common fault of converter. The open-circuit semiconductor cannot conduct current when receiving control signal. Figure 2 illustrates location of vector states in space of CHB-MLI. When open-circuit problem occurs, some level states cannot function. For example, the 11-level CHB-MLI can create output voltage in range of $-10\ V_{dc}$ to $10\ V_{dc}$. Assume that S_1 of a random module on phase A is open-circuit, and phase A output voltage is reduced from $-10\ V_{dc}$ to $9\ V_{dc}$. All the 10 level states on phase A are unusable. Figure 3 shows the vector space of CHB-MLI in case of situations where one or several cells are facing problems. Red triangles and red lines represent error vector state and layer fault vector, respectively. Locations of space vectors are summarized in Table 1.

2.2. Configuration of Converter. A contactor is added to output of each cell to remove module. Normally, cell is connected to system; if one of the semiconductors of cell is open, the contactor will close and take off that cell by connecting 2 outputs, as described in Figure 4.

2.3. Configuration of Converter Detecting Location of Fault. In the proposed technique, output voltage of cell x is measured and standardized and then is compared with corresponding control signal. While observing these 2 signals, if the error exceeds the given conditions, that cell is considered to be a faulty cell and will be removed from the system. Figure 5 portrays the structure of error detection algorithm.

2.3.1. V_{out_cellx} and Standardized Block. The output voltage of cell x is measured; it can be $-V_{dc}$; 0; V_{dc}. V_{out_cellx} then will be passed into standardized block and compared with a given threshold (TH) and finally changed into logic signal:

$$\begin{cases} V_{\text{out\_cell}x} \geq \text{TH} \Longrightarrow V_{\text{c\_cell}x} = 1, \\ V_{\text{out\_cell}x} \leq -\text{TH} \Longrightarrow V_{\text{c\_cell}x} = -1, \\ -\text{TH} \leq V_{\text{out\_cell}x} \leq \text{TH} \Longrightarrow V_{\text{c\_cell}x} = 0. \end{cases} \quad (1)$$

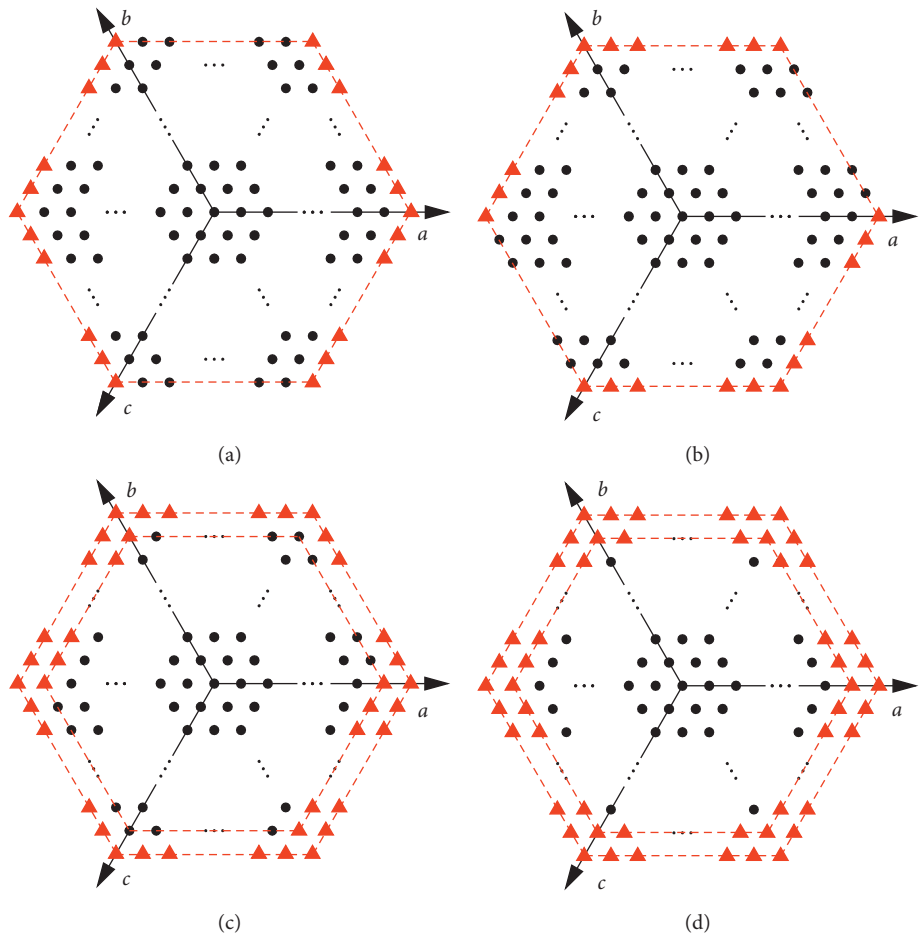


Figure 3: Effect of open-circuit problem to space vector. (a) One faulty cell in A. (b) One faulty cell in B. (c) One faulty cell in each of phase A and phase B. (d) One faulty cell in each of phase A, phase B, and phase C.

Table 1: Affected sector by fault.

Affected sector	Phase with faulty cells		
	Phase A	Phase B	Phase C
I	Yes	No	Yes
II	No	Yes	Yes
III	Yes	Yes	No
IV	Yes	No	Yes
V	No	Yes	Yes
VI	Yes	Yes	No

In fact, V_{dc} can fluctuate; the TH value must be calculated carefully to compensate for this tolerance to make the standardized signal accurate. Therefore, $V_{dc}/2$ is the appropriate value for TH threshold [20].

2.3.2. KH_{cellx} and Error. KH_{cellx} is the corresponding control signal of cell x, which can be used to create desired output voltage. Table 2 describes the relationship between KH_{cellx} and V_{out_cellx} in stabilized state. V_{c_cellx} is compared with KH_{cellx}; error is set to 1 if V_{c_cellx} is not equal to KH_{cellx} and equals 0 when V_{c_cellx} equals KH_{cellx}:

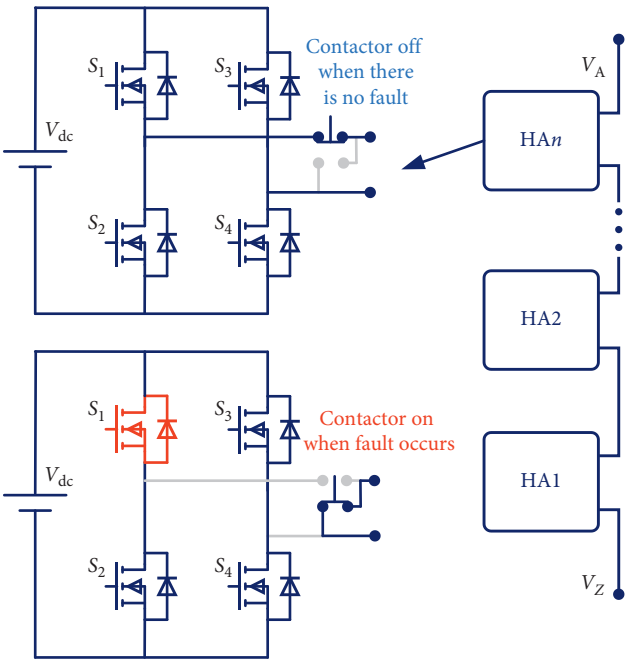


Figure 4: Output contactor of cell.

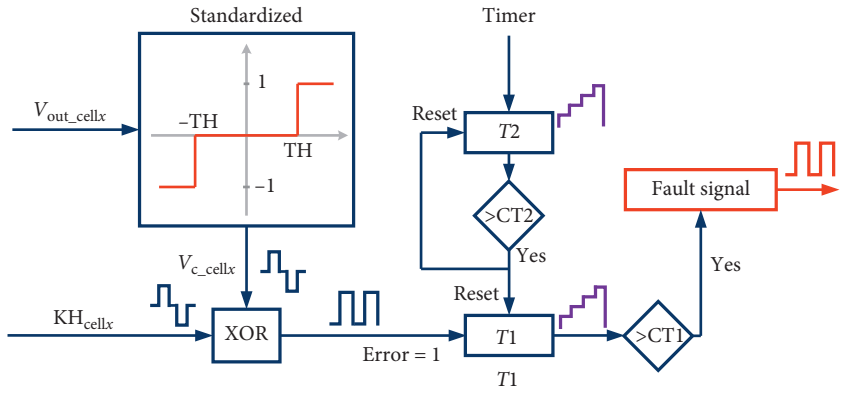
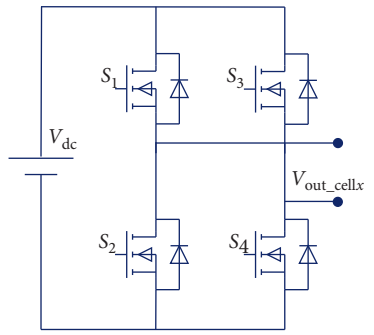


Figure 5: Block diagram of the proposed fault detection method.

Table 2: Relationship between output voltage and control signal of cell x.

Switching state				V_{out_cellx}	KH_{cellx}
S_1	S_2	S_3	S_4		
1	0	1	0	0	0
1	0	0	1	V_{dc}	1
0	1	1	0	$-V_{dc}$	−1
0	1	0	1	0	0



$$V_{c\_cellx} = KH_{cellx} \Longrightarrow \text{error} = 0,$$
$$V_{c\_cellx} \neq KH_{cellx} \Longrightarrow \text{error} = 1. \quad (2)$$

2.3.3. T1 and T2. Due to the delay of sensor signal, the semiconductors being not switched immediately, deadtime requirement, and delay of controller, there is always a delay time between V_{c_cellx} and KH_{cellx}, even in normal condition, called T_{delay}. To overcome this issue, 2 counter $T1$ and $T2$ are used. $T1$ starts to count when error = 1, until reaching CT1; then the fault signal will be set. CT1 selection depends on T_{delay}. Assume that T_{delay} = 1 ms; CT1 needs to be bigger than 1 ms to avoid wrong error detection. This algorithm operates in a certain period, controlled by $T2$ counter: at the end of the period, when $T2 > CT2$, both $T1$ and $T2$ are reset.

$$T1 > CT1 \Longrightarrow \text{faultsignal} = 1,$$
$$T2 > CT2 \Longrightarrow \begin{cases} T1 = 0, \\ T2 = 0. \end{cases} \quad (3)$$

The relationships between signals in algorithm are illustrated in Figure 6.

Table 3 compares the proposed method with methods cited in the last section. With CHB-MLI topology, various methods are implemented: using average output voltage of each cell [9], analyzing load current and THD of output voltage [10], and using neural network for output voltage analysis [11]. In [12], voltage of input capacitor and the direction of the current are used for NPC structure. In [13], neural network is used for analyzing parameters of MMC system. By observing the table, we can realize that the proposed method has a simple structure and quick identification in 1 ms, in addition to being less affected by noise, but needs an additional sensor to measure the voltage at the output of each cell.

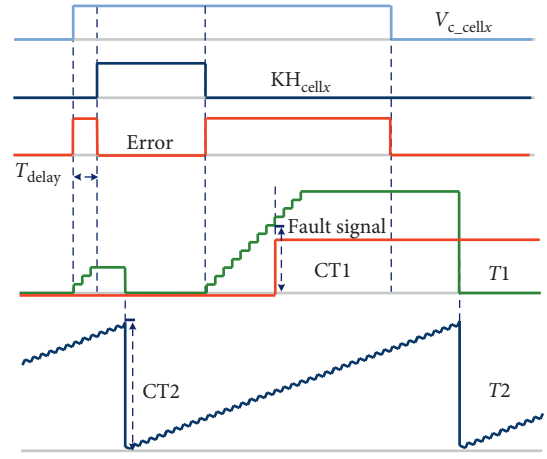


Figure 6: V_{c_cellx}, KH_{cellx}, fault signal, and $T1$ and $T2$.

2.4. SVM Method in Faulty Conditions for CHB-MLI. To make sure that CHB can work precisely while facing open-circuit problem, this paper proposes SVM technique, which

Table 3: Comparison of detected fault method for multilevel inverters.

Comparison indexes	[9]	[10]	[11]	[12]	[13]	Proposed
Software complexity	Complex	Simple	Complex	Simple	Complex	Simple
Input data	Output voltage cell	Current load	Output voltage inverters	Capacitor voltage and current	53 inputs	Output voltage cell
Modularity and expandability	High	Low	Low	High	Low	High
Location time	40 ms	20 ms	10 ms	1.4 ms	20 ms	1 ms
Type of inverter	CHB	CHB	CHB	NPC	MMC	CHB
Hardware configuration	Additional voltage sensors at the output of each cell	Existing hardware	Additional voltage sensors at the output of inverters	Existing hardware	A lot of sensors	Additional voltage sensor at the output of each cell
Noise robustness	Weak	Weak	Weak	Weak	Weak	Strong

is developed from general method. Based on the advantage of having many redundant states, the faulty states can be removed, and the nonfault states can be chosen to achieve the minimum CMV.

2.4.1. New Reference Voltage Calculation. When open-circuit problem happens, some level states cannot be performed, creating layer fault vector. These layers need to be removed to keep operating the system. This section will determine the number of layer fault vectors and the maximum voltage that can be modulated and then calculate a new reference voltage.

2.4.2. Determine Level State under Faulty Condition. The number of layers on sectors of vector space can be obtained by the following equation:

$$\begin{cases} e_{\mathrm{I}} = e_{\mathrm{A}} + e_{\mathrm{C}}, \\ e_{\mathrm{II}} = e_{\mathrm{B}} + e_{\mathrm{C}}, \\ e_{\mathrm{III}} = e_{\mathrm{A}} + e_{\mathrm{B}}, \\ e_{\mathrm{IV}} = e_{\mathrm{A}} + e_{\mathrm{C}}, \\ e_{\mathrm{V}} = e_{\mathrm{B}} + e_{\mathrm{C}}, \\ e_{\mathrm{VI}} = e_{\mathrm{A}} + e_{\mathrm{B}}, \end{cases} \tag{4}$$

where $e_{\mathrm{I}\ldots\mathrm{VI}}$ is the number of faulty vector layers on sectors I...VI. The maximum number of faulty vector layers can be determined:

$$e_{\max} = \max\left(e_{\mathrm{I}}; e_{\mathrm{II}}; e_{\mathrm{III}}; e_{\mathrm{IV}}; e_{\mathrm{V}}; e_{\mathrm{VI}}\right). \tag{5}$$

The maximum magnitude of reference voltage can be achieved corresponding to the radius of the incircle of the largest hexagon, which is not affected, as depicted in Figure 7.

$$v'_{\max} = \frac{V_{\mathrm{dc}}}{\sqrt{3}}\left(m - 1 - e_{\max}\right). \tag{6}$$

After obtaining $v'_{\max}$, the new reference voltage v'_{ref} can be determined by the following algorithm in Figure 8.

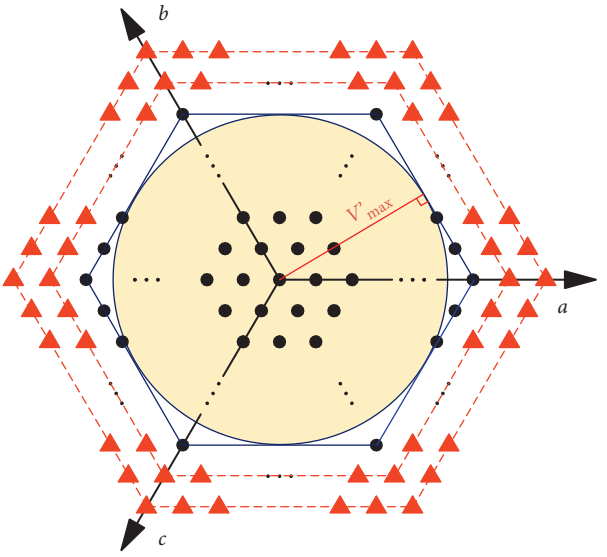


Figure 7: Calculating maximum voltage vector in faulty condition.

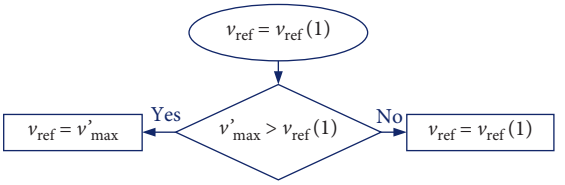


Figure 8: Algorithm flowchart of finding new reference voltage when there is an error.

2.4.3. Determine Level State under Faulty Condition. According to [21], each vector in space is determined by level states $[k_{\mathrm{AN}}, k_{\mathrm{BN}}, k_{\mathrm{CN}}]$. When phases A, B, and C have e_{A}, e_{B}, and e_{C} faulty cells, respectively, the inverter needs to be reconstructed by short-circuiting these cells through the output contactors. Thus, the output voltages are

$$\begin{cases} V_{\mathrm{AN}} = k_{\mathrm{AN}}.V_{\mathrm{dc}}, \\ V_{\mathrm{BN}} = k_{\mathrm{BN}}.V_{\mathrm{dc}}, \\ V_{\mathrm{CN}} = k_{\mathrm{CN}}.V_{\mathrm{dc}}, \end{cases} \tag{7}$$

where

$$\begin{cases} k_{\mathrm{AN}} \in \overline{-n + e_{\mathrm{A}}; n - e_{\mathrm{A}}}, \\ k_{\mathrm{BN}} \in \overline{-n + e_{\mathrm{B}}; n - e_{\mathrm{B}}}, \\ k_{\mathrm{CN}} \in \overline{-n + e_{\mathrm{C}}; n - e_{\mathrm{C}}}. \end{cases} \tag{8}$$

For sector I, consider 1 voltage vector with coordinates illustrated in Figure 9. According to [21], this voltage vector is represented as follows:

$$\begin{cases} v_{\mathrm{g}} = \dfrac{2}{3} V_{\mathrm{dc}} k_{\mathrm{g}} = \dfrac{2}{3} V_{dc} \left(k_{\mathrm{AN}} - k_{\mathrm{BN}}\right), \\ v_{\mathrm{h}} = \dfrac{2}{3} V_{\mathrm{dc}} k_{\mathrm{h}} = \dfrac{2}{3} V_{dc} \left(k_{\mathrm{BN}} - k_{\mathrm{CN}}\right), \end{cases} \tag{9}$$

$$\begin{bmatrix} k_{\mathrm{g}} \\ k_{\mathrm{h}} \end{bmatrix} = \begin{bmatrix} \left(k_{\mathrm{AN}} - k_{\mathrm{BN}}\right) \\ \left(k_{\mathrm{BN}} - k_{\mathrm{CN}}\right) \end{bmatrix}.$$

Considering a parameter k_{AN}, where $k_{\mathrm{AN}} = k$, the coordinates in 3-axis abc can be obtained in the following equation:

$$\begin{bmatrix} k_{\mathrm{g}} \\ k_{\mathrm{h}} \end{bmatrix} \Rightarrow \begin{bmatrix} k_{\mathrm{AN}} \\ k_{\mathrm{BN}} \\ k_{\mathrm{CN}} \end{bmatrix} = \begin{bmatrix} k \\ k - k_{\mathrm{g}} \\ k - k_{\mathrm{g}} - k_{\mathrm{h}} \end{bmatrix}. \tag{10}$$

The selection of the level states is done by choosing k. Therefore, for error correction and suppression of CMV, we can make the following selection. To make sure that CHB-MLI can process precisely while facing open-circuit problem, the level states must satisfy (8):

$$\begin{cases} -n + e_{\mathrm{A}} \le k \le n - e_{\mathrm{A}}, \\ -n + e_{\mathrm{B}} \le k - k_{\mathrm{g}} \le n - e_{\mathrm{B}}, \\ -n + e_{\mathrm{C}} \le k - k_{\mathrm{g}} - k_{\mathrm{h}} \le n - e_{\mathrm{C}}, \end{cases} \tag{11}$$

$$\Leftrightarrow \begin{cases} -n + e_{\mathrm{A}} \le k \le n - e_{\mathrm{A}}, \\ -n + k_{\mathrm{g}} + e_{\mathrm{B}} \le k \le n + k_{\mathrm{g}} - e_{\mathrm{B}}, \\ -n + k_{\mathrm{g}} + k_{\mathrm{h}} + e_{\mathrm{C}} \le k \le n + k_{\mathrm{g}} + k_{\mathrm{h}} - e_{\mathrm{C}}. \end{cases}$$

Therefore, k must be restricted by the following equation:

$$\max \begin{Bmatrix} -n + e_A \\ -n + k_g + e_B \\ -n + k_g + k_h + e_C \end{Bmatrix} \le k \le \min \begin{Bmatrix} n - e_A \\ n + k_g - e_B \\ n + k_g + k_h - e_C \end{Bmatrix}. \tag{12}$$

On the other hand, $V_{\mathrm{CMV}} = k_{\mathrm{CMV}} \cdot V_{\mathrm{dc}}$, where

$$k_{\mathrm{CMV}} = \frac{k_{\mathrm{AN}} + k_{\mathrm{BN}} + k_{\mathrm{CN}}}{3} = \frac{3k - 2k_{\mathrm{g}} - k_{\mathrm{h}}}{3}. \tag{13}$$

Therefore, with given k_g and k_h, k value can be easily obtained (13) while having k_{CMV} minimum. The level states can be determined as follows:

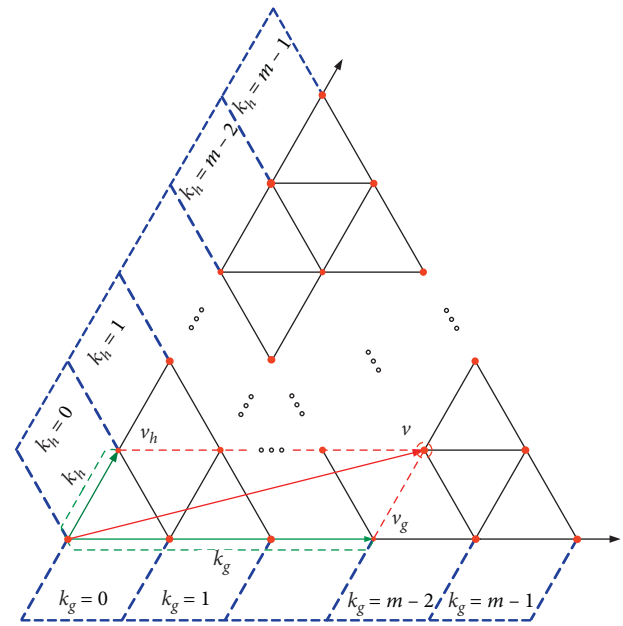


Figure 9: Voltage vector v on sector I.

$$\begin{bmatrix} k_{\mathrm{AN}} \\ k_{\mathrm{BN}} \\ k_{\mathrm{CN}} \end{bmatrix} = \begin{bmatrix} 2/3 & 1/3 & 1 \\ -1/3 & 1/3 & 1 \\ -1/3 & -2/3 & 1 \end{bmatrix} \cdot \begin{bmatrix} k_g \\ k_h \\ k_{\mathrm{CMV}} \end{bmatrix}. \tag{14}$$

Similarly, the relationships in other sectors can be acsquired, as shown in Table 4.

3. Simulation Results

Here, several simulations have been carried out on 11-level CHB-MLI by Matlab/Simulink program to verify the proposed fault-tolerant method. The proposed fault-tolerant strategy has been applied to the inverter in different conditions, such as single-fault and double-fault (simultaneous fault) conditions. Parameters of the system are shown in Table 5. Simulation scenarios are shown in Table 6.

3.1. Fault Detection. Figure 10 illustrates $V_{\mathrm{c\_cellHA3}}$, $\mathrm{KH}_{\mathrm{cellHA3}}$ signals, $T1$ and $T2$, and fault signal of HA3 in simulation. Before 0.1 s, the system operates normally and fault signal equals 0. Due to deadtime and measurement delay, T_{delay} appears, but the $T1$ counter is used for avoiding error in detection. $T2$ counter resets the algorithm after 2 ms period. After 0.1 s $S1$ switch of HA3 faces the problems, measured $V_{\mathrm{c\_cellHA3}}$ is different from $\mathrm{KH}_{\mathrm{cellHA3}}$, $T1$ starts to count and the fault is detected after 1 ms, fault signal equals 1, and HA3 is removed from the system.

Figure 11 describes fault signal of HA3, HB1, HB3, and HB5. Open-circuit problems on phase B appear at 0.2 s, according to the scenario shown in Table 6. The algorithm can detect the problem at any position and can be applied for multiple cells at the same time.

Table 4: Transition matrix $[k_{AN}, k_{BN}, k_{CN}]$ and $[k_x, k_y, \text{CMV}]$.

Sector I	$X_1 = \begin{bmatrix} 2/3 & 1/3 & 1 \\ -1/3 & 1/3 & 1 \\ -1/3 & -2/3 & 1 \end{bmatrix}$	Sector IV	$X_4 = \begin{bmatrix} -2/3 & -1/3 & 1 \\ 1/3 & -1/23 & 1 \\ 1/3 & 2/3 & 1 \end{bmatrix}$
Sector II	$X_2 = \begin{bmatrix} 1/3 & -1/3 & 1 \\ 1/3 & 2/3 & 1 \\ -2/3 & -1/3 & 1 \end{bmatrix}$	Sector V	$X_5 = \begin{bmatrix} -1/3 & 1/3 & 1 \\ -1/3 & -2/3 & 1 \\ 2/3 & 1/3 & 1 \end{bmatrix}$
Sector III	$X_3 = \begin{bmatrix} -1/3 & -2/3 & 1 \\ 2/3 & 1/3 & 1 \\ -1/3 & -1/3 & 1 \end{bmatrix}$	Sector VI	$X_6 = \begin{bmatrix} 1/3 & 2/3 & 1 \\ -2/3 & -1/3 & 1 \\ 1/3 & -1/3 & 1 \end{bmatrix}$

Table 5: Parameters for simulation.

Parameters	Value
V_{dc}	40 V
V_{ref}	185 V
Frequency	50 Hz
R load	50 ohm
L load	4 mH

Table 6: Simulation scenarios.

Time (s)	Phase with faulty cell		
	A	B	C
0-0, 1	0	0	0
0, 1-0, 2	HA3	0	0
0, 2-0, 3	HA3	HB1; HB3; HB5	0

3.2. SVM Algorithm in Faulty Condition. The simulation results are shown in Table 7 and Figure 12. When normally inverter load voltage is 185 V, inverter current is 3.8 A, 3 phases are balanced, and CMV equals $\pm V_{dc}/3$. The time interval after 0.1 s, $S1$, of HA3 is fault, and the issue is detected after 1 ms and overcome by SVM method. Voltage level of phase A falls down to 4 due to removed faulty cell. Inverter load voltage is still 185 V, and output current and the quality of voltage remain unchanged. The time intervals after 0.2 s, $S3$, of HB1, HB3, and HB5 are faults. The maximum voltage that CHB-MLI can generate is reduced, and output voltage is 138 V. Voltage level of phase B decreases to 2. Due to a change in reference voltage, the output current is reduced to 2.7 A. The CMV in these 2 situations will increase because the level states that make CMV minimum are removed.

4. Experiment Results

To verify the fault detection algorithm and the proposed SVM method, 11-level CHB-MLI system is used as shown in Figure 13. The parameters are shown in Table 5. The system is controlled by FPGA ZYNQ Z7 to increase processing speed.

4.1. Fault Detection. According to Table 6, cell HA3 is made to have open-circuit error intentionally to verify the fault detection algorithm. The results are shown in Figures 14 and 15.

Figure 14 illustrates fault signal and $KH_{cellHA3}$ and $V_{c\_cellHA3}$ signals in 2 cases. In unfaulty case, $KH_{cellHA3}$ equals $V_{c\_cellHA3}$ and fault signal is 0. When $S1$ of cell HA3 is fault, $V_{c\_cellHA3}$ is 0, while $KH_{cellHA3}$ is 1. After 1 ms, fault signal is set and cell is considered to be error. The error detection result of HB1 is exactly the same as measured on HA3. Open-circuit fault of $S3$ switch of HB1 was detected after 1 ms, shown in Figure 16. Figure 17 shows the fault signals of the cells while operating. Therefore, the error detection algorithm can detect open-circuit fault at multiple positions of CHB-MLI.

Figure 15 describes $T1$ and $T2$ signals, fault signal, and $KH_{cellHA3}$ and $V_{c\_cellHA3}$ signals of cell HA3 in FPGA. Two counters $T1$ and $T2$ have 100 kHz clock frequency, and TC1 = 100 and TC2 = 200 which correspond to 1 ms and 2 ms, respectively.

4.2. SVM Algorithm in Faulty Condition. To verify SVM algorithm in faulty condition, we do test with scenarios in Table 6. $S1$ of cell HA3 breaks down first; after 0.1 s, $S3$ of cells HB1, HB3, and HB5 are facing problem. The results for each case were put in order: (1) normal operation, (2) cell HA3 is inoperative, (3) and cells HA3, HB1, HB3, and HB5 are inoperative. In normal operation, the inverter phase's voltage has 11 levels as shown in Figure 18 (1). The inverter load voltage and inverter current are 185 V and 3.8 A, respectively, shown in Figures 19(1) and 20(1).

When $S1$ of cell HA3 is not functioning, the fault detection algorithm removes HA3 from the system, phase A has 4 active cells, and the inverter load voltage and inverter current are balanced and remain unchanged, as shown in Figures 19 (2) and 20 (2). After 0.1 s, $S3$ of cell HB1, HB3, and HB5 is not working, and the algorithm continues to remove these cells from the system. The maximum voltage on the inverter decreases, makes the inverter phase voltage and inverter current remain balanced but reduced to 138 V and 2.7 A, as shown in Figures 19 (3) and 20 (3).

Figure 21 illustrates CMV in three cases. Normally, the CMV is ±13 V. When errors occur, the CMV value increases because level states which have small CMV cannot be used for modulation.

The experiment results are the same as the simulation results in part 3, thereby verifying the accuracy of the error detection algorithm and the improved SVM algorithm.

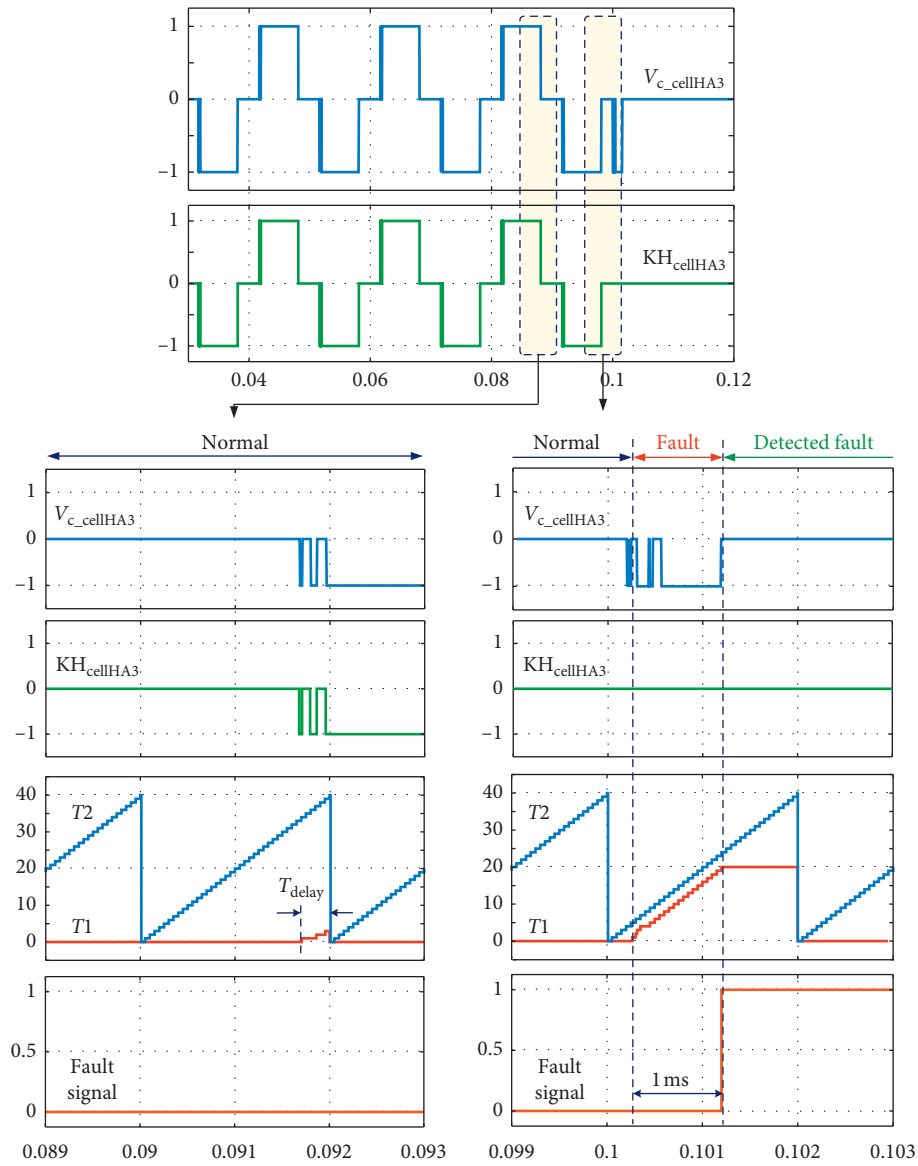


Figure 10: Waveforms of $KH_{cellHA3}$, $V_{c\_cellHA3}$, fault signal, and $T1$ and $T2$ of cell HA3 in (a) normal operation and (b) faulty condition from simulation.

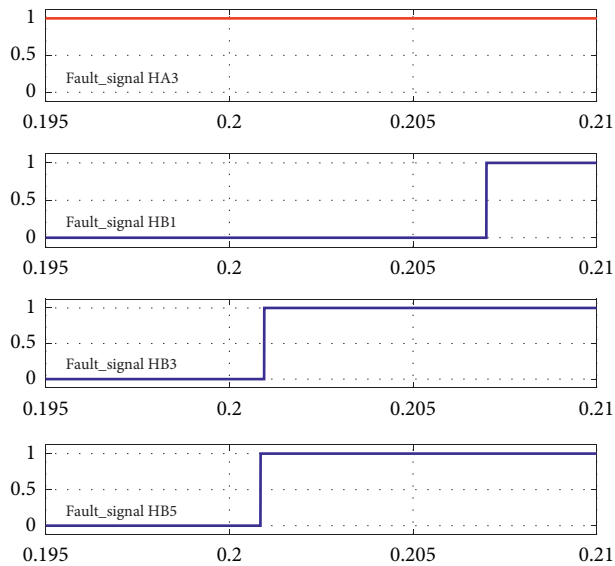


Figure 11: Fault signal of cells HA3, HB1, HB3, and HB5.

Table 7: Simulation results.

Scenarios		Normal	HA3 is fault	HA3, HB1, HB3, and HB5 are fault
Time		0–0.1 s	0.1 s–0.2 s	0.2 s–0.3 s
Reference voltage		185 V		
Output voltage		185 V		138 V
Level state	Phase A	[−5; 5]	[−4; 4]	[−4; 4]
	Phase B	[−5; 5]	[−5; 5]	[−2; 2]
	Phase C	[−5; 5]	[−5; 5]	[−4; 4]
THD (%)		3.04	3.04	5.42
Current (A)		3.8	3.8	2.7
CMV		[−13 V; 13 V]	[−40 V; 40 V]	[−66 V; 66 V]

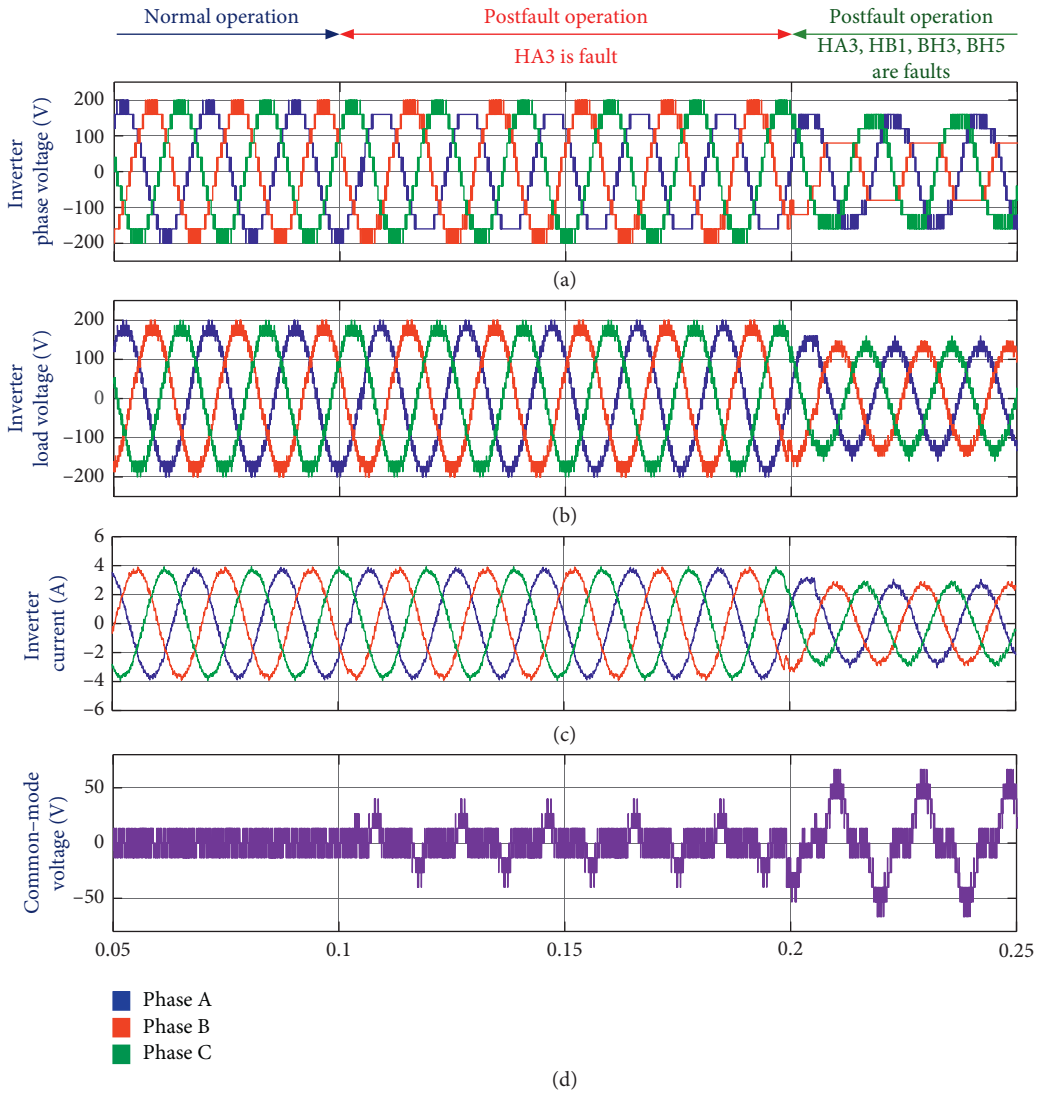


Figure 12: Waveforms of (a) inverter phase voltage, (b) inverter load voltage, (c) inverter current, and (d) CMV from simulation.

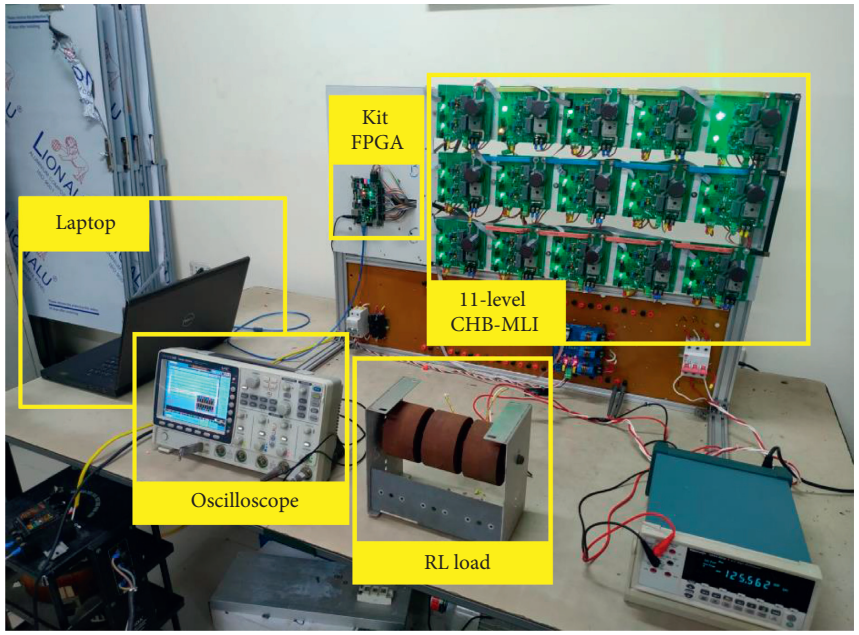
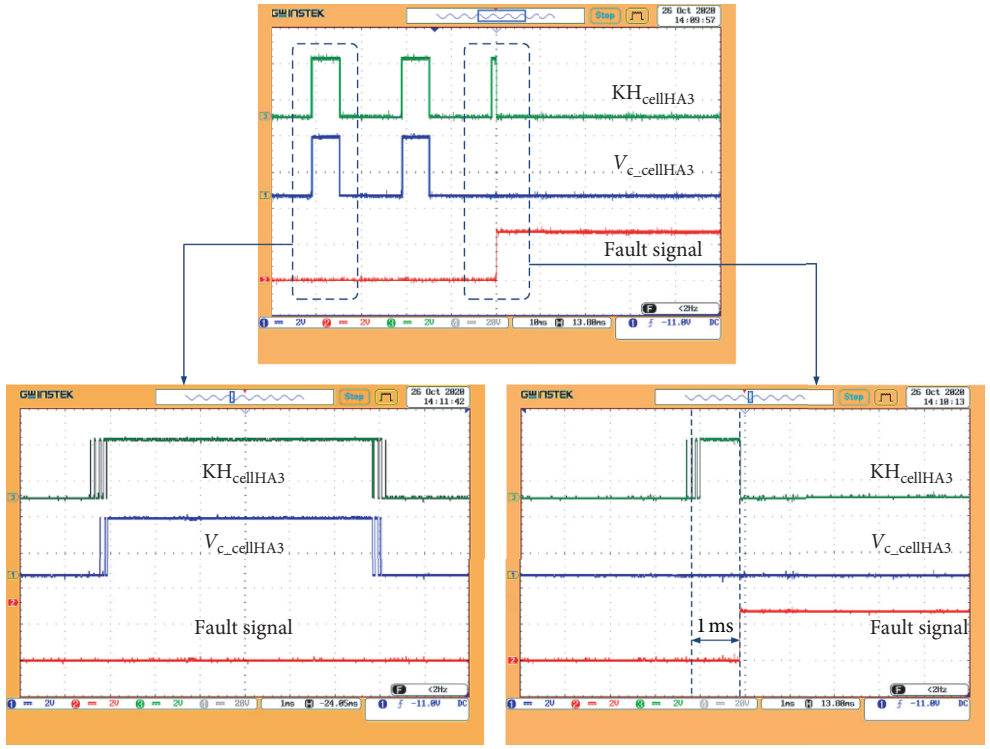
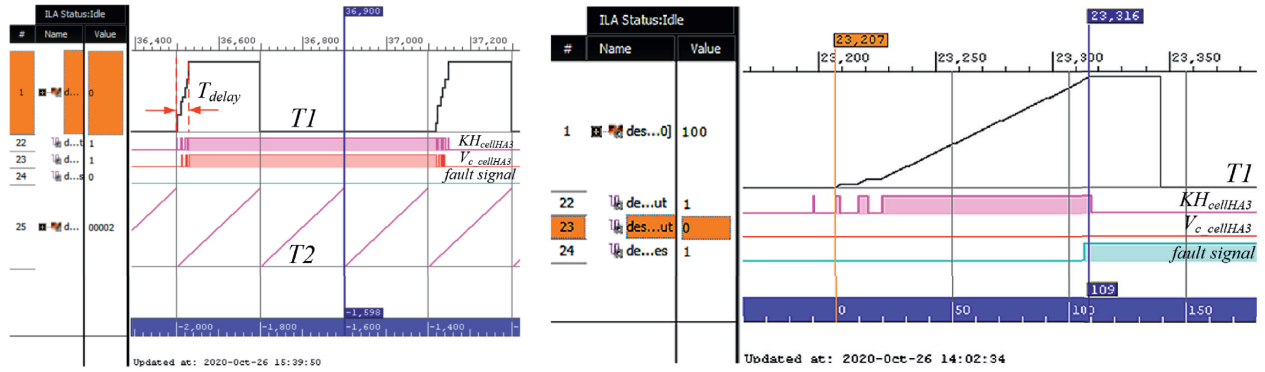


Figure 13: Laboratory experimental setup.



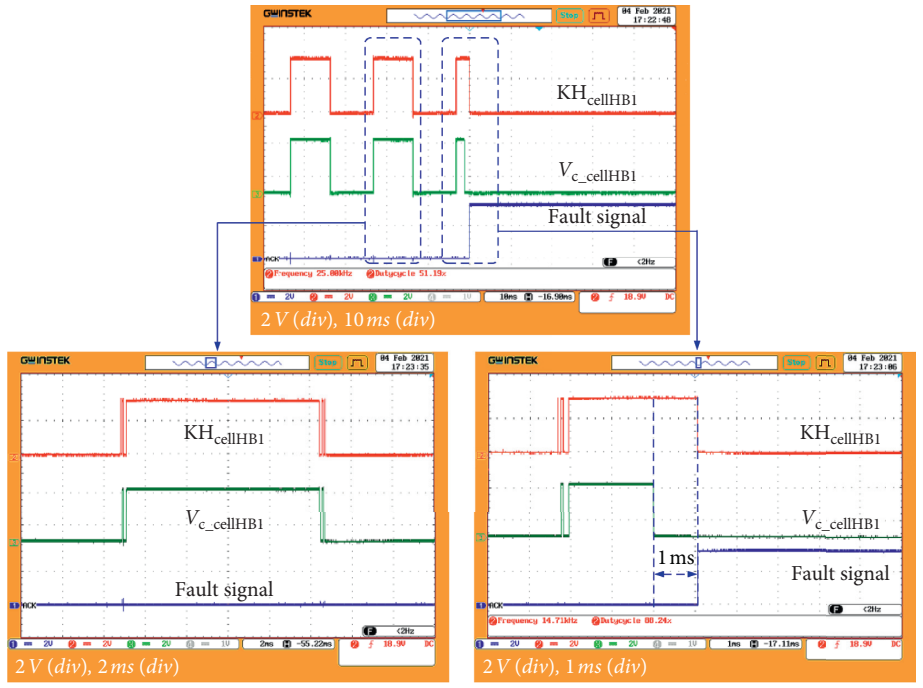
(a) (b)

Figure 14: Waveforms of fault signal and $KH_{cellHA3}$ and $V_{c\_cellHA3}$ of cell HA3 in (a) normal operation and (b) faulty condition from experiment.



(a) (b)

FIGURE 15: Waveforms of $T1$ and $T2$, fault signal, and $KH_{cellHA3}$ and $V_{c\_cellHA3}$ of cell HA3 on FPGA in (a) normal operation and (b) faulty condition from experiment.



(a) (b)

FIGURE 16: Waveforms of fault signal and $KH_{cellHB1}$ and $V_{c\_cellHB1}$ of cell HB1 in (a) normal operation and (b) faulty condition from experiment.

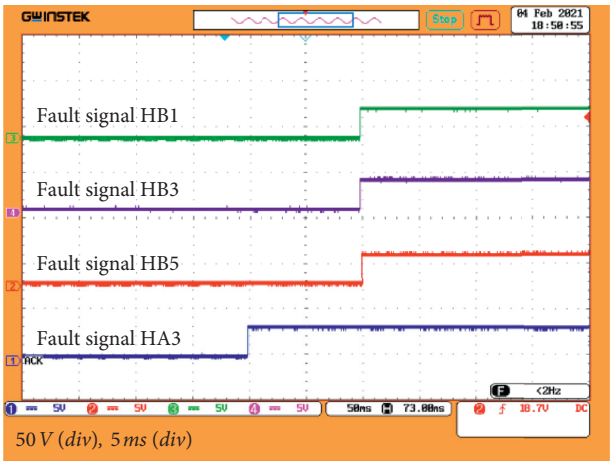


FIGURE 17: Fault signals on cells.

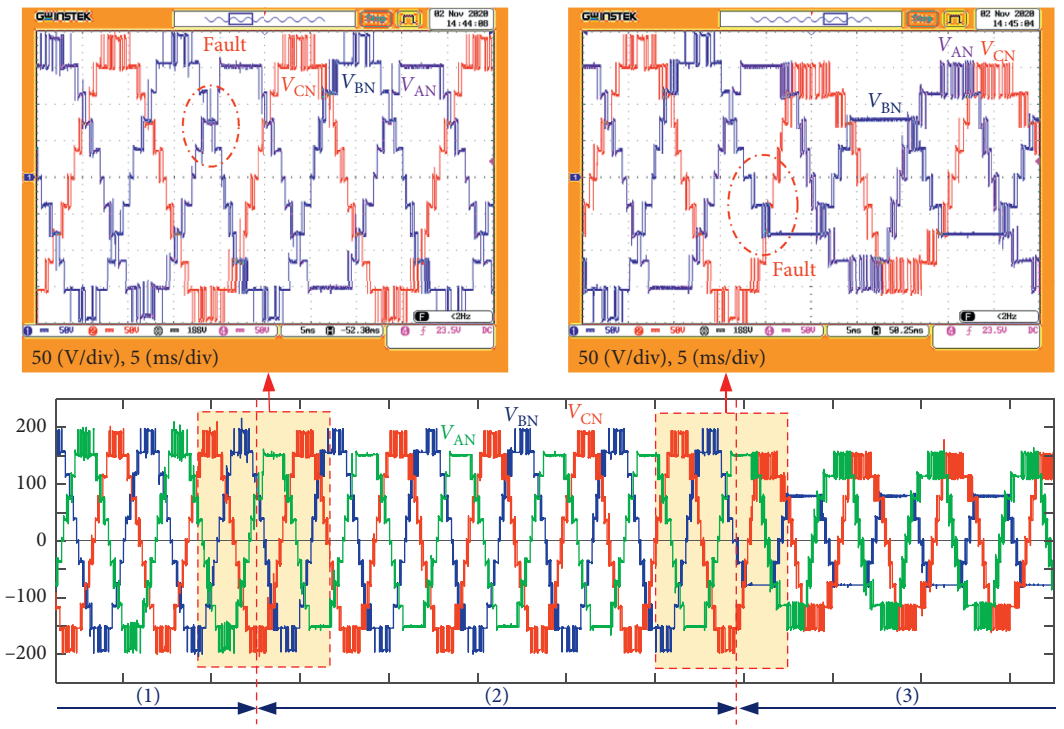


Figure 18: Inverter phase's voltage.

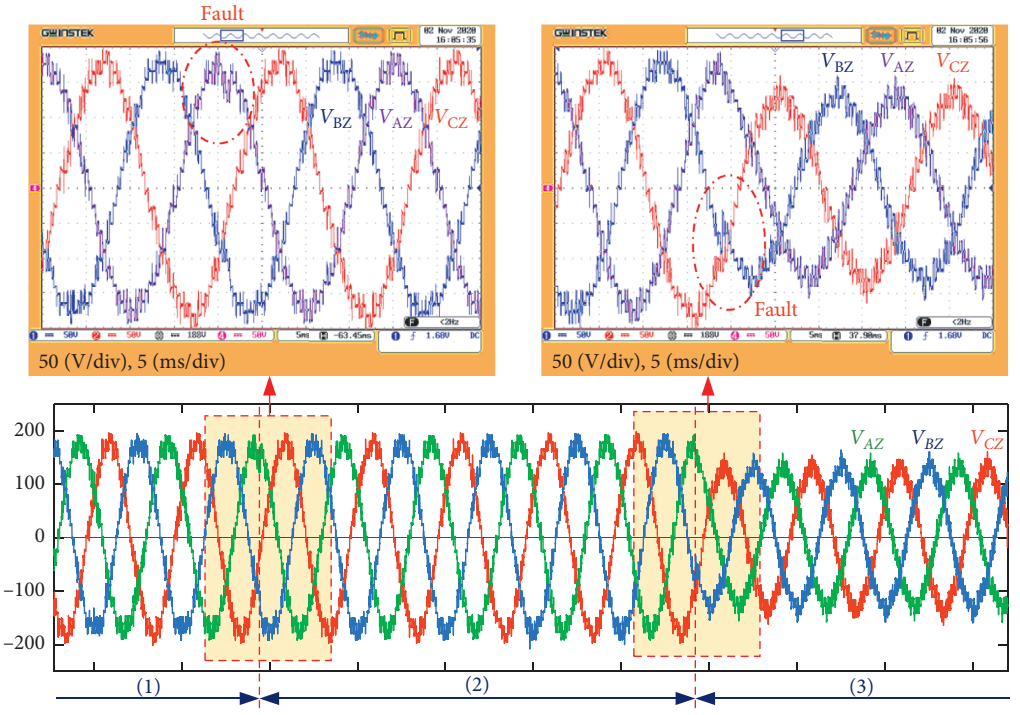


Figure 19: Inverter load's voltage.

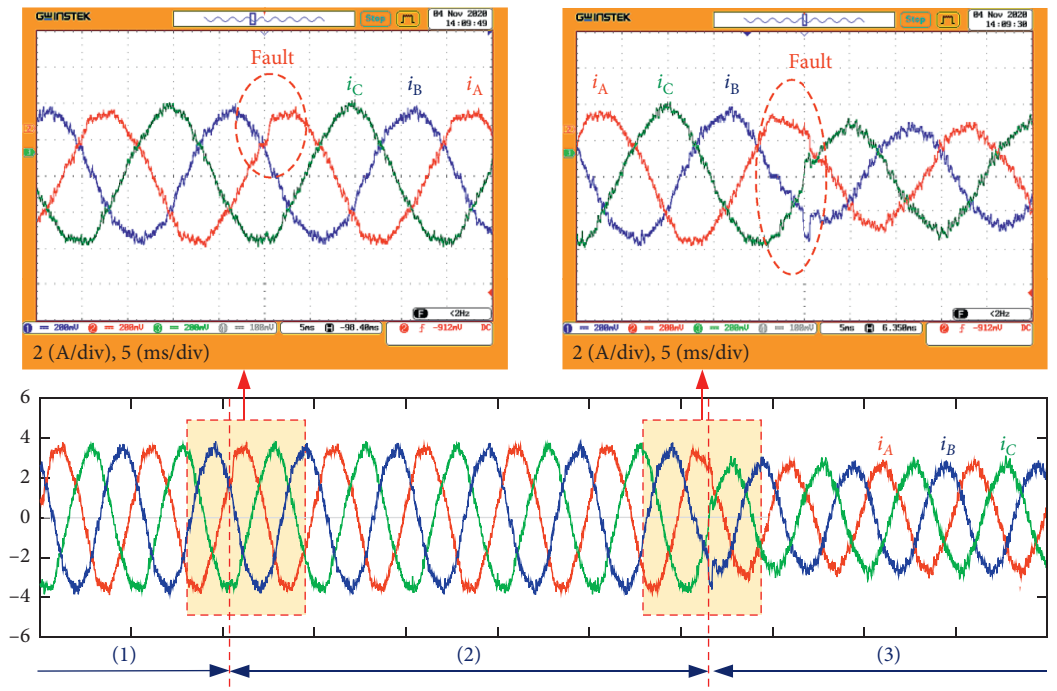


Figure 20: Inverter current.

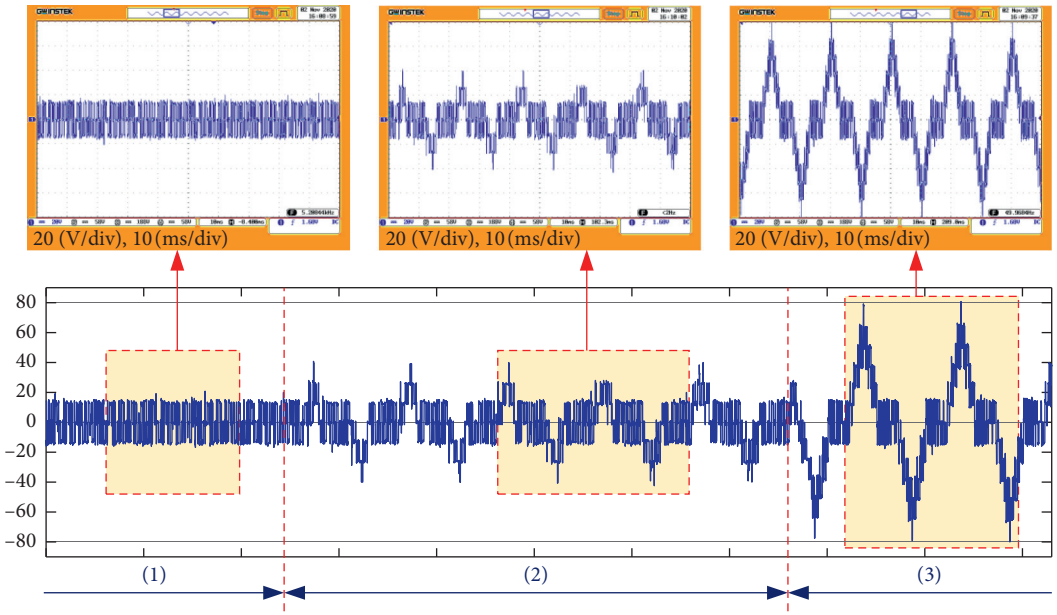


Figure 21: CMV.

5. Conclusion

In this paper, error detection method and improved SVM algorithm are proposed to increase the reliability of multilevel inverter in case of open-circuit problems. The algorithm works precisely with 1 ms detection time, comes with simple measurement circuit, is easy to program, and can detect multiple faulty locations at the same time. SVM algorithm in case of faulty situations is generalized and can be applied to multilevel inverter with any number of levels.

The algorithm ensures the balance of voltage and current and reduces the output voltage drop to minimum when there is an error, and the CMV is minimized.

Data Availability

This publication is supported by multiple datasets, which are available at locations cited in the References section.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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