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Research Article

Novel Switched Configuration-Based Multilevel Inverter Topology for Industrial Applications

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Multilevel inverters proved its capabilities nowadays operating in the symmetrical and asymmetrical source of voltages to bring output voltage nearly to a sinusoid. Several variations in topological strategies put forth better output quality with lesser harmonic distortion. However, it suffers from several issues predominantly such as more number of devices, higher blocking voltage, and power loss for higher voltage levels. This paper forays a fresh topology on switched configuration multilevel inverters with optimum dc sources, switches, voltage level, and filter requirements. The proposed topology has the flexibility to extend for higher voltage levels with make use of less switches. The proposed structure has been simulated in MATLAB/Simulink and validated the results in a laboratory setup.

1. Introduction

Multilevel inverters (MLI) have been fostered up to 230 kV voltage with applications such as industrial drives, static compensators, and renewable energy applications [1–4]. Multilevel inverters have been devised to synthesize stepped waveform through several isolated dc sources or dc link capacitors and accord minimum harmonic distortion, lower voltage stress across the devices compared with overall inverting operating voltage and lower electromagnetic interference [5]. These advantages explore multilevel inverters to put forth for lower power applications over high-voltage medium-power applications [6, 7]. Precisely, multilevel inverters acknowledge good harmonic profile only when a number of voltage levels tends to increase utilizing more number of IGBT or MOSFET devices and voltage sources which raises the cost of the entire device [8, 9]. The fundamental topology in the multilevel inverter family is cascaded-type topologies which include several isolated dc sources with the arrangement of switching devices to bring multilevel structure voltage waveform without the issue of d-link voltage balancing [10]. Several researches have been carried out with the goal of developing innovative topologies with fewer components and dc voltage sources. Several asymmetrical inverter structures with unequal source voltage ratios and modulation strategies comprising carrier-based pulse width modulation (PWM), space vector PWM (SVPWM), selective harmonic elimination PWM (SHE-PWM) in the field of multilevel power converters have been reported [11–14].

A new topology for producing multilevel voltage waveforms has been reported in the literature, using isolated symmetric input DC sources coupled in reverse polarities in a laddered structure through a series of power semiconductor devices. The higher voltage levels can be reached by extending the inverter by simply adding a voltage source with a preceding voltage source in the reverse direction with two series switches. If one of the outer layer switches is under fault, the topology is inefficient to produce alternating multilevel waveform [15, 16]. A single-phase cascaded-type multilevel inverter topology includes two five-level transistor-clamped multilevel inverters in series connection to offer nine-level output voltage has been presented. The system employs an array of split capacitors to synthesize pole

voltage waveform which results in capacitor balancing issues [17]. A new topology has been reported for the concatenation of several sub-MLI blocks in the H six structure to offer a stepped voltage waveform [18] that slightly varied in a structure presented in [15, 16]. A new topology using half bridge cells and a level doubling network (LDN) to double the output voltage levels has been conceived in [19]. A new inverter topology using cascaded H Bridge cells having asymmetric binary voltage ratio is devised to eliminate the need for isolated dc sources by dc capacitors adapting only one DC source for the whole structure. The magnitude of the voltage source has been selected as the highest value while the remaining DC capacitors magnitudes are chosen as half of the preceding DC capacitor voltages and remain unbalanced dc link voltages with the same number of switching devices as used in classical cascaded H Bridge inverter [20]. A topology based on dual voltage sources with an H Bridge inverter has been introduced using several switching devices and diodes. The topology suffers from the requirement of more number of switching devices and diodes for the increased number of voltage levels [21].

A switched capacitor module is suggested using a single dc source and two capacitors to generate 9 levels with a voltage boosting gain of two and also to ensure total device blocking voltage is limited to dc source voltage [22]. In [23], a new MLI topology connects the level generation module and polarity reversal unit to achieve any required level depending on the configuration of the level generation units to be added with the developed topology. A new cascaded MLI consists of high-frequency magnetic link (HFML) and full bridge rectifiers in addition to compact cascaded MLI has been reported in the literature. To obtain higher voltage levels in the output voltage, more cascaded cells have been added, which is a key weakness of this proposed topology for low-power applications [24]. Two new MLI topologies have been suggested to achieve reduced components. However, the topology is incapable of generating a voltage ratio with a binary voltage ratio of voltage source magnitudes [25]. An improved symmetrical four-level submodule and polarity reversal inverter is used to generate multiple voltage levels has been presented in [26]. The topology losses its modularity to produce succeeding voltage levels in the output voltage. A new topology has been formulated to reduce switches, isolated dc voltage sources without losing modularity for an increase in output voltage levels [27]. A new cascaded MLI structure to offer minimum switches has been reported in [28], but this topology requires switches with high blocking voltage capability for achieving an increased number of voltage levels.

The detailed literature review in the field of multilevel inverter topologies brings an avenue to draw out new multilevel inverter structure with a view of reduced component counts. The developed work has been oriented to bring new cascaded-type multilevel inverter topology overwhelming the drawbacks in classical cascaded type.

2. Detail Explanation of Proposed Multilevel Inverter Topology

The generalized circuit for the proposed topology is represented in Figure 1 that uses voltage sources ($V_1 - V_n$) and the switches ($S_1 - S_{n+5}$) to synthesize multilevel dc link voltage and an H Bridge inverter with switches ($S_a - S_d$) for polarity reversal in the proposed topology.

The diode (D_1) in the proposed structure helps to avoid interlooping problems between the voltage sources V_3 and ($V_2 - V_n$). The voltage sources ($V_1 - V_3$) act as permanent voltage source module, and the voltage sources ($V_4 - V_n$) act as add-on module to synthesize higher voltage levels. With the voltage sources ($V_1 - V_3$), the proposed topology produces 7 level in the output side with an equal value of voltage sources. To understand the modes of operation, the generalized topology is configured to generate nine-level output as depicted in Figure 2. Figure 3 forges to synthesize level 1 (magnitude of V_1) in the output voltage by switching the devices in a sequence of (S_1, S_3, S_4, S_5, S_a, and S_b) and (S_1, S_3, S_4, S_5, S_c, and S_d), respectively while the switches (S_1, S_9, S_4, S_6, S_a, and S_b) and (S_1, S_9, S_4, S_6, S_c, and S_d) in Figure 4 are switched on to produce level 4 (magnitudes of $(V_1 + V_2 + V_3 + V_4)$) in the output voltage, respectively. The proposed topology is capable of generating more voltage levels by properly choosing the magnitude of voltage sources as asymmetrical values. Table 1 tabulates the switching states for different modes of operation. Switches S_7 and S_8 are utilized for the inductive load (RL-Load) to freewheel the current.

The relationship between the voltage sources and switches in the proposed topology is $(n + 9)$, where "n" is the number of voltage sources and is greater than 3, while the number of voltage levels with given "n" is $((2 \times n) + 1)$. The blocking voltage across each switch will be

$$\begin{aligned} &V_{S2} = V_{S5} = V_{S6} = V_{dc}, \\ &V_{S1} = V_{S3} = V_{S4} = V_{S7} = V_{S8} = V_{S9} = \left(2 \times V_{dc}\right), \\ &V_{Sa} = V_{Sb} = V_{Sc} = V_{Sd} = \left(4 \times V_{dc}\right). \end{aligned} \tag{1}$$

The primary goal of formulating any innovative topology is to generate all voltage levels which depend on the selection of the magnitude of voltage sources. Therefore, in order to generate all desired voltage levels, seven techniques have been conceived to find out the voltage sources' magnitude.

Table 2 tabulates the design equations suitable for the proposed topology relating to the magnitude of voltage sources and voltage levels to be acquired using these equations. To evaluate the methods tabulated in Table 2, a submultilevel topology with four dc voltage sources is considered in this study, and the structure is represented in Figure 5. It is mandatory to compare the proposed methods among them and identify the best one suited to offer higher voltage levels with least switching devices, voltage sources, blocking voltages, and gate drivers for the developed topology. The number of switching devices employing the proposed submultilevel inverter modules is compared in Figure 6. The switching devices increase as the number of

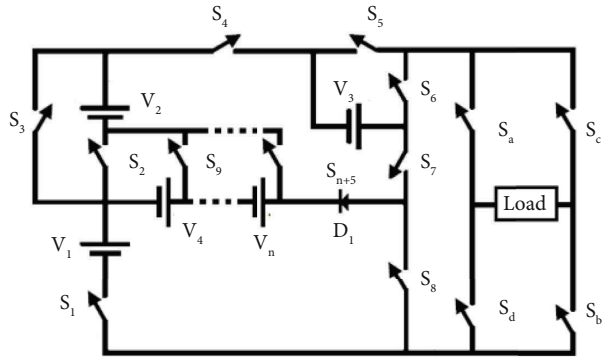


Figure 1: Generalized structure of proposed multilevel inverter topology.

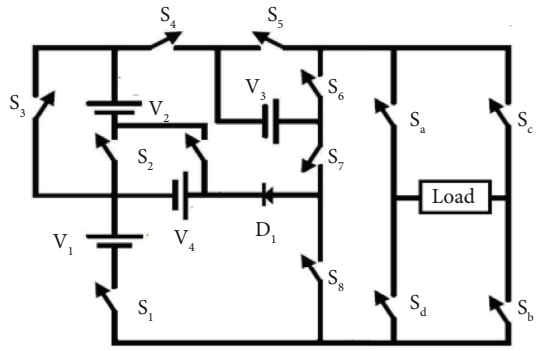


Figure 2: Proposed nine-level inverter.

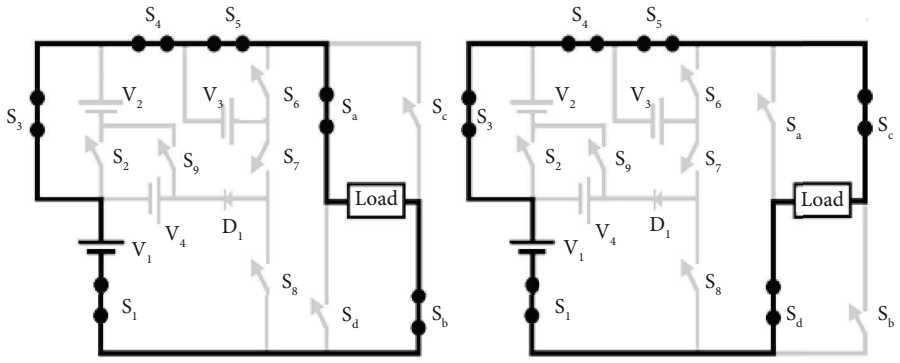


Figure 3: Operating mode: $\pm V_1$.

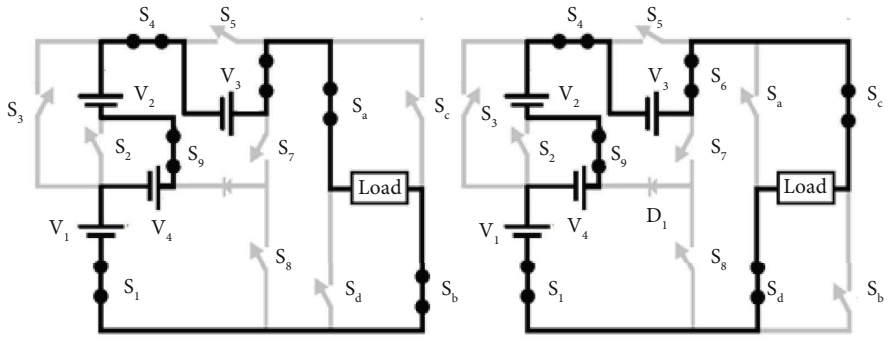


Figure 4: Operating mode: $\pm (V_1 + V_2 + V_3 + V_4)$.

Table 1: Switching states for different operating modes.

Operating modes	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_a	S_b	S_c	S_d
$+V_1$	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
$-V_1$	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
$+(V_1+V_2)$	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
$-(V_1+V_2)$	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
$+(V_1+V_2+V_3)$	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
$-(V_1+V_2+V_3)$	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
$+(V_1+V_2+V_3+V_4)$	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF
$-(V_1+V_2+V_3+V_4)$	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON

Table 2: Magnitude value of voltage sources for different methods.

Methods	Magnitude value of voltage sources	Number of voltage levels	Maximum output voltages	Total blocking voltages
I	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=V_{dc};\quad (j=1,2,\ldots,n)$	$((8\times n)+1)$	$(4\times n)\times V_{dc}$	$(32\times n)\times V_{dc}$
II	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=2V_{dc};\ (j=1,2,\ldots,n)$	$((16\times n)-7)$	$((8\times n)-4)\times V_{dc}$	$((64\times n)-32)\ \times V_{dc}$
III	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=2^{j-1}V_{dc};\ (j=2,\ldots,n)$	$8\times(\sum_{i=1}^{n}2^{i-1})+1$	$4\times(\sum_{i=1}^{n}2^{i-1})\times V_{dc}$	$32\times(\sum_{i=1}^{n}2^{i-1})\times V_{dc}$
IV	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=3V_{dc};\ (j=1,2,\ldots,n)$	$((24\times n)-15)$	$((12\times n)-8)\times V_{dc}$	$((96\times n)-64)\times V_{dc}$
V	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=3^{j-1}V_{dc};\ (j=2,\ldots,n)$	$8\times(\sum_{i=1}^{n}3^{i-1})+1$	$4\times(\sum_{i=1}^{n}3^{i-1})\times V_{dc}$	$32\times(\sum_{i=1}^{n}3^{i-1})\times V_{dc}$
VI	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=4V_{dc};\ (j=1,2,\ldots,n)$	$((32\times n)-23)$	$((16\times n)-12)\times V_{dc}$	$((128\times n)-96)\times V_{dc}$
VII	$V_{1,1}=V_{1,2}=V_{1,3}=V_{1,4}=V_{dc}$ $V_{j,1}=V_{j,2}=V_{j,3}=V_{j,4}=4^{j-1}V_{dc};\ (j=2,\ldots,n)$	$8\times(\sum_{i=1}^{n}4^{i-1})+1$	$4\times(\sum_{i=1}^{n}4^{i-1})\times V_{dc}$	$32\times(\sum_{i=1}^{n}4^{i-1})\times V_{dc}$

sub-MLI modules increases. Figure 7 shows the variation of voltage levels with proposed inverter modules using proposed voltage magnitude determination methods. It is confirmed that higher voltage is achieved in the sixth and seventh proposed methods with a minimum number of switching devices.

Figures 8 and 9 elaborate the maximum output voltage and total blocking voltage required by the proposed topology for different proposed methods, respectively. From Figures 8 and 9, the seventh proposed method needs a lower number of inverter modules to generate particular levels with reduced blocking voltage. Moreover, the first proposed algorithm requires more numbers of dc voltage sources as it is common for any topology. It is observed that the first proposed method has lower voltage amplitudes of the used sources, and the seventh proposed method needs a minimum number of switching devices and high combinations magnitudes of the voltage sources. However, its performance is better than the other proposed methods except the first one. Therefore, it is concluded that the seventh method forays a better performance among all the proposed methods.

Table 3 elaborates the mathematical relations to achieve switching devices, dc sources, and switching devices in the current conduction path for symmetrical configurations.

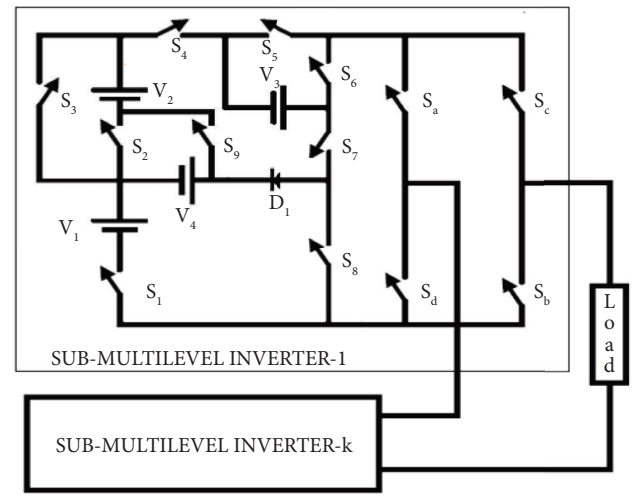


Figure 5: Submultilevel inverter topology.

Figures 10–12 represent a plot between number of voltage levels and dc sources, switching devices, and switches in the current conduction path. In Figure 10, the proposed topology requires less number of dc sources to produce higher voltage levels. From Figures 11 and 12, the proposed

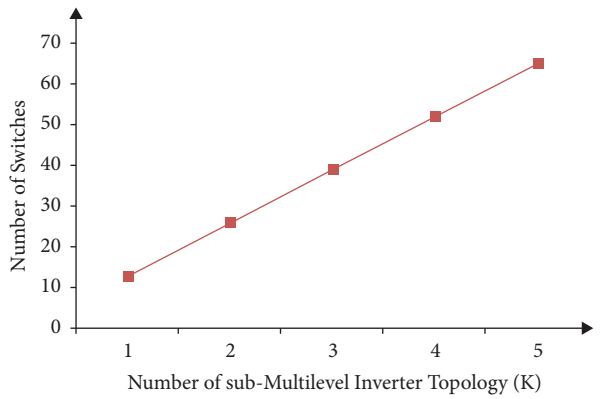


Figure 6: Variation of switching devices with proposed sub-multilevel inverters.

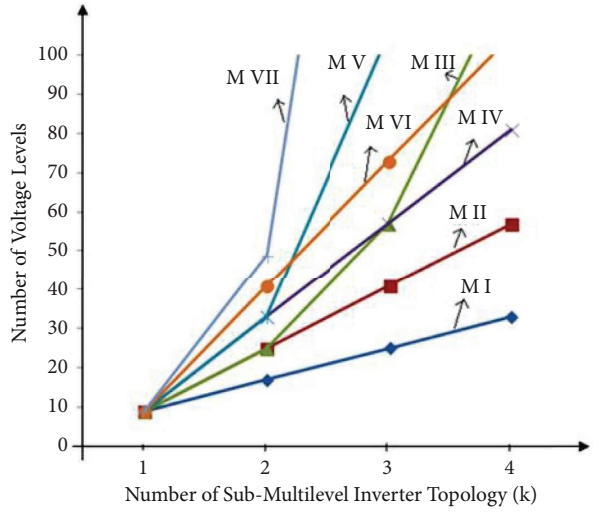


Figure 7: Voltage level variation with proposed submultilevel inverters.

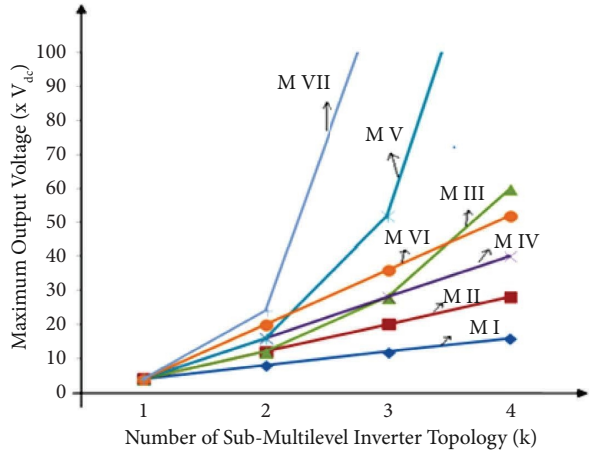


Figure 8: Variation of maximum output voltage with proposed submultilevel inverters.

topology requires a marginal increase in switching devices compared with R [32] and the same number of current conducting switches except R [29–31].

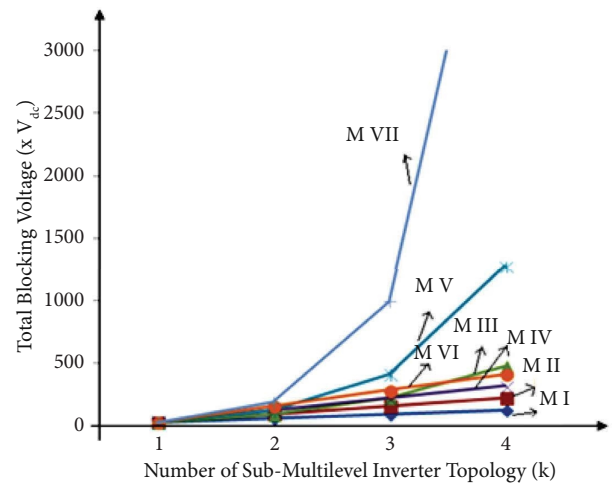


Figure 9: Variation of total blocking voltage with proposed submultilevel inverters.

It is essential to investigate the cost reduction of the component counts in comparison between the proposed and reduced counts topologies in view of producing higher number of voltage levels in symmetrical configuration. The recent component count topologies reported in the literature [21, 33–36] are devised by arranging the dc sources in a suitable way to reduce the number of components for producing the desired voltage levels in output. In this perspective, an analysis has been taken to consider two different voltage levels 45 and 47 to showcase the drastic reduction in the switch count with a fixed number of voltage sources. For 47-level inverter, the topology reported in [33] requires 50 and the topologies in [34, 35] utilize 48, while the proposed topology requires only 32 switching devices. Similarly, for 45-level inverter, the proposed topology requires only 31, and the topologies reported in [21, 36] need 41 and 66 switching devices, respectively. It shows that proposed topology is compact and more economical.

3. Measured Simulation and Experimental Results

The effectiveness and viability of the topology have been simulated with Matlab R2015b, and the same simulation specifications are taken to construct the laboratory prototype for experimental investigations. The topology shown in Figure 1 is reconfigured to produce 9 level in the output voltage, and the input dc voltage source magnitudes are considered as 75 V each with the specifications 2 kHz switching frequency, RL load of resistance 150 Ω, and inductance 100 mH, respectively. Figure 13 portrays the gating pulses for the switches (S_1 to S_9) in the switched configured stage of the proposed topology to produce 9 levels in the output voltage waveform. Figures 14 and 15 demonstrate nine-level output voltage of proposed inverter topology and inductive load current waveforms, respectively. The THD spectrum with THD of 12.67% is displayed in Figure 16.

Table 3: Mathematical relations to achieve switching devices and dc sources for "m" levels.

Topology	Minimum no. of voltage levels	No. of switches	No. of DC sources	No. of freewheeling diodes	No. of switches in the current conduction path
R [29]	5	$(m+1)$	$(m+1)/2$	—	$(m+1)/2$
R [30]	5	$(m+3)$	$(m-1)/2$	—	$(m+3)/2$
R [31]	5	$(m+1)$	$(m+1)/2$	—	$(m+1)/2$
R [32]	5	$(m+11)/2$	$(m-1)/2$	$(m-5)/2$	$(m+3)/2$
Proposed	7	$(m+17)/2$	$(m-1)/2$	—	$(m+3)/2$

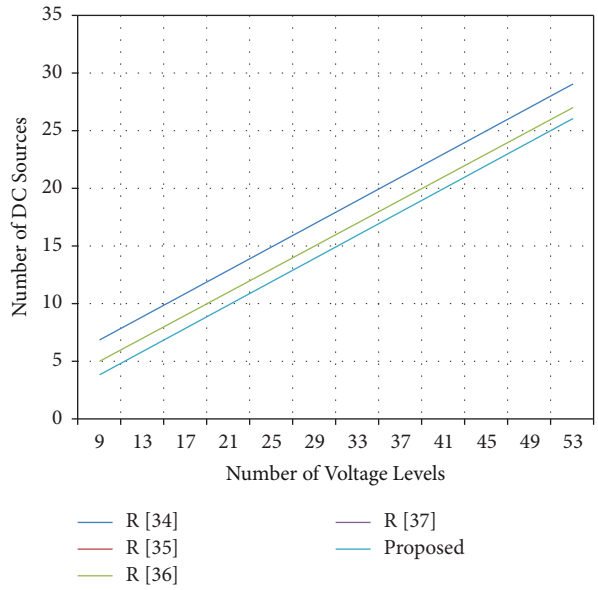


Figure 10: No. of voltage levels vs no. of DC sources.

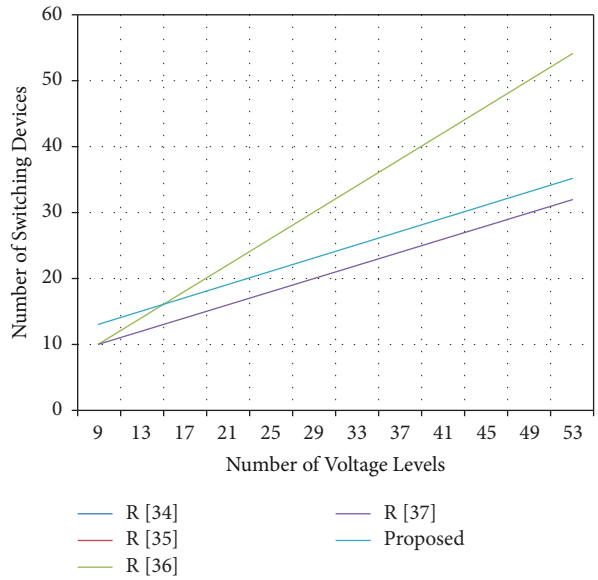


Figure 11: No. of voltage levels vs no. of switching devices.

The pictorial representation of the experimental prototype built in the laboratory has been depicted in Figure 17 to showcase the practical reliability of the proposed topology. The gating pulse generation avails LUTs to synthesize the desired pulse train using the Xilinx Spartan 3E FPGA controller as portrayed in Figure 18. Gating pulses for the switches (S_1 to S_8) in the switched configured stage of the proposed topology to produce 9 level in the output voltage waveform are shown in Figure 19.

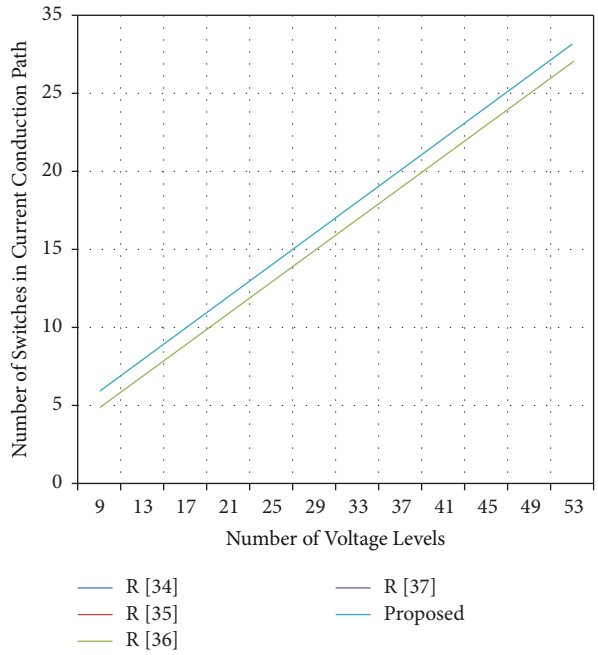


Figure 12: No. of voltage levels vs no. of switches in current conduction path.

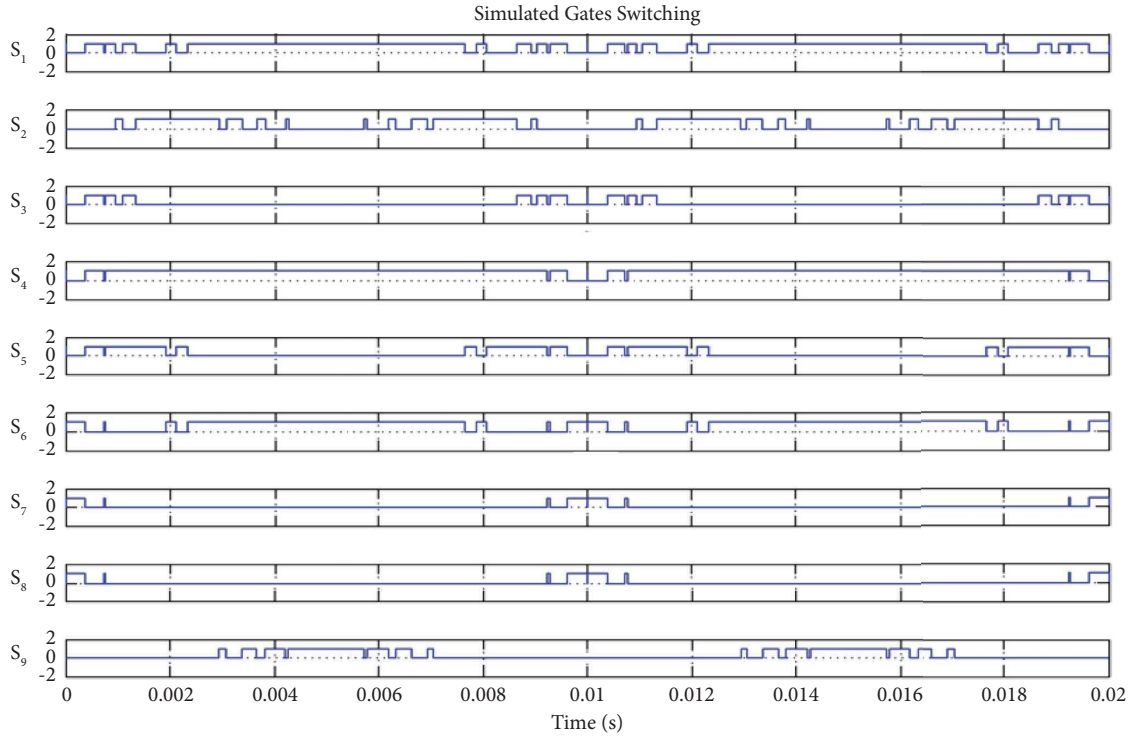


Figure 13: Gating pulse for 9-level inverter.

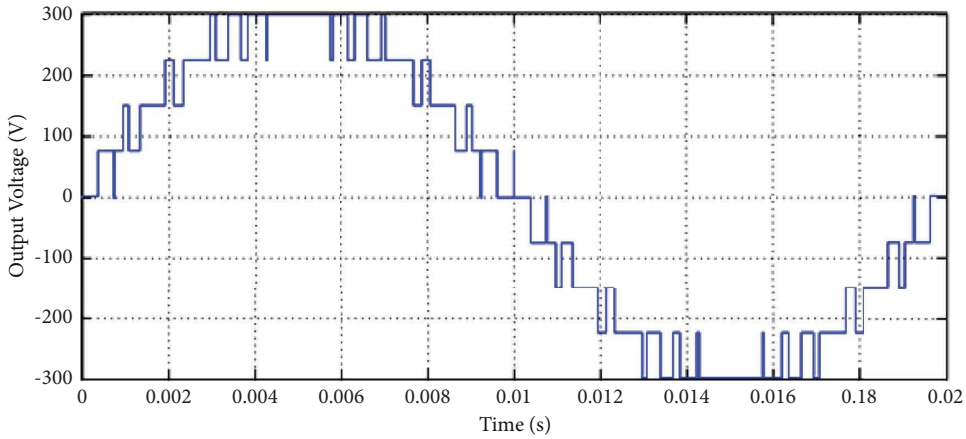


Figure 14: Output voltage of proposed 9-level inverter for *R-L* load.

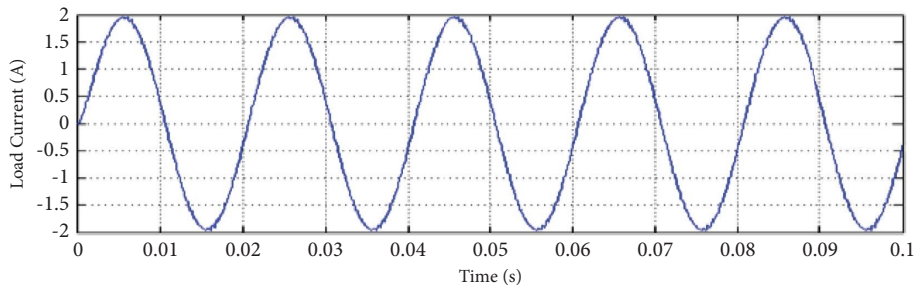


Figure 15: Inductive load current waveform.

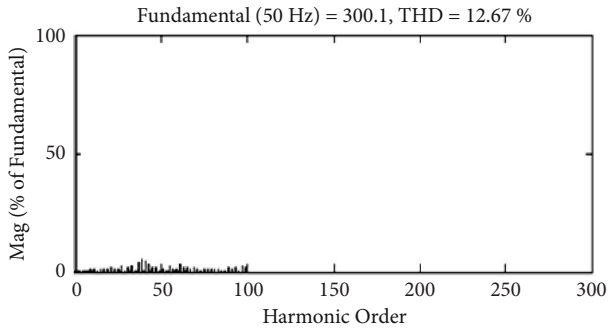


Figure 16: Voltage THD waveform.

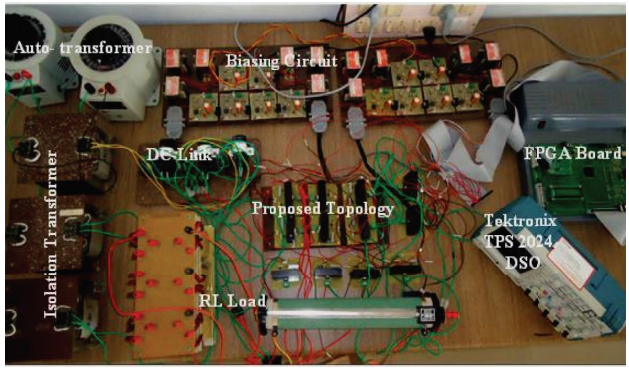


Figure 17: Experimental setup of proposed inverter topology.

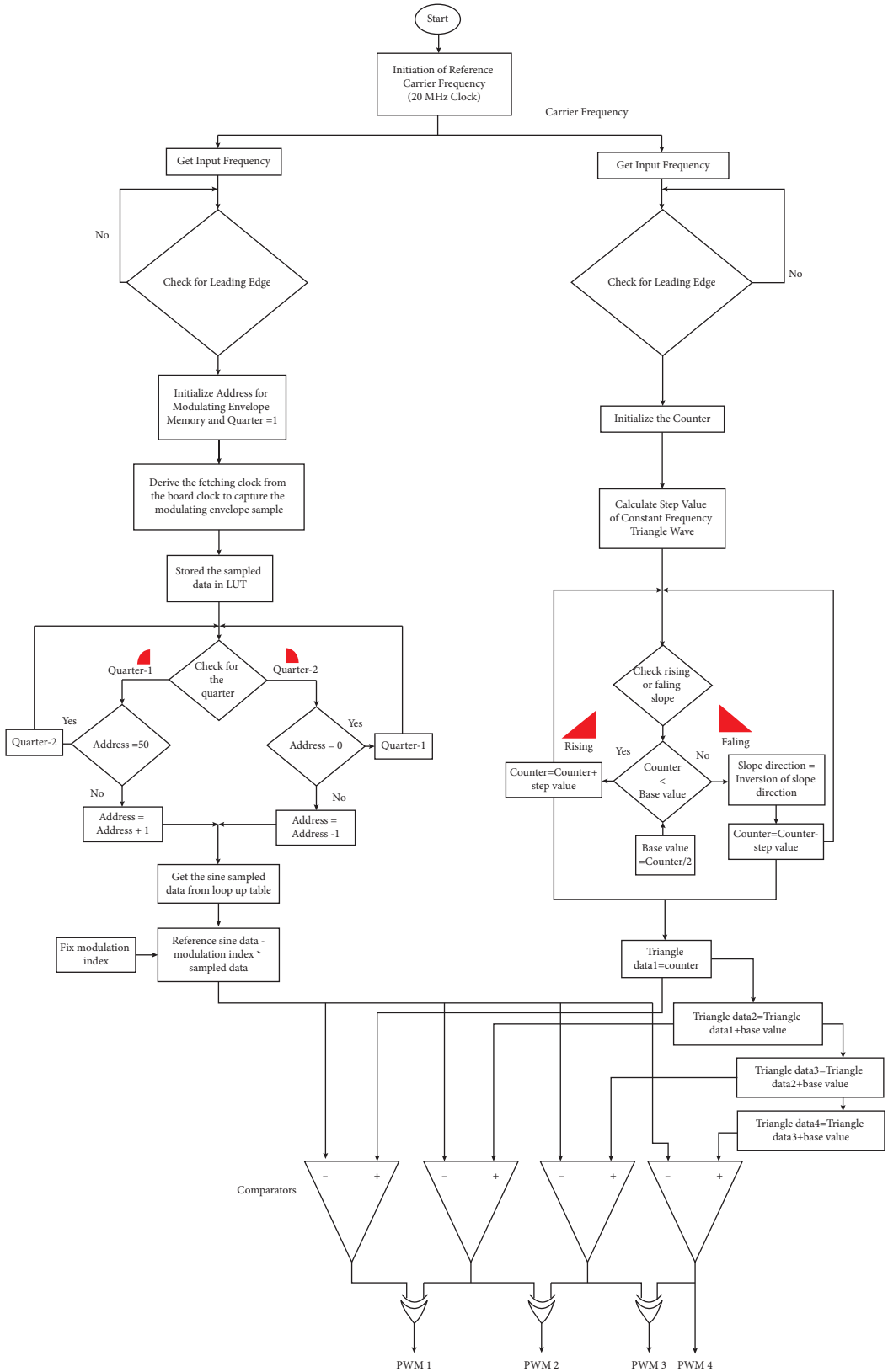
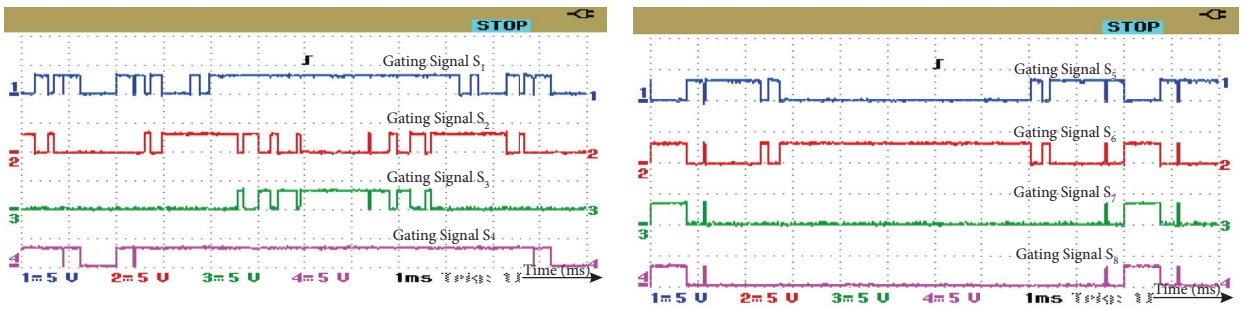


Figure 18: Experimental flow chart for FPGA pulse generation.



(a) (b)

Figure 19: Gating pulses for proposed nine-level inverter switches (a) S_1 to S_4 and (b) S_5 to S_8.

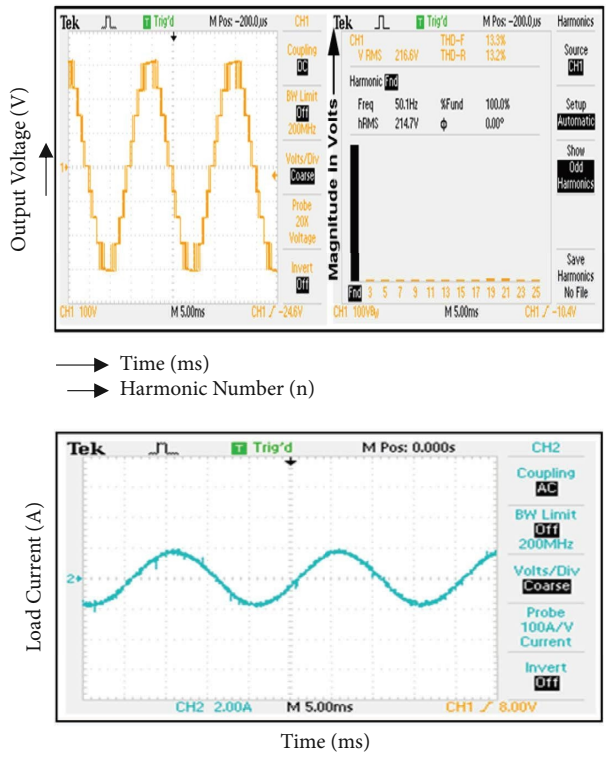


Figure 20: Output voltage waveform and voltage spectrum.

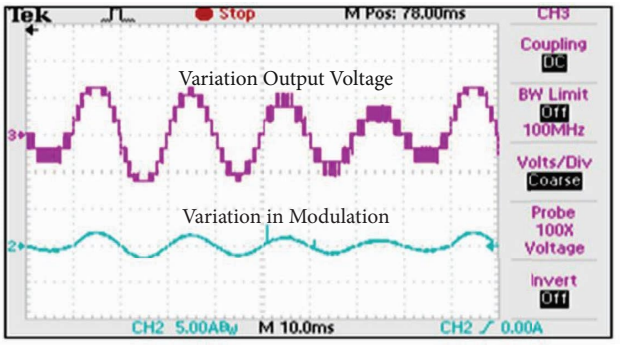


Figure 21: Inductive load current waveform.

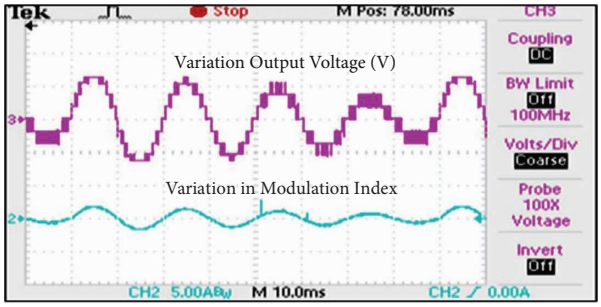


FIGURE 22: Variation of output voltage with change in modulation index.

The nine-level output voltage waveform of improved quality in near sinusoidal shape along with better harmonic spectrum has been depicted in Figure 20. From the harmonic spectrum, it is observed that the total harmonic distortion (THD) of the output voltage waveform is near to the specified acceptable limits, and it results in the minimum requirement of the output filter size. Figure 21 depicts the experimental inductive load current waveform. Figure 22 represents the output voltage variation with a change in amplitude modulation index. It is inferred that the developed topology responds well with change in voltage variation. The experimental results accorded with simulation results.

4. Conclusion

In comparison to traditional MLI topologies, the proposed topology is formulated with a view of figuring out reduced components to produce a higher number of voltage levels. The operating modes for generating nine levels have been presented with the flow path. The proposed MLI topology has been described in depth, as well as methods for determining the magnitude of voltage sources. The proposed topology requires only one switching device to add a single voltage source with the parent module and thus making the reduced number of switches in the current conduction path thereby making less power loss. The simulation and experimental results showcase the merits of the proposed topology for the practical applications like renewable and drive sectors.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] B. P. Reddy and S. Keerthipati, "A multilevel inverter configuration for an open-end-winding Pole-Phase-Modulated-Multiphase induction motor drive using dual inverter principle," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 3035–3044, 2018.

[2] P. Nijhawan, R. S. Bhatia, and D. K. Jain, "Improved performance of multilevel inverter-based distribution static synchronous compensator with induction furnace load," *IET Power Electronics*, vol. 6, no. 9, pp. 1939–1947, 2013.

[3] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "A STATCOM based on a three-phase, triple inverter modular topology for multilevel operation," *IEEE Transactions on Power Delivery*, vol. 34, no. 5, pp. 1988–1997, 2019.

[4] P. Anbarasan, V. Krishnakumar, S. Ramkumar, and S. Venkatesan, "A new three-phase multilevel DC-link inverter topology with reduced switch count for photovoltaic applications," *Circuit World*, vol. 47, no. 2, Article ID 173183, 2020.

[5] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," *IEEE Transactions on Industry Applications*, vol. 19, no. 6, pp. 1057–1069, 1983.

[6] P. Anbarasan, S. Ramkumar, and S. Thamizharasan, "A new three phase reduced switch multilevel dc-link inverter for medium voltage application," in *Proceedings of the IEEE Electrical Computer and Communication Technologies (IEEE ICECCT)*, pp. 1–4, Coimbatore, India, March 2015.

[7] H. Mhiesan, J. Umuhoza, K. Mordi, C. Farnell, and H. A. Mantooth, "Evaluation of 1.2 kV SiC MOSFETs in multilevel cascaded H-bridge three-phase inverter for medium-voltage grid applications," *Chinese Journal of Electrical Engineering*, vol. 5, no. 2, pp. 1–13, 2019.

[8] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[9] G. J. Su, D. Multilevel, and C. L. inverter, "Multilevel DC-link inverter," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 848–854, 2005.

[10] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2197–2206, 2010.

[11] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867, 2002.

[12] A. K. Gupta and A. M. Khambadkone, "A Space vector PWM scheme for multilevel inverters based on two-level Space vector PWM," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1631–1639, 2006.

[13] P. Sochor and H. Akagi, "Theoretical and experimental comparison between phase-shifted PWM and level-shifted PWM in a modular multilevel SDBC inverter for utility-scale photovoltaic applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4695–4707, 2017.

[14] S. K. Sahoo and T. Bhattacharya, "Phase-shifted carrier-based synchronized sinusoidal PWM techniques for a cascaded H-bridge multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 513–524, 2018.

[15] K. K. Gupta and S. Jain, "Multilevel inverter topology based on series connected switched sources," *IET Power Electronics*, vol. 6, no. 1, pp. 164–174, 2013.

[16] S. Thamizharasan, J. Baskaran, S. Ramkumar, and S. Jeevananthan, "Cross-switched multilevel inverter using auxiliary reverse-connected voltage sources," *IET Power Electronics*, vol. 7, no. 6, pp. 1519–1526, 2014.

[17] C. I. Odeh and D. B. N. Nnadi, "Single-phase 9-level hybridised cascaded multilevel inverter," *IET Power Electronics*, vol. 6, no. 3, pp. 468–477, 2013.

[18] M. R. Banaei, M. R. Jannati Oskuee, and H. Khounjahan, "Reconfiguration of semi-cascaded multilevel inverter to

improve systems performance parameters," *IET Power Electronics*, vol. 7, no. 5, pp. 1106–1112, 2014.

[19] S. K. Chattopadhyay and C. Chakraborty, "A new multilevel inverter topology with self-balancing level doubling network," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4622–4631, 2014.

[20] R. Vasu, S. K. Chattopadhyay, and C. Chakraborty, "Asymmetric cascaded H-bridge multilevel inverter with single DC source per phase," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5398–5409, 2020.

[21] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6712–6724, 2014.

[22] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8204–8207, 2018.

[23] A. Hota, S. Jain, and V. Agarwal, "An optimized three-phase multilevel inverter topology with separate level and phase sequence generation part," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7414–7418, 2017.

[24] M. M. Hasan, A. Abu-Siada, S. M. Islam, and M. S. A. Dahidah, "A new cascaded multilevel inverter topology with galvanic isolation," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3463–3472, 2018.

[25] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, Article ID 58584, 2019.

[26] S. S. Lee, M. Sidorov, C. S. Lim, N. R. N. Idris, and Y. E. Heng, "Hybrid cascaded multilevel inverter (HCMLI) with improved symmetrical 4-level submodule," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 932–935, 2018.

[27] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, Article ID 24498, 2019.

[28] E. Babaei and S. Laali, "Optimum structures of proposed new cascaded multilevel inverter with reduced number of components," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 6887–6895, 2015.

[29] B. Mahato, S. Majumdar, and K. C. Jana, "Reduction in controlled power switches for a single-phase novel multilevel inverter," *International Journal of Electronics*, vol. 106, no. 8, pp. 1200–1215, 2019.

[30] B. Mahato, S. Mittal, and P. K. Nayak, "N-Level Cascade Multilevel Converter with optimum number of switches," in *Proceedings of the International Conference on Recent Trends in Electrical, Control and Communication (RTECC)*, pp. 228–233, Malaysia, March 2018.

[31] B. Mahato, S. Majumdar, and K. C. Jana, "Reduction of power electronic devices in a single-phase generalized multilevel inverter," *Journal of Circuits, Systems, and Computers*, vol. 29, no. 06, Article ID 2050093, 2020.

[32] B. Mahato, S. Majumdar, and K. C. Jana, "A new and generalized MLI with overall lesser power electronic devices," *Journal of Circuits, Systems, and Computers*, vol. 29, no. 04, Article ID 2050058, 2020.

[33] V. Anand and V. Singh, "Compact symmetrical and asymmetrical multilevel inverter with reduced switches," *International Transactions on Electrical Energy Systems*, vol. 30, no. 8, Article ID 12458, 2020.

[34] S. Edwin Jose and S. Titus, "A level dependent source concoction multilevel inverter topology with a reduced number of power switches," *Journal of Power Electronics*, vol. 16, no. 4, pp. 1316–1323, 2016.

[35] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3269–3278, 2014.

[36] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 922–929, 2015.