Research Article

Novel Switched Configuration-Based Multilevel Inverter Topology for Industrial Applications

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Multilevel inverters proved its capabilities nowadays operating in the symmetrical and asymmetrical source of voltages to bring output voltage nearly to a sinusoid. Several variations in topological strategies put forth better output quality with lesser harmonic distortion. However, it suffers from several issues predominantly such as more number of devices, higher blocking voltage, and power loss for higher voltage levels. This paper forays a fresh topology on switched configuration multilevel inverters with optimum dc sources, switches, voltage level, and filter requirements. The proposed topology has the flexibility to extend for higher voltage levels with make use of less switches. The proposed structure has been simulated in MATLAB/Simulink and validated the results in a laboratory setup.

1. Introduction

Multilevel inverters (MLI) have been fostered up to 230kV voltage with applications such as industrial drives, static compensators, and renewable energy applications [1–4]. Multilevel inverters have been devised to synthesize stepped waveform through several isolated dc sources or dc link capacitors and accord minimum harmonic distortion, lower voltage stress across the devices compared with overall inverting operating voltage and lower electromagnetic interference [5]. These advantages explore multilevel inverters to put forth for lower power applications over high-voltage medium-power applications [6, 7]. Precisely, multilevel inverters acknowledge good harmonic profile only when a number of voltage levels tends to increase utilizing more number of IGBT or MOSFET devices and voltage sources which raises the cost of the entire device [8, 9]. The fundamental topology in the multilevel inverter family is cascaded-type topologies which include several isolated dc sources with the arrangement of switching devices to bring multilevel structure voltage waveform without the issue of d-link voltage balancing [10]. Several researches have been carried out with the goal of developing innovative topologies with fewer components and dc voltage sources. Several asymmetrical inverter structures with unequal source voltage ratios and modulation strategies comprising carrier-based pulse width modulation (PWM), space vector PWM (SVPWM), selective harmonic elimination PWM (SHE-PWM) in the field of multilevel power converters have been reported [11–14].

A new topology for producing multilevel voltage waveforms has been reported in the literature, using isolated symmetric input DC sources coupled in reverse polarities in a laddered structure through a series of power semiconductor devices. The higher voltage levels can be reached by extending the inverter by simply adding a voltage source with a preceding voltage source in the reverse direction with two series switches. If one of the outer layer switches is under fault, the topology is inefficient to produce alternating multilevel waveform [15, 16]. A single-phase cascaded-type multilevel inverter topology includes two five-level transistor-clamped multilevel inverters in series connection to offer nine-level output voltage has been presented. The system employs an array of split capacitors to synthesize pole
voltage waveform which results in capacitor balancing issues [17]. A new topology has been reported for the concatenation of several sub-MLI blocks in the H six structure to offer a stepped voltage waveform [18] that slightly varied in a structure presented in [15, 16]. A new topology using half bridge cells and a level doubling network (LDN) to double the output voltage levels has been conceived in [19]. A new inverter topology using cascaded H Bridge cells having asymmetric binary voltage ratio is devised to eliminate the need for isolated dc sources by dc capacitors adapting only one DC source for the whole structure. The magnitude of the voltage source has been selected as the highest value while the remaining DC capacitors magnitudes are chosen as half of the preceding DC capacitor voltages and remain unbalanced dc link voltages with the same number of switching devices as used in classical cascaded H Bridge inverter [20]. A topology based on dual voltage sources with an H Bridge inverter has been introduced using several switching devices and diodes. The topology suffers from the requirement of more number of switching devices and diodes for the increased number of voltage levels [21].

A switched capacitor module is suggested using a single dc source and two capacitors to generate 9 levels with a voltage boosting gain of two and also to ensure total device blocking voltage is limited to dc source voltage [22]. In [23], a new MLI topology connects the level generation module and polarity reversal unit to achieve any required level depending on the configuration of the level generation units to be added with the developed topology. A new cascaded MLI consists of high-frequency magnetic link (HFML) and full bridge rectifiers in addition to compact cascaded MLI has been reported in the literature. To obtain higher voltage levels in the output voltage, more cascaded cells have been added, which is a key weakness of this proposed topology for low-power applications [24]. Two new MLI topologies have been suggested to achieve reduced components. However, the topology is incapable of generating a voltage ratio with a binary voltage ratio of voltage source magnitudes [25]. An improved symmetrical four-level submodule and polarity reversal inverter is used to generate multiple voltage levels has been presented in [26]. The topology loses its modularity to produce succeeding voltage levels in the output voltage. A new topology has been formulated to reduce switches, isolated dc voltage sources without losing modularity for an increase in output voltage levels [27]. A new cascaded MLI structure to offer minimum switches has been reported in [28], but this topology requires switches with high blocking voltage capability for achieving an increased number of voltage levels.

The detailed literature review in the field of multilevel inverter topologies brings an avenue to draw out new multilevel inverter structure with a view of reduced component counts. The developed work has been oriented to bring new cascaded-type multilevel inverter topology overwhelming the drawbacks in classical cascaded type.

2. Detail Explanation of Proposed Multilevel Inverter Topology

The generalized circuit for the proposed topology is represented in Figure 1 that uses voltage sources \( V_1 - V_n \) and the switches \( (S_1 - S_{n+5}) \) to synthesize multilevel dc link voltage and an H Bridge inverter with switches \( (S_a - S_d) \) for polarity reversal in the proposed topology.

The diode \( (D_i) \) in the proposed structure helps to avoid interlooping problems between the voltage sources \( V_2 \) and \( (V_2 - V_3) \). The voltage sources \( (V_1 - V_3) \) act as permanent voltage source module, and the voltage sources \( (V_4 - V_n) \) act as an on module to synthesize higher voltage levels. With the voltage sources \( (V_1 - V_3) \), the proposed topology produces 7 level in the output side with an equal value of voltage sources. To understand the modes of operation, the generalized topology is configured to generate nine-level output as depicted in Figure 2. Figure 3 forges to synthesize level 1 (magnitude of \( V_1 \) in the output voltage by switching the devices in a sequence of \( (S_1, S_5, S_4, S_3, S_2, S_1, S_0) \) and \( (S_1, S_4, S_3, S_2, S_1, S_0, S_5) \) respectively while the switches \( (S_1, S_5, S_4, S_3, S_2, S_1, S_0, S_5) \) and \( (S_1, S_4, S_3, S_2, S_1, S_0, S_5) \) in Figure 4 are switched on to produce level 4 (magnitudes of \( (V_1 + V_2 + V_3 + V_4) \)) in the output voltage, respectively. The proposed topology is capable of generating multiple voltage levels by properly choosing the magnitude of voltage sources as asymmetrical values. Table 1 tabulates the switching states for different modes of operation. Switches \( S_a \) and \( S_b \) are utilized for the inductive load (RL-Load) to freewheel the current.

The relationship between the voltage sources and switches in the proposed topology is \((n + 9)\), where “\(n\)” is the number of voltage sources and is greater than 3, while the number of voltage levels with given “\(n\)” is \((2 \times n + 1)\). The blocking voltage across each switch will be

\[
V_{S_2} = V_{S_5} = V_{S_6} = V_{dc}, \quad V_{S_3} = V_{S_4} = V_{S_7} = V_{S_8} = V_{S_9} = (2 \times V_{dc}),
\]

\[
V_{S_a} = V_{S_b} = V_{S_c} = V_{S_d} = (4 \times V_{dc}).
\]

The primary goal of formulating any innovative topology is to generate all voltage levels which depend on the selection of the magnitude of voltage sources. Therefore, in order to generate all desired voltage levels, seven techniques have been conceived to find out the voltage sources’ magnitude.

Table 2 tabulates the design equations suitable for the proposed topology relating to the magnitude of voltage sources and voltage levels to be acquired using these equations. To evaluate the methods tabulated in Table 2, a submultilevel topology with four dc voltage sources is considered in this study, and the structure is represented in Figure 5. It is mandatory to compare the proposed methods among them and identify the best one suited to offer higher voltage levels with least switching devices, voltage sources, blocking voltages, and gate drivers for the developed topology. The number of switching devices employing the proposed submultilevel inverter modules is compared in Figure 6. The switching devices increase as the number of...
Figure 1: Generalized structure of proposed multilevel inverter topology.

Figure 2: Proposed nine-level inverter.

Figure 3: Operating mode: ± $V_1$.

Figure 4: Operating mode: ± ($V_1 + V_2 + V_3 + V_4$).
Table 1: Switching states for different operating modes.

<table>
<thead>
<tr>
<th>Operating modes</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
<th>S9</th>
<th>S10</th>
<th>S11</th>
<th>S12</th>
<th>S13</th>
</tr>
</thead>
<tbody>
<tr>
<td>+V1</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>-V1</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2)</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2)</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2 + V3)</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2 + V3)</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2 + V3)</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>(V1 + V2 + V3)</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Table 2: Magnitude value of voltage sources for different methods.

<table>
<thead>
<tr>
<th>Methods</th>
<th>Magnitude value of voltage sources</th>
<th>Number of voltage levels</th>
<th>Maximum output voltages</th>
<th>Total blocking voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>(8 \times n) + 1</td>
<td>(4 \times n) \times V_{dc}</td>
<td>(32 \times n) \times V_{dc}</td>
</tr>
<tr>
<td>II</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>(16 \times n) - 7</td>
<td>(8 \times n) - 4 \times V_{dc}</td>
<td>(64 \times n) - 32 \times V_{dc}</td>
</tr>
<tr>
<td>III</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>8 \times (\sum_{i=1}^{n} 2^{-i}) + 1</td>
<td>4 \times (\sum_{i=1}^{n} 2^{-i}) \times V_{dc}</td>
<td>32 \times (\sum_{i=1}^{n} 2^{-i}) \times V_{dc}</td>
</tr>
<tr>
<td>IV</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>(24 \times n) - 15</td>
<td>(12 \times n) - 8 \times V_{dc}</td>
<td>(96 \times n) - 64 \times V_{dc}</td>
</tr>
<tr>
<td>V</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>8 \times (\sum_{i=1}^{n} 3^{-i}) + 1</td>
<td>4 \times (\sum_{i=1}^{n} 3^{-i}) \times V_{dc}</td>
<td>32 \times (\sum_{i=1}^{n} 3^{-i}) \times V_{dc}</td>
</tr>
<tr>
<td>VI</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>(32 \times n) - 23</td>
<td>(16 \times n) - 12 \times V_{dc}</td>
<td>(128 \times n) - 96 \times V_{dc}</td>
</tr>
<tr>
<td>VII</td>
<td>v_{1,1} = v_{1,2} = v_{1,3} = v_{1,4} = V_{dc} (j = 1, 2, \ldots, n)</td>
<td>8 \times (\sum_{i=1}^{n} 4^{-i}) + 1</td>
<td>4 \times (\sum_{i=1}^{n} 4^{-i}) \times V_{dc}</td>
<td>32 \times (\sum_{i=1}^{n} 4^{-i}) \times V_{dc}</td>
</tr>
</tbody>
</table>

Figures 8 and 9 elaborate the maximum output voltage and total blocking voltage required by the proposed topology for different proposed methods, respectively. From Figures 8 and 9, the seventh proposed method needs a lower number of inverter modules to generate particular levels with reduced blocking voltage. Moreover, the first proposed algorithm requires more numbers of dc voltage sources as it is common for any topology. It is observed that the first proposed method has lower voltage amplitudes of the used sources, and the seventh proposed method needs a minimum number of switching devices and high combinations magnitudes of the voltage sources. However, its performance is better than the other proposed methods except the first one. Therefore, it is concluded that the seventh method forays a better performance among all the proposed methods.

Table 3 elaborates the mathematical relations to achieve switching devices, dc sources, and switching devices in the current conduction path for symmetrical configurations.

Figure 5: Submultilevel inverter topology.

Figures 10–12 represent a plot between number of voltage levels and dc sources, switching devices, and switches in the current conduction path. In Figure 10, the proposed topology requires less number of dc sources to produce higher voltage levels. From Figures 11 and 12, the proposed
It is essential to investigate the cost reduction of the component counts in comparison between the proposed and reduced counts topologies in view of producing higher number of voltage levels in symmetrical configuration. The recent component count topologies reported in the literature [21, 33–36] are devised by arranging the dc sources in a suitable way to reduce the number of components for producing the desired voltage levels in output. In this perspective, an analysis has been taken to consider two different voltage levels 45 and 47 to showcase the drastic reduction in the switch count with a fixed number of voltage sources. For 47-level inverter, the topology reported in [33] requires 50 and the topologies in [34, 35] utilize 48, while the proposed topology requires only 32 switching devices. Similarly, for 45-level inverter, the proposed topology requires only 31, and the topologies reported in [21, 36] need 41 and 66 switching devices, respectively. It shows that proposed topology is compact and more economical.

### 3. Measured Simulation and Experimental Results

The effectiveness and viability of the topology have been simulated with Matlab R2015b, and the same simulation specifications are taken to construct the laboratory prototype for experimental investigations. The topology shown in Figure 1 is reconfigured to produce 9 level in the output voltage, and the input dc voltage source magnitudes are considered as 75 V each with the specifications 2 kH switching frequency, RL load of resistance 150 Ω, and inductance 100 mH, respectively. Figure 13 portrays the gating pulses for the switches (S1 to S9) in the switched configured stage of the proposed topology to produce 9 levels in the output voltage waveform. Figures 14 and 15 demonstrate nine-level output voltage of proposed inverter topology and inductive load current waveforms, respectively. The THD spectrum with THD of 12.67% is displayed in Figure 16.
The pictorial representation of the experimental prototype built in the laboratory has been depicted in Figure 17 to showcase the practical reliability of the proposed topology. The gating pulse generation avails LUTs to synthesize the desired pulse train using the Xilinx Spartan 3E FPGA controller as portrayed in Figure 18. Gating pulses for the switches ($S_1$ to $S_8$) in the switched configured stage of the proposed topology to produce 9 level in the output voltage waveform are shown in Figure 19.

Table 3: Mathematical relations to achieve switching devices and dc sources for “m” levels.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Minimum no. of voltage levels</th>
<th>No. of switches</th>
<th>No. of DC sources</th>
<th>No. of freewheeling diodes</th>
<th>No. of switches in the current conduction path</th>
</tr>
</thead>
<tbody>
<tr>
<td>R [29]</td>
<td>5</td>
<td>($m + 1$)</td>
<td>($m + 1)/2</td>
<td>—</td>
<td>($m + 1)/2</td>
</tr>
<tr>
<td>R [30]</td>
<td>5</td>
<td>($m + 3$)</td>
<td>($m - 1)/2</td>
<td>—</td>
<td>($m + 3)/2</td>
</tr>
<tr>
<td>R [31]</td>
<td>5</td>
<td>($m + 1$)</td>
<td>($m + 1)/2</td>
<td>—</td>
<td>($m + 1)/2</td>
</tr>
<tr>
<td>R [32]</td>
<td>5</td>
<td>($m + 11)/2</td>
<td>($m - 1)/2</td>
<td>($m - 5)/2</td>
<td>($m + 3)/2</td>
</tr>
<tr>
<td>Proposed</td>
<td>7</td>
<td>($m + 17)/2</td>
<td>($m - 1)/2</td>
<td>—</td>
<td>($m + 3)/2</td>
</tr>
</tbody>
</table>

Figure 10: No. of voltage levels vs no. of DC sources.

Figure 11: No. of voltage levels vs no. of switching devices.
Figure 12: No. of voltage levels vs no. of switches in current conduction path.

Figure 13: Gating pulse for 9-level inverter.
**Figure 14:** Output voltage of proposed 9-level inverter for R-L load.

**Figure 15:** Inductive load current waveform.

**Figure 16:** Voltage THD waveform.

**Figure 17:** Experimental setup of proposed inverter topology.
Start

Initiation of Reference Carrier Frequency
(20 MHz Clock)

Carrier Frequency

Get Input Frequency

Check for Leading Edge

No

Initialize Address for Modulating Envelope Memory and Quarter = 1

Draw the fetching clock from the board clock to capture the modulating envelope sample

Store the sampled data in LUT

Check for the quarter

Quarter 1

Yes

Address = 0

No

Address + 1

Get the sine sampled data from look up table

Reference sine data - modulation index * sampled data

Fix modulation index

Reference sine data - modulation index * sampled data

Counter = Counter + step value

Yes

Counter

Counter < Base value

Slope direction = Inversion of slope direction

Counter - Counter + step value

No

Triangle data1=Counter 

Triangle data2=Triangle data1+base value

Triangle data3=Triangle data2+base value

Triangle data4=Triangle data3+base value

Comparators

–+ –+ –+ –+

PWM 1 PWM 2 PWM 3 PWM 4

Figure 18: Experimental flow chart for FPGA pulse generation.
Figure 19: Gating pulses for proposed nine-level inverter switches (a) $S_1$ to $S_4$ and (b) $S_5$ to $S_8$.

Figure 20: Output voltage waveform and voltage spectrum.

Figure 21: Inductive load current waveform.
The nine-level output voltage waveform of improved quality in near sinusoidal shape along with better harmonic spectrum has been depicted in Figure 20. From the harmonic spectrum, it is observed that the total harmonic distortion (THD) of the output voltage waveform is near to the specified acceptable limits, and it results in the minimum requirement of the output filter size. Figure 21 depicts the experimental inductive load current waveform. Figure 22 represents the output voltage variation with a change in amplitude modulation index. It is inferred that the developed topology responds well with change in voltage variation. The experimental results accorded with simulation results.

4. Conclusion

In comparison to traditional MLI topologies, the proposed topology is formulated with a view of figuring out reduced components to produce a higher number of voltage levels. The operating modes for generating nine levels have been presented with the flow path. The proposed MLI topology has been described in depth, as well as methods for determining the magnitude of voltage sources. The proposed topology requires only one switching device to add a single voltage source with the parent module and thus making the reduced number of switches in the current conduction path thereby making less power loss. The simulation and experimental results showcase the merits of the proposed topology for the practical applications like renewable and drive sectors.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References


