A High Gain DC-DC Converter Based on Coupled Inductor and Switched-Capacitor Cell with Low-Voltage Stress

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Received 15 January 2022; Revised 7 April 2022; Accepted 25 April 2022; Published 25 May 2022

Academic Editor: Bhargav Appasani

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This paper presents a nonisolated ultrahigh step-up DC-DC converter with an interleaved structure that is suitable for high power and voltage applications. In order to increase the voltage gain, the proposed structure uses coupled inductors and switched-capacitor cells. Achieving this goal is accompanied by avoiding the imposition of any extreme duty cycle or high turns ratio to the converter. The current ripple is reduced due to the use of the interleaved structure. Since the voltage stress of the switches is lower than the output voltage, by selecting the low-voltage rated switches and small RDS(on), the conduction losses are reduced. In addition, alleviating the phenomenon of reverse recovery of diodes and creating soft-switching conditions in MOSFETs, which leads to a reduction of switching losses, are other advantages of the proposed converter. Therefore, there is no need to use clamp circuits in the mentioned structure. The experimental results, using a prototype of 350 W-18 V/400 V, verify the effective performance of the proposed converter.

1. Introduction

In recent years, attention to power electronic equipment has increased due to the ability to work at high voltage and high power. Also, environmental problems caused by fossil fuels and exposure to global warming have increased the need to pay attention to renewable sources. Since these power sources do not have the ability to generate high voltage DC voltage, the need to use the power electronic converters as one of the types of power electronic equipment to increase the output voltage levels has increased more than before. Therefore, along with the increasing development of renewable energy, the power electronic converters, which are one of their vital elements, have also undergone changes, including design in the structure in order to increase efficiency and performance. The conventional DC-DC boost converters have been widely used in photovoltaic (PV) systems in the past. Although they have a simple structure, their high voltage stress, low power density, output voltage sensitivity to the duty cycle, reverse recovery problem, and high current ripple limit their use. By storing energy at the input of the step-up DC-DC converter and releasing it towards the output, the DC voltage increases [1]. Basically, such topologies are divided into isolated and nonisolated structures [2]. The isolated converters, although they have a high voltage conversion ratio [3], are large in size due to the use of transformers and inductors. Their production cost and electromagnetic interference (EMI) are high. The flyback [4, 5] and the forward [6, 7] are examples of this category. Therefore, understanding the above conditions in relation to the first category, the desire to use nonisolated converters is quite evident. The nonisolated step-up DC-DC converters are based on conventional boost converters that are designed and created by applying and adding voltage boosting techniques to their circuit structure and creating novel topologies. These techniques are mainly created with the help of circuit elements, including diodes, capacitors, and inductors. The switched capacitors [8, 9], the switched inductors [8, 10], and the voltage multipliers [11] are among the most important voltage boosting techniques. The use of coupled inductors [12] and multiphase converter topology, the so-called interleaved [13], are some of the most effective

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voltage gain boosting techniques that researchers today use frequently in their designs. The number of magnetic cores will definitely decrease with the help of coupled inductors. Also, the current ripple is reduced using the interleaved technique, and as a result, the power density will be increased. At present, the problem of increasing the voltage gain by using voltage boosting techniques, either individually or in combination with these techniques in newer topologies, is still of interest to researchers. In such complex structures, in addition to the voltage gain in high power applications, other important characteristics such as reducing the voltage stress of semiconductors, reducing current ripple, and creating soft-switching conditions to reduce loss and increase efficiency should also be considered. In [20], a nonisolated high step-up DC-DC converter is introduced. Although the converter has a low input current ripple, the voltage gain is entirely dependent on the number of stages of the converter. The switched-capacitor/the switched-inductor technique is used in [15]. The voltage and current stress are less than the output voltage in this converter, but the pulsating input current and the developed modules from the switched capacitor/the switched inductor are among the disadvantages of this converter. A high step-up DC-DC converter topology consisting of coupled inductors and switched capacitors has been introduced by researchers in [16]. The zero-voltage switching (ZVS) conditions have increased the efficiency of the converter. The dependence of the voltage gain on the duty cycle is the most important defect of this converter. The same technique is used in [17]. This integration has increased the output voltage for use in the renewable energy conversion systems, but the leakage energy of the inductors has caused voltage spikes on the power switches, necessitating a passive or active clamp circuit. In [18], a novel topology is introduced based on the coupled inductor and SEPIC DC-DC converter, which have been evaluated from different aspects. This structure has low efficiency along with the desired characteristics. An ultrastep-up DC-DC converter was proposed in [19], which increases the output voltage by using a lift circuit. Due to the multiplicity of circuit components, the converter control becomes complicated. In [20], a nonisolated high step-up DC-DC converter is provided, which is based on quasi-Z-source (QZS) and the coupled inductor. In this topology, the input current is completely continuous. Also, by applying high turns ratios, there is no interference in boosting the output voltage level. In [21], a high step-up DC-DC converter is introduced. Researchers at [21] were able to increase the output voltage level by integrating and embedding voltage multiplier cell (VMC) and three-winding coupled inductor techniques in the design. Also, leakage energy absorption, low-voltage stress, reduction of reverse recovery loss, and desired efficiency are the advantages of this converter. Of course, it is noted that the complexity of the circuit increases with the three-winding coupled inductor. It was shown by researchers in [22] that the voltage boosting capability is carried out by the interleaved structure, coupled inductors, and voltage lift capacitors. In addition to the features provided in [21], the input current ripple is also drastically reduced. In this converter, soft-switching conditions can also be seen on MOSFETs. Table 1 shows the shortcomings of the above techniques.

This paper suggests a novel nonisolated ultrahigh step-up DC-DC converter with interleaved structure and a design that includes a combination of coupled inductors and switched-capacitor cells. The main contributions of this study are as follows:

(i) The voltage conversion ratio increases with the help of the switched-capacitor technique and the series connection of the secondary windings of the coupled inductors. Such an achievement is achieved without imposing any high extreme duty cycles on the system and high turns ratios. Therefore, the proposed converter is suitable for high voltage and high power applications.

(ii) The proposed converter has a very low switch voltage stress; thus, low-voltage-rating MOSFETs with a small on-resistance can be used to reduce conduction loss and as a result high efficiency.

(iii) The ZCS turn-on of the switches is realized in the proposed converter, and the reverse recovery problem of the diodes is alleviated, which helps reduce the switching losses.

(iv) The input current ripple is significantly reduced with the help of the interleaved technique.

(v) The leakage energy is absorbed, and there is no need to use active or passive clamp circuits.

(vi) The proposed converter has a desired dynamic response so that by changing the load current, the output voltage changes quickly and with the appropriate magnitude.

This paper consists of the following sections. The structure and operation principles of the converter are described in Section 2. The steady-state converter analysis is described in Section 3. The design of the converter circuit components is given in Section 4. The converter losses analysis is described in Section 5. The dynamic performance of the proposed converter is described in Section 6. A comparison of the performance of the proposed converter with other similar converters is presented in Section 7. The experimental results and conclusions are described in Sections 8 and 9, respectively.

2. Proposed Converter Structure

Figure 1 shows the structure and power circuit of the proposed converter. The converter is based on a boost converter and has a two-phase interleaved form [23]. It consists of circuit components as follows: the input stage has two coupled inductors and two power switches (S1; S2). In the middle stage, it has six diodes (D1–D6) and five capacitors (C1–C5) as energy transfer. Finally, the output capacitor (C0) and the load (R) are located in the output stage. As can be seen from Figure 1, the converter has two coupled inductors with primary and secondary windings that are parallel and series, respectively, neutralizing the current ripple and increasing the voltage.
Also, the two cells of the switched capacitors were placed back to back in order to achieve ultrahigh voltage gain. The turns ratios are similar for both coupled inductors. Coupling references are shown in Figure 1 with symbols □ and ○. The equivalent circuit of the proposed structure is illustrated in Figure 2. The coupled inductors are modeled by an ideal transformer, the leakage inductances \( L_k \), and the magnetizing inductances \( L_m \). Due to the relevant topology, analysis is performed in the continuous conduction mode (CCM), this analysis is in the steady state, and then the duty cycle should be selected larger than 0.5 in design. The converter has eight operation modes, the details of which are described in the following. The key waveforms for the proposed converter are shown in Figure 3. The equivalent circuits of all eight operation modes are also illustrated in detail in Figure 4.

2.1. Operation Principles. To simplify the analysis of the proposed structure, the following assumptions are taken into account:

(1) All the circuit components are ideal in the proposed structure.
(2) The capacitors are large enough so that the voltages across them are constant.
2.1.1. Mode 1 \([t_0-t_1]\). \(S_1\) and \(S_2\) are ON in this mode as shown in Figure 4(a). \(D_1, D_2, D_3,\) and \(D_5\) are OFF. \(i_{D4}\) and \(i_{D6}\) start to decrease from the beginning of this mode. The leakage inductances dominate the falling rate of both diodes and will alleviate the reverse recovery problem. The falling rates of \(D_4\) and \(D_6\) are as follows:

\[
\frac{di_{D4}(t)}{dt} = -\frac{V_{C2} + V_{C4} - V_{C1} - V_{C3}}{n^2(L_{k1} + L_{k2})},
\]

\[
\frac{di_{D6}(t)}{dt} = -\frac{V_o - V_{C1} - V_{C3} - V_{C5}}{n^2(L_{k1} + L_{k2})},
\]

where \(n = N_{a1}/N_{a0} = N_{b1}/N_{b0}\).

2.1.2. Mode 2 \([t_1-t_2]\). It is clear from Figure 4(b) that all diodes are OFF in this mode. The magnetizing inductances and the leakage inductances are supplied by the input voltage source. By ignoring the leakage inductance relative to the magnetizing inductance in terms of quantity, the following equations are obtained:

\[
v_{m1} = V_i - V_{C1},
\]

\[
v_{m2} = V_i.
\]

2.1.3. Mode 3 \([t_2-t_3]\). \(S_1\) is turned off at \(t_2\) as shown in Figure 4(c). \(D_1\) and \(D_5\) conduct. \(L_{k2}\) and \(L_{m2}\) are charged through the input, and \(L_{k1}\) and \(L_{m1}\) are releasing energy. The leakage current, \(i_{L1}\), charges \(C_1\), and the other capacitors are exchanging energy. The resulting equations are as follows:

\[
\frac{di_{D1}(t)}{dt} = \frac{V_{C1} + V_{C3} - V_{C2}}{n^2(L_{k1} + L_{k2})},
\]

\[
\frac{di_{D5}(t)}{dt} = -\frac{V_{C1} + V_{C5} + V_{C3} - V_{C2} - V_{C4}}{n^2(L_{k1} + L_{k2})}.
\]

2.1.4. Mode 4 \([t_3-t_4]\). In the previous mode, \(i_{D1}\) decreases linearly. This current becomes zero at \(t_3\), and \(D_1\) turns off naturally according to Figure 4(d), which will alleviate the reverse recovery problem. In this mode, \(D_3\) starts to conduct. The equations are as follows:

\[
v_i = V_{C1} - V_{C2} + V_{C3} - n(v_{m2} - v_{m1}) + v_{m1},
\]

\[
v_{m2} = V_i.
\]

2.1.5. Mode 5 \([t_4-t_5]\). \(S_1\) is turned on at \(t_4\) as shown in Figure 4(e). Because the leakage inductance prevents the changes in the current rate, zero-current switching (ZCS) is achieved for this switch. \(i_{D2}\) and \(i_{D3}\) decrease. The leakage inductances dominate the falling rate of \(D_3\) and \(D_5\) and will alleviate the reverse recovery problem. The falling rates of \(D_3\) and \(D_5\) are as follows:

2.1.6. Mode 6 \([t_5-t_6]\). In this mode, \(i_{D3}\) and \(i_{D5}\) become zero at \(t_5\), and both diodes are turned off. In this way, all the
2.1.7. Mode 7 [t6-t7]. S2 is turned off at t6 as shown in Figure 4(g). D3 and D4 conduct. Lk1 and Lm1 are charged through the input source, and Lk2 and Lm2 are releasing energy. C1 and C3 are discharged, and the load current is supplied instead. The series windings and C3 play the role of a voltage source, which further expands the voltage gain. iD2 is decreased, and subsequently, C2 is charged. The resulting equations are as follows:

\[ v_{m1} = V_i \]  \hspace{1cm} (7)  
\[ v_{m2} = V_i + V_{C1} - V_{C2}. \]  \hspace{1cm} (8)  

2.1.8. Mode 8 [t7-t0]. iD2 was decreasing linearly in the previous mode so that it becomes zero at t7. D2 is turned off naturally according to Figure 4(h), which will alleviate the reverse recovery problem. In this mode, D6 starts to conduct. C1 and C3 are discharged, and the load current is supplied. S2 is turned on at the end of mode 8 at t0. The ZCS is achieved for this switch because the leakage inductance prevents the changes in the current rate. The equations are as follows:

\[ V_i = V_o + V_{m2} - V_{C1} - V_{C3} - V_{CS} - n(v_{m1} - v_{m2}). \]  \hspace{1cm} (9)  

3. Steady-State Analysis

3.1. Voltage Gain. With the help of the volt-second balance principle and its use for magnetizing inductance, the following expressions are expressed:

\[ v_{m1}^{on} DT + v_{m1}^{off} (1-D) T = 0 \Rightarrow V_i DT + (V_i - V_{C1})(1-D) T = 0, \]  \hspace{1cm} (10)  

where D and T are the duty cycle and the switching period, respectively.

By solving (18), the voltage of C1 is obtained as follows:

\[ V_{C1} = \frac{1}{1-D} V_i. \]  \hspace{1cm} (11)  

Using (19) and placing (20) in it, the following equation can be reached:
Figure 4: Continued.
Using equations (3)–(5) and (7) and also (20) and (21), the voltage of \( C_3 \) is obtained as follows:

\[
V_{C3} = \frac{n + 2}{1 - D}V_i. \tag{13}
\]

Using equations (9)–(11) and (16) to (17), the voltage of \( C_4 \) is obtained as follows:

\[
V_{C4} = \frac{2n + 2}{1 - D}V_i. \tag{14}
\]

Thus, using (10),

\[
V_{C5} = \frac{2n + 2}{1 - D}V_i. \tag{15}
\]

Using (14) and (16) and also (20) to (22) and (24), the voltage gain of the proposed converter is found as follows:

\[
M = \frac{V_o}{V_i} = \frac{4n + 6}{1 - D}. \tag{16}
\]

Figure 5 shows the relationship between the voltage gain of the proposed converter and the duty cycle based on the different turns ratios. It is clear that the proposed converter has an ultrahigh step-up voltage gain without any extreme duty cycle imposition or a high turns ratio.

3.2. Voltage Stress. The voltage stresses of the circuit capacitors are found using the capacitor voltage equations described in the previous section. Thus, by applying equations (20) to (24) and placing (25) in them, the voltage stresses equations associated with the capacitors are obtained as follows:

\[
V_{C1} = \frac{1}{4n + 6}V_o; \tag{17a}
\]

\[
V_{C2} = \frac{2}{4n + 6}V_o; \tag{17b}
\]

\[
V_{C3} = \frac{n + 2}{4n + 6}V_o; \tag{17c}
\]

\[
V_{C4} = V_{C5} = \frac{2n + 2}{4n + 6}V_o. \tag{17d}
\]

The voltage stress of the second switch is clamped by \( C_1 \) and \( C_2 \) in mode 7. Therefore, considering \( V_{C2} - V_{C1} \),

\[
V_{S1} = V_{S2} = \frac{1}{1 - D}V_i \tag{18a}
\]

\[
= \frac{1}{4n + 6}V_o. \tag{18b}
\]

It is clear from (27) that, by considering \( n = 1 \), the voltage stresses of the switches are one-tenth of the output voltage. As a result, the conduction losses are reduced with a small RDS(on).
According to the operation principles of the proposed converter and operation modes, as well as using Kirchhoff’s voltage law, the voltage stresses of the diodes can be found from the voltage equations of the capacitors as follows:

\[
V_{D1} = V_{D2} = |V_{C2}|
\]

\[
= \frac{2}{4n + 6} V_o
\]

\[
V_{D3} = V_{D4} = |V_{C4}|
\]

\[
= \frac{2n + 2}{4n + 6} V_o
\]

\[
V_{D5} = |V_{C5}|
\]

\[
= \frac{2n + 2}{4n + 6} V_o
\]

\[
V_{D6} = |V_{C1} + V_{C3} + V_{C5} - V_o|
\]

\[
= \frac{n + 1}{4n + 6} V_o
\]

(19)

Figure 6 depicts the normalized voltage stresses of semiconductors and the circuit capacitors based on equations (26) to (28). It is clear from Figure 6 that the voltage stresses on S1, S2, C1, C2, D1, and D2 decrease by increasing the turns ratio of the coupled inductors. Voltage stresses increase very little for the other circuit components by increasing the turns ratio. However, their voltage stresses are still lower than the output voltage.

3.3. Input Current Ripple and Magnetizing Inductance. By the voltage gain equation and as well as \(P_i = P_o\), the ratio of the output current to the input current of the proposed converter can be expressed as follows:

\[
\frac{I_o}{I_i} \langle \text{Avg} \rangle = \frac{1 - D}{4n + 6}
\]

(20)

Due to the use of a two-phase interleaved structure and considering that the average magnetizing currents are called \(I_{m1, \text{Avg}}\) and \(I_{m2, \text{Avg}}\) as well as \(I_{m1, \text{Avg}} = I_{m2, \text{Avg}} = I_{m, \text{Avg}}\), they are described by the following equation with the help of (29):

\[
I_{m1, \text{Avg}} = I_{m2, \text{Avg}} = I_{m, \text{Avg}} = \frac{I_o}{2} = \frac{2n + 3}{1 - D} I_{m, \text{Avg}}
\]

(21)

where \(I_{m, \text{Avg}}\) and \(I_{o, \text{Avg}}\) are the average input and output currents, respectively. It is clear from (30) that these currents are balanced. In association with the secondary windings of the coupled inductors, which are in series, it is pointed out that they share the same secondary current. Given this point and the fact that the input current is the sum of the primary currents in the coupled inductors, therefore the input current is expressed as follows:

\[
i_i = (i_{m1} + ni_{\text{Sec}}) + (i_{m2} - ni_{\text{Sec}})
\]

\[
i_i = i_{m1} + i_{m2}.
\]

(22)

According to the operation principles of the proposed converter and according to the interleaved structure, the input current ripple frequency is twice the switching frequency, \(f_o\), which means that the input current is continuous and its ripple is remarkably reduced. The power switches are turned on in DT, and the voltage of the input inductors is equal to \(V_i\). Therefore, using Faraday’s law, the ripple of the magnetizing and input currents is expressed by (32) and (33).

\[
\Delta i_m = \frac{D}{I_m f_s} V_i,
\]

\[
\Delta i_i = \frac{2D - 1}{I_m f_s} V_i.
\]

(23)

(24)

Figure 7 shows the current ripple curve normalized for the input current and the magnetizing current. The current ripple is also lower in smaller duty cycles. This means that
the size of the coupled inductors can also be designed less. Consequently, the current stress is reduced in the input capacitor, which increases the power density.

4. Design Considerations

4.1. Coupled Inductors. It is necessary to select a duty cycle that is larger than 0.5 to determine the turns ratio of the coupled inductors. By selecting the required output voltage, the turns ratio of the coupled inductors can be found with consideration of (25) and according to the following equation:

\[ n = \frac{M(1 - D) - 6}{4} \]  

(25)

The magnetizing inductance are obtained by considering \( I_m = I_{m1} = I_{m2} \) and considering (32) and based on the magnetizing current ripple according to (35),

\[ L_{m1} = L_{m2} = L_m = \frac{D}{\Delta t_{fs}} V_i. \]  

(26)

It should be \( I_{m-Avg} \geq \frac{1}{2} \cdot \Delta i_m \) to ensure that the converter operates in CCM. Therefore, the minimum magnetizing inductance is in accordance with (36):

\[ L_m \geq \frac{1}{2} \frac{(1 - D)D}{(2n + 3)I_{o-Avg}} V_i. \]  

(27)

Since the leakage inductances play an important role in alleviating the reverse recovery problem of diodes, therefore, the falling rate of diodes can be used to calculate the leakage inductances. Thus, by applying the absolute of (11) as well as considering equations (20) to (22) and (25), (37) is obtained:

\[ L_{k1} = L_{k2} = L_k = \frac{n + 1}{4(2n + 3)n^2} V_o, \quad \frac{dI_{D3}(t)}{dt} = x. \]  

(28)

The peak magnetizing currents are obtained by considering (30) and (32) according to the following equation:

\[ I_{m1-Pk} = I_{m2-Pk} = I_{m-Pk} = 2n + 3 \frac{D}{1 - D} I_{o-Avg} + \frac{1}{2} \frac{D}{L_m f_s} V_i. \]  

(29)

4.2. Semiconductors. All diodes and power switches are designed based on their voltage stresses. Furthermore, the average current of all diodes is equal to the average output current because the converter operates in CCM, and also the average current of the capacitors is zero in one switching period. Then,

\[ I_{D1-Avg} \cdots I_{D6-Avg} = I_{o-Avg}. \]  

(30)

Also, the relationship between the average output current and the peak current of the diodes can be expressed according to equations (40). The peak current of the diodes will then be obtained by arranging equation (40) according to equation (41):

\[ I_{D1-Pk} \cdots I_{D6-Pk} = \frac{2}{1 - D} I_{o-Avg}. \]  

(32)

Using the principles of operation of the proposed converter and the fourth and seventh operation modes, the peak current of the power switches is expressed as follows:

\[ I_{S1-Pk} = \frac{I_{o-Avg}}{2} + nI_{D1-Pk} \; \frac{4n + 5}{1 - D} I_{o-Avg} \]  

\[ I_{S2-Pk} = \frac{I_{o-Avg}}{2} + nI_{D3-Pk} + nI_{D5-Pk} \; \frac{6n + 3}{1 - D} I_{o-Avg}. \]  

(33)

Also, the RMS current of the switches using the operation principles and (30) is as follows:

\[ I_{S1-RMS} = \frac{2n + 3}{1 - D} I_{o-Avg} \left( \sqrt{1 - (2D) - \frac{4(1 - D)(n^3 + 3n^2 + 3n + 1)}{n^4 + 4n^2 + 5n + 2}} \right), \]  

(34)

\[ I_{S2-RMS} = \frac{2n + 3}{1 - D} I_{o-Avg} \left( \sqrt{3 - 2D} \right). \]  

(35)

4.3. Capacitors. The circuit capacitors are calculated and designed based on their voltage stresses, output power, and considering the voltage ripple according to the following equations:
where \( P_o \) and \( \Delta V_C \) are the output power and the voltage ripple of capacitors, respectively. It is worth noting that the use of capacitors with a low equivalent series resistance (ESR) such as metalized polyester film (MKT) can reduce power losses and improve efficiency.

5. Loss Breakdown

The proposed converter losses mainly consist of three important parts, including losses related to the power switches, the diodes, and the coupled inductors. Here, the losses of circuit capacitors are neglected due to the use of a low ESR type. Therefore, using the steady-state analysis as well as the circuit components datasheet used here, the loss breakdown of the proposed converter is as follows.

5.1. Diodes. The diode losses consist of the conduction loss and the reverse recovery loss as follows:

\[
P_{D_{\text{Loss}}} = P_{D_{\text{Con}}} + P_{D_{\text{Rev}}}
\]

where \( P_{D_{\text{Con}}} \) and \( P_{D_{\text{Rev}}} \) are the conduction loss and the reverse recovery loss, respectively. The first term is related to when the diode is conducted. It is found by relying on the diode datasheet and the average diode current as follows:

\[
P_{D_{\text{Con}}} = V_F \cdot I_{D_{\text{Avg}}}
\]

where \( V_F \) is the forward voltage. Due to the performance of the proposed converter, which alleviates the reverse recovery of the diodes, \( P_{D_{\text{Rev}}} \) can be neglected. Therefore, the total losses of the diodes are extracted as follows:

\[
P_{D_{\text{Loss}}} = 6 \cdot V_F \cdot I_{D_{\text{Avg}}}
\]

\[
= 3 \cdot 0.86 \cdot 0.87 + 3 \cdot 0.9 \cdot 0.87
\]

\[
= 4.5W.
\]

5.2. Switches. The switch losses consist of the conduction loss and the switching loss as follows:

\[
P_{S_{\text{Loss}}} = P_{S_{\text{Con}}} + P_{S_{\text{Sw}}}
\]

where \( P_{S_{\text{Con}}} \) and \( P_{S_{\text{Sw}}} \) are the conduction loss and the switching loss, respectively. \( P_{S_{\text{Con}}} \) is found by relying on the switch datasheet and equations (44) and (45) as follows:

\[
P_{S_{\text{Con}}} = R_{ds} \cdot (\text{On}) \cdot I_{S_{\text{RMS}}}^2
\]

\[
= \frac{7.2}{\text{mfl}} \cdot (9.3^2 + 14.5^2)
\]

\[
= 2.1W.
\]

5.3. Coupled Inductors. The losses of the coupled inductors consist of their core and the copper used in the windings. These losses include both the primary and secondary sides. Thus,

\[
P_{C_{\text{Loss}}} = P_{C_{\text{Core}}} + P_{C_{\text{Cop}}}
\]

The core loss, a large part of which is related to hysteresis loss, according to the Steinmetz equation, can be expressed as follows:

\[
P_{C_{\text{Core}}} = K \cdot f^\alpha \cdot B_{\text{MAX}}^\beta \cdot A_c \cdot l_c
\]

\[
= 2 \cdot 0.56
\]

\[
= 1.12W.
\]

In equation (51), the coefficients of \( K = 0.000214 \), \( \alpha = 1.26 \), and \( \beta = 2.21 \) can be found from the core datasheet. \( B_{\text{MAX}}, A_c, \) and \( l_c \) are the maximum core flux density, a cross-sectional area of the core, and the mean path length of the core, respectively.

The copper loss is calculated for both primary and secondary with \( I_{\text{Nat0,RMS}} = 12.8A, \) \( I_{\text{Nat1,RMS}} = I_{\text{Sec,RMS}} = 4.9A, \) and \( R_{\text{DC}} = 7.32 \text{ m\Omega} \) as follows:

\[
P_{C_{\text{Cop}}} = 2R_{\text{DC}} \left( I_{\text{Nat0,RMS}}^2 \cdot I_{\text{Nat1,RMS}}^2 \right)
\]

\[
= 2.75W.
\]

Figure 8 illustrates the distribution of loss in the proposed converter. As can be seen, the largest share of the proposed converter losses is for the diode loss. As mentioned earlier, in this part, the major share of loss generation is related to the conduction loss of the diodes. After that, although the loss of the coupled inductors was calculated and expressed separately, as can be seen from Figure 8, their aggregation into two forms of the core and the copper loss also include a major share of the proposed converter losses. The lowest losses belong to the power switches, which is the sum of the switching and the conduction loss.

6. Dynamic Performance

The dynamic performance of the proposed converter can be analyzed using the small-signal model and the state-space averaged technique and applying Kirchhoff’s laws. Consider the following. All semiconductors are ideal. Leakage inductances are ignored. The converter is in a steady state. The
ESR of inductors is ignored. The ESR of all circuit capacitors except the output capacitor is equal to \( r_c \). Also, state-space equations are achieved in one switching period, regardless of the small intervals, and in the modes where \( S_1 \) and \( S_2 \) are in the form of \([\text{ON ON}, \text{ON OFF}, \text{OFF ON}]\). According to equation (51), the state variables are the current of inductors and voltage of capacitors. The arrays of matrices \( A, B, \) and \( C \) in equation (50) are given in equations (51). The vector of input and output variables is also given in equation (51). The weight coefficients for three switching states in the state matrix are as follows: \((1 - d), (2d - 1)\), and \((1 - d)\).

\[
\begin{bmatrix}
  \hat{x}_i(t) \\
  \hat{y}_i(t) \\
  \hat{z}_i(t) \\
  \hat{u}_i(t) \\
  \hat{y}_o(t)
\end{bmatrix} = \begin{bmatrix}
  [A][\hat{x}_i(t)] + [B][\hat{u}_i(t)] \\
  [C][\hat{z}_i(t)] \\
  \hat{z}_i(t) \\
  \hat{u}_i(t) \\
  \hat{y}_o(t)
\end{bmatrix},
\]

\begin{align}
\hat{x}_i(t) &= [A]\hat{x}_i(t) + [B]\hat{u}_i(t), \\
\hat{y}_i(t) &= [C]\hat{z}_i(t), \\
\hat{z}_i(t) &= \begin{bmatrix}
  \hat{u}_1(t) \\
  \hat{u}_2(t) \\
  \hat{u}_3(t) \\
  \hat{u}_4(t) \\
  \hat{u}_5(t) \\
  \hat{u}_6(t)
\end{bmatrix}^T, \\
\hat{u}_i(t) &= \begin{bmatrix}
  \hat{v}_1(t) \\
  \hat{v}_2(t) \\
  \hat{v}_3(t) \\
  \hat{v}_4(t) \\
  \hat{v}_5(t) \\
  \hat{v}_6(t)
\end{bmatrix}, \\
\hat{y}_i(t) &= \begin{bmatrix}
  \hat{v}_o(t)
\end{bmatrix}
\end{align}

\( A \) is defined as:

\[
A = \begin{bmatrix}
  0 & 0 & -n(2d - 1) & n(2d - 1) & -n(2d - 1) & 0 & 0 & 0 \\
  0 & 0 & n(1 - d) & -n(1 - d) & n(1 - d) & -n(1 - d) & 0 & 0 \\
  -n(2d - 1) & 1 - d & \frac{1}{r_c C_1} & \frac{1}{r_c C_1} & 0 & 0 & 0 & 0 \\
  0 & 0 & n(1 - d) & -n(1 - d) & n(1 - d) & -n(1 - d) & 0 & 0 \\
  \frac{2d - 1}{r_c C_2} & \frac{d - 1}{r_c C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\
  \frac{n(2d - 1)}{r_c C_3} & \frac{1 - d}{r_c C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\
  0 & \frac{d - 1}{r_c C_4} & 0 & 0 & 0 & 0 & 0 & 0 \\
  0 & 0 & \frac{1}{r_c C_5} & \frac{1}{r_c C_5} & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & \frac{-1}{R C_o} & 0 & 0 & 0
\end{bmatrix},
\]

\( A_{\text{ROM}} \) is the reduced order model.
The phase margin in the Bode diagram shown in Figure 9 is 67.4°. Therefore, the stability of the system is guaranteed. Figure 10 shows the proposed converter control block diagram. In this system, a Type-2 PI controller is used to control the voltage. The $K$-factor method can be used to find the coefficients of the PI controller. This is achieved by determining the main parameters, namely, the phase margin (PM) and the crossover frequency ($f_c$).

The design steps of the $K$-factor approach are as follows:

Step 1: Plot the frequency response, Bode, and plot of the open-loop transfer function. Choose the desired crossover frequency ($f_c$), depending on the transient response requirements, and determine the phase shift and gain of the open-loop converter.

Step 2: Choose the desired phase margin (PM) depending on the maximum allowable overshoot requirement.

Step 3: Calculate the required phase boost and hence determine the $K$-value. Here, this $K$-value will be useful for selecting the appropriate compensator PI or PID type and so on.

Step 4: Using pole-zero locations, determine the compensator parameter values.

By using the above steps, the compensator design can do with the help of popular MATLAB software. If the closed-loop performance specifications are not matching with the requirements, then repeat the above steps until fulfilling the requirements by changing the crossover frequency. By using any power electronic simulator (PSIM), verify the time domain responses through simulations.

In this work, the Type-2 PI controller has been used to keep overall closed-loop stability and good dynamic response of the proposed converter. The “Type-2” controller is one kind of lead-type controller with a pole at the origin. Hence, this controller provides a maximum 90° phase boost with zero steady-state errors. Even though the boost converter has a nonminimum phase problem, it exhibits a better closed-loop performance with a Type-2 controller. With proper tuning of this controller, the converter performs a faster response, with minimal overshoots and zero steady-state errors. Therefore, by considering PM = 67.4° and $f_c = 1000$ Hz, the following coefficients are obtained: $k = 1000$, $k_1 = 1221.2$, and $k_2 = 32323$. 

\[
B = \begin{bmatrix} 1 & 1/L_{m1} & 0 & 0 & 0 & 0 & 0 \\ 1/L_{m2} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T, \tag{50}
\]

\[
C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 \end{bmatrix}. \tag{51}
\]
7. Comparison

Table 2 compares the proposed converter with other converters that are similar in structure and topology. The characteristics that are compared include voltage gain, maximum voltage stress of power switches, maximum voltage stress of diodes, and number of circuit components in the structure, including switches, diodes, capacitors, and coupled inductors, as well as features such as soft-switching conditions and amount current ripple. Therefore, by reviewing Table 2, the advantages of the proposed structure over similar structures are revealed. In the column related to the voltage gain, it is observed that the converters proposed in previous papers, namely, [22, 24–30], have a lower voltage gain than the proposed converter. This is also true for the second column of Table 2. The proposed converter, as mentioned in the previous sections, has voltage stress of one-tenth of the output considering a unique turns ratio. Therefore, the proposed converter is superior to other converters in this characteristic. With the same numbering for the maximum voltage stress equations of the diodes in the third column, only converters [24, 31] are slightly smaller than the proposed converter. However, as mentioned in the previous sections, the voltage stress of the diodes and even the power switches in the proposed converter is still less than the output voltage. In terms of the number of circuit components, the converters of [22, 29–31] have more diodes and capacitors than the proposed converter. Also, the number of power switches of the converters [25, 26] is more than two. The converter of [26] also has 9 capacitors. In this regard, the coupled inductors are wound on three cores in the topologies of [22, 25, 27, 29], while the proposed converter has two cores. Obviously, more circuit components mean more losses. Finally, the converters of [28, 30] do not have soft-switching conditions, and of course, all converters have low current ripples. Figure 11 shows the comparison curve of the proposed converter voltage gain with other similar converters of the same class. Obviously, the proposed converter has an ultrahigh voltage gain than other converters without any extreme duty cycle or high turns ratio applied to the system, and it is quite suitable for high power and high output voltage applications. The efficiency of the topologies mentioned above is also listed in Table 2.

8. Experimental Results

To verify the desired performance of the proposed converter, a prototype of 350 W-18 V/400 V was made from which laboratory results were extracted. The main specifications of the prototype and its image are given in Table 3 and Figure 12, respectively. MOSFETs with excellent switching performance and fast Schottky diodes have been used in the implementation of the prototype. The sampling time at 47 kHz is 21 microseconds. The winding turns ratio of the coupled inductors is 1 with the number of turns 35. According to the previously mentioned statement, the duty cycle is concluded for the proposed converter greater than 0.5. Thus, the duty cycle associated with the power switch gates is about 0.55. This means that step-up voltage

---

Table 2: Comparison of the proposed converter with other similar converters.

<table>
<thead>
<tr>
<th>Topologies</th>
<th>Voltage gain (M)</th>
<th>Max. voltage stress (switches)</th>
<th>Max. voltage stress (diodes)</th>
<th>S*</th>
<th>D*</th>
<th>C*</th>
<th>M*</th>
<th>η* (%)</th>
<th>Soft switching/input current ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>[22]</td>
<td>3n₂ (1 + n₁) + 2/1 – D</td>
<td>V_o/3n₂ (1 + n₁) + 2</td>
<td>(2n₂ (1 + n₁) + 1)V_o/3n₂ (1 + n₁) + 2</td>
<td>2</td>
<td>8</td>
<td>7</td>
<td>3</td>
<td>95.2</td>
<td>Yes/low</td>
</tr>
<tr>
<td>[24]</td>
<td>2n + 4/1 – D</td>
<td>V_o/2n + 4</td>
<td>nV_o/n + 2</td>
<td>2</td>
<td>6</td>
<td>2</td>
<td>7.2</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td>[25]</td>
<td>2n + 4/1 – D</td>
<td>V_o/2n + 4</td>
<td>(n + 1)V_o/n + 2</td>
<td>3</td>
<td>6</td>
<td>3</td>
<td>96.2</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td>[26]</td>
<td>2n + 2/1 – D</td>
<td>V_o/2n + 2</td>
<td>V_o/2</td>
<td>4</td>
<td>6</td>
<td>2</td>
<td>97.2</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td>[27]</td>
<td>n + 2/1 – D</td>
<td>V_o/n + 2</td>
<td>V_o</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>97.3</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td>[28]</td>
<td>4n + 4/1 – D</td>
<td>V_o/4n + 4</td>
<td>V_o/2</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>94.5</td>
<td>No/low</td>
<td></td>
</tr>
<tr>
<td>[29]</td>
<td>3n + 1/1 – D</td>
<td>V_o/3n + 1</td>
<td>2nV_o/3n + 1</td>
<td>2</td>
<td>8</td>
<td>3</td>
<td>97</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td>[30]</td>
<td>2nk + N + 1/1 – D</td>
<td>V_o/2nk + N + 1</td>
<td>2V_o/2nk + N + 1</td>
<td>2</td>
<td>10</td>
<td>2</td>
<td>94</td>
<td>No/low</td>
<td></td>
</tr>
<tr>
<td>[31]</td>
<td>6n + 1/1 – D</td>
<td>V_o/6n + 1</td>
<td>2nV_o/6n + 1</td>
<td>2</td>
<td>8</td>
<td>2</td>
<td>96.1</td>
<td>Yes/low</td>
<td></td>
</tr>
<tr>
<td><strong>Proposed</strong></td>
<td>4n + 6/1 – D</td>
<td>V_o/4n + 6</td>
<td>(2n + 2)V_o/4n + 6</td>
<td>2</td>
<td>6</td>
<td>2</td>
<td>96.6</td>
<td>Yes/low</td>
<td></td>
</tr>
</tbody>
</table>

S*: number of power switches; D*: number of diodes; C*: number of capacitors; M*: number of magnetic cores; η*: efficiency.

---

Figure 11: Comparison of the proposed converter in terms of voltage gain with other similar converters in Table 2.
Table 3: Main specifications of the prototype.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value/description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage: $V_i$</td>
<td>18 V</td>
</tr>
<tr>
<td>Output voltage: $V_o$</td>
<td>400 V</td>
</tr>
<tr>
<td>Output power: $P_o$</td>
<td>350 W</td>
</tr>
<tr>
<td>Switching frequency: $f_s$</td>
<td>$\approx 47$ kHz</td>
</tr>
<tr>
<td>Capacitors: $C_1$, $C_2$, ... $C_5$, $C_o$</td>
<td>20, 10, 2 $\times$ 56 $\mu$F</td>
</tr>
<tr>
<td>Magnetizing and leakage inductances: $L_m$ and $L_k$</td>
<td>100 $\mu$H, 2.5 $\mu$H</td>
</tr>
<tr>
<td>Turns ratio: $n$</td>
<td>1:1</td>
</tr>
<tr>
<td>Diodes: $D_3$, $D_4$, and $D_5$</td>
<td>MBR40250</td>
</tr>
<tr>
<td>Diodes: $D_1$, $D_2$, and $D_6$</td>
<td>MBR20150</td>
</tr>
<tr>
<td>Power switches: $S_1$ and $S_2$</td>
<td>IPB072N15N3G</td>
</tr>
</tbody>
</table>

Figure 12: Image of the prototype and laboratory tests.

Figure 13: Continued.
Figure 13: Continued.
conversion rates are achieved without imposing a high duty cycle on the proposed converter, and as a result, power losses are naturally reduced, and the efficiency increases reciprocally. Film capacitors were selected for the proposed structure circuit capacitors to offer the significant advantage of low ESR in order to eliminate the losses of these devices. The output capacitors are also electrolytic. It should be noted that, by considering a certain percentage of the voltage ripple, the capacitors have been selected to be larger than their design value due to their lower ESR. Note that since in the proposed interleaved converter both phases have the same operation, one phase can be analyzed. However, in this study, the performance of both phases has been investigated. In the following, the waveforms extracted from the tests performed on the prototype in the laboratory are analyzed, and the experimental results are examined. They are depicted in Figure 13 together. Figure 13(a) shows the driving signals. It indicates that the converter operates in CCM and the issue of reverse recovery has been reduced. Figure 13(b) shows the voltage stress of switches. They are less than the output voltage, about 40 V. This result is theoretically consistent with the mathematical operations related to the voltage stress of the power switches. This low amount of voltage stress no longer leads to the destruction of the power semiconductor and thus does not change the circuit MOSFET parameters. In addition, this stress significantly reduces the conduction losses and therefore allows the use of MOSFETs with low-voltage rates. It is also worth noting that there are small voltage spikes in the MOSFET voltage stress, which are caused by the leakage inductance of the coupled inductors, but since their magnitude is in the safety range, no damage is done to the power switches. The input voltage of 18 V and the output voltage of 400 V are shown in Figure 13(c). The high voltage gain is obtained by considering the turns ratio of 1. Therefore, using the proposed converter is possible and suitable for high power and high output voltage applications.

The voltage of diodes is illustrated in Figure 13(d) to Figure 13(f). According to (28) and considering the turns ratio of 1, the voltage of the first, second, and sixth diodes is

![Figure 13: Experimental results](image-url)

**Figure 13**: Experimental results: (a) driving signals of the power switches, \( S_1 \) and \( S_2 \); (b) voltage stress of the power switches, \( S_1 \) and \( S_2 \); (c) input voltage and the output voltage, \( V_i \) and \( V_o \); (d) voltages of diodes, \( D_1 \) and \( D_2 \); (e) voltages of diodes, \( D_3 \) and \( D_4 \); (f) voltages of diodes, \( D_5 \) and \( D_6 \); (g) voltages of capacitors, \( C_1 \) to \( C_3 \); (h) voltages of capacitors, \( C_4 \) and \( C_5 \); (i) currents of diodes, \( D_1 \) and \( D_2 \); (j) currents of diodes, \( D_3 \) and \( D_4 \); (k) The currents of diodes, \( D_3 \) and \( D_6 \); (l) primary winding currents of the coupled inductors; (m) voltage and current of power switches in ZCS conditions; (n) dynamic response for load increase; (o) dynamic response for load decrease.

![Figure 14: Measured efficiency in terms of output power](image-url)

**Figure 14**: Measured efficiency in terms of output power.
about 80 V with an output of 400 V. It is about 160 V for the third to fifth diodes. The resulting values are proportional to the theoretical and mathematical relationship. Figures 13(g) and 13(h) show the voltage stress of the capacitors. The obtained results are consistent with the mathematical equations of the capacitors. Assuming the unit turns ratio in equation (22) and the output voltage of 400 V, the voltage of the first to fifth capacitors is about 40 V, 80 V, 120 V, 160 V, and 160 V, respectively. With the presence of the leakage inductance associated with the coupled inductors, the alleviation of the reverse recovery problem of the diodes is achieved. This case is illustrated in Figure 13(i) to Figure 13(k). These figures show the current of the converter diodes. Figure 13(l) shows the primary winding currents of the coupled inductors, which indicate the proper sharing of current between the legs of the converter. Figure 13(m) shows the voltage and current of power switches. One of the main features of the proposed converter is the turn-on of the main switches under ZCS conditions. The dynamic response of the proposed converter with respect to the load variation and in the range of half to full load (50% to 100%) in the two modes of load increase and load decrease is shown in Figures 13(n) and 13(o), respectively. Considering both of the mentioned figures, it is clear that the dynamic response of the converter is fast, and the load regulation is performed efficiently. This means that the system is completely robust by the control model. The measured efficiency of the proposed converter based on the prototype is illustrated in Figure 14. The efficiency is measured in terms of different loads. The maximum efficiency is 96.6% at full load.

9. Conclusion

An ultrahigh step-up DC-DC converter with interleaved structure is presented in this paper. The proposed converter is made of a combination of coupled inductors along with the switched-capacitor cells. The advantages of the proposed converter include the low current ripple due to the interleaved structure, low conduction loss due to the lower voltage stress in the power switches, the soft-switching conditions, low converter losses and consequently high efficiency of 96.6%, alleviation of the reverse recovery problem for the diodes, desired stability and dynamic performance due to the precision closed-loop control design, the leakage energy absorption, and achieving high voltage conversion ratio without any extreme duty cycle and high turns ratio. Experimental results based on a prototype were extracted and analyzed. The results showed the effectiveness and desired performance of the proposed converter.

Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>V</td>
<td>Voltage</td>
</tr>
<tr>
<td>W</td>
<td>Watt</td>
</tr>
<tr>
<td>RDS(on)</td>
<td>Drain-source on resistance</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic interference</td>
</tr>
<tr>
<td>CW</td>
<td>Cockcroft-Walton</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-voltage switching</td>
</tr>
<tr>
<td>QZS</td>
<td>Quasi-Z-source</td>
</tr>
<tr>
<td>VMC</td>
<td>Voltage multiplier cell</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous conduction mode</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero-current switching</td>
</tr>
<tr>
<td>M</td>
<td>Voltage gain</td>
</tr>
<tr>
<td>D</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>T</td>
<td>Switching period</td>
</tr>
<tr>
<td>f_s</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent series resistance</td>
</tr>
<tr>
<td>MKT</td>
<td>Metalized polyester film</td>
</tr>
<tr>
<td>PM</td>
<td>Phase margin</td>
</tr>
<tr>
<td>f_c</td>
<td>Crossover frequency</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional integral</td>
</tr>
<tr>
<td>V_i</td>
<td>Input voltage</td>
</tr>
<tr>
<td>V_o</td>
<td>Output voltage</td>
</tr>
<tr>
<td>R</td>
<td>Resistance</td>
</tr>
<tr>
<td>C_i, C_2, ...</td>
<td>Capacitors</td>
</tr>
<tr>
<td>D_1, D_2, ...</td>
<td>Diodes</td>
</tr>
<tr>
<td>P</td>
<td>Powers and losses</td>
</tr>
<tr>
<td>r_c</td>
<td>ESR of capacitors</td>
</tr>
<tr>
<td>n</td>
<td>Turns ratio</td>
</tr>
<tr>
<td>S_1, S_2</td>
<td>Power switches</td>
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<td>I, i</td>
<td>Currents</td>
</tr>
<tr>
<td>L_m</td>
<td>Magnetizing inductance</td>
</tr>
<tr>
<td>L_k</td>
<td>Leakage inductance</td>
</tr>
<tr>
<td>A, B, and C</td>
<td>State-space matrices</td>
</tr>
</tbody>
</table>

Data Availability

All data are included within this paper.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

References


