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Research Article

Low Noise Amplifier at 60 GHz Using Low Loss On-Chip Inductors

Karthigha Balamurugan, M. Nirmala Devi, and M. Jayakumar

Department of Electronics and Communication Engineering, Amrita School of Engineering, Coimbatore, Amrita Vishwa Vidyapeetham, India

Correspondence should be addressed to M. Nirmala Devi; m_nirmala@cb.amrita.edu

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This paper proposes the technique of using low loss on-chip inductors in the design of low noise amplifier (LNA) that offers high gain and lower noise figure. Upon the substrate of octagonal spiral inductors, a surface of patterned ground shield is inserted that significantly reduces the substrate loss. This effect limits the penetration of electric filed into the substrate, thereby improving the inductor's Quality (Q) factor and decouples the substrate parasitic that results with smaller series resistance. These effects result with improved gain and noise figure of LNA at 60 GHz when the designed inductors are included in it to serve as gate, source, and load inductances. The proposed work uses an inductively degenerated 3-stage common-source LNA in a 65-nm CMOS process. Simulation results show that the LNA using custom designed inductors achieves the peak gain of 17.02 dB at 56 GHz with a noise figure of 5 dB at 60 GHz for the power consumption of 10 mW. The figure-of-merit (*FOM*) is 14.56 which is 0.8 times more than the LNA design using off-chip inductors. A complete LNA layout using custom designed inductor footprints has been presented and analyzed.

1. Introduction

Due to increasing requirements of high data rate communications and information processing, 5G wireless data services proliferate by extending ISM band to higher frequencies like 60 GHz. This emerges the need for the design of low cost, RF solutions [1] at millimeter (mm) wave frequencies. Efforts have been made to develop integrated front-end receivers using nanoscale CMOS technology with a feature size of 65 nm or lesser [2], targeting mass production.

Being the first active block, the low noise amplifier (LNA) is considered as the key component that decides the noise figure (*NF*) of the entire receiver [3]. The signal received by the antenna is usually a weak signal, so prior to subsequent processing, it has to be amplified without producing noise on its own in order to maintain constant signal-to-noise ratio. Therefore, higher gain and lower *NF* are the major requirements for LNA design over the frequency band of interest. Additional features required are the good input and output reflection coefficients, wider bandwidth, and low power consumption [3, 4].

At mm wave frequencies, the impact of passive components forming LC load, matching network and degenerative inductor greatly influence the RF performances of LNA. Due to conductive nature of the substrate, on-chip spiral inductor experiences substantial loss, thereby reducing its quality (Q) factor. Also, to subside the problem of attaining self-resonance of spiral inductors at higher frequencies, various alternate design approaches have been followed [5–11]. This work presents the technique of employing low loss, on-chip inductors in the design of LNA with an aim of improving its gain and noise performance.

A surface of patterned ground shield (PGS) consisting of polysilicon strips is inserted upon the substate of an octagonal spiral inductor. The ground shield acts like a short that terminates the electric field penetration into the substrate. The pattern of polysilicon strips exhibits high resistance that decouples the substrate parasitic from inductor. These effects improve the Q-factor of the inductor that subsequently increases the LNA gain and reduces its thermal noise. For demonstration, this work uses 3-stage common-source amplifier in a 65-nm

CMOS process. The first stage is designed using the inductive degeneration technique that offers lower noise figure, while the second and third stages are designed for achieving higher gain. Our results have been compared with other reported results including their simulation and measurement data and validated using respective figure-of-merits (*FOMs*).

In papers [5, 6], authors have proposed parallel stacked spiral inductor design formed by multimetal layers that intended to reduce series resistance and mitigate substrate effects. In [7], varying metal strips that balances ohmic loss and eddy current loss has been reported to achieve optimal *Q*-factor. Though followed different methodologies for inductor realizations and LNA implementations, none has dealt the impact of substrate parasitic on inductor series resistance. Along with it, this work presents the gain and *NF* analysis of LNA in proportion with inductor *Q*-factor.

Apart from LNA implementations, voltage-controlled oscillator (VCO)-based resonators have been designed with different inductor structures. A *U*-shaped inductor line enclosing finger capacitors has been presented to realize the interdigital resonator [8]. This serves as a notch filter to switch between two bands of Ku-band VCO. Virtual inductances with a substantial *Q*-factor have been realised by defected ground structure (DGS) [9–11] that is placed exactly below the microstrip line. Etching the ground plane of substrate interrupts the electromagnetic waves, resulting in a notch-type performance. This is due to the formation of virtual inductance on the DGS structure which has been utilised in a 22-GHz band oscillator [9]. Paper [10] introduces transmission poles around the parallel resonator by using different DGS structures that results with multiresonant designs. These designs [9–11] claim to reduce the phase noise of *K*-band VCO. Overall, it is found that a low loss, high *Q* inductor that is compatible with CMOS technology has been always in demand for RF circuits.

2. Octagonal Spiral Inductor

At mm wave frequencies, an extremely small inductances in the range of 50 pH to 300 pH are required. They are realized by on-chip planar inductors with desired features such as low loss, high *Q*-factor, wide bandwidth, low power, and linear tuning range [12]. Unfortunately, they are designed on a conductive silicon substrate in which some quantity of RF signals is radiated out. This is due to capacitive and inductive coupling of substrate with inductor that results with displacement and induced currents to flow in it [13]. This is shown in Figure 1(a). The substrate loss stems from the penetration of electric field (*E*) causing the power loss.

$$P_{\text{Sub}} = \frac{E^2}{2\rho}, \tag{1}$$

where ρ is the substrate resistivity which is inversely proportional to background carrier generation. The higher the resistivity (ρ) is, the lesser the induced currents in the substrate. Resistivity with $\rho > 1.5\,\text{k}\Omega\text{-m}$ can be preferred, but then the high resistivity materials create incompatibility issues with standard CMOS process [14] and require complicated postprocessing steps. Hence, the proposed work uses CMOS compatible low resistivity substrate in disparity to equation (1) with ρ varying from $(0.1 \times 10^{-3}$ to 1) Ω-m. An octagonal spiral is chosen in this work because it forms the compromise structure between square and circular shapes in terms of inductance density and *Q*-factor [15].

The inherent behavior of the substrate is difficult to capture at RF frequencies, and hence, the on-chip inductor models are inaccurate in CMOS process design kits (PDKs). Figure 1(b) shows the octagonal inductor, while its equivalent lumped and simplified models are shown in Figures 1(c) and 1(d) [16]. In this, L_S represents the inductance reactance [17] that contributes 90° lag current and R_S accommodates all resistive loss associated with inductor including skin effects. C_s represents the overlap capacitance between the spiral structure and the underpass centre conductor [18], while C_{ox} represents the oxide capacitance between the spiral and silicon substrate. The values of R_{sub} and C_{sub} denote the resistance and capacitance of the silicon substrate.

The most important *FOM* of an integrated inductor is its *Q*-factor. It shows how well an inductor (L_S) can store energy without dissipating to R_{sub}. Unfortunately, the substrate loss causes the *Q*-factor to decrease and degrades the overall performance of low noise blocks [5, 16]. From [16], *Q*-factor can be expressed as

$$Q = \frac{\omega L_s}{R_s} \bullet \text{SLF} \bullet \text{SRF}, \tag{2}$$

where SLF is the substrate loss factor and SRF is the self-resonance factor which are given by

$$\text{SLF} = \left[\frac{R_p}{R_p + \left[\left(\omega L_s/R_s\right)^2 + 1\right]R_s}\right], \tag{3}$$

$$SRF = \left[1 - \frac{R_s^2\left(C_p + C_s\right)}{L_s} - \omega^2 L_S\left(C_S + C_P\right)\right]. \tag{4}$$

The parameters, R_P and C_P, in equations (3) and (4) represent the equivalent parallel resistance and capacitance as represented in Figure 1(d) and are given by

$$R_P = \frac{1}{\omega^2 C_{ox}^2 R_{\text{sub}}} + \frac{R_{\text{sub}}\left(C_{ox} + C_{sub}\right)^2}{C_{ox}^2}, \tag{5}$$

$$C_P = C_{ox}\frac{1 + \omega^2\left(C_{ox} + C_{\text{sub}}\right)C_{\text{sub}}R_{\text{sub}}^2}{1 + \omega^2\left(C_{ox} + C_{\text{sub}}\right)R_{\text{sub}}^2}. \tag{6}$$

In equation (5), if R_{sub} approaches either zero or infinity, then R_P tends to become infinity. Hence, the substrate loss factor as given in equation (3) tends to become unity which is essential to stop degradation of the *Q*-factor as per equation (2). This work shorts the R_{sub} by inserting a low impedance metal sheet upon the substrate that acts like ground shield and thus tends to approach zero. This process terminates the penetration of the electric field into the substrate, thus improving the *Q*-factor of the designed

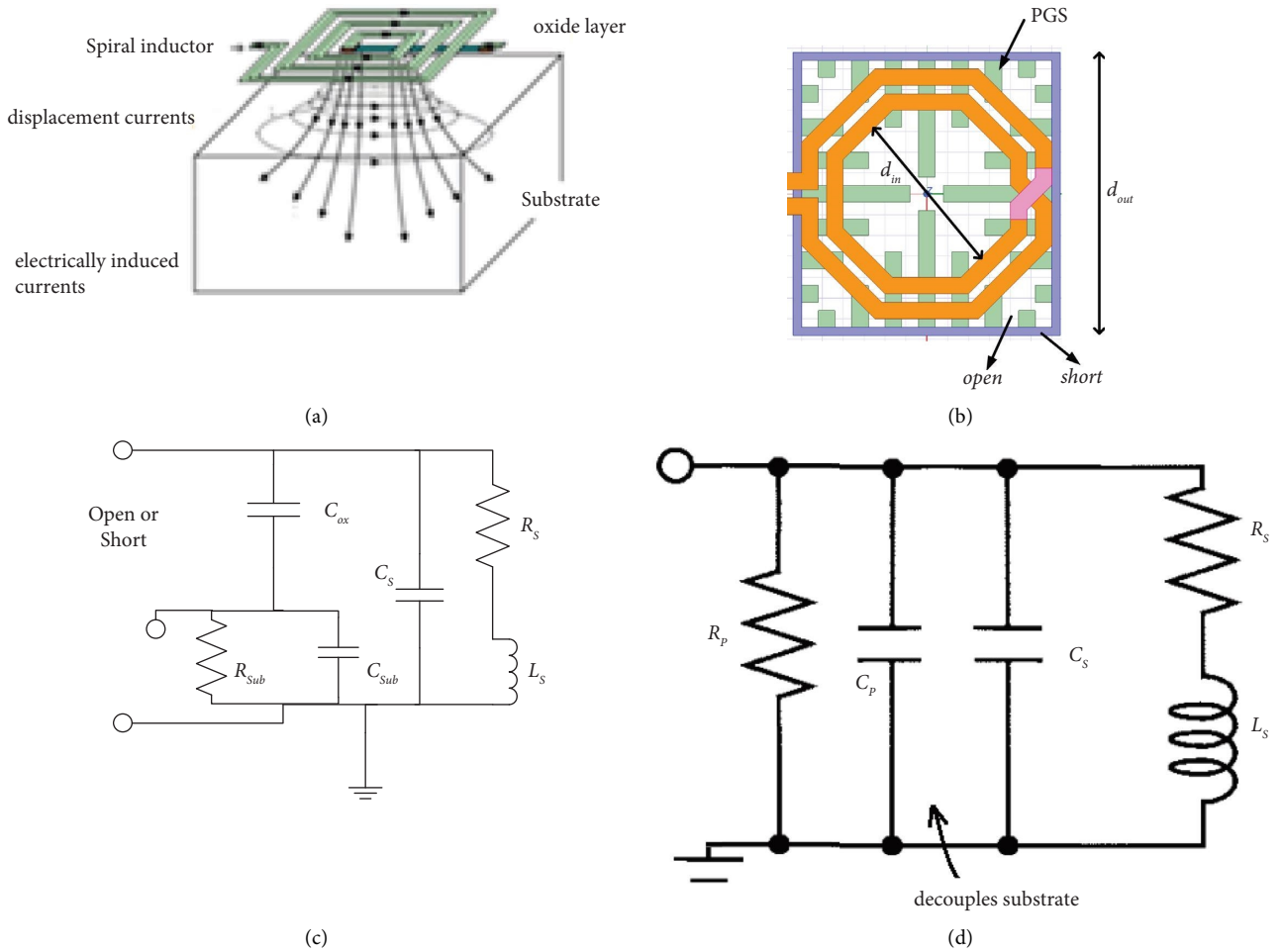


FIGURE 1: On-chip inductor: (a) displacement and eddy currents in the substrate, (b) octagonal inductor, (c) equivalent lumped model, and (d) simplified model.

inductor. This also reduces C_P to reach C_{ox} at higher frequencies as noted in equation (6). However, there exists a finite small resistance on ground shield that still conducts some form of induced currents generated due to inductor field variations. Hence, adding features like patterned ground shields (PGS) is suggested [13, 16] that consists of slots of polysilicon strips built orthogonal to L_S. As shown in Figure 1(b), polystrips are surrounded by vertical metal shield (blue color). The slots serve like open circuit that decouples substrate parasitic from L_S. This results with small series resistance, R_s, on inductor coil, thus reducing the thermal noise generation within it. As per Figure 1(d), without the PGS layer, the impedance looking into an on-chip inductor is given by

$$Z_{\text{in}} = \left(j\omega L_S + R_S\right) \left\| \left(\frac{1}{j\omega C_S}\right) \right\| \left(R_P \left\| \frac{1}{j\omega C_P}\right.\right). \tag{7}$$

With PGS layer, Z_{in} is as follows:

$$Z_{in} = \left(j\omega L_S + R_S\right) \left\| \left(\frac{1}{j\omega C_S}\right). \right. \tag{8}$$

It can be noted that equation (8) decouples the substrate parasitic. At resonance frequency, $\omega = \sqrt{(1/L_S C_S)}$, the real part of Z_{in} reduces to

$$Re\left(Z_{\text{in}}\right) = \frac{L_S}{R_S C_S}. \tag{9}$$

Unlike the real part of equation (7), equation (9) indicates that the input impedance is independent of substrate parasitic such as R_P and C_P. Based on geometric properties of the octagonal spiral inductors, L_s is calculated using current sheet approximation [15].

$$L_s = \frac{\mu\left(N^2\right) d_{\text{avg}} c_1}{2} \left(\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right), \tag{10}$$

where $\rho = (d_{\text{out}} - d_{\text{in}})/(d_{\text{out}} + d_{\text{in}})$, $d_{\text{avg}} = (d_{\text{out}} + d_{\text{in}})/2$ and $d_{in} = d_{\text{out}} - 2Nw - 2(N-1)s$. Here, the inner diameter is "d_{in}," the outer diameter is "d_{out}," the width of the inductor coil is "w," the space distance between the turns is "s," and "N" is the number of turns. For octagonal inductors, $c_1 = 1.07$, $c_2 = 2.29$, $c_3 = 0.0$, and $c_4 = 0.19$ are considered.

The 65-nm technology is explored to fix the geometrical layout of the custom designed octagonal spiral inductor. Substrate height is taken as 400 μm with a conductivity of 1000 S/m. PGS is placed 0.5 μm away from the substrate. To avoid weakening of the magnetic field in L_S, our design uses narrow strips with a thickness of 0.2 μm which is kept lesser than the skin depth of aluminium, that is, 0.334 μm at 60 GHz. Metal1 is chosen with a thickness of 1 μm, while Metal6 and Metal7 are selected with 2 μm thicknesses. Octagonal spirals are designed at Metal7 layer, underpass is designed at Metal6 layer, and Metal1 is used for ground. Three sets of inductors are designed with the inductance values of 210 pH, 150 pH, and 70 pH which are imported to model the LNA circuit. Port parameters are extracted to calculate L_S and Q-factor using the following equations:

$$L_S = \frac{I_m\{1/Y_{11}\}}{\omega};$$
$$Q = \frac{I_m\{1/Y_{11}\}}{R_e\{1/Y_{11}\}}. \tag{11}$$

The EM simulation using full-wave ANSYS HFSS is performed in the frequency range between (50 and 70) GHz. The results of the 210 pH custom designed octagonal inductor are demonstrated here. Figures 2(a) and 2(b) show the vertical penetration depth of electric fields in the substrate with and without PGS, respectively. The electric field penetration is stopped at 140 μm with the PGS inductor, whereas it extends up to 360 μm in its peer.

The respective L_s and Q values are improved as noticed in Figures 3(a) and 3(b). With PGS, the achieved inductance is 208 pH at 60 GHz, whereas it is 199 pH for without PGS. With respect to the reference inductance of 210 pH, ΔL is 2 pH for former, whereas it is 11 pH for later. This shows that the magnetic field present in the inductor with PGS does not interact much with substrate parasitic. Figure 3(a) shows that both inductors have increased inductances with frequency even though they are affected by the skin effect and eddy current loss. This is due to reduced magnetic field interactions with the substrate at higher frequencies. Similarly, in Figure 3(b), the Q-factor observed has been improved from 16.3 to 17.3 in the PGS inductor. This is due to the reduced flow of induced currents in the substrate with PGS. However, at higher frequencies, the Q-factor of both inductors falls which is due to *SRF*. Table 1 presents the extracted parameters such as L_S, Q, equivalent parallel resistance (R_p), equivalent parallel capacitance (C_p), and inductor series resistance (R_s) observed for both with and without PGS inductors. R_p has increased from 1.358 KΩ to 61.4 KΩ with PGS, while C_p reduces to 9.33 fF from 44.27 fF. These are the validating results as per equations (5) and (6) due to the presence of PGS. The inductor series resistance is observed to be 4.78 Ω, a substantial decrease from the inductor without PGS having 807.19 Ω. This proves that the proposed inductor improves the Q-factor and limits the thermal noise generation within it.

From Table 1, it is also found that the proposed work achieves substantial Q when compared with alternative design approaches mentioned in [8, 11]. The added advantage of the PGS structure is that it produces slow wave phenomena on microwave components. In paper [19], a similar PGS structure formed on the ground layer of the microstrip line serves as the resonating component. This is utilized in the design of 60 GHz compact band pass filter, and reports improved insertion loss.

3. 60 GHz Low Noise Amplifier

For LNA implementations, common-source and common-gate topologies are widely used. The former [20, 21] offers high gain and lower *NF* but suffers from the effect of overlap capacitance, C_{gd}, that reduces the gain at mm wave frequencies. The later achieves good matching and wider bandwidth characteristics [22, 23] but at the cost of higher *NF*. Various architectural designs have been executed for improving LNA performance parameters. The cascode topology [24–28] provides high gain and better reverse isolation characteristics, but with the price of voltage headroom reduction, high frequency noise, and offers degraded performance for smaller loads. Several UWB LNAs have been constructed using cascode topology, and in order to extend bandwidth, design of shunt and series peaking inductors have been utilized [29]. To achieve minimum group delay, the series peaking inductor with output resistance termination [30] has been implemented. To reduce the channel noise of the common-gate transistor present in cascode topology, several current reuse methods [30–33] and *gm*-boosting techniques [34] have been reported.

To improve linearity and wide input matching, inverter topology with resistive feedback [29] and capacitive-resistive feedback have been employed in common-source stage [30]. Compared to all the above, this work adopts a 3-stage inductively degenerated common-source structure because it offers more available gain than cascode for medium and small loads at mm wave frequencies. Multistage design [35–38] is utilized in this work in order to compensate the Miller capacitance.

Figure 4(a) shows the circuit of the 3-stage common-source LNA with the inductive degenerative technique applied to the first stage. To increase the gain and noise performance, the low loss, high-Q octagonal inductors presented in Section 2 are utilized in place of L_G, L_S, L_{D1}, L_{D2}, and L_{D3}.

3.1. Input Impedance. The input matching is performed using the gate inductance, L_G, and the source inductance, L_s, in order to cancel the pure capacitive input, C_{gs}, gate-to-source capacitance of M_1. The inherent resistive part, $\omega_T L_S$, is designed to be matching with $Z_{\text{in}} = 50\,\Omega$ [4].

$$z_{\text{in}} = \left(j\omega\left(L_G + L_S\right) + \left(\frac{1}{j\omega C_{gs}}\right) + \left(\omega_T L_S\right)\right), \tag{12}$$

where $\omega_T = g_m/C_{gs}$ is the transit frequency of the device. Since no physical resistor is involved, the *NF* is lower in this configuration. As in Figure 4(a), L_G provides an additional

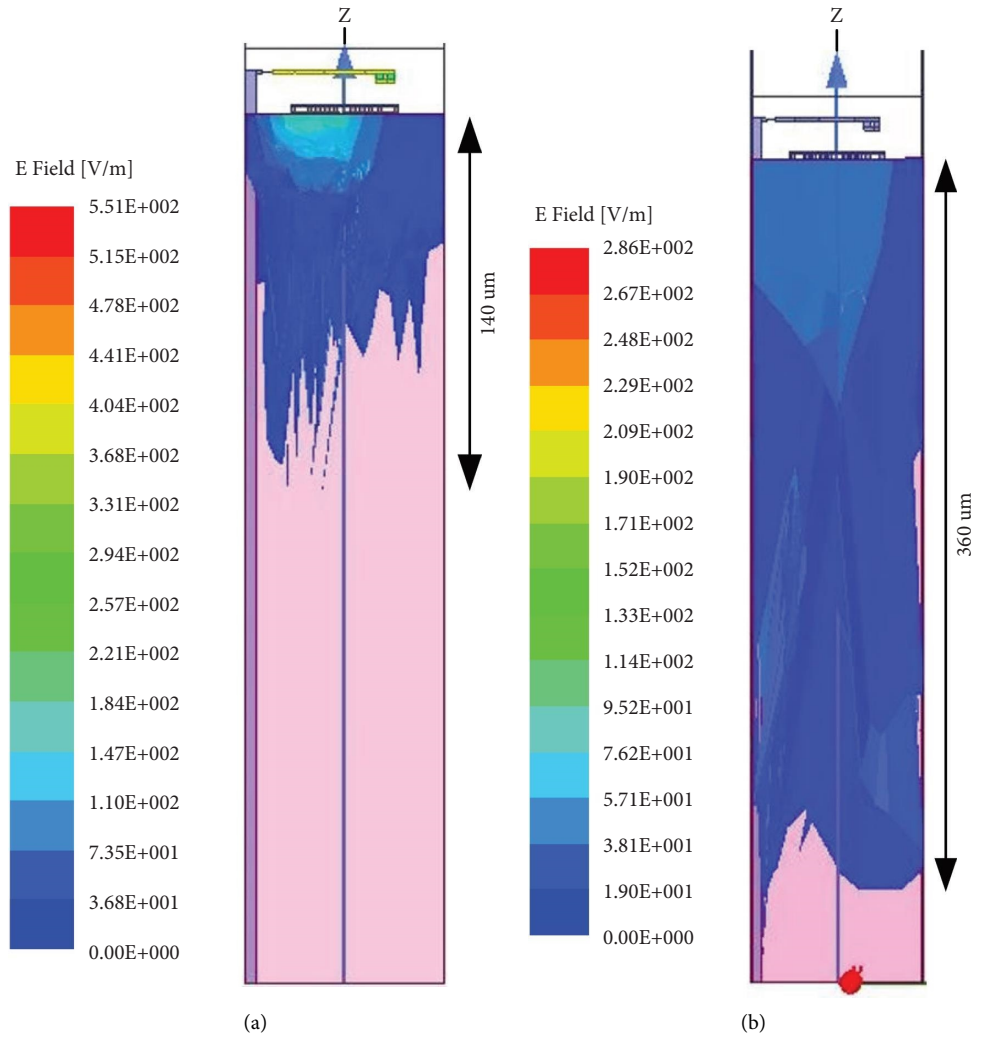


Figure 2: Electric field strength in the substrate: (a) with PGS and (b) without PGS.

degree of freedom for achieving 50 Ω impedance and helps in transforming the resistance upward when seeing through C_{gs}. At resonance frequency, the series circuit formed by L_G, L_S, and C_{gs} increases the signal input voltage, v_{in}, by Q-times. This in turn increases the small signal voltage gain. The Q-factor of the input matching network formed by L_G and L_S with C_{gs} is given by Q_{in}.

$$\begin{aligned} v_{gs1} &= v_{\text{in}} Q_{\text{in}} \\ &= v_{\text{in}} \left(\frac{\omega (L_G + L_S)}{R_{s(\text{LG})} + R_{s(LS)}} \right), \end{aligned} \tag{13}$$

where $R_{s(LG)}$ and $R_{s(LS)}$ are the series resistance of the designed inductors as mentioned in Section 2.

3.2. Input Transconductance and Operating Frequency. The input stage transconductance is given by

$$G_m = g_{m1} Q_{\text{in}}. \tag{14}$$

With inclusion of the resistive part, $\omega_T L_S = R_S$

$$\begin{aligned} G_m &= \frac{g_{m1}}{\omega R_S C_{gs}} \\ &= \frac{g_{m1}}{\omega \omega_T L_S C_{gs}} \\ &= \frac{1}{\omega L_S}. \end{aligned} \tag{15}$$

Here, it is noted that the input transconductance of the circuit is independent of device transconductance which is the advantage of using inductive degenerative technique. The operating frequency is given by

$$\omega = \frac{1}{\sqrt{C_{gs} (L_S + L_G)}}. \tag{16}$$

As per equations (15) and (16), the choice of L_S and L_G determine the values of input transconductance and operating frequency (ω).

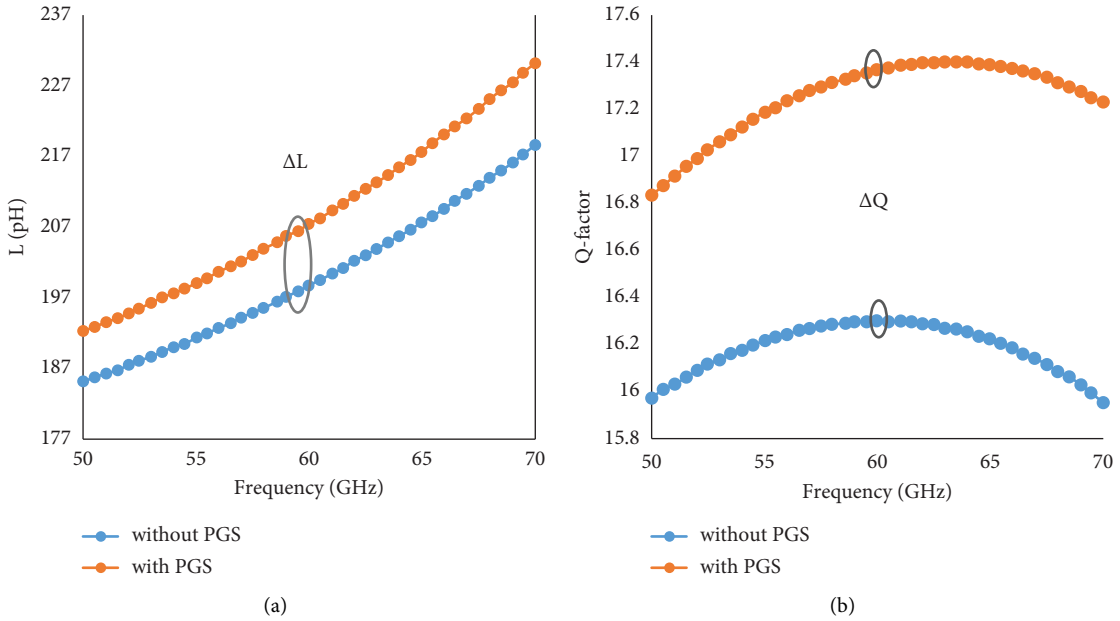


Figure 3: Inductance parameter comparisons: (a) L_s comparisons and (b) Q-factor comparisons.

Table 1: Extracted parameters of the proposed inductors at 60 GHz.

Reference L_s	L_s (pH)	Q	R_p (KΩ)	C_p (fF)	R_s (Ω)
With PGS	208	17.30	61.40	9.33	4.78
Without PGS	199.1	12.06	1.358	44.27	807.2

3.3. Output Node. Here, L_{D1}, L_{D2}, and L_{D3} act as the load inductances for three stages formed by M_1, M_2, and M_3. The second and third stages are designed to achieve high gain. In order to consume low power, the proposed design utilizes transistors with a smaller area. The first two stages use 20 μm multifingered transistors having 1 μm as finger width, while the third stage uses a 40 μm multifingered transistor having 2 μm as finger width. The gate bias voltage of 0.8 V is provided to all stages through resistors, R_1, R_2, and R_3. Capacitors, C_1–C_3, serve as coupling capacitors, while C_4 combined with output capacitance of M_3 resonates with L_{D3} at 60 GHz. The advantage of using an on-chip spiral inductor at the output side is that its series resistance multiplied by Q^2 times provides the required output resistance of 50 Ω at resonance frequency. As shown in Figure 4(b), the effective parallel resistance at load side is constant that limits the output noise power. This property improves the *NF*.

3.4. Gain Analysis. This work presents the two cases of small signal equivalents for the LNA circuit shown in Figure 4. That is, Figure 5(a) gives the small signal equivalent without considering C_{gs} and C_{gd} effects, while Figure 5(b) includes the internal capacitances.

The value of v_{01} in Figure 5(a) is given by

$$v_{01} = -g_{m1}[Q_{\text{in}} \bullet v_{\text{in}}]r_{01}. \tag{17}$$

Using equation (14) in equation (17), we have

$$v_{01} = -G_{m1}[v_{\text{in}}]r_{01}. \tag{18}$$

Similarly, v_{02} at the second stage

$$v_{02} = g_{m2}[v_{01}]r_{02}. \tag{19}$$

The output voltage, $v_{0\text{ut}}$ at the third stage is given by

$$v_{\text{out}} = -g_{m3}[v_{02}]r_{03}. \tag{20}$$

Substituting equations (18) and (19) in equation (20)

$$v_{\text{out}} = -[G_{m1} \bullet v_{\text{in}}]r_{01}g_{m2}r_{02}g_{m3}r_{03}. \tag{21}$$

At resonance frequency, the load inductor resonates with drain capacitance. The load impedances formed by L_{D1}, L_{D2}, and L_{D3} are given as Z_{LD1}, Z_{LD2} and Z_{LD3} at its respective stage. These impedances possess high value ($\approx Q^2R_S$) of resistance at resonance frequency and falls to lower value elsewhere. Therefore, it is appropriate to note that load impedance, Z_{LD}, is proportional to the Q-factor of the component used as load as per Figure 4(b).

$$Z_{LD}\alpha\,(Q * R_s). \tag{22}$$

A_V in terms of load impedances

$$\begin{aligned} |A_V| &= \left|\frac{v_{0\text{ut}}}{v_{\text{in}}}\right| \\ &= G_{m1}g_{m2}g_{m3}Z_{LD1}Z_{LD2}Z_{LD3}. \end{aligned} \tag{23}$$

Substituting equation (22) in equation (23), A_V becomes

$$|A_V|\alpha\,(g_m)^3\,(QR_S)^3. \tag{24}$$

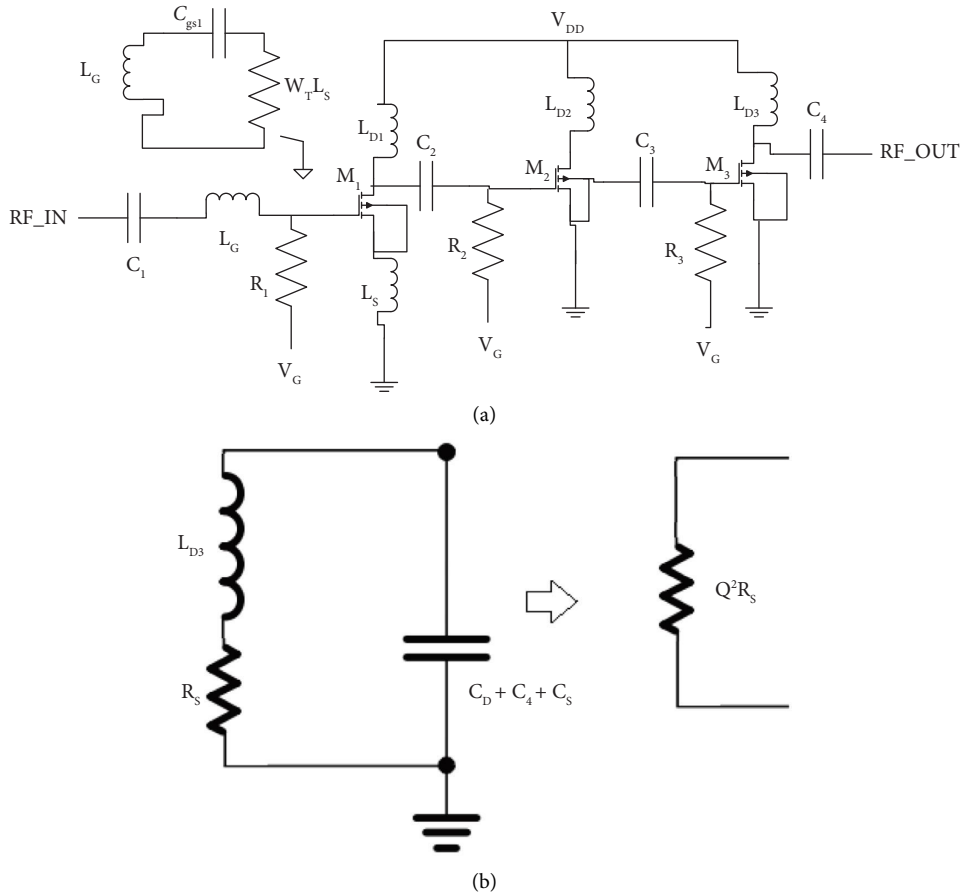


Figure 4: Low noise amplifier: (a) schematic and (b) load inductor at resonance frequency.

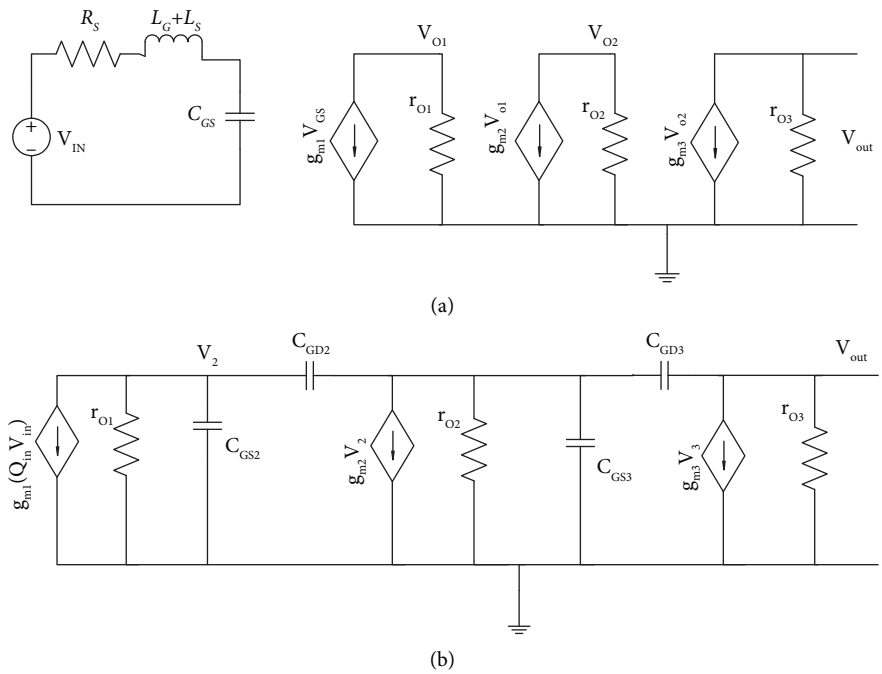


Figure 5: Small signal analysis of LNA: (a) without C_{gs} and C_{gd} effects and (b) with C_{gs} and C_{gd} effects.

In next case, similar analysis is performed by including C_{gs} and C_{gd} effects as in Figure 5(b). The equations at nodes v_2, v_3, and v_{0ut} are given by

$$g_{m1}Q_{\text{in}}v_{\text{in}} + v_2\left[r_{01} + SC_{gs2}\right] = 0, \tag{25}$$

$$g_{m2}v_2 + v_3\left[r_{02} + SC_{gs3}\right] = 0, \tag{26}$$

$$\frac{v_0}{r_{03}} + \frac{v_{0ut} - v_3}{\left(1/SC_{gd3}\right)} + g_{m3}v_3 = 0. \tag{27}$$

From equation (25), v_2 can be written as

$$v_2 = \frac{-g_{m1}Q_{\text{in}}v_{\text{in}}}{r_{01} + SC_{gs2}}. \tag{28}$$

Substituting equation (28) in equation (26) to determine v_3 as follows:

$$v_3 = \frac{g_{m1}g_{m2}Q_{in}v_{\text{in}}}{\left(r_{01} + SC_{gs2}\right)\left(r_{02} + SC_{gs3}\right)}. \tag{29}$$

Substituting equation (29) in equation (27) to get voltage gain as follows:

$$\frac{v_{out}}{v_{in}} = \frac{-G_{m1}g_{m2}g_{m3}\left(1 - \left(SC_{gd3}/g_{m3}\right)\right)r_{03}}{\left(r_{01} + SC_{gs2}\right)\left(r_{02} + SC_{gs3}\right)\left(1 + SC_{gd3}r_{o3}\right)}. \tag{30}$$

It is noted that in equation (30), additional poles are formed due to the transistor parasitic that results in decreasing the voltage gain at higher frequencies. Apart from this, if $r_{o3} = Z_{LD3}$ formed due to on-chip inductors then substituting equation (22) gives the voltage gain as

$$\left|A_V\right| \alpha \left(g_m\right)^3 \left(QR_S\right). \tag{31}$$

From equations (24) and (31) , it is evident that the small signal voltage gain of LNA directly depends on the Q-factor of designed on-chip inductors.

3.5. Noise Figure Analysis. Figure 6 shows the noise model of intrinsic MOSFET consisting of mainly two thermal noise sources, namely, the drain current noise and the induced gate noise [4].

(a) The model of drain current noise is given by

$$\overline{i_{n,d}^2} = \left(4KT\gamma g_{d0}\right)\Delta f. \tag{32}$$

Here, γ is the bias dependent parameter that takes unity at zero V_{DS} and decreases to 2/3 in saturation. g_{d0} is the drain-to-source conductance at zero V_{DS}, and Δf is the noise bandwidth.

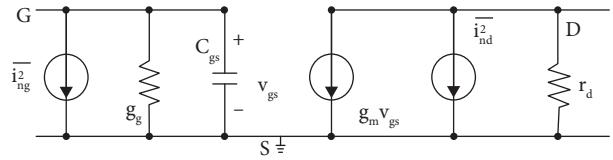


Figure 6: MOSFET noise model.

(b) The induced gate noise is generated due to fluctuating channel potential which is coupled to gate terminal. This is given by

$$\overline{i_{n,g}^2} = \left(4KT\delta g_g\right)\Delta f. \tag{33}$$

Here, the gate conductance is given by $g_g = \left((\omega C_{gs})^2/5g_{do}\right)$ and δ is the bias dependent parameter that takes 4/3 for long channel devices.

(c) The third type of noise source available in the circuit is due to inductive load resistance (R_S) formed due to the on-chip inductor, L_D. The input mean square noise current due to R_S is given by

$$\overline{i_{n,R_S}^2} = 4KT\left(\frac{1}{R_S}\right)\Delta f. \tag{34}$$

As per Figure 4(b), at resonance frequency, the load resistance appears parallel with its equivalent value as $\approx R_S Q^2$.

Noise figure (NF) is given by

$$\text{NF} = \frac{\text{Total output noise power}}{\text{Noise power due to input source}}. \tag{35}$$

The output noise powers available at LNA due to input noise sources represented from equations (32)–(34) are given as follows:

$$\overline{i_{o,d}^2} = \left(4KT\gamma g_{d0}\right)\Delta f * R_L^2, \tag{36}$$

$$\overline{i_{o,g}^2} = \left(4KT\delta g_g\right)\Delta f * R_L^2, \tag{37}$$

$$\overline{i_{o,R_S}^2} = \left(4KT\left(\frac{1}{R_S}\right)\right)\Delta f * R_L^2. \tag{38}$$

The output noise power due to source resistance, R_{sou}, is given by

$$\overline{v_{o,R_{sou}}^2} = \left(4KTR_{sou}\right)\Delta f * \left(G_{m1}^2 R_L^2\right). \tag{39}$$

Substituting equations (36)–(39) in equation (35)

$$NF = 1 + \frac{\gamma}{g_m R_{sou} Q_{in}^2} + \left(\frac{\omega}{\omega_T}\right)^2 \frac{1}{5 g_m^2 R_{sou} Q_{in}^2} + \frac{1}{g_m^2 R_{sou} Q_{in}^2 \left(R_S Q^2\right)}. \quad (40)$$

In equation (40), after unity, the first term is due to drain current noise, the second term is due to induced gate current noise, and the last term is due to inductive load resistance formed by the on-chip load inductor. It is observed that *NF* can be improved by increasing Q_{in} and Q as given in equations (14) and (22) of the proposed inductor.

4. Results and Discussion

The designed LNA uses UMC 65-nm CMOS technology by selecting low leakage RF transistors. The circuit is constructed in Cadence Virtuoso Environment, and simulations are performed in the Spectre simulator. To validate the performance of proposed PGS octagonal inductors presented in Section 2, the first stage uses 210 pH, 70 pH, and 210 pH inductors at gate, source, and load side, while the second and third stage use 150 pH and 210 pH as load inductors, respectively. For comparison purpose, test LNA is designed using ideal inductors which are equivalent to off-chip inductors.

The performance comparison of both LNAs is shown in Table 2. It is observed that LNA with proposed octagonal spiral inductors achieves a peak gain of 17.02 dB at 56 GHz while producing a substantial gain of 15.74 dB at 60 GHz with the respective *NF* of 5 dB, which is comparatively better than the LNA with equivalent off-chip inductors. The netlists used for the equivalent off-chip inductors have been selected from the analog library that possesses the finite *Q*-factor. This value has been chosen to be equal to the achieved *Q*-value of the PGS inductors as shown in Figure 3(b). This by default produces its own effect on circuit performance. Thus, the equivalent off-chip inductors are made little more realistic so that the LNA performance using the proposed PGS-based inductors has been compared against it and listed in Table 2. The 3-dB bandwidth is found to be 11 GHz observed from 53 to 64 GHz. The reflection coefficients, S_{11} and S_{22}, are −12 dB and −11 dB, respectively, at 60 GHz, while the reverse gain, S_{12}, is −43.2 dB. The plots of S_{21}, S_{11}, S_{22}, and *NF* of LNA using custom designed inductors are shown in Figures 7(a) to 7(c).

The circuit draws the DC current of 10 mA from a 1 V supply voltage leading to power consumption of 10 mW only. The design achieves unconditional stability with $K_f > 1$ and $B_{1f}(\Delta) < 1$ from 50 to 70 GHz frequency range [4].

The *FOM* of LNA employing PGS octagonal inductors is 14.56, while its peer using off-chip analog library inductors is 7.747 as per the following equation:

$$FOM = \frac{\text{Gain}\,(abs) * f_c\,(GHz)}{(NF - 1)\,(abs) * P_{DC}\,(mW)}. \quad (41)$$

That is, *FOM* of the proposed work has increased by 0.8 times. Table 3 shows the performance comparison of the proposed work with the simulated results of the state-of-the-art LNAs available at 60 GHz. The reported simulated results listed in this table have been collected from the works based on 65-nm CMOS technology designs, and hence, we have compared our results with their respective *FOM*s.

Table 4 shows the comparison of our results with the average results of other reports. Though we followed different methodologies, the second and third columns consolidate average gain and *NF* of the measured data of other reported results [26, 27, 32, 34–38] available at 60 GHz and presented as 16.6 dB and 4.95 dB, respectively. The respective results of our work have been noticed as 15.7 dB and 5 dB which are quite close with the reported average values. Though our results presented are from the simulation environment, if when fabricated, our work also stands close to the reported measured results. This proves our work's suitability for the problem at hand. The following section explains the layout of LNA using the footprints of custom designed inductors designed at 60 GHz and its results.

First, the layout of the custom designed inductor structure is obtained, and its performance has been presented in Figure 8 over 50–70 GHz. Figure 8(a) shows the insertion loss (S_{21}) which is observed to be close to −0.55 dB and S_{11} value which is less than −30 dB at 60 GHz. This shows that the designed inductor footprint maps properly with layer stack. The far field and current visualization have been observed at 63.33 GHz. From Figure 8(b), the observed electric field is 1.56×10^3 V/m and we presented the entire lobe at the mentioned frequency. Figure 8(c) shows the current distribution which is visualized from port 1 to port 2. Also, parameters such as inductance, resistance, capacitance, and equivalent *Q*-factor have been extracted at 60 GHz which are as follows: 266 pH, 10.3 Ω, 7.4 fF, and 9.73, respectively.

Next, the layout of a single-stage amplifier is designed using the presented custom designed inductor footprint serving as gate inductance, source inductance, and load inductance. The schematic of it is presented in Figure 9(a) in which the numbered icons such as 1,2, and 3 indicate the mapped footprints of custom designed inductors. Figure 9(b) shows the 2-D view of the schematic presented in Figure 9(a). Here, the substrate stack-up layers have been added by selecting "Rogers_RO4350" as the base substrate. Also, the port calibration is performed at probing points such as input, output, and supply and ground nodes by inserting appropriate pins. Further processing is conducted after ensuring the placement of pins upon appropriate layers. Routing is performed to follow up the right trace among the nets such as components, pins, custom designed footprints, and substrate. A similar procedure is conducted in all three stages, and the complete layout for 3-stage LNA design is presented in Figure 9(c). Port calibration is once again checked, and appropriate mesh generation has been performed to invoke full wave EM simulation over the frequency range from 50 to 70 GHz. The *S*-parameter results of the

Table 2: Comparison of LNA performance using the proposed on-chip inductors with off-chip inductors.

LNA at 60 GHz	Gain (dB)	*NF* (dB)	Power (mW)
PGS octagonal inductors	15.74	5.0	10.0
Off-chip inductors	15.5	5.5	13.9

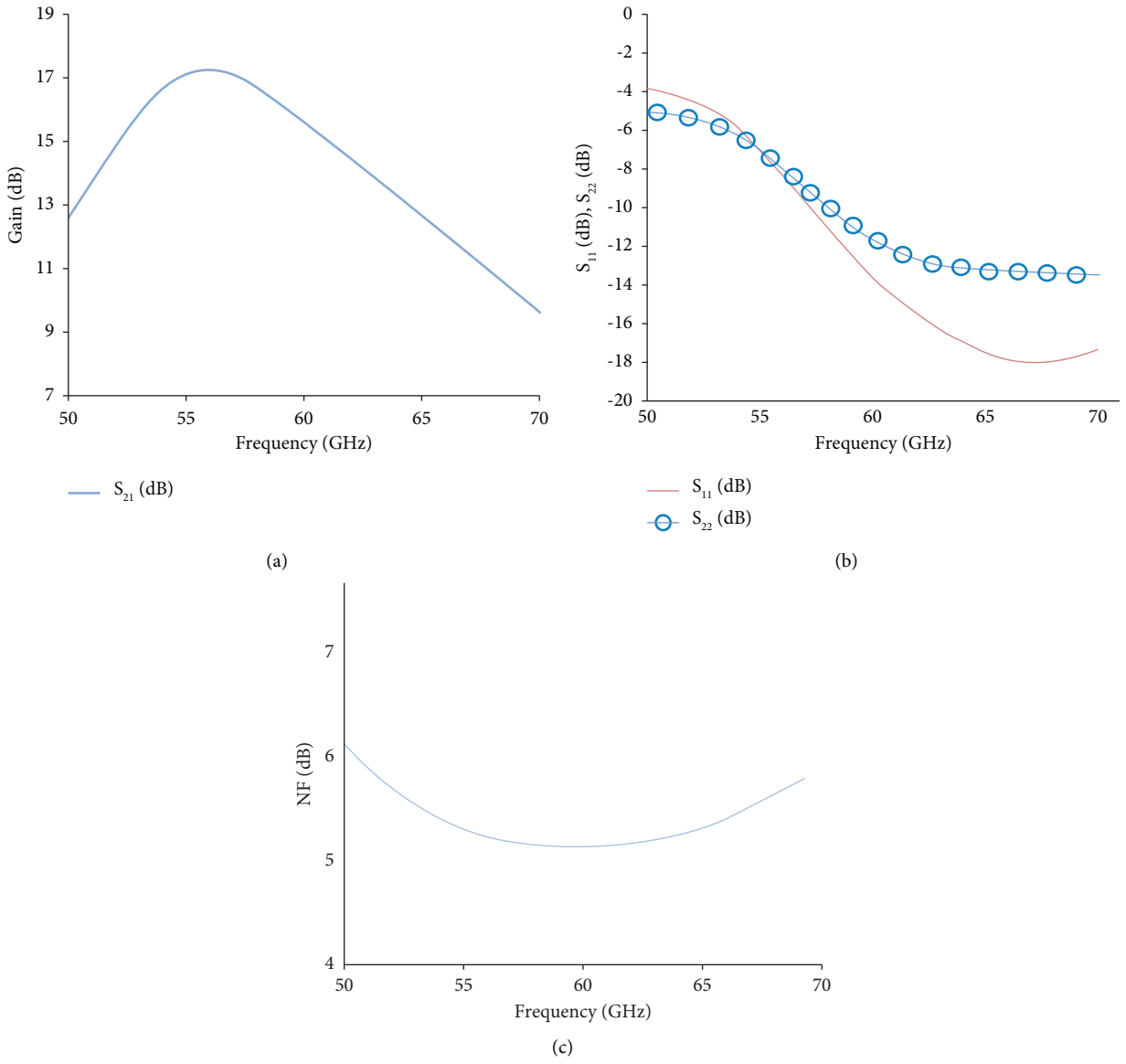


Figure 7: Results of LNA using PGS octagonal inductors: (a) S_{21} plot, (b) S_{11} and S_{22} plots, and (c) *NF* plot.

complete LNA layout are presented in Figure 10. The corresponding S_{11}, S_{22}, and S_{12} are found to be <−8 dB, <−11 dB, and <−22 dB over the frequency range of 57–64 GHz. The forward gain is observed to be >10 dB at 60 GHz. It is found that the reduced gain is due to the availability of inaccurate models used in simulation. However, the S-parameter results in Figure 10

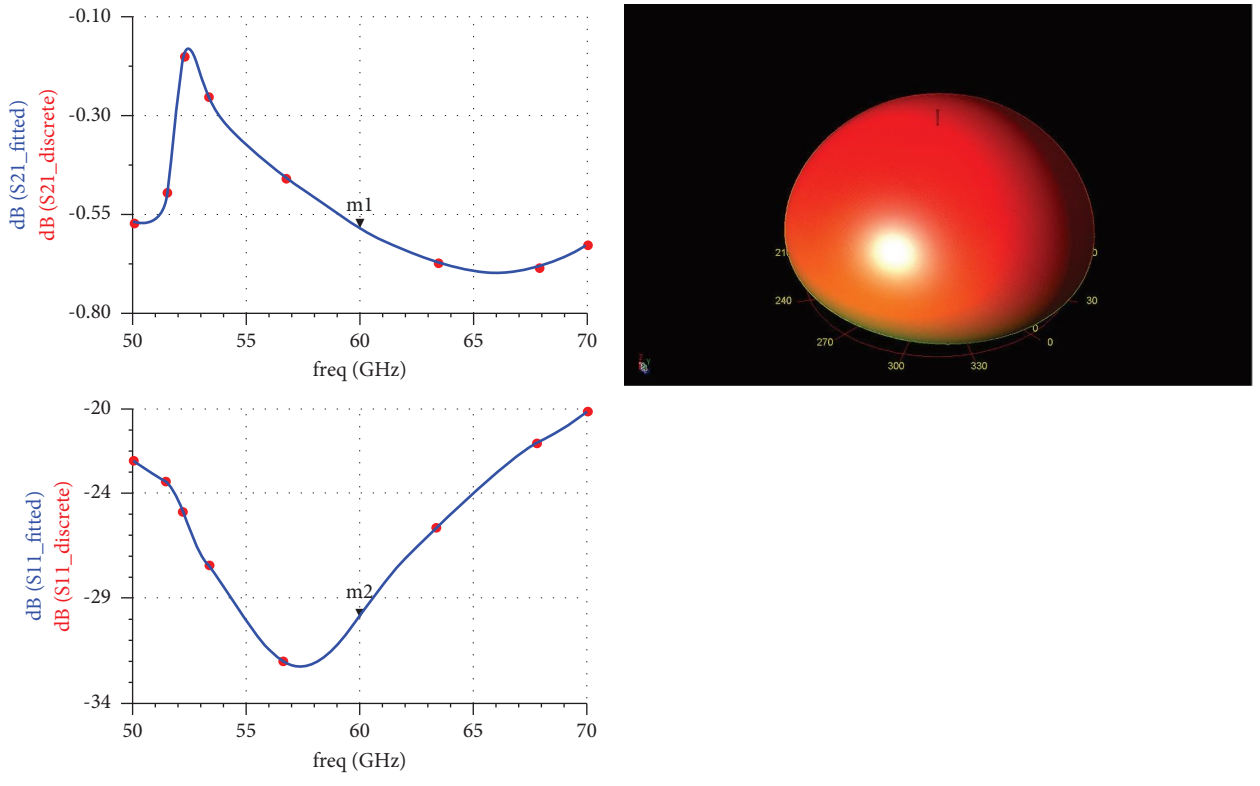
Table 3: Comparison with reported results.

Reference, year	Center freq. (GHz)	3-dB BW (GHz)	Gain (dB)	*NF* (dB)	S_{11} (dB)	S_{22} (dB)	DC power (mW)	*FOM*
[27], 2008	59.3	7.7	22.3	6.1	−12	—	35	4.828
[31], 2011	58.3	—	16.8	5.2	—	—	11	11.073
[35], 2012	55–67	12	10.8	3.8	<−7	<−20	35	2.3
[24], 2013	58.5	4.5	22	5	−20	—	27.9	3.066
[20], 2015	60	9.5	*NA*	4.6	−7.5	−10	8.9	*NA*
[38], 2015	58	7	18	4.9	<−10	<−10	20	7.454
[34], 2016	50.1–57.9	7.8	28	3.8	<−15	<−15	19.8	21.17
[21], 2016	62.9–67	4.1	33	4.7*	<−10	<−7	6	136.32
[36], 2018	57	17	22.3	5	<−7	<−10	36	6.524
[26], 2019	55–64	9	13.2	3.6	<−25	<−15	8.8	13.64
[37], 2020	53.5–61	7.5	23	4.8	<−10	<−10	25**	3.844
[39], 2020	57.1	10.94	17.4	4.1	<−10	<−10	10	21.45
This work (LNA with PGS inductors)	60	11	15.7	5	−12	−11	10	14.56
(With off-chip inductors)	60	11	15.5	5.5	−12	−11	13	7.747

NA: not available; *NF_{min} is considered; **min. dc power.

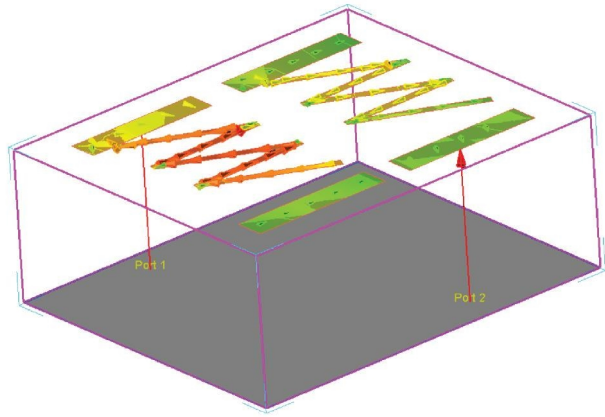
Table 4: Comparison with other reported simulation results at 60 GHz.

Work	Gain (dB)	*NF* (dB)
Average [26, 27, 32, 34–38]	16.6	4.95
This work (PGS octagonal inductors)	15.7	5
This work (off-chip inductors)	15.5	5.5



(a) (b)

Figure 8: Continued.



(c)

Figure 8: Parameters observed from layout of the custom designed inductor: (a) insertion loss (S_{21}) and S_{11}, (b) far field, and (c) current distribution from the input port to the output port.

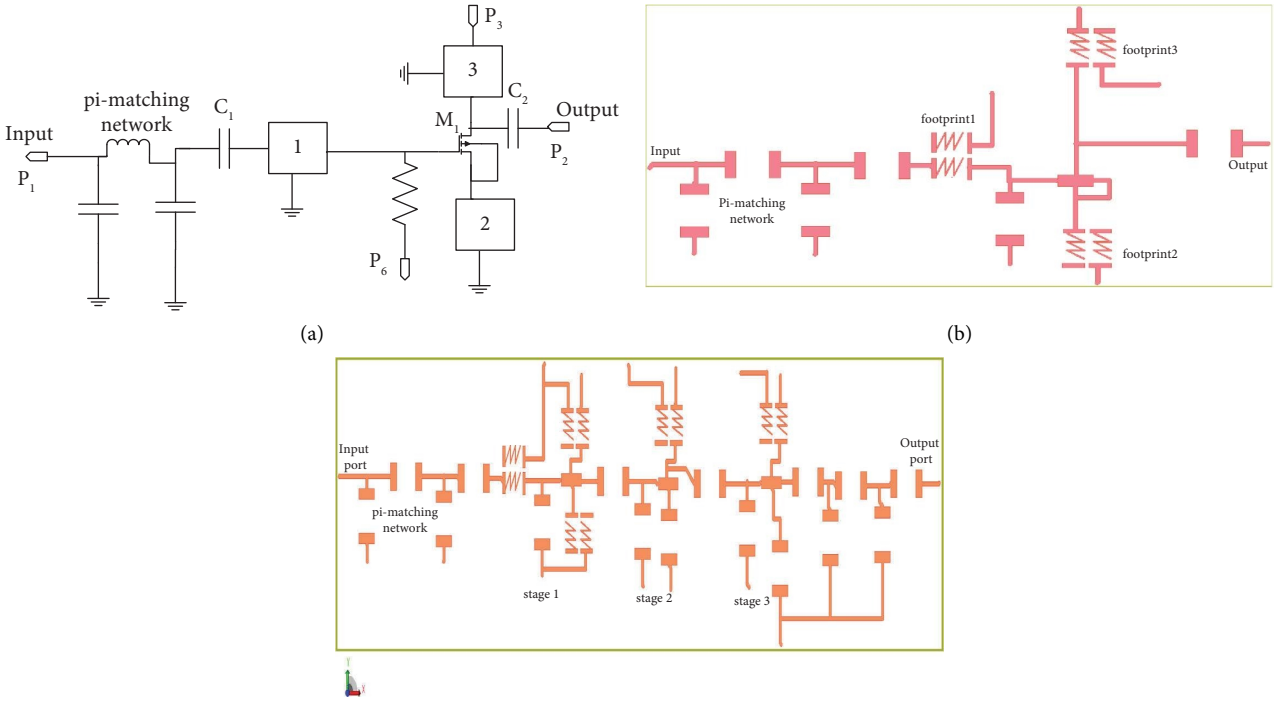


Figure 9: (a) A single-stage LNA schematic with custom designed inductors and pi-matching network, (b) layout of 2-D single stage LNA with embedded inductor footprints, and (c) complete 3-stage LNA layout.

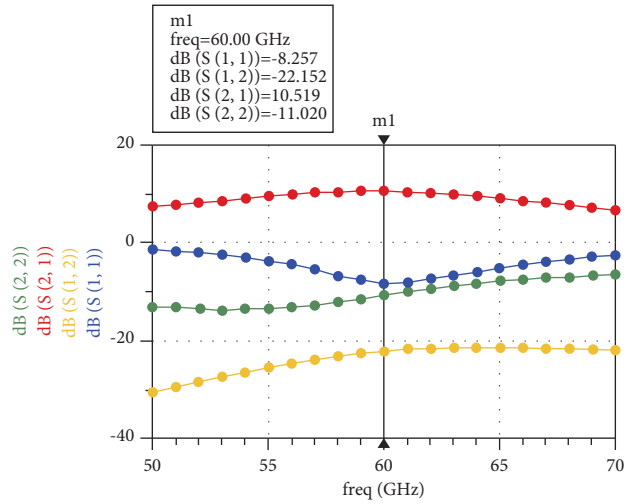


Figure 10: *S*-parameters of complete 3-stage LNA layout.

ensure that the complete LNA layout works in compatibility with the embedded custom inductor footprints designed at 60 GHz.

5. Conclusions

The design and performance analysis of 60 GHz LNA implemented using custom designed inductors has been presented. Based on the investigations conducted for reducing substrate loss, this work uses the patterned ground shield layered upon the substrate of octagonal spiral structures. It results with a significant improvement in the *Q*-factor and minimal thermal noise generation. Detailed analysis of small signal voltage gain and noise figure has been presented relating with the *Q*-factor of the proposed inductors. The designed LNA achieves a power gain of 15.7 dB at 60 GHz, the minimum noise figure of 5 dB, and a 3 dB bandwidth of 11 GHz from 53 to 64 GHz with 10 mW power consumption only. A complete layout of LNA along with custom designed inductor footprints has been analyzed and verified for both EM and circuit properties. These results provide staunch support for the effectiveness of the proposed work in 60 GHz receiver designs and can be extended to include electrostatic discharge (ESD) protection circuit for reliability.

Data Availability

The *S*-parameter data used to support the findings of this study are included within the article.

Disclosure

This research has been performed as part of academic progress towards Ph.D. of one of the authors. All authors are affiliated to Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Amrita Nagar (Post), Coimbatore, Pin code-641 112, India.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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