Hindawi
Journal of Electrical and Computer Engineering
Volume 2023, Article ID 5182455, 10 pages
https://doi.org/10.1155/2023/5182455

Research Article

Four-Channels High-Resolution Frequency Counter for QCM Sensor Array Using Generic FPGA XC6SLX9 Board

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Received 13 December 2022; Revised 14 April 2023; Accepted 18 April 2023; Published 9 May 2023

Academic Editor: Jit S. Mandeep

A frequency counter is essential for resonance-based sensors like quartz crystal microbalance. An electronic nose or tongue using a QCM sensor array requires a multichannel frequency counter to detect the frequency shift of the sensors simultaneously. The frequency counter's resolution, precision, and sampling speed are important factors. Board size, energy consumption, and rapid deployment are also considered in the design. This work shows the development of an independent multichannel frequency counter using a commercial Xilinx Spartan 6 series XC6SLX9 board module and a microcontroller board. Both modules are general-purpose modules; therefore, there is no need for a printed circuit board design, resulting in a quick implementation: the use of FPGA results in a compact size and low energy consumption. The developed counter is designed based on a reciprocal counter utilizing the internal logic block of the FPGA. The FPGA module has a built-in 50 MHz TCXO clock and is the reference clock. The high-resolution timing of the counter is realized by multiplying the 50 MHz clock by 6 to reach 300 MHz. The multiplication utilizes the PLL modules in the FPGA. The high precision and accuracy of the counter are achieved by calibrating the timing clock to a 10 MHz rubidium oscillator. The data communication to the microcontroller is done via the SPI by implementing the SPI protocol in the FPGA. The resource is optimized by utilizing PLL and DSP blocks for the counter. Only 5% registers and 5% LUTs of the FPGA resource are used to build a four-channel frequency counter. The result shows that the counter can measure the frequency of incoming signals with a resolution of 0.033 Hz at 10 MHz with a sampling time of 1 second. The system has been tested to monitor the frequency changes of a QCM sensor array.

1. Introduction

As a mass-sensitive sensor, the quartz crystal microbalance (QCM) works on the principle of frequency shift. The sensor's resonance frequency changes according to the amount of the absorbing or desorbing molecule on the sensor surface [1] or by other influences such as force [2, 3], friction [4], and others. A frequency counter is used as a data acquisition system. The frequency counter is developed using discrete electronic components [5], the microcontroller [6], CPLD [7], FPGA [8], or a combination of them [9]. These days, CPLDs or FPGAs are preferred because they have high-density logic components, are flexible to configure, and are small in size, so they do not take up PCB space and consume a small amount of energy.

For many measurements, the frequency counter's resolution is essential to enable the high sensitivity of the QCM sensors [10]. The high-resolution means that small frequency changes can be detected. There are many methods that have been developed to obtain a high-resolution frequency counter by using high-frequency reference clock [11], FFT [12], TDC [13, 14], and others. However, the selection of this method needs to be selected by the application and capabilities of the device used. The method

commonly used is the conventional method [15] or reciprocal [16]. Both methods are very favorable to be applied in digital circuits.

The development of QCM sensors as an electronic nose [14] or electronic tongue [15] requires a multiple-frequency counter to measure the frequency shift of each sensor. Sensor arrays require many sensors and nearly simultaneous sampling [17]. Multiple counter devices can measure the electronic nose or tongue sensor array. Another method uses an electronic switch [18] or multiplexer [19]. Multichannel counters mean more signal paths in the circuit and potentially create new challenges and complexities due to interference (crosstalk) and logic timing, especially signals in the MHz order [20]. That problem also arises in developing the multichannel frequency counter using FPGA.

Multichannel measurement on the microcontroller utilizes the existing timers [6]. However, the channel number is limited by the available timers. In addition, it only works with a conventional method using the timers as time gates. The timer on the microcontroller works with different frequencies and resolutions as its works serially. The development of FPGA devices has many advantages. Its processing units can be performed in parallel according to the basic architecture of the FPGA. Conventional methods with multiple channels can also be applied to FPGAs [20]. Several studies have shown that this method can achieve high-resolution [21].

This paper presents the development of 4 input channels frequency counter with a resolution better than 1 Hz for 1 second sampling time. The counter consists of four independent reciprocal counters that work in parallel. Each counter works independently with a separate up counter for the reciprocal timing determination. Signal synchronization between the timing and measured signals was done locally on each counter. The system was developed using available general purposes FPGA board and microcontroller board modules in the market.

2. Materials and Methods

The components used are FPGA Spartan 6 XC6SLX9 and STM32F103C microcontroller. The Spartan 6 used is a general-purpose development board. The STM32F103C is a generic microcontroller board. Both are available in the market, as depicted in Figure 1. This board has a minimum system and a TCXO crystal oscillator with a frequency of 50 MHz. The FPGA is configured for the reciprocal counter, and the microcontroller works as a data processing and communication interface to a personal computer. The FPGA is configured using Xilinx ISE Webpack, and the microcontroller is programmed using Arduino IDE.

The block diagram of the system is presented in Figure 2. In the FPGA board, reciprocal counters and SPI communication is implemented. The counted data in the common counter are sent to the microcontroller via SPI communication. The microcontroller receives the data, processes the digital data, and sends the data in frequency values to the host computer.

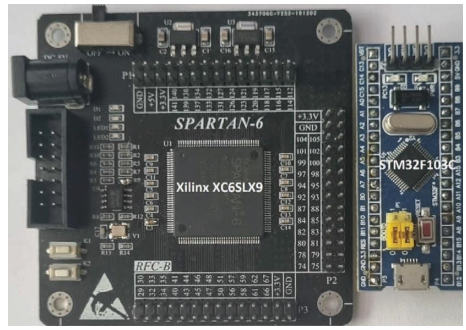

Figure 1: FPGA board and microcontroller board.

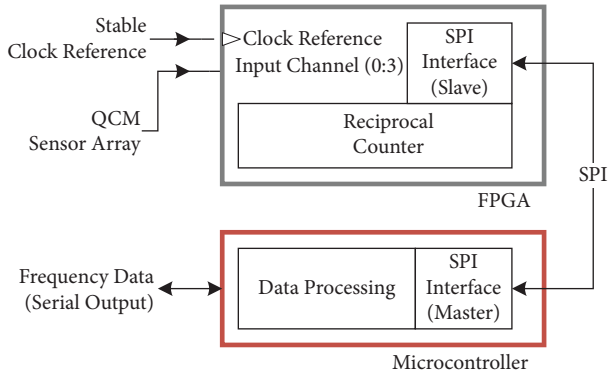

Figure 2: Block diagram of FPGA and MCU.

The reciprocal time counter diagram is shown in Figure 3. The reference clock determines the time interval used in calculating the frequency. The time intervals are determined using an internally generated 300 MHz reference clock derived from an external 50 MHz clock. The multiplication uses a PLL on the Xilinx XC6SLX9 to generate a 300 MHz clock. The time interval setting is calibrated with a 10 MHz rubidium oscillator. The calibration aims to set the counter value on the reference clock counter to determine the time interval for the time gate signal. The reference clock counter is sent from the FPGA to the microcontroller for frequency calculation.

The input signal and the reference clock signal are calculated in the time gate signal intervals. The sync gate of each counter signal synchronizes the frequency count. The counter starts once the time gate is high and the first rising edge of the input channel signal is encountered. This input signal's first rising edge event triggers a transition of the sync gate signal to high. When the sync gate signal is high, the reference clock counter starts counting the reference signal, and the input line counter starts counting the input channel signal. At the end of the enumeration period, the input channel counter and reference clock counter result values are sent to the microcontroller via SPI communication. The microcontroller calculates the frequency value based on the counter value received from the input signal and the reference signal.

Each channel has two counter data, i.e., the reference clock and the input signal value. The frequency calculation of

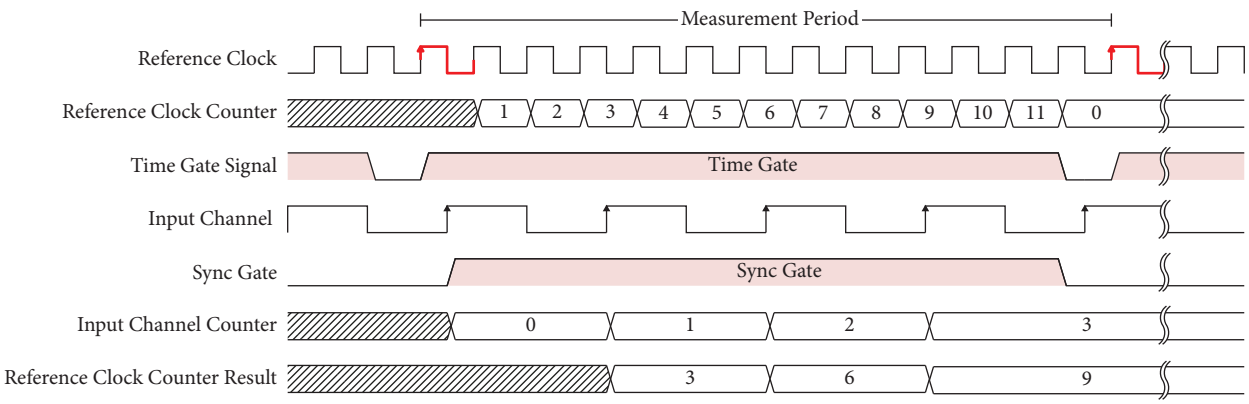

Figure 3: Reciprocal time counter diagram.

the incoming signal from the QCM oscillator is carried out using the following equation:

$$f_{\text{input}} = \frac{N_{\text{input}}}{N_{\text{ref}}} \bullet f_{\text{ref}}. \quad (1)$$

The f_{input} value is the calculated frequency of the QCM oscillator. The N_{input} is the signal from the QCM oscillator, and the N_{ref} is the counted from the reference clock. The f_{ref} value is the reference signal frequency used in the reciprocal block, calibrated to 300 MHz.

The system's hardware is implemented using Xilinx XC6SLX9 FPGA board, STM32F103 board, and UART to USB module. The pin connection among the modules is presented in Figure 4. Only four digital I/O connections exist between the FPGA and microcontroller boards. Pins 45, 47, 50, and 56 are selected. The global clock at Pins 124, 126, 133, and 134 is connected to the input signal from the QCM sensor oscillator output. Measurement data are sent via UART to the CH340 serial USB module.

3. Results and Discussion

3.1. Counter Design. A VHDL code has been developed in the XILINX ISE Webpack. The program consists of four digital blocks and is presented in the ISE Webpack in the top view in Figure 5. The blocks are *reference clock*, *time gate*, *reciprocal counter*, and SPI. The reference clock multiplies the 50 MHz signal from the external oscillator (TCXO) to the internal clock of 300 MHz and 100 MHz. The PLL circuit inside the FPGA performs multiplication. The reciprocal counter uses the output signal 300 MHz, while the Time Gate module uses the 100 MHz to generate a one-second signal. The reciprocal counter block (consists of four identical blocks) counts the upcoming signal within the one-second time gate. The counter value of the measured signal and reference clock is sent to the SPI. The SPI module communicates with the external microcontroller.

The one-second time gate is only used to generate a sampling rate of approximately one second for the acquisition. A sampling rate inaccuracy of 10–100 ns from one second is adequate for typical QCM sensor data acquisition. The time gate module is an up counter which counts the incoming signal from the generated clock of 100 MHz. The VHDL code for the time gate is presented in Figure 6. The RTL schematic generated by the XILINX ISE Webpack of the time gate is shown in Figure 7. The counter starts from zero up to a number around 100000000 to reach one second. The exact number of the counter is determined by calibrating it to the 10 MHz Rubidium oscillator. The timing diagram of the time gate module is presented in Figure 8.

The RTL schematic diagram of the reciprocal counter is presented in Figure 9. The main element of the reciprocal counter is an up counter for the incoming signal (CH_CLK) and an up counter for the reference clock (300 MHz) (REF_CLK). Every reciprocal counter consists of two up counters; each up counter uses the 32 bits DSP48 in the FPGA. A synchronizing gate is added in the diagram to control both counters. The timing diagram of the reciprocal counters is presented in Figure 10. The counter starts when the time gate signal is high and the sync gate signal is rising. The counting ends when the Sync Gate is falling and the time gate signal is high. The counting values are sent to the microcontroller via the SPI module block.

The four reciprocal counter blocks work using a single reference clock. It ensures the system has identical implementation results for each channel and works in parallel. This design is implemented on Spartan using Xilinx ISE. VHDL design is synthesized with balanced optimization. The floor plan of the system is presented in Figure 11. It can be seen that the whole system only occupies one-fourth of the available block. The reciprocal counter is placed in the two clock region, i.e., X0Y1 for counter channels 3 and 4 and X0Y2 for channels 1 and 2.

The used resources of the FPGA are presented in Table 1. The registers and LUTs (Look Up Table) occupy only 3% and 5% of the FPGA capacity, respectively. The Spartan XC6SLX9 has 16 DAP48 slices; eight are used in this implementation. The PLL resources are used 50% of the FPGA capacity. It means there is still much room to add other functionality or counter.

3.2. Counter Testing. The counter was tested using a VCOCXO and QCM sensor made of a 10 MHz Quartz Crystal resonator. Each source was split into four channels, i.e., Channel 1, Channel 2, Channel 3, and Channel 4 of the counter. The VCOCXO oscillator is the 10 MHz OX200-SC

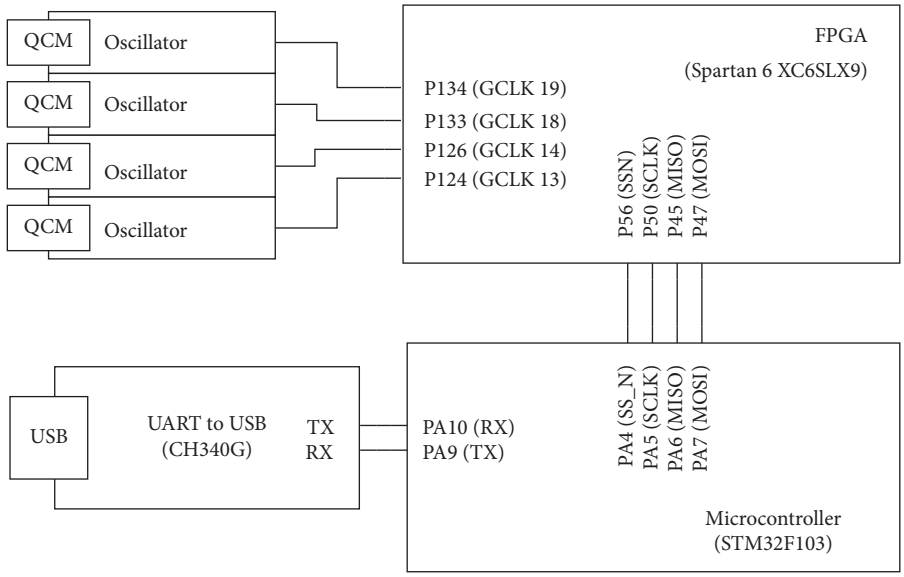

Figure 4: Board module connection.

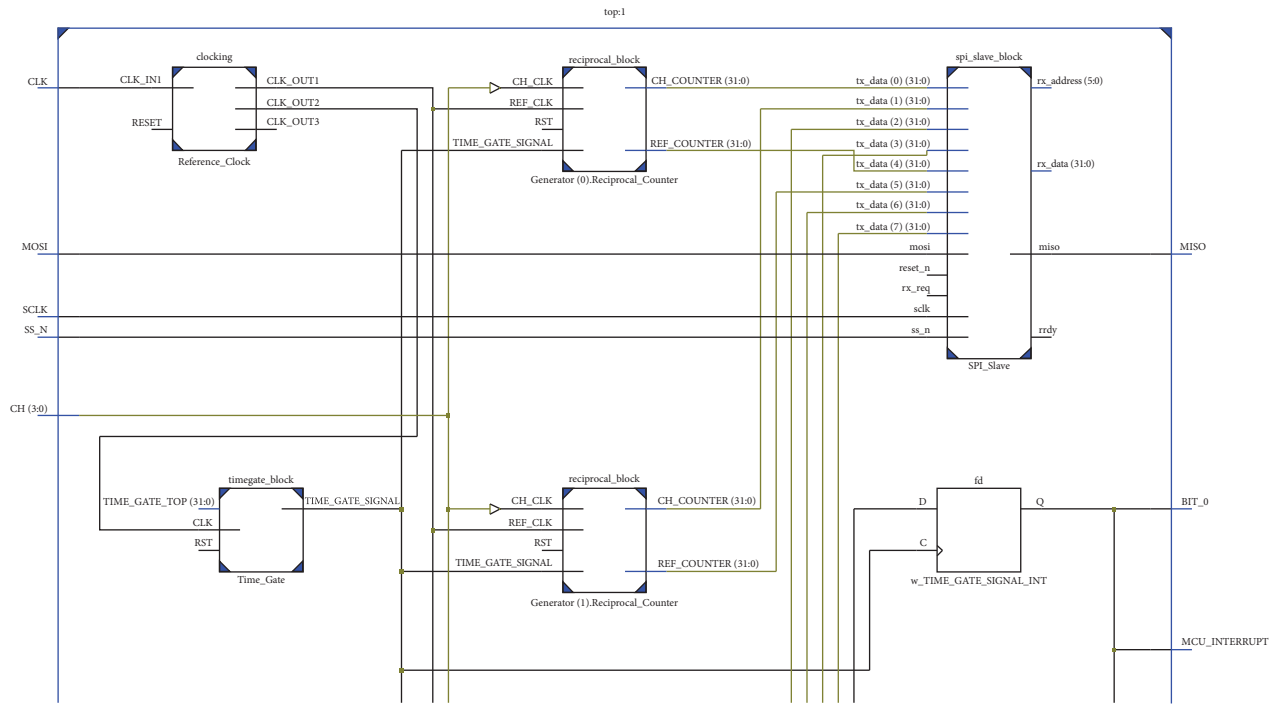

Figure 5: Schematic diagram of the one-second counter.

(Connor Winfield) with a center frequency of 10 MHz, an accuracy of 25 ppb, and a frequency to the temperature stability of 1.5 ppb. The recorded data are presented in Figure 12. The graphic image shows a resolution of the frequency measurement of 0.033 Hz, as expected.

For each channel, the average frequency of VCOCXO is 10000000.12 Hz, and the recorded frequency varies from 10000000.07 Hz to 10000000.20. There is no significant frequency difference among the frequency counter. The maximum difference among the four channels is 0.033 Hz; i.e., the frequency resolution differs from one clock reference signal of 300 MHz. The difference is due to the rounding error of the reciprocal method and the signal propagation delay from each counter which works independently without clock synchronization among four counters. This result is better than the other approach [22].

Figure 12 shows the occurrence of the measured frequency of the incoming signal. The frequency of each channel is presented in a different color, i.e., black, red, green, and blue, with the blue color (Channel 4) presented in

```
entity fi_timegate_var is
        port (
                RST                             : in std_logic;
                ENA                             : in std_logic;
                CLK                             : in std_logic;
                TIME_GATE_TOP                   : in slv_32t;
                TIME_GATE_SIGNAL                : out std_logic
        );
end fi_timegate_var;

architecture Behavioral of timegate_block is
        signal sim_r_TIME_GATE_counter_i        : slv_32t := slv_zero;

begin
        process (CLK, ENA, RST)
                variable r_TIME_GATE_counter_i : slv_32t:=slv_zero
        begin
                 if RST = '0' then
                        r_TIME_GATE_counter_i <= (others => '0');
                        TIME_GATE_SIGNAL <= '0';
                 elsif rising_edge (CLK) then
                          r_TIME_GATE_counter_i := r_TIME_GATE_counter_i + 1;
                          if r_TIME_GATE_counter_i < (TIME_GATE_TOP-1) then
                                  TIME_GATE_SIGNAL <= '1';
                             else
                                  TIME_GATE_SIGNAL <= '0';
                                  r_TIME_GATE_counter_i <= (others => '0');
                             end if;
                end if;
        end process;
end Behavioral;
```

Figure 6: Time gate VHDL code.

the top layer of the graphic. A different counted frequency among the counters is shown with a black, red, or green dot color. From the 1800 recorded dataset, 74.2% of the recorded frequency shows the exact frequency among the four channels. The difference between the one channel compared to the other is only 0.033 Hz due to the rounding error of the reciprocal counter. It means that the four channels work very well. Ideally, the four channels should show the same counted frequency. The difference may occur from the time delay difference between the counter to the reference clock source and the incoming signal. One clock signal difference occurs when the propagation delay in the flip-flop of the counter is more prolonged than 2 ns. The difference is the consequence of the design; as we mentioned before, each counter was designed to work independently without synchronization in the counter time gate.

Figure 13 shows the measured frequency of the incoming signal from a silver electrode 10 MHz QCM sensor made of AT Cut Quartz resonator with a frequency tolerance and stability of 30 ppm. The measured frequency changed from 9995317.37 to 9995321.33 Hz with the measured frequency's resolution of 0.033 Hz. The most significant difference among the four channels is 0.13 Hz. From the 1800 measured signal, 61.2% shows the same frequency for the four channels.

Allan variance test has been done to investigate the potential noise of the counter. Figure 14 presents the Allan deviation of the recorded signal from the VCOCXO and QCM resonator. The datasheet of the oscillator states a temperature stability of 1.5 ppb. Figure 14 shows a maximum deviation of 0.05 for the VCOCXO, which equals five ppb relative to the 10 MHz center frequency. The deviation is

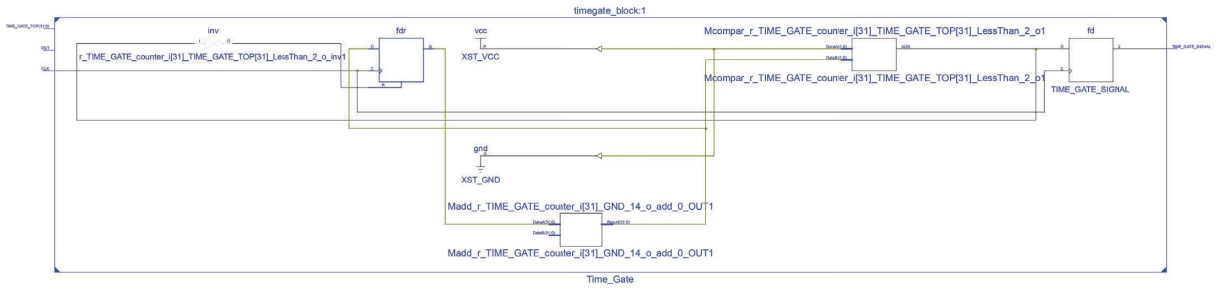

Figure 7: Block diagram of the time gate module.

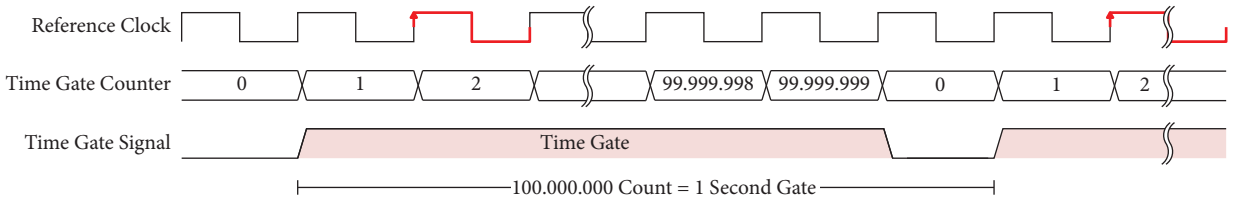

Figure 8: The timing diagram of the time gate module.

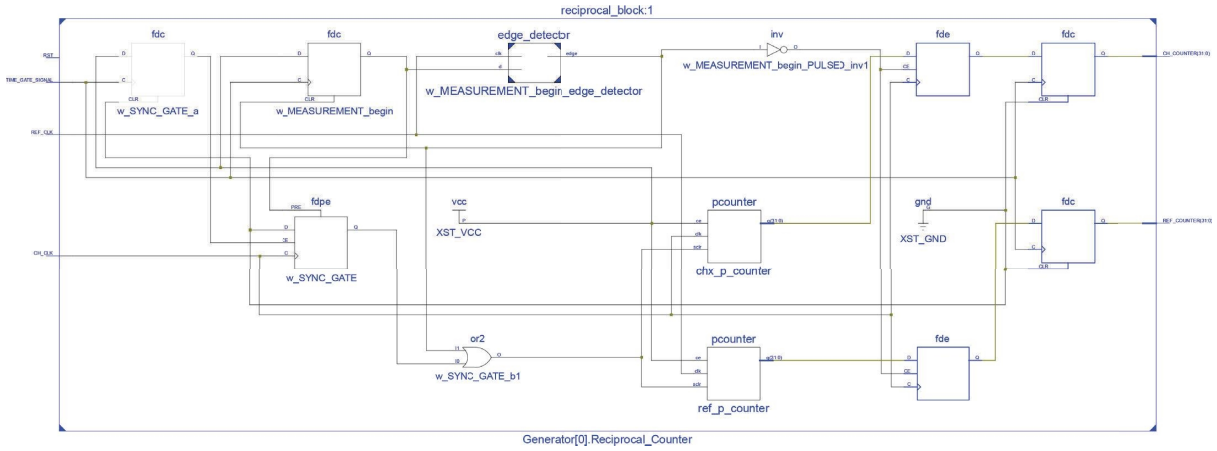

Figure 9: Reciprocal counter block diagram.

slightly higher than the described temperature stability in the datasheet.

The deviation of the QCM signal increases with time intervals and reaches the constant deviation at around 1. The maximum deviation of the QCM sensor is 1.7, as depicted in Figure 14. Interestingly, the crystal resonator with tolerance and temperature stability of 30 ppm has a maximum deviation of only 1.7, equivalent to 0.17 ppm deviation. The VCOCXO and quart crystal resonator Allan variance test showed that the developed frequency counters work very well.

The developed frequency counter was tested to measure the frequency change of the QCM sensor with different coatings in contact with gases. A sample of the measurement result is presented in Figure 15. The QCM sensor in channel 1 is QCM without coating. It means the sensitive layer is the silver electrode itself. Sensors from Channel 2 to Channel 4 are sensors with polystyrene. The coating thickness of the sensor is 0.092 μm, 0.2 μm, and 1.25 μm for Channel 2, Channel 3, and Channel 4, respectively. The target gas is chloroform at 15 ppm concentration. One can see that the system can measure the frequency and hence the frequency change of the QCM sensor with a different coating to a target gas. The sensitivity of the frequency measurement can be seen in Figure 15 (see inset). The frequency change resolution is 0.03 Hz. There is no jitter observed in Figure 15. Each counter works independently without any signal crosstalk among the frequency counter.

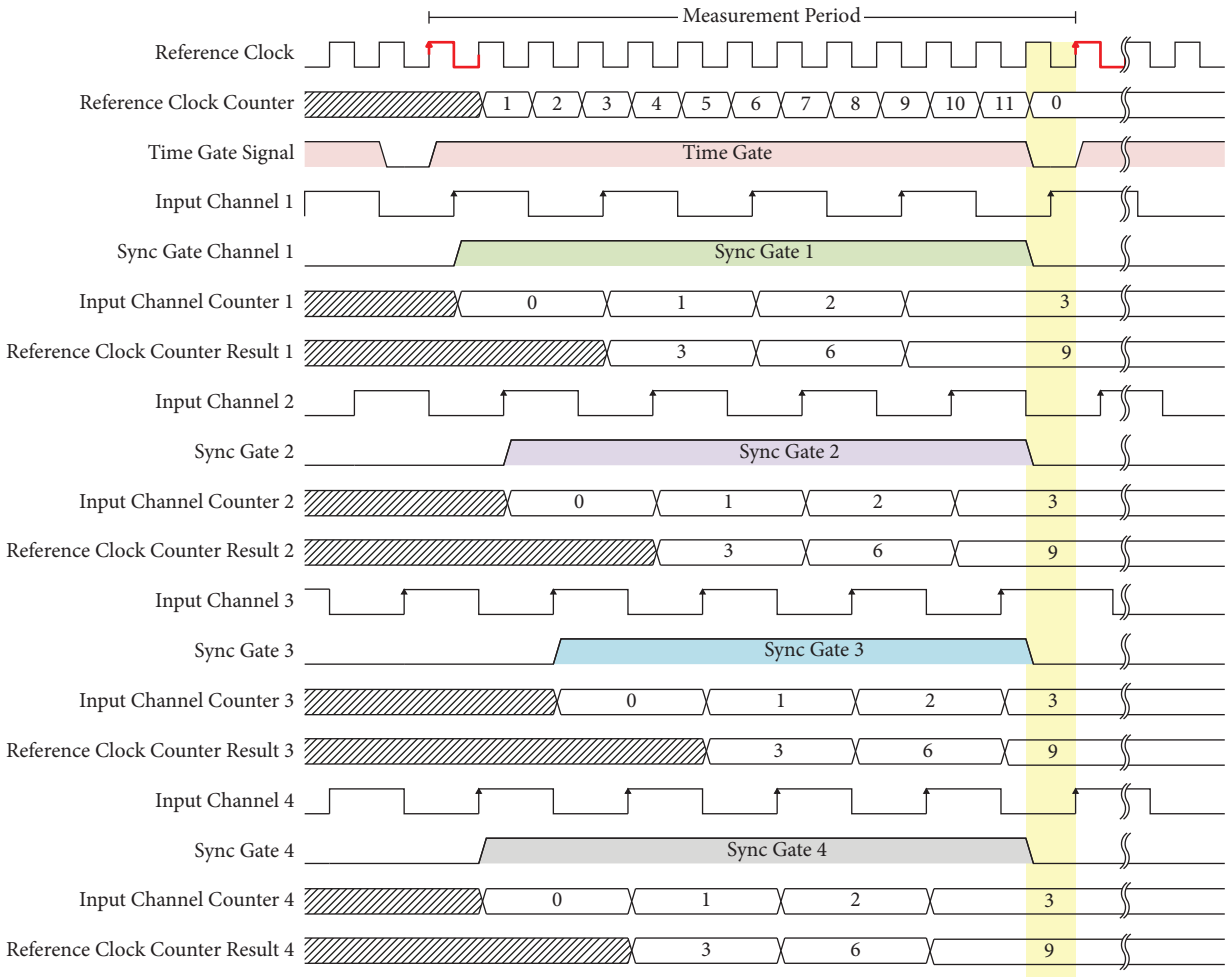

Figure 10: Reciprocal counter timing diagram.

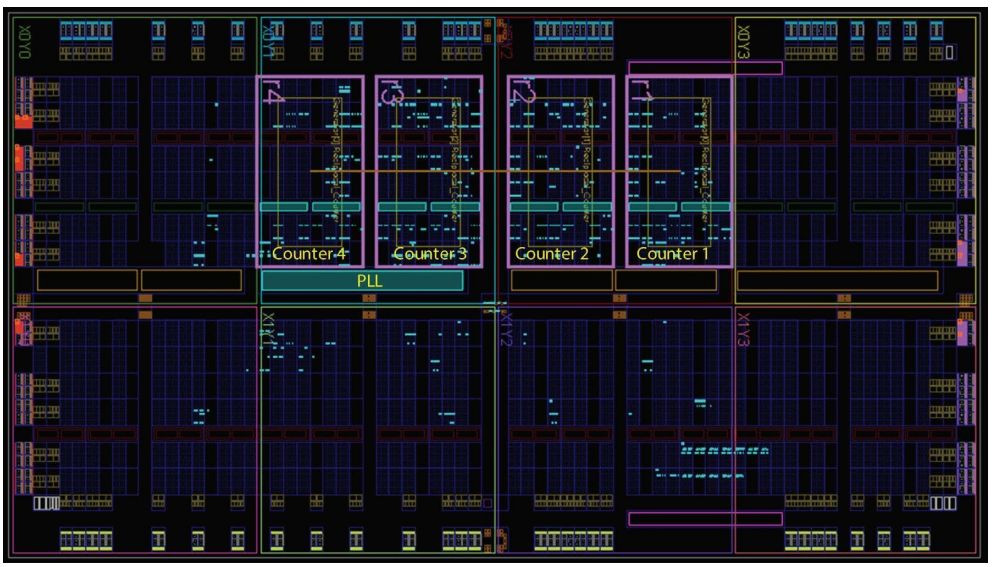

Figure 11: Floorplan of the system.

Table 1: Summary of slice logic utilization.

Slice logic utilization	Used	Available	Utilization (%)
Number of slice registers	630	11,440	5
Number of slice LUTs	336	5,720	5
Number of BUFGs	9	16	56
Number of DSP48A1s	8	16	50
Number of PLL_ADVs	1	2	50
Number of bonded IOBs	11	102	10

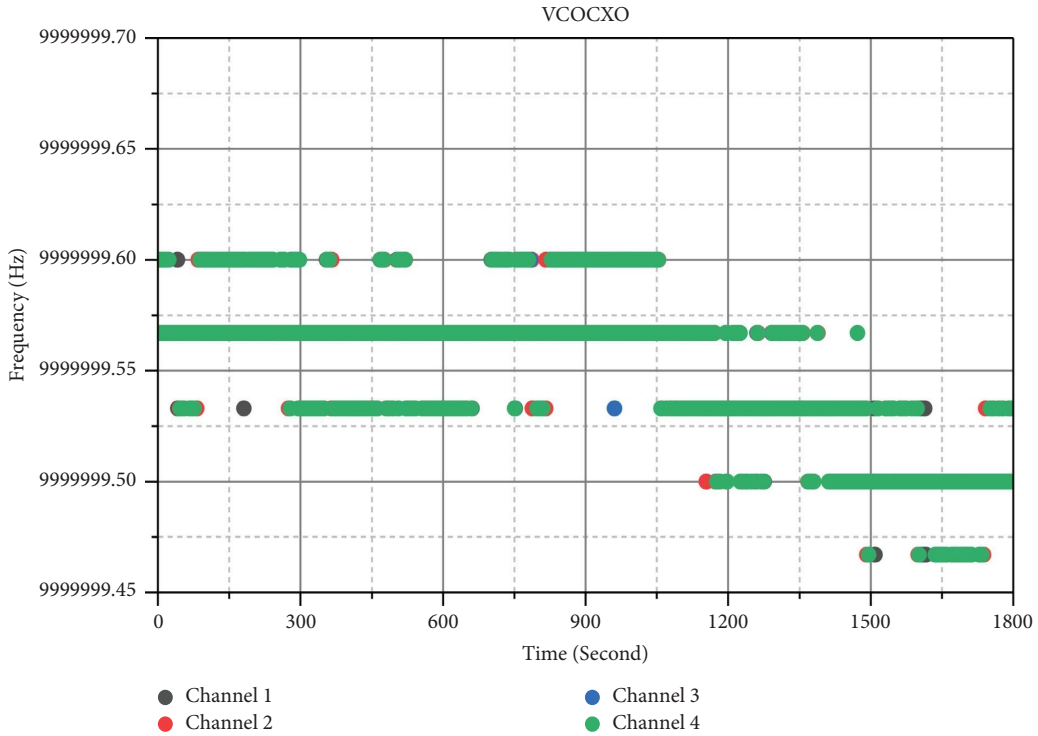

Figure 12: The frequency measurement result of a 10 MHz VCOCXO.

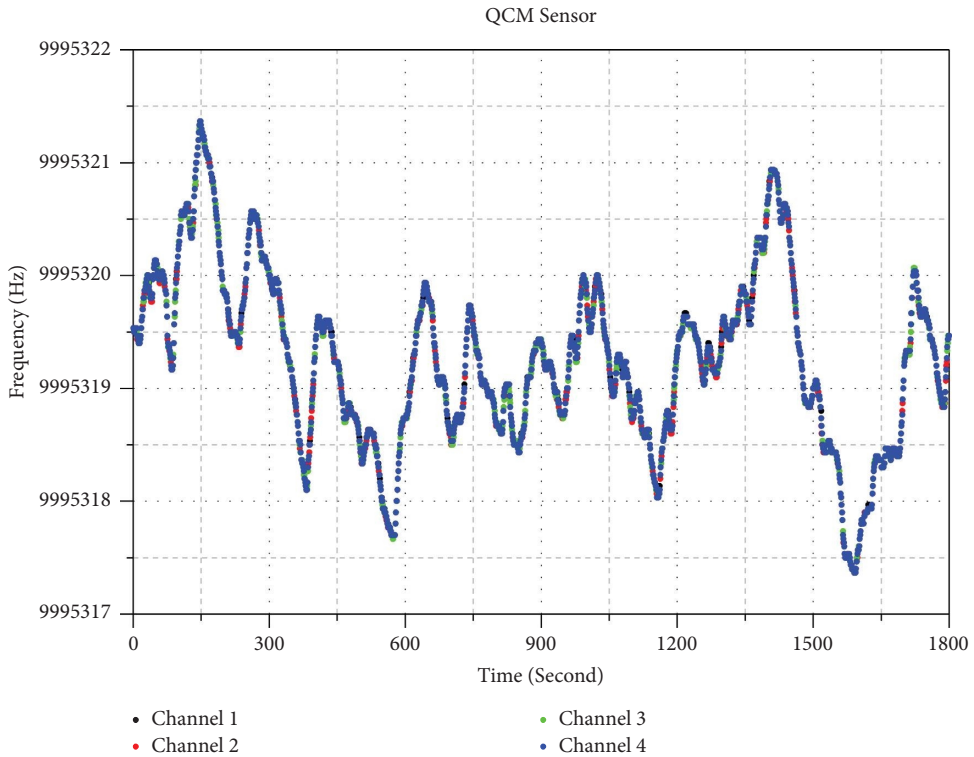

Figure 13: The frequency measurement result of the 10 MHz QCM oscillator.

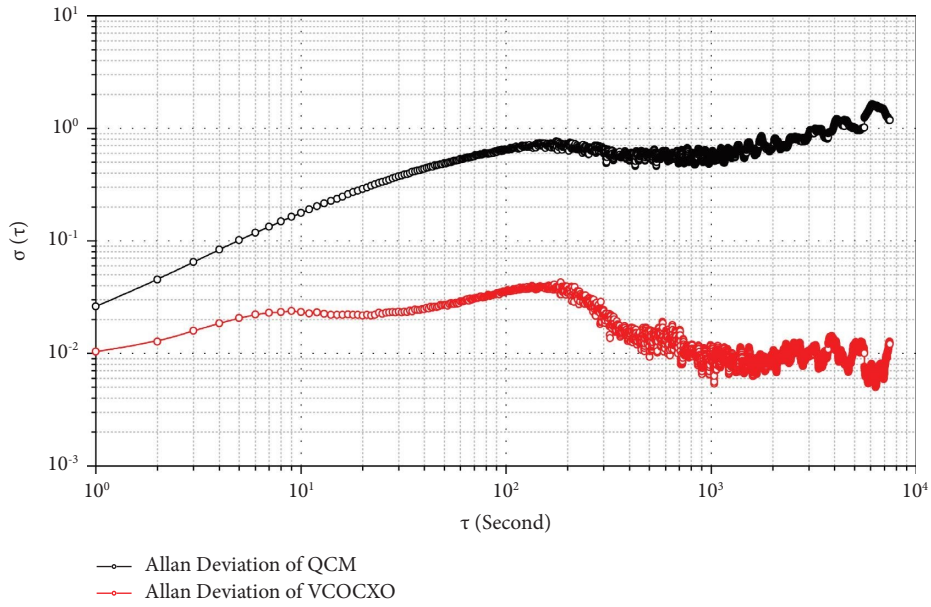

Figure 14: Allan variance test of the system to three different signal sources.

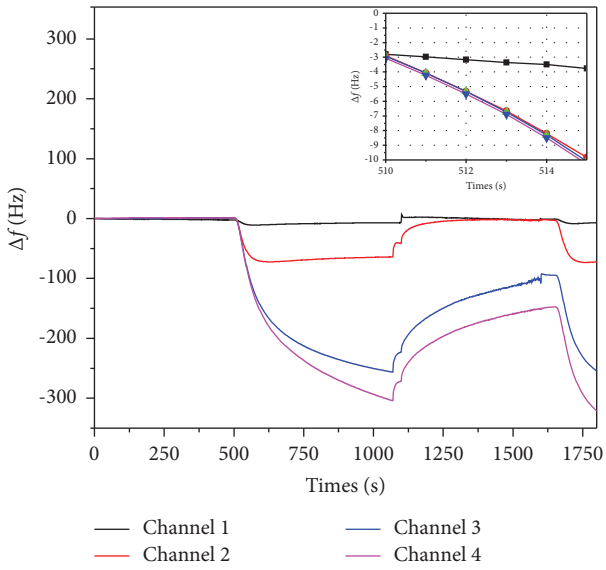

Figure 15: Measurement result with four channel QCM sensor in response to a gas.

4. Conclusion

A four-channel independent reciprocal frequency counter was successfully developed using a generic board of FPGA and microcontroller modules. The precision of the counter is 0.03 Hz. The four-channel frequency counter work paralleled independently. The maximum frequency difference among the four channels is only 0.033 Hz for the VCOCXO signal source and 0.13 H for the signal source from the quartz resonator. The four reciprocal counters consume only 5% of registers and 5% LUTs, and 50% of PLL FPGA resources. The reciprocal counter utilizes the PLL module to generate a 300 MHz reference clock from 50 MHz TCXO.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that there are no conflicts of interest.

Acknowledgments

This work was funded by the Ministry of Research and Technology of the Republic of Indonesia under the research grant PTUPT scheme 2022.

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