Research Article

Design of a Novel Decimal to Multicode Converter in QCA Technology

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Researchers are always looking for the improvement of existing methods. Today, CMOS technology is widely used, which has some advantages and disadvantages. One of the alternative methods for CMOS technology is QCA technology which compared to CMOS, has the advantages of low energy consumption and small occupied area. In this paper, by using the concepts and methods of QCA technology, a digital code converter is presented. In this converter, a new gate is used, which can produce outputs such as 4-input AND, 4-input OR, 4-input NAND, and 4-input NOR. The proposed converter has 10 inputs and 12 outputs. The 10 inputs are decimal numbers from 0 to 9, producing the output equivalent to excess-3, BCD, and gray codes. One of the advantages of this circuit is providing three different codes per input in just one circuit. In addition, due to the use of the new 4-input gate, the occupied area and the number of used cells were minimized. Simulations were performed by using QCADesigner-E version 2.2, and outcomes illustrated that the occupied area is equal to $0.29\,\mu m^2$ and 380 QCA cells with 7 clock phases are used. The energy dissipation of the presented circuit is 171 meV. Also, given the favorable performance exhibited by the 4-input gate across various measurement parameters, it possesses the capability to be efficiently employed within larger and intricately designed circuits.

1. Introduction

New methods are always being introduced in the world of technology. Quantum-dot cellular automata (QCA), being one of the new nanotechnologies, can be widely used in future systems and circuits [1]. Nowadays, one of the most important technologies is CMOS technology which has some disadvantages, of which the most considerable ones are high energy consumption and large circuit sizes [2]. Researchers and scientists are always looking for a way to improve the used methods, and that is why, QCA technology has been introduced [3, 4]. As a matter of fact, there are many different kinds of practical applications for digital code converters. For instance, BCD forms are utilized in 7-segment display decoder ICs, and the RTC (real-time clock) device stores the data in BCD. Moreover, gray code can be used to reduce the error rate in certain parts of a PCM system, and it has a critical role in analog-digital converters (ADCs). Finally, excess-3

code can be utilized in designing full adder/subtractor in the digital world. It is clear that having a single converter that can produce multiple code formats can be really useful in devices that use BCD, gray code, and excess-3 code. The main novelty of the proposed converter is presenting a new converter that can produce three popular codes in the digital world, that is, BCD, gray, and excess-3, and this can bring versatility and flexibility in data representation and interface with different systems that use the aforementioned codes. The main parts of this paper are categorized as follows. In Section 2, a literature survey and some of the previous investigations are presented. In Section 3, basic concepts and methods of QCA and used blocks in the proposed circuit are introduced. In Section 4, the proposed circuit is presented by taking the decimal number and simultaneously producing excess-3, BCD, and gray code in the output. In Section 5, the results of the circuit are given, and finally, the conclusion of the paper is provided in Section 6.

2. Literature Survey

In this part, some of the previous investigations are presented. Lent and his coworkers introduced the QCA technology for the first time in 1993 [5]. QCA offers a large number of advantages, and the most significant ones are low energy consumption and small circuit size compared to CMOS technology [6]. One of the most imperative circuits in digital processors is the code converter. Various codes are used to display numbers, such as decimal, excess-3, BCD, and gray. One of the critical parts of digital systems is the circuits that convert different codes to each other. Each system works with a special code, and this fact shows why there is a need to code converter circuits and establish a correct connection with these systems. Since there are different codes of numbers, it is obvious that there are also various converter circuits, such as decimal to excess-3, BCD to decimal, and decimal to gray. [7]. QCA technology allows users to design new blocks to implement a variety of digital circuits, including code converters, and this leads to the optimization of circuits as much as possible, as in this paper, using a new block, a new converter is implemented. Although the code converter is very important, many articles have not been published about it in the QCA technology, especially in converting decimals to other codes such as excess-3 and gray. Raina and his coworkers in [8] have presented seven separate circuits to generate a seven-segment code. All presented circuits take a BCD number and calculate its equivalent for each segment of the seven-segment. Among the disadvantages of these circuits, it can be mentioned that they were separate, and it was better that all of the seven outputs were produced in one circuit. Ramesh and his colleagues have proposed a binary to BCD converter [9]. A new full adder was presented, and after that, the code converter was designed using this full adder. This converter was not optimized as much as possible. Feynman gate was presented in [10], and using that, four different code converters were provided. Binary to gray, gray to binary, excess-3 to binary, and binary to excess-3 are the converters that are presented in this work. The authors in [11] have presented a new NAND gate with two inputs and called it an LTEx module containing 26 cells with four clock-phase usage. Using the mentioned gate, a binary to gray code converter was presented. Karthik and other authors in [12] have introduced a BCD to excess-3 code converter without any new idea, and there is just a simple converter in this design. In [13], a new majority gate with 5 outputs was provided. In order to create this gate, 3 clock phases were used, and by using the proposed gate, a BCD to excess-3 code converter was presented. A BCD adder in reference [14] was presented. The realization of this BCD adder involves the introduction of several innovative gates, namely, the half-adder/subtraction (HAS-PP), full-adder/subtraction (FAS-PP), and overflow-detection (OD-PP), all of which rely on parity-preserving logic synthesis. By integrating these gates, a novel tree-based methodology emerges as the proposed approach to effectively implement the requisite BCD adder. Also, in reference [15], a comprehensive proposal was put forth for a parity-preserving reversible binary to BCD code converter.

This converter is designed to facilitate quantum computations and is constructed using a standard library of reversible gates, which includes NCT (NOT, CNOT, and Toffoli gates), MCT (multiple control Toffoli gate), and NCV (NOT, CNOT, and the square root of NOT). These gates form the foundation of the quantum equivalent circuit, enabling efficient conversion from binary to BCD code while maintaining parity preservation throughout the process.

As can be seen, there were not many papers that worked on the conversion of decimal numbers to other digital codes, and one of the reasons for this may be having a high number of inputs in this type of converter, leading to a larger circuit size. In this article, by using a new 4-input gate, a new converter is introduced that takes the decimal code as an input and simultaneously produces all three equivalents of the BCD code, excess-3 code, and gray code.

3. Quantum-Dot Cellular Automata Basis

QCA is completely dependent on the movement of electrons inside a QCA cell. Two electrons move freely and continue to move until a force is applied that puts them in a fixed state, and the electrons get trapped in the dots which can be seen in Figure 1(a). Two main situations are considered for the placement of electrons inside the cell given in Figure 1(b). When the electrons have a polarization of −1 and +1, a logical value of 0 and 1 is considered for the cell, respectively. As mentioned earlier, QCA technology has a lower energy consumption than CMOS technology, and the main reason for this is the movement of electrons only in a specific space (cell) instead of flowing of electrons in a conductive path (such as a wire). One of the most basic and important gates in QCA technology is the majority gate because it can be used to implement AND and OR gates. This gate can be seen in Figure 2(a). The function of the majority gate, AND gate, and OR gate is given in (1)–(3), respectively. Among the other important gates, the NOT gate can be mentioned, which is presented in Figure 2(b). Finally, another important gate, the wire gate is shown in Figure 2(c), and it is very important for data transmission.

Another important concept of QCA technology is clocking, being essential to follow its rules to produce the correct output. Clocking has 4 separate parts (phases) and each one of these phases has a special meaning, as shown in Figure 3. The first phase is called the switch phase in which the incoming force to the electrons inside the cell is increased and the electrons get fixed. In the second phase known as the hold phase, the incoming force to the electrons reaches its maximum value, and the cell takes one of the logical values of 0 or 1. In the third phase called the release phase, the incoming force is reduced, and in this phase, the electrons change from a stable state to a moving state. Finally, in the fourth phase, or the relax phase, the incoming force reaches its minimum value and the electrons completely move freely in the cell.

$$\text{Maj}(A, B, C) = AB + AC + BC, \tag{1}$$

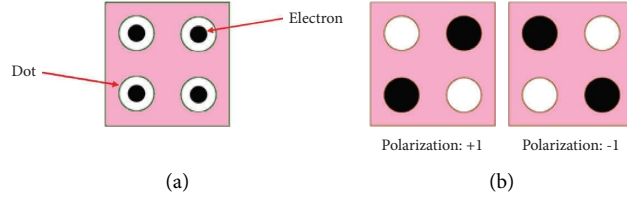$$\text{Maj}(A, B, 0) = AB, \tag{2}$$

FIGURE 1: QCA cell (a) and polarizations of QCA cell (b).
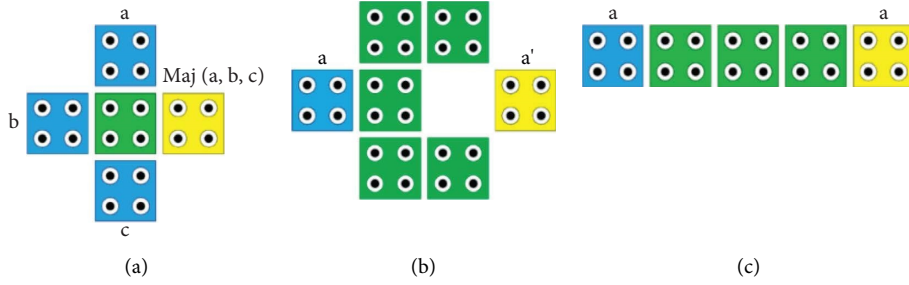

FIGURE 2: Majority gate (a), NOT gate (b), and wire (c) in QCA.

$$
\begin{aligned}
\text{Maj}\,(A, B, 1) &= AB + A + B \\
&= A\,(B + 1) + B \quad\quad\quad (3) \\
&= A + B.
\end{aligned}
$$

4. Proposed Digital Code Converter

In this section, a new digital code converter using a new 4-input block is presented, and this new block is shown in Figure 4 [4]. This block has 4 different inputs and one programming input called the "select" cell shown in Figure 4. This block produces $A + B + C + D$ and $A.B.C.D$ outputs meaning that this block can provide 4-input AND and OR gates. When the polarization of this cell is equal to -1 and $+1$, this block is a 4-input AND and a 4-input OR gate, respectively.

The presented converter can convert a decimal code to excess-3, BCD, and gray codes simultaneously, and because of this, it has 10 inputs for decimal numbers from 0 to 9 and 12 outputs. Every 4 outputs are for a unique code. In Table 1, different decimal inputs and expected outputs for 3 different codes are given. It is to be noted that inputs ranging from I0 to I9 are known as decimal numbers from 0 to 9. Also, for every state, for example, the state that just I5 is equal to "1" and others are equal to "0" means that the input is a decimal number that is equal to 5. In the following, the intended functions for producing each output are given, which have been tried to optimize as much as possible by establishing relationships between different outputs. Therefore, it can be concluded that this circuit is optimized in 2 ways by creating relationships between the desired outputs and then by using the new 4-input block. The logical circuit of this converter is shown in Figure 5 which contains two 2-input OR gates, three 4-input OR gates, six 5-input OR gates, and one 6-input OR gate.

$$
\begin{aligned}
O1 &= I5 + I6 + I7 + I8 + I9 \\
&= O5\,(\text{or } O9) + 1 \text{ unit shift of } O6,
\end{aligned} \quad (4)
$$

$$
O2 = I1 + I2 + I3 + I4 + I9, \quad (5)
$$

$$
\begin{aligned}
O3 &= I0 + I3 + I4 + I7 + I8 \\
&= I0 + 1 \text{ unit shift of } O7,
\end{aligned} \quad (6)
$$

$$
O4 = I0 + I2 + I4 + I6 + I8, \quad (7)
$$

$$
\begin{aligned}
O5 &= I8 + I9 \\
&= O9,
\end{aligned} \quad (8)
$$

$$
O6 = I4 + I5 + I6 + I7, \quad (9)
$$

$$
O7 = I2 + I3 + I6 + I7, \quad (10)
$$

$$
\begin{aligned}
O8 &= I1 + I3 + I5 + I7 + I9 \\
&= \text{invert of } O4,
\end{aligned} \quad (11)
$$

$$
\begin{aligned}
O9 &= I8 + I9 \\
&= O5,
\end{aligned} \quad (12)
$$

$$
\begin{aligned}
O10 &= I4 + I5 + I6 + I7 + I8 + I9 \\
&= O5\,(\text{or } O9) + O6,
\end{aligned} \quad (13)
$$

$$
O11 = I2 + I3 + I4 + I5, \quad (14)
$$

$$
O12 = I1 + I2 + I5 + I6 + I9. \quad (15)
$$

The obtained functions, ranging from (4) to (15), were produced by utilizing the Karnaugh map which is an efficient method for getting relationships between inputs and outputs
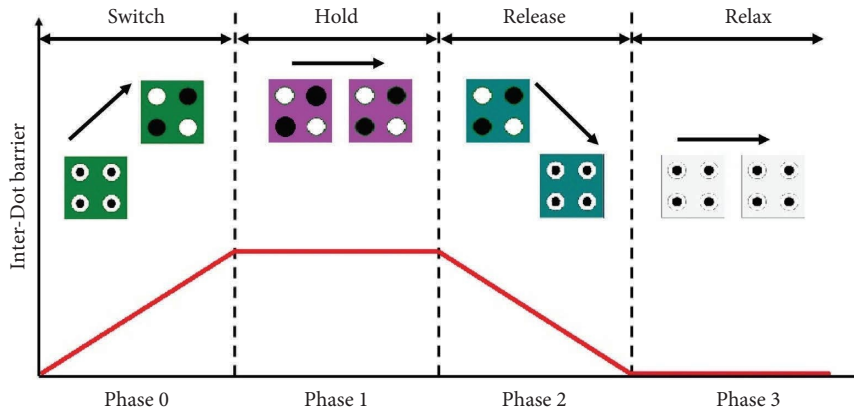
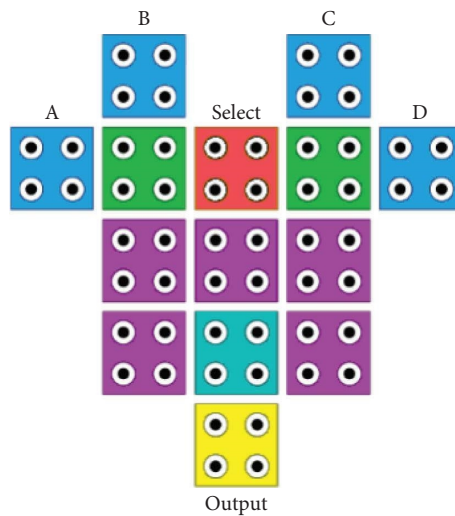FIGURE 3: Clocking in QCA technology.

FIGURE 4: The new 4-input block.

[16]. For example, by forming the mentioned map, it can be achieved that O7 is formed from OR operation between I2, I3, I6, and I7 belonging to decimal numbers equal to 2, 3, 6, and 7, respectively. It is crystal clear that BCD is a decimal code with a 4-digit binary code, but it is an on-paper definition. To have BCD in the real world, there is a need for a converter to accept numbers from 0 to 9 and produce BCD numbers from 0000 to 1001 and the proposed converter is able to perform this. Besides, an excess-3 code is a BCD + 3 and this rule was considered in Table 1, and excess-3 code numbers were from 0011 to 1100. All of the aforementioned things were performed for gray code, too. To simplify the proposed circuit as much as possible, logical relationships have been established between the expected outputs. For example, in (4), O1 was produced using O5 and O6, and the reason for using one unit shift of O6 was to provide the necessary inputs to produce O1; therefore, I4 + I5 + I6 + I7 using this shifting can be considered as I5 + I6 + I7 + I8, and if the obtained results will be OR with O5, then the output will be O1. Moreover, inverting O4 could produce O8 because every bit of O4 that is equal to binary "0" in O8 is equal to binary "1" and vice versa. So, (11) can simplify the proposed circuit much more.

If the circuit in Figure 5 will be designed and implemented with the typical majority gate, then there will be a need for 40 majority gates, making the size of the circuit much larger. However, by utilizing the new 4-input block, there is a need for 8 majority gates and 5 new blocks which result in using a smaller number of cells for the designing of the circuit. The block diagram of the proposed converter is illustrated in Figure 6. Also, the proposed digital converter is presented in Figure 7.

The presented digital code converter was implemented in three layers. The main layer which has the largest number of cells, the top layer, and, finally, the via layer connecting the main layer to the top layer. These layers are shown in Figures 8–10.

5. Simulation and Results

In this section, the presented digital code converter is simulated in the QCADesigner-E software version 2.2. This software has been developed by the University of Calgary and gives some reports such as occupied area, cell count, and energy consumption [17, 18]. There are 10 decimal inputs

TABLE 1: The truth table of decimal to excess-3 code, BCD, and gray code.

| Inputs										Excess-3 outputs				BCD outputs				Gray outputs			
I0	I1	I2	I3	I4	I5	I6	I7	I8	I9	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12
1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1
0	0	0	0	0	0	1	0	0	0	1	0	0	1	0	1	1	0	0	1	0	1
0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	1	1	0	1
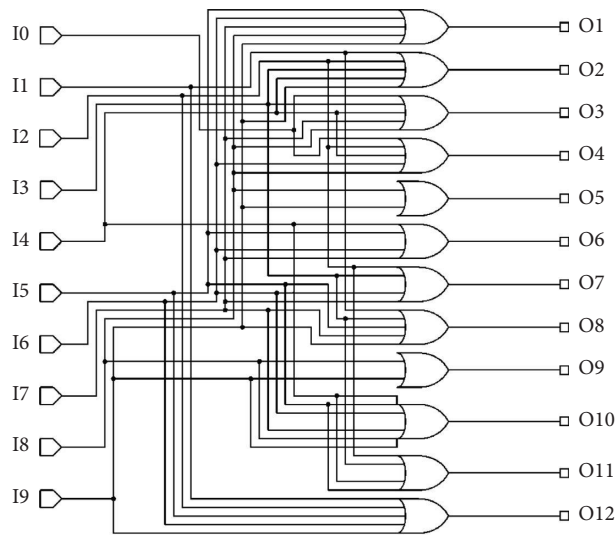
FIGURE 5: Decimal to excess-3 code, BCD, and gray code converter.
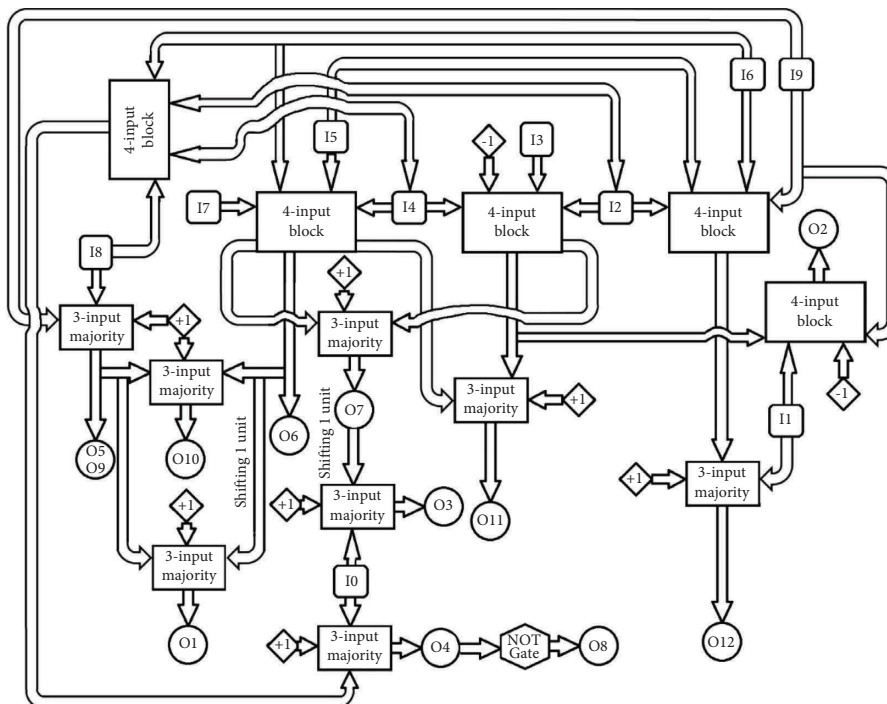

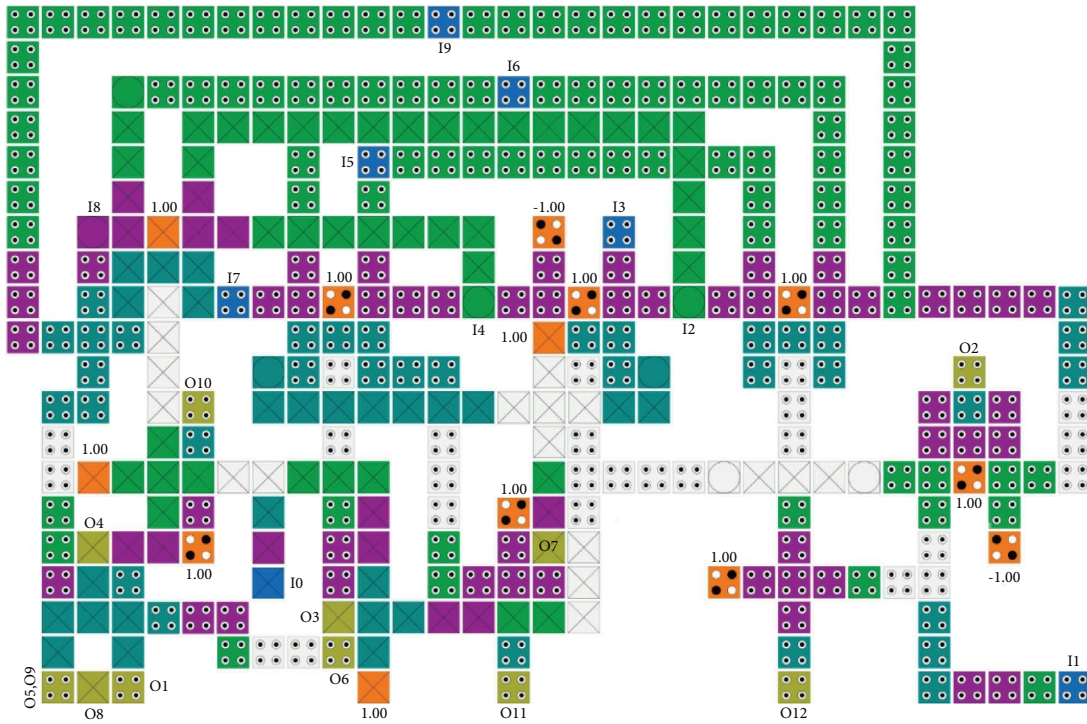FIGURE 6: Block diagram of the proposed digital code converter.

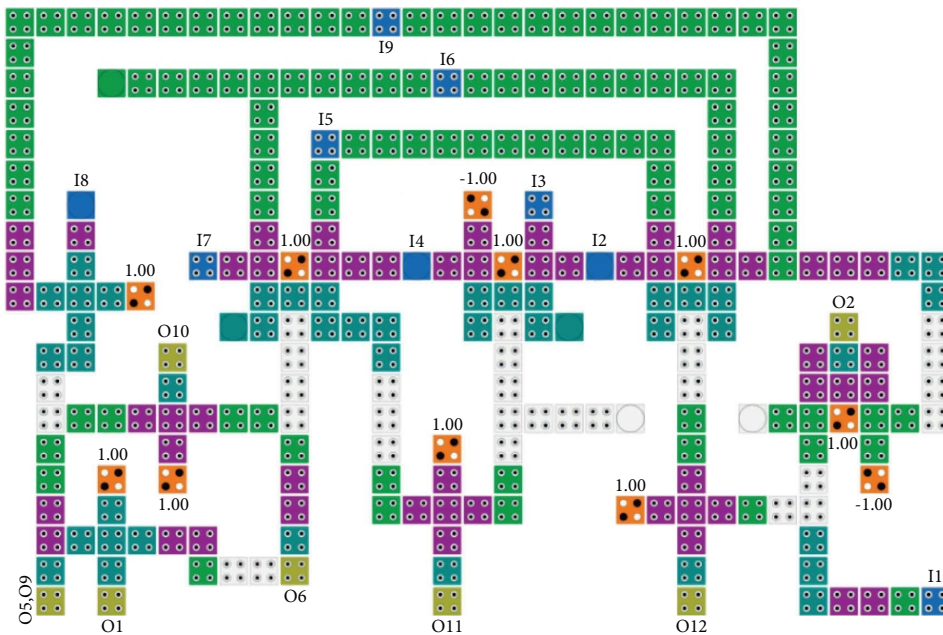Figure 7: Proposed digital code converter in QCA.

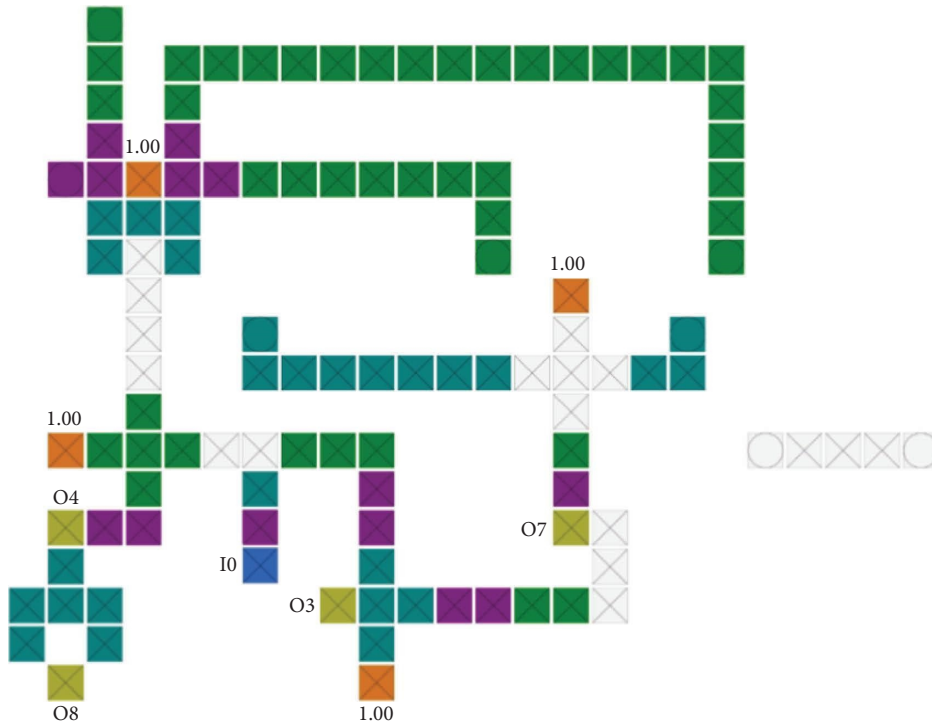Figure 8: The main layer of the presented digital code converter.

FIGURE 9: The top layer of the presented digital code converter.

FIGURE 10: Via layer of the presented digital code converter.

from 0 to 9 which are shown in Figure 11. After simulating the proposed converter, the obtained results are given in Figure 12, containing 12 different outputs for three different codes.

As can be seen from the simulation results in Figure 12, the simulated circuit has produced the correct outputs. For example, to convert the decimal number "4" to excess-3 code, the output must be binary "0111," which means O1, O2, O3, and O4 must be equal to binary "0," binary "1," binary "1," and binary "1," respectively, as can be seen in Figure 13. To convert the decimal number "6" to BCD, the output must be binary "0110," which means O5, O6, O7, and O8 must be equal to binary "0," binary "1," binary "1," and binary "0," respectively, as can be seen in Figure 14. In the

end, to convert the decimal number "8" to gray code, the output must be binary "1100," which means O9, O10, O11, and O12 must be equal to binary "1," binary "1," binary "0," and binary "0," respectively, as can be seen in Figure 15. The presented digital code converter that converts the decimal number to excess-3, BCD, and gray codes has used 7 clock phases, and the total power consumption of this circuit is equal to 1.71-001 eV. Also, the occupied area is equal to 0.29 μm^2, and 380 QCA cells are used in this circuit. In Table 2, details of the proposed circuit are given.

The calculation of circuit latency is directly influenced by the clock cycle, establishing a clear relationship between the two. In this research paper, a multicode converter was

FIGURE 11: Inputs of the proposed digital code converter.

introduced, which is capable of converting decimal numbers to BCD, excess-3, and gray codes, and the latency of the presented converter was measured to be 1.75. Table 3 provides a comparison of the converter's details with a few relevant papers. It is worth noting that the number of

papers focusing on excess-3 converters, especially those converting decimal numbers to excess-3, BCD, and gray codes, is limited. Consequently, the closest available circuits were selected and compared against the proposed circuit. The evaluation of QCA schemes primarily relies on key
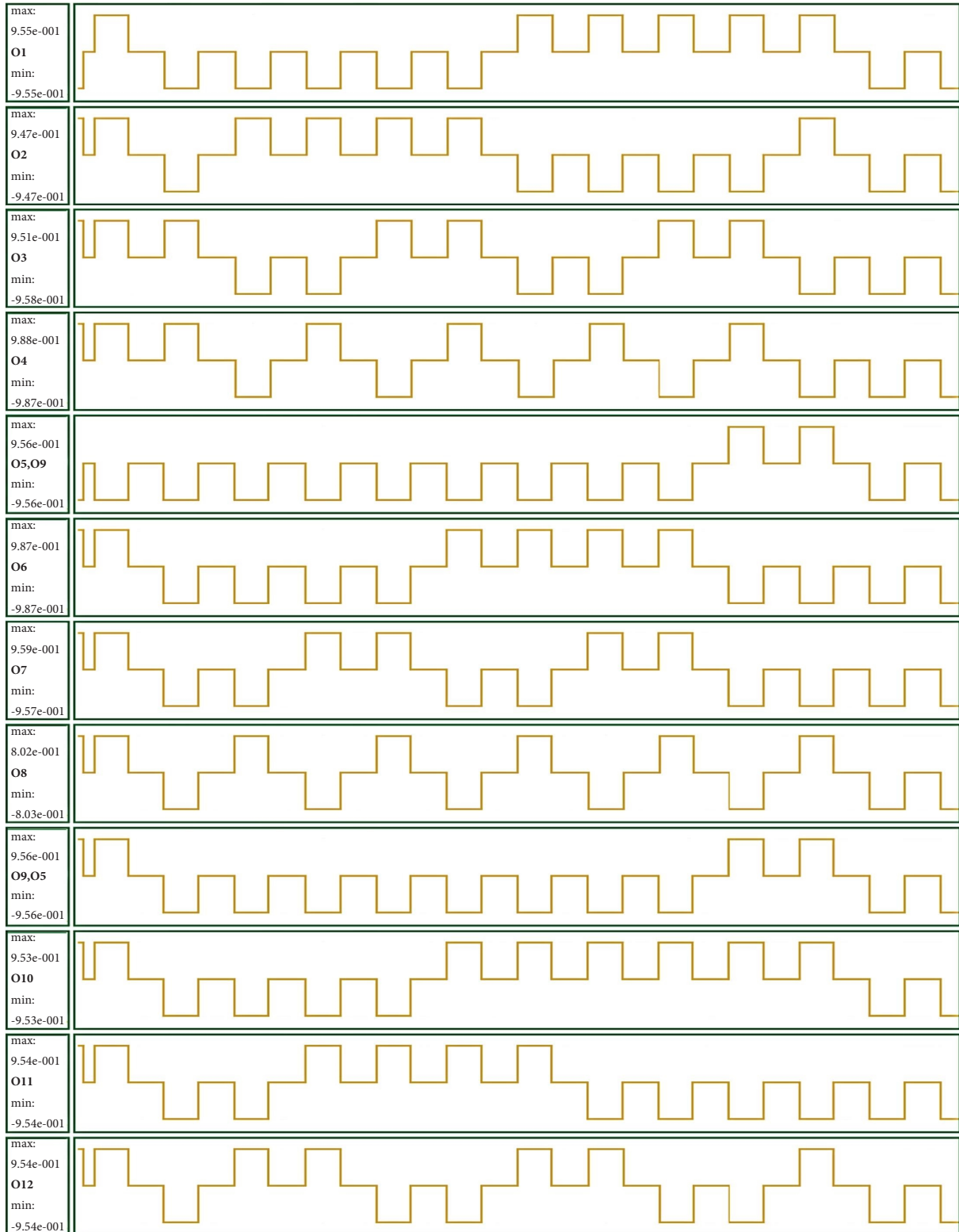
FIGURE 12: Outputs of the proposed digital code converter.

metrics, including the number of cells utilized, latency, and occupied area. In comparison to some similar converters, the proposed one demonstrated superior performance in terms of the number of used NOT gates which play a crucial role in

increasing the latency of circuits. Also, in terms of cell number and occupied area, although the proposed circuit offers 3 types of converters together and needs much more cells, its cell usage is less than that of some previous
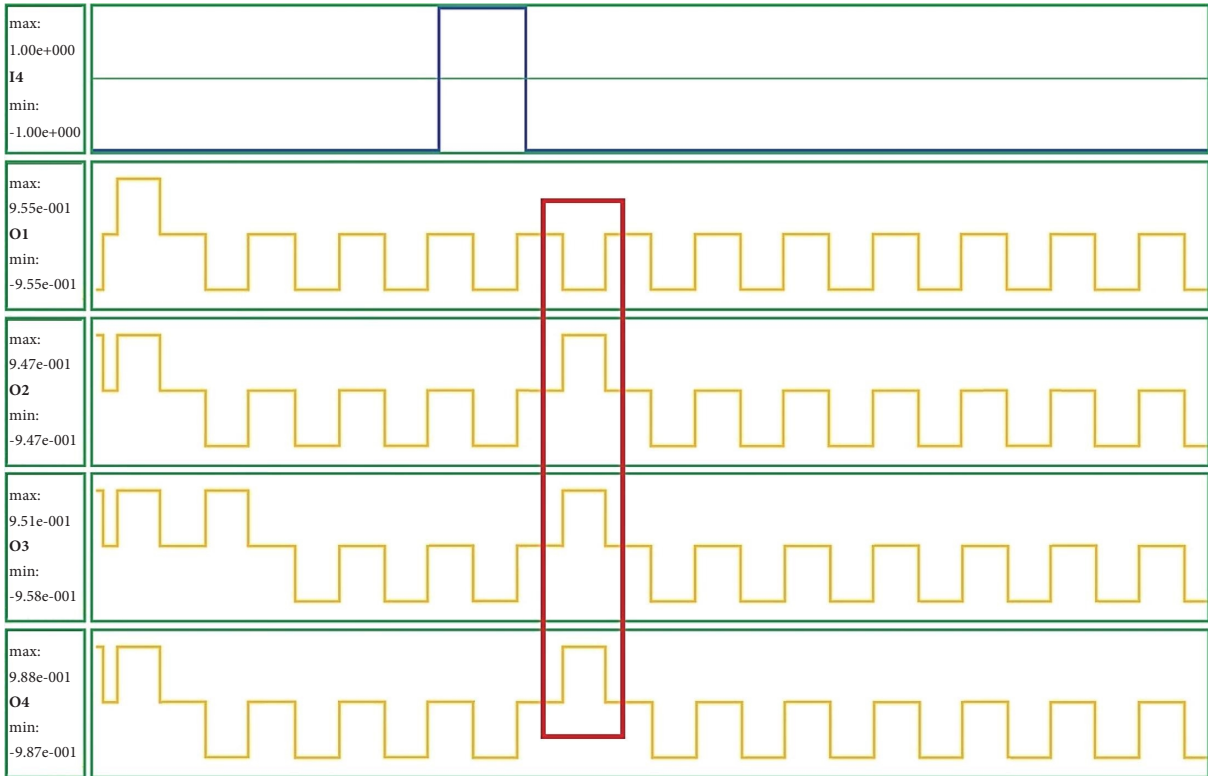
FIGURE 13: An example of converting the decimal number to the excess-3 code with the proposed digital code converter.
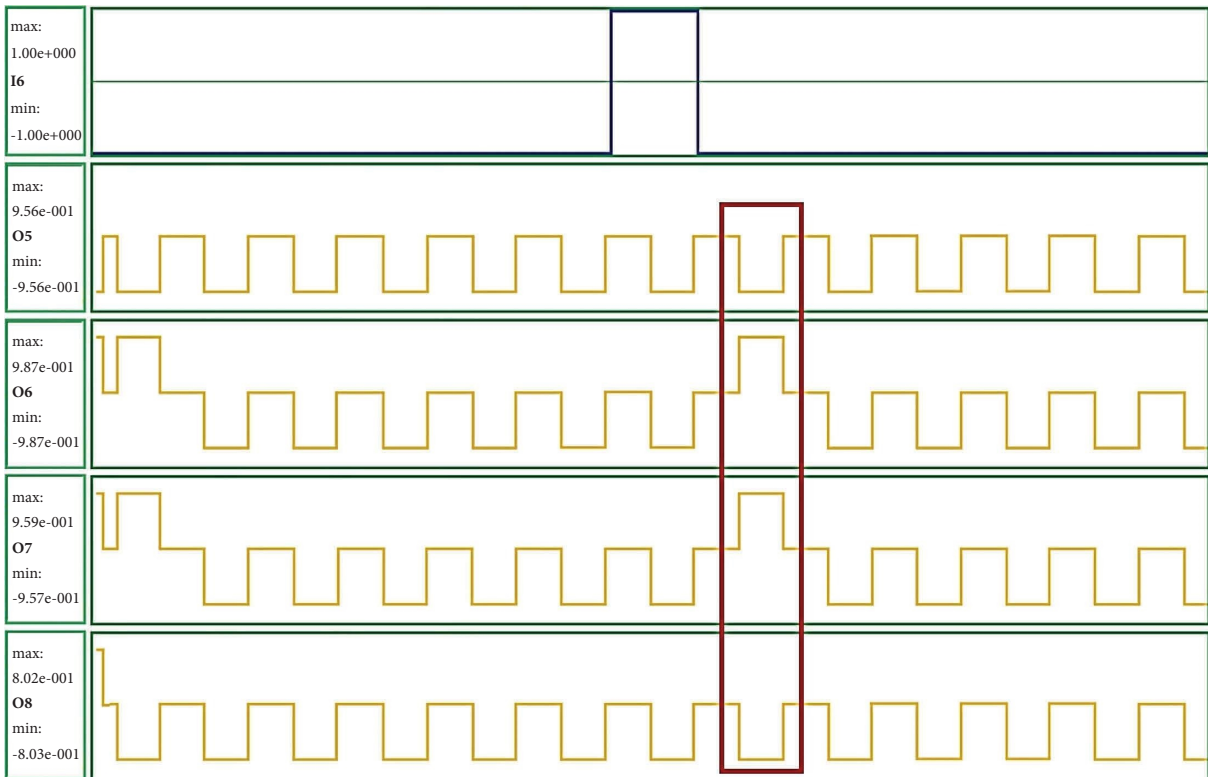

FIGURE 14: An example of converting the decimal number to the BCD with the proposed digital code converter.
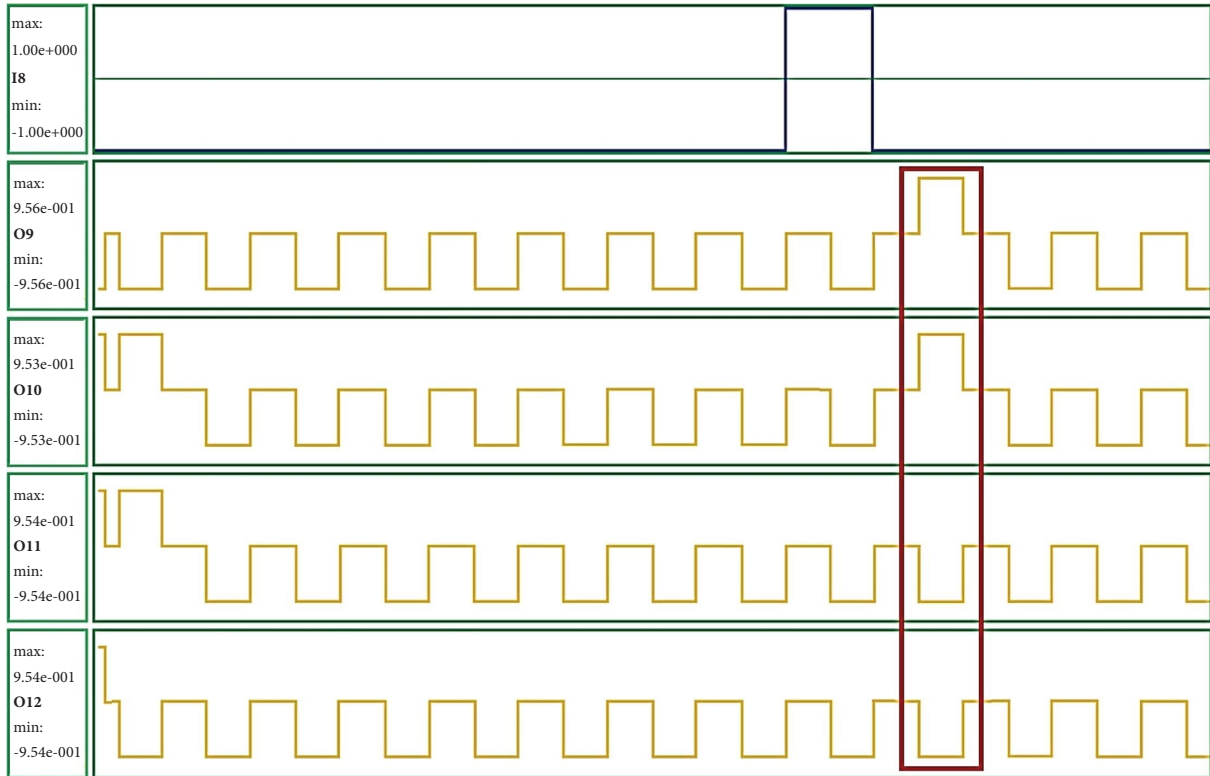
Figure 15: An example of converting the decimal number to the gray code with the proposed digital code converter.

Table 2: Details of the proposed circuit.

Items	Decimal to excess-3, BCD, and gray codes converter
Cell count	380
Delay (clock phases)	7
New 4-input block count	5
Majority gate count	8
Inverter gate count	1
Power consumption	$1.71\,e-001$ eV
Number of layers	3

Table 3: Comparison table of different QCA code converters with the proposed converter.

Circuit	Type	Cell count	Total area (μm^2)	Latency (clock cycle)	Scalability	Inverter gate	Circuit layer type
[13]	BCD to excess-3	414	0.52	2.25	No	19	Multilayer
[19]	BCD to excess-3	191	0.29	3.00	No	4	Single-layer
[20]	BCD to excess-3	143	0.22	1.50	No	3	Multilayer
[21]	BCD to excess-3	254	0.31	1.00	No	4	Multilayer
[22]	Binary to gray	225	0.43	1.00	No	3	Multilayer
[23]	Thermometer code to gray	134	0.20	1.75	No	7	Single-layer
[12]	BCD to excess-3	137	0.16	0.75	No	6	Single-layer
[24]	Binary to excess-3	176	0.20	1	No	5	Single-layer
Proposed converter	Decimal to excess-3 Decimal to BCD Decimal to gray	380	0.29	1.75	Yes	1	Multilayer

investigations which presented just one conversion. Last, but not least, it is to be noted that, due to the usage of the new block, the proposed circuit is the only converter that is able to use scalability.

6. Conclusion

In this article, by using a 4-input gate that can give 4-input AND, 4-input OR, 4-input NAND, and finally, 4-input NOR, a new circuit was presented that has the ability to simultaneously convert the decimal number to excess-3, BCD, and gray code. The circuit was designed in three layers. Some reports such as cell count, delays, and power consumption were presented, and the circuit was evaluated with the QCADesigner-E software. This circuit has 10 inputs for decimal numbers from 0 to 9 and 12 outputs for three different types of codes. One of the advantages of the proposed circuit is its scalability which can be a promising work for improving future circuits.

Data Availability

The data that support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Authors' Contributions

Farhad Fouladinia conceptualized, validated, investigated, and visualized the study, developed the methodology and software, performed formal analysis, collected the resources, and wrote the original draft. Mohammad Gholami conceptualized, investigated, and supervised the study, developed the methodology, collected the resources, and wrote, reviewed, and edited the article.

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