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Research Article

Design and Development of Efficient SRAM Cell Based on FinFET for Low Power Memory Applications

M. V. Nageswara Rao,[1] Mamidipaka Hema,[2] Ramakrishna Raghutu,[3] Ramakrishna S. S. Nuvvula,[3] Polamarasetty P. Kumar,[3] Ilhami Colak,[4] and Baseem Khan[5]

[1]*Department of ECE, GMR Institute of Technology, Rajam, India*
[2]*Department of ECE, JNTU-GV College of Engineering, Vizianagaram, India*
[3]*Department of Electrical and Electronics Engineering, GMR Institute of Technology, Rajam, India*
[4]*Department of Electrical and Electronics Engineering, Faculty of Engineering and Architecture, Nisantasi University, Istanbul, Turkey*
[5]*Department of Electrical and Computer Engineering, Hawassa University, Hawassa, Ethiopia*

Correspondence should be addressed to Baseem Khan; baseem.khan1987@gmail.com

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Stationary random-access memory (SRAM) undergoes an expansion stage, to repel advanced process variation and support ultra-low power operation. Memories occupy more than 80% of the surface in today's microdevices, and this trend is expected to continue. Metal oxide semiconductor field effect transistor (MOSFET) face a set of difficulties, that results in higher leakage current ($I_{leakage}$) at lower strategy collisions. Fin field effect transistor (FinFET) is a highly effective substitute to complementary metal oxide semiconductor (CMOS) under the 45 nm variant due to advanced stability. Memory cells are significant in the large-scale computation system. SRAM is the most commonly used memory type; SRAMs are thought to utilize more than 60% of the chip area. The proposed SRAM cell is developed with FinFETs at 16 nm knot. Power, delay, power delay product (PDP), $I_{leakage}$, and stationary noise margin (SNM) are compared with traditional 6T SRAM cells. The designed cell decreases leakage power, current, and read access time. While comparing 6T SRAM and earlier low power SRAM cells, FinFET-based 10T SRAM provides significant SNM with reduced access time. The proposed 10T SRAM based on FinFET provides an 80.80% PDP reduction in write mode and a 50.65% PDP reduction in read mode compared to MOSEFET models. There is an improvement of 22.20% in terms of SNM and 25.53% in terms of $I_{leakage}$.

1. Introduction

Memory cells were designed using complementary metal oxide semiconductor (CMOS), but at lower technology nodes. CMOS suffered from a number of drawbacks, such as subthreshold leakage current ($I_{leakage}$) and gate-induced barrier lowering (GIBL), whereas FinFET technology is capable of solving these issues [1]. Bulk CMOS devices are limited to short channel widths of the less than 45 nm, whereas FinFETs can use technology knots as small as 7 nm without sacrificing conducting capabilities. Since the majority of devices are developed in nano range, memory design must utilize the same [2]. Additionally, FinFETs replace MOSFETs, to overcome all drawbacks [3]. Memory cell's read-out path, threshold voltage and stacking scheme can reduce $I_{leakage}$ for error-free read operation [4]. The structure comparison of FinFET and normal FET is illustrated in Figure 1.

FinFET technology adds a second gate opposite the normal gate to improve controllability for low voltage operations. FinFET requires both gates to function [5]. When these gates attain equal potential, it reaches shorted gate (SG) mode. Three

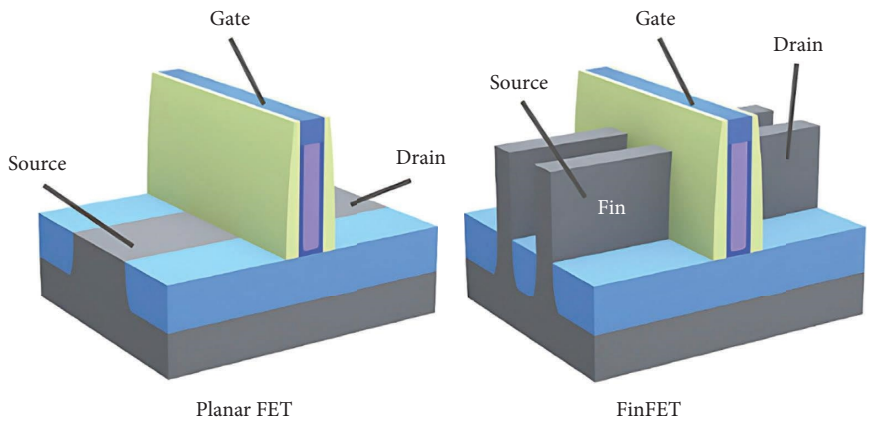

Figure 1: Structure comparison of planar FET and FinFET.

terminal devices with shorted gates are known as SG FinFETs, whereas 4 terminal devices with physical isolation between gates are known as independent-gate (IG) FinFETs. IG FinFET has a greater degree of flexibility than SG FinFET. Two-dimensional view of FinFETs is depicted in Figure 2.

IG operation starts when two gates have dissimilar voltages and the remaining gate is employed to switch devices and control transistor threshold voltage [6–8]. The various height elements of a fin are quantized width (W) and H_{fin} [9, 10]. The quantization width of a SG FinFET and quantization width of IG FinFET can be calculated using the following equation:

$$W_{SG} = 2xH_{fin} + T_{si}, \quad (1)$$

$$W_{IG} = 2xH_{fin}. \quad (2)$$

When calculating quantization width IG FinFETs, the fin thickness (T_{si}) can be ignored. The number of fins is raised in both circumstances to enhance the device's width. The FinFET structure is discussed in this study from the device to the architecture level, as illustrated in Figure 3.

The objective of this research is to develop a 10T SRAM cell using FinFET technology and improve the performance parameters. The power delay product (PDP) need to be reduced to improve the performance and faster response in SRAM. The SNM values for read and hold operations need to be improved. The value of $I_{leakage}$ must be reduced to provide precise switching capabilities. This research ought to explore the effect of FinFET in the design and development of SRAM cells. The advantages of FinFET are explored to provide a better 10T SRAM cell with 16 nm technology. The improvement in features enables these cells to utilize in real-time applications. The proposed cell's performance parameters are shown together with their impressions of process parameter modifications, and they are contrasted with previously proposed SRAM cells.

2. Related Works

The solution for SRAM cell stability issue may be classified into two ways. First one is circuit topologies, and the second is the use of nonconventional MOSFETs. In a 7T SRAM, Akashe and Sharma [11] demonstrated that lowering the power supply lowers gate $I_{leakage}$. The voltage at ground was then increased using the power gating technique, which lowered gate $I_{leakage}$ as well. Finally, effective voltages between the two terminals were adjusted, resulting in a considerable drop in both $I_{leakage}$. The double-feedback 8T SRAM cell described by Vaknim et al. [12] decreases leakage power. In this research, the authors used a power gating technique on a typical 6T SRAM cell, in which the supply voltage is dropped in standby mode by severing the link from the power supply to the cell and also boosting the ground potential to avoid providing a direct path to ground. As a result, the leakage power has decreased. Moradi et al. [13] suggested a new SRAM design that uses body biassing to lower the power supply to 0.3 V, which is extremely low for proper SRAM cell operation.

Zhang et al. [14] looked at three different types of $I_{leakage}$ in bit cells. Leakage reduction strategies such as device body biassing, source biassing with controls, dynamic supply voltage, negative word line voltage, and bit line floating structures were also examined. Ensan et al. [15] designed a single-ended strong 11T cell that is based on feedback-oriented FinFET. Dynamic power reduction occurs because the SRAM cell has single bit interconnection for write and read operations. By using segregated paths and feedback-assisted techniques, respectively, this cell can enhance write SNM (WSNM) and read SNM (RSNM). These enhancements slow down reading and writing speed. It is discovered as reliable close to the threshold. Ahmad et al. [16] proposed cells that use 11T to enhance RSNM and WSNM while lowering power consumption. The configuration, which was created in accordance with 45 nm technological standards, has a 2x larger surface area than a 6T cells.

Sachdeva and Tomar [17] discussed 12T cell that utilize differential writing and one end reading architectures. Even though it uses the power gating write-assist mechanism, read disturbance still affects it and nevertheless displays significant WSNM. This cell, however, is adversely affected by the space and decrease the dynamic read power consumption. According to Nidhi et al. [18], two access transistors and two straightforward cross-coupled inverters are often found in SRAM cells. The access transistors that connect Bit Line (BL)

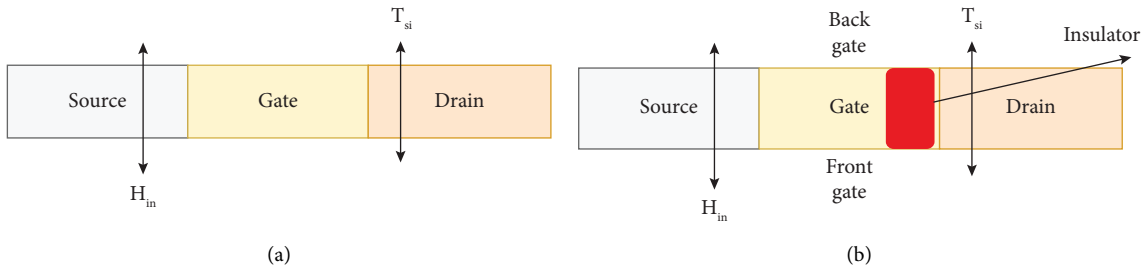

Figure 2: Representation of FinFET (a) SG FinFET, (b) IG FinFET.

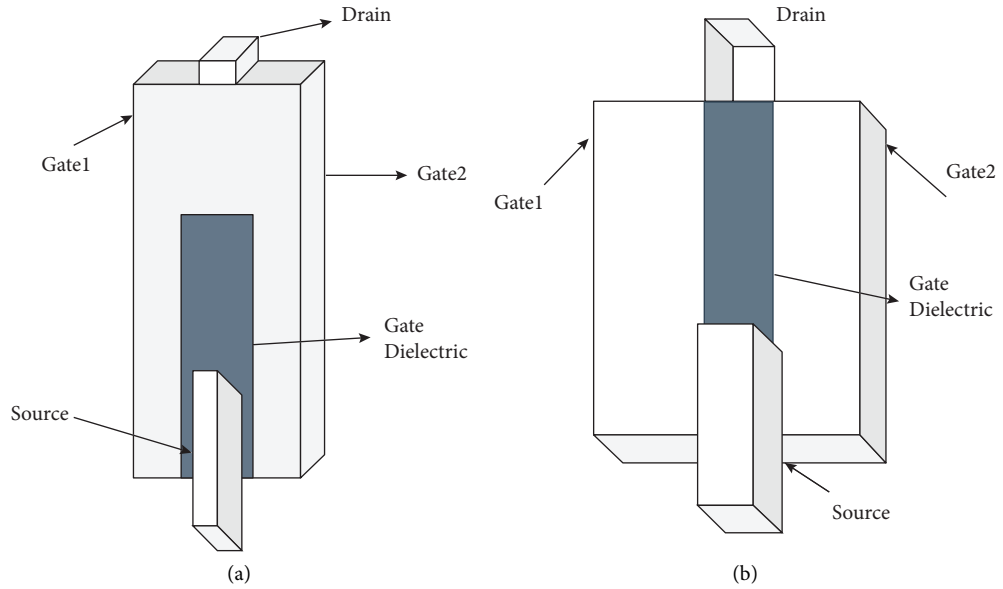

Figure 3: 2D representation of FinFET (a) SG FinFET, (b) IG FinFET.

are switched ON to enable operations. Medium consumption of power and reduced $I_{leakage}$ are the most significant benefits. Lakshmi et al. [19] introduced 8T FinFET SRAM cell to get around the shortcomings of the 6T cell. Low stationary noise margin (SNM) in read mode may exhibit better writing capabilities. As a result, circuit designers have more freedom to optimise and the functions are perfectly isolated.

Yatimi et al. [20] created a 9T cell with double subsection as its main component. Data are kept in the primary subsection. The data kept in the cell affects how transistors (XM8 and XM7) function. XM9 is dependent upon the distinct read signal (RD). Write access is carried out by the write access transistors under the control of WBL and WBLB. Additionally, the read access transistor carries out read access that is managed by RWL. 10T SRAM cell developed by Singh et al. [21] has two access transistors. Transistors in the read path are used to implement the dual threshold-voltage approach, which improves the current ON or else OFF ratio. RWL is connected to both the source and gate of the XM10 and XM9 transistors. Additionally, access FinFETs are connected to WWL, BL, and BLB. The transistors XM7 and XM8 increase the write margin. This research attempts to overcome these technical gaps through our effort in developing a better SRAM cell for future low-power applications. Low power memory circuit design and fault modelling have also been considered in the review.

Shruti Oza [22] conducted study on SRAM technology provides high performance and low power consumption. To reduce short channel effects (SCE) and leakage current in deep-submicron circuits, FinFET has emerged as an alternative to bulk FETs. Its favorable device characteristics make it suitable for nanoscale memory circuits design, especially with the increasing impact of process variations in ultra-deep-submicron technologies. FinFETs are becoming more popular in industry due to their efficiency.

Chakraborty et al. [23] conducted a study on optimizing performance parameters such as power, delay, leakage, and time to market has been a key focus of the IC industry since its inception. Efforts have been increasing over time to achieve the maximum throughput from these settings, particularly with regards to the voltage of the power source. This is the driving force behind Moore's Law.

Pal et al. [24] conducted a study on a comparison of the proposed design to contemporary SRAM designs, including 7T feedback-cutting, FD8T and SEDF9T bitcells, has evaluated design metrics and reliability under process variations.

Minimized dynamic and leakage power are achieved due to single bitline and transistor stacking in the discharge path, respectively

In the study by Jiang et al. [25], there have been few studies comparing the state-of-the-art soft error tolerant SRAM cells in near/subthreshold voltage regarding write stability, read/write access time, and RSNM under temperature and process corner variations. Existing reports mainly focus on conventional soft error vulnerable SRAM cells.

Xue et al. [26] found that memory in computers is used to store information and instructions. It can be temporary or permanent. Contrasting serial access memory is random access memory (RAM), which allows immediate access for reading and writing. Technological advancements enable complex designs on a single chip, having small size, low power consumption, cheap cost, and high speed.

Navaneetha and Bikshalu [27] state that the VLSI industry requires anticipating tolerance of variability to ensure optimized performance of FinFET circuits. In this research, the Cadence Virtuoso tool is used to investigate the impact of fluctuations in voltage and temperature on 7 nm FinFET-based circuits.

In the study by Ahmed et al. [28], soft errors in semiconductor memories can be caused by charged particles striking sensitive nodes. Voltage and technology scaling has drastically increased the vulnerability of SRAMs to soft errors. Table 1 presents the existing characteristics P-type FinFETsof finfet. Table 2 presents the performance and reliability of 6T and 8T AUF SRAM.

3. Materials and Methods

The proposed methodology emphasises in developing less power consuming FinFET-oriented SRAM cells that outperform conventional 6T SRAM cells. A 10T SRAM cell based on a MOSFET is defined, as illustrated in Figure 4. Since read and write word lines are shared, a distinct path for read operation having 4 transistors is created to increase read SNM while maintaining write SNM [31].

Read current (I_{on} or I_{read}) is identified to be the summation of current passing through the drains of transistors N1 (I_{Dn}) as well as P1 (I_{Dp}) throughout the read process. The size limitations of transistor N3, N5, and N8 have a significant impact on I_{ON} in the proposed 10T topology [32]. To evaluate this model for I_{read}, the drain in N3 and N4 must be articulated. The drain current can be analysed as follows:

$$\begin{aligned} I_{\text{read}} &= I_{N3}, \\ V_{\text{GS}} &= V_{\text{DS}} = V_{\text{DD}} - V_Y, \\ I_D &= I_0 \exp\left(\frac{V_{\text{GS}} - V_{\text{th}}}{\eta V_T}\right)\left(1 - e^{\frac{-V_{\text{DS}}}{V_T}}\right), \end{aligned} \tag{3}$$

where η denotes the swing, V_T is the thermal voltage, and I_0 denotes drain current given by

$$I_0 = \mu C_{\text{ox}}\left(\frac{W}{L}\right)(\eta - 1)V_T^2. \tag{4}$$

To keep SNM in the 10T SRAM cell, RSNM is drawn approximately equal. Due to bit line (BL) capacitances, this circuit runs at ultra-low supply voltages [33]. BLs are connected to access transistors, while word lines are frequently connected to BL, BLB, and both transistors (WL). Individual transistors for read access and write pass are used to improve SNM and stability. Read access transistors M7–M9 are utilized, while write access transistors M6, M5 are used. Different access transistors enable transistors to be sized for better read and write stability. $I_{leakage}$ and sneaky current were present in prior SRAM cells, comparable to normal SRAM cells, resulting in read errors [34]. Three transistors are employed in read cycle of this 10T SRAM cell, which employs stacking techniques and improves the I_{ON}/I_{OFF} ratio. Figure 5 depicts the suggested circuit with FinFET for an ultra-low-power SRAM cell.

Since read transistors are not shared with other cells, $I_{leakage}$ does not occur in the path of read operation. As a result, having a higher I_{ON}/I_{OFF} ratio allows more SRAM cells to share the same bit line. Because of the greater I_{ON}/I_{OFF} ratio, the SRAM peripheral for read and write of each column can be shared by more and more cells [35]. The more space, power, and money saved in the design of SRAM for huge storing capacity, the better. The read word line (RWL) is connected to M9 and M8. Word line (WL) is connected to M5, M3, and M1, hence read and write margins have been increased. Reduce static current even further by using access transistors that are twice the size of pull-up transistors. This cell comprises of 3 operating modes, which are further discussed: read, write, and hold [36]. Using access transistors that are twice the size of pull-up transistors to further reduce static current there will be data to be stored on both bit lines. Data are not sent to QB and Q until WWL is enabled. RWL is constantly OFF in write mode. To improve write stability, M10 transistors will supply virtual GND [37]. When the potential of the WWL is low, BLB and BL are detached from SRAM. Since RWL is at a low potential there is an increment in threshold voltage [38]. In the hold state, power consumption and $I_{leakage}$ are reduced, which is advantageous. M10 increases the margin in write operation and decrease static current by strengthening draw-up and pull-down networks.

One of the crucial factors in memory design that determines its intended use is power dissipation, which should be kept to a minimum for bio-medical applications. The following equation can be used to illustrate how a FinFET reduces power usage.

$$P_s = V_{\text{DD}} \times I_{\text{leakage}}, \tag{5}$$

$$\begin{aligned} P_D &= \frac{V_{\text{DD}}^2 \times C_L}{t_p}, \\ P_{\text{SC}} &= \frac{\beta t_{\text{rf}}}{2t_p}\left(V_{\text{DD}}^3 - 8V_t^3\right), \\ T_p &= \frac{T_{\text{pHL}} + T_{\text{pLH}}}{2}, \\ \text{PDP} &= T_p \times P. \end{aligned} \tag{6}$$

Table 1: Existing characteristics P-type FinFETsof finfet [29].

p-FinFET	ION	IOFF (nA/μm)	SS (mV/dec)	DIBL (mV/V)	Ion/Ioff
SUF	1.99 mA/μm	100.44	78.4	74.9	1.98×104
DTCO_F	26.90 μA/μm	0.004	64.34	24.1	6.72×106

Table 2: Performance and reliability of 6T and 8T AUF SRAM [29, 30].

AUF SRAM designs		6T SRAM	8T SRAM
Supply voltage		500 mV	
Standby leakage power (nW)		2.71	2.98
Read	Delay (ns)	2.25	2.85
	Power (nW)	2.415	2.764
Write	Delay (ns)	0.65	0.75
	Power (nW)	2.512	2.109
Static noise margins	HSNM (mV)	181.3	185.8
	RSNM (mV)	135.6	180.2
	WSNM (mV)	420.4	436.2
N-curve	SVNM (mV)	206.79	228.06
	SINM (μA)	84.74	93.02
	WTV (mV)	255.29	271.94
	WTI (μA)	−11.98	−28.49

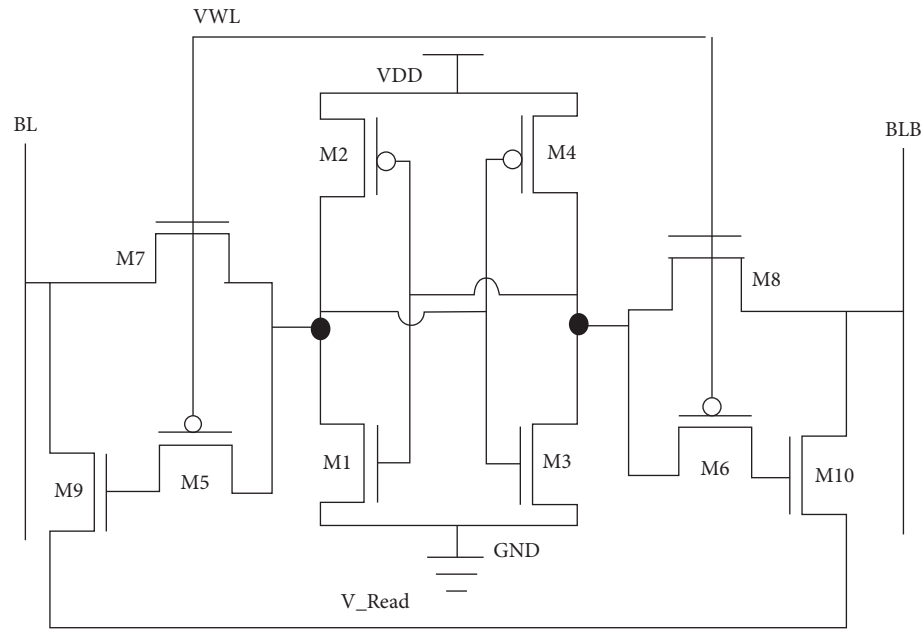

Figure 4: Internal circuit of 10T SRAM cell.

Supply voltage is VDD; low-to-high propagation delay TpLH, high-to-low propagation delay TpHL, propagation delay Tp, static power dissipation Ps, dynamic power dissipation PD, power dissipation when short-circuited PSC, and power delay product PDP are all included in the analysis.

4. Results and Discussion

During the initial phase (0–20 ns) of the spice simulator, WL = 1, delivered data on BLs towards QB and *Q* are provided by M5 and M6. WL is set to logic "1" for write operation. The 2nd stage (20–40 ns) denotes a hold operation for WL = 0. This will keep access to be OFF and delivered data on BLs will not reflect on the node of a cell. WL is activated during third phase (40 to 60 ns), and the data on the BL = "0" (for initial 20 ns) and BL = "1" (for remaining 20 ns). Since the data available in BLB is complementary, data on node *Q* will change in the same way. Half of the V_{DD} is precharged with RBL. While QB is at logic "1," M7 is ON, and when RWL is at logic "1," M8, M9 is ON. As a result, the precharged read BL is cleared by incrementing the BL

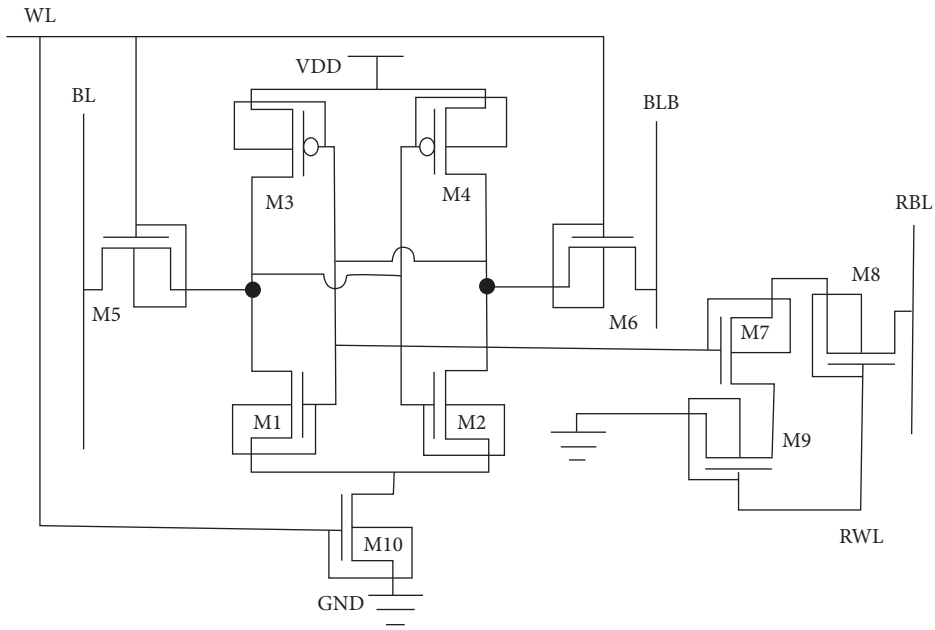

Figure 5: Low-power FinFET-based 10T SRAM.

discharge current. As a result, I_{read} rises, time requirement falls. Table 3 displays the outcomes from the investigation of numerous parameters used in the design of FinFET-oriented SRAM cells at 16 nm.

The SRAM cell size for 10T and 6T with 16 nm is given in Tables 4 and 5. The fin number of FinFET is listed in Table 2. The measurement of FinFET is displayed in Table 5, and the length of all transistors is the same, i.e., 16 nm.

Figure 6 shows how simulation is performed for 200 ns depending on the voltages provided. During the read operation, RWL is at logic "1", as illustrated in Figure 7. QB = "0" for the 1st stage (0–50 ns), and QB = "1" for next stage (50–200 ns).

The performance parameters considered in this work are power, delay, and power delay product (PDP). PDP is calculated by multiplying average power wasted during the delay in propagation. PDP is calculated theoretically using SRAM cell transient analysis. The suggested SRAM cells have the lowest PDP (for write and read), as displayed in Tables 6 and 7. These tables show that the proposed 10T SRAM cell has a lower PDP compared to 6T cell. Figure 8 presents the performance of the proposed SRAM cells in write mode.

Figure 9 presents the performance of the proposed SRAM cells in read mode. Subthreshold current flows in through transistors with no applied input, nevertheless some current is employed. $I_{leakage}$ is kept in hold if WL has 0 V. Table 8 compares the $I_{leakage}$ of different SRAM cells.

Figure 10 presents the $I_{leakage}$ Analysis of SRAM cells. SNM is considered to be the smallest voltage (noise) required to alter the hold data in an SRAM cell and is used to describe the cell's stability. SNM is calculated by performing separate DC analyses on 2 inverters. SNM is calculated using a graph that identifies the largest square fit inside a butterfly curve, when the inverters are connected in cascade. The

Table 3: Parameters for 16 nm FinFET.

Parameter	Mathematical value
V_{DD}	0.8 V
I_{GF}	15 nm
I_{GB}	16 nm
T_{OXF}	1.30 nm
T_{OXB}	1.30 nm
T_{SI}	8.5 nm
H_{FIN}	24 nm
H_{GF}	24 nm

calculated values from SRAM cell butterfly curves are shown in Table 9.

The SNM of 6T version and 10T version are measured in the read and hold states. A significant disadvantage of a 6T topology is high RSNM. Figure 11 depicts the butterfly curves of SNM of 6T and 10T topologies in hold and read operations.

The performance of the proposed 10T SRAM cell based on FinFET is analysed with respect to traditional MOSFET-based 6T and 10T SRAM cells. While considering PDP in write mode, FinFET shows higher level of improvement (68.58% for 6T and 80.80% for 10T). While considering the PDP in read mode, FinFET shows improvement (40.01% for 6T and 50.65% for 10T). This indicates that the proposed 10T SRAM cells based on FinFET consumes less power and the time delay during operations is very low. During the evaluation of $I_{leakage}$, FinFET shows a higher level of improvement (50.22% for 6T and 25.53% for 10T). This indicates that $I_{leakage}$ in proposed 10T SRAM cells based on FinFET is very low compared to MOSFET-based SRAM cells. For 6 T SRAM cells, there is an improvement of 13.63% in HSNM and 15.38% in RSNM for FinFET. For 10T SRAM cells, there is an improvement of 22.20% in HSNM and 22.20% in RSNM for FinFET. This indicates that SNM for proposed 10T SRAM

Table 4: Number of fins of FinFET-based SRAM cells.

SRAM cell (T)	Load transistors	Driver transistors	Access transistors	Read-path transistors
6	2	1	3	—
10	1	1	2	2

Table 5: Width of FinFET in SRAM cells.

SRAM cell (T)	Load transistors (nm)	Driver transistors (nm)	Access transistors (nm)	Read-path transistors
6	128	64	256	Nil
10	128	64	256	48 nm

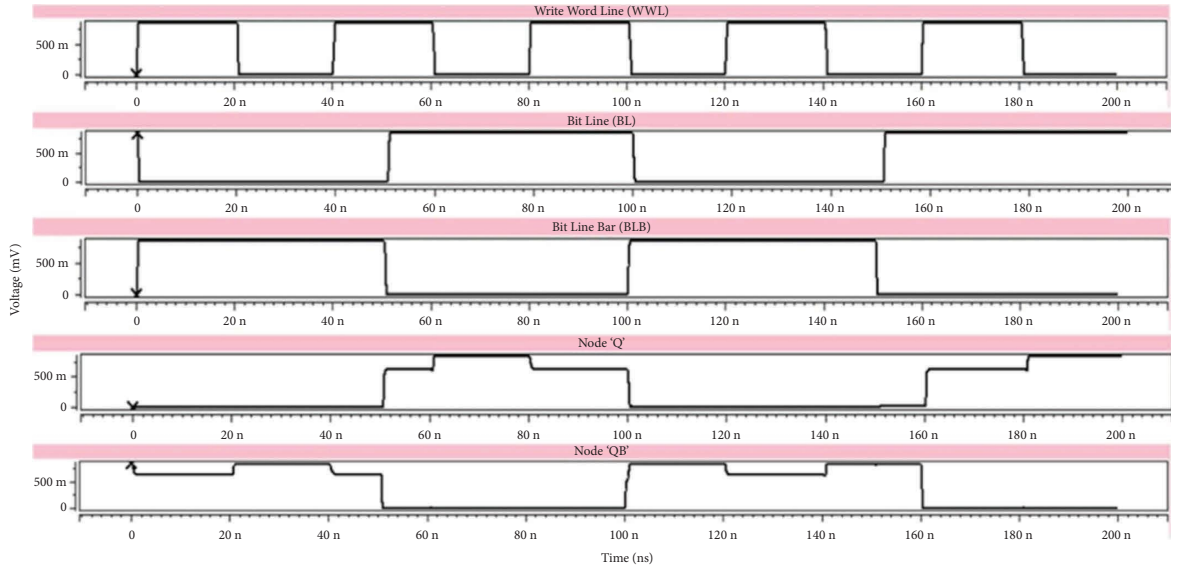

Figure 6: Write and hold operation 10T SRAM.

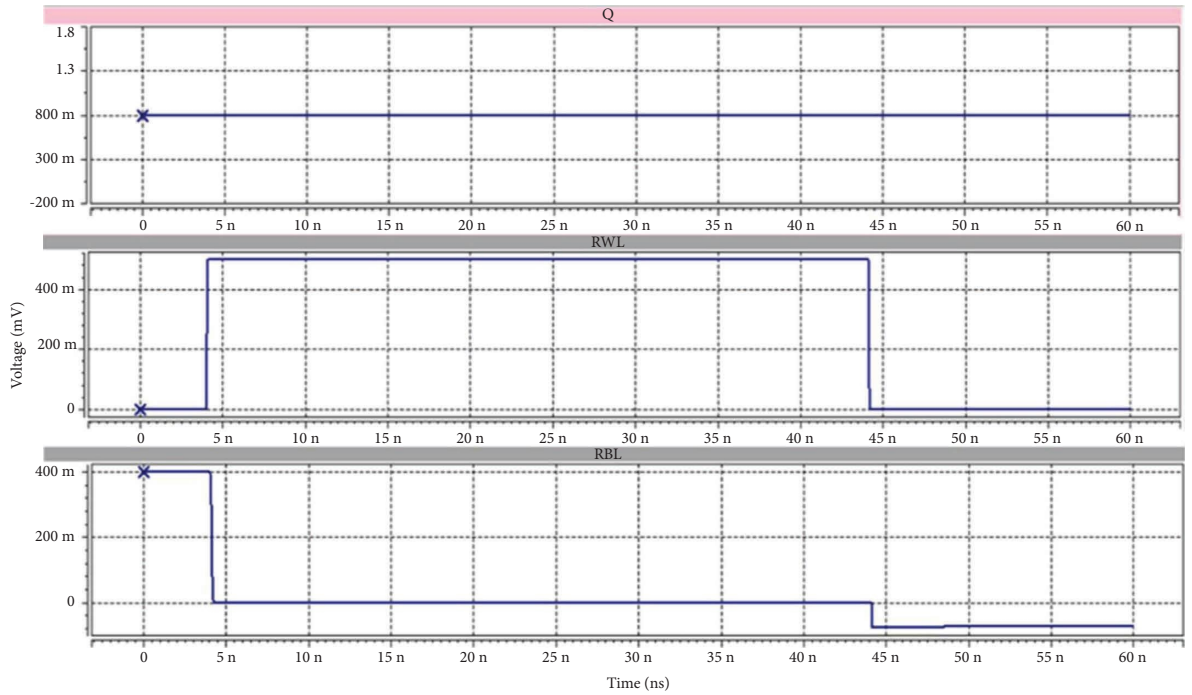

Figure 7: Read operation 10T SRAM.

Table 6: Performance of proposed SRAM cells in write mode.

SRAM (T)	Transistor	Power (nW)	Delay (ns)	PDP (nJ)	Percentage improvement
6	MOSFET	78.92	60.02	4736	68.58
	FinFET	24.53	60.69	1488	
10	MOSFET	70.46	44.69	3148	80.80
	FinFET	18.82	32.02	602	

Table 7: Performance of proposed SRAM cells in read mode.

SRAM (T)	Transistor	Power (nW)	Delay (ns)	PDP (nJ)	Percentage improvement
6	MOSFET	31.234	0.27	8.43	40.01
	FinFET	28.321	0.16	4.53	
10	MOSFET	16.7	0.1825	3.04	50.65
	FinFET	12.52	0.12	1.50	

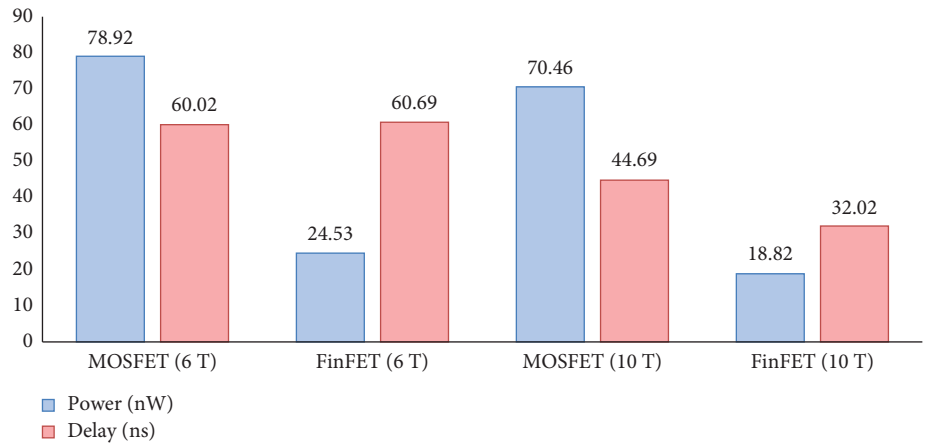

Figure 8: Performance of proposed SRAM cells in write mode.

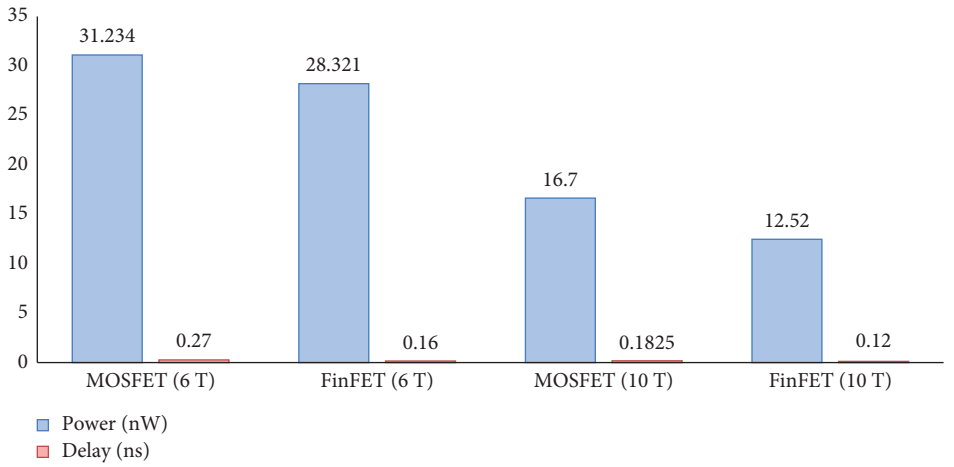

Figure 9: Performance of proposed SRAM cells in read mode.

Table 8: $I_{leakage}$ analysis of SRAM cells.

SRAM (T)	Transistor	$I_{leakage}$ (nA)	Percentage improvement
6	MOSFET	44.608	50.22
	FinFET	22.204	
10	MOSFET	39.169	25.53
	FinFET	29.439	

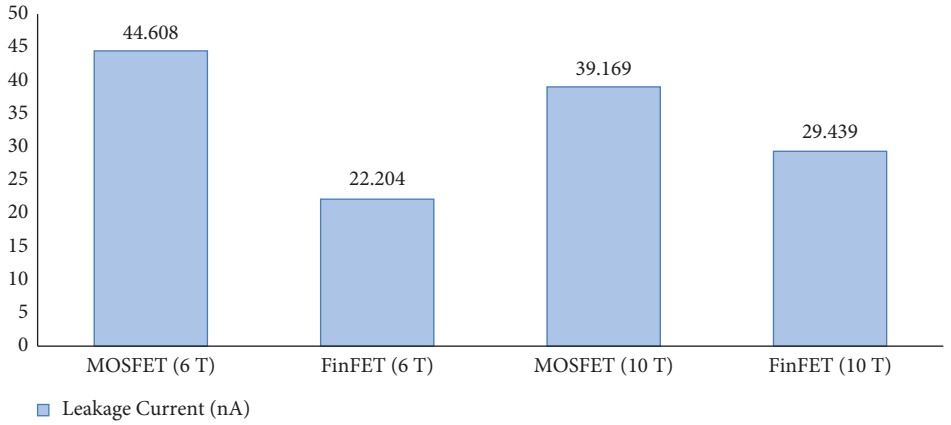

Figure 10: $I_{leakage}$ analysis of SRAM cells.

Table 9: SNM evaluation.

SRAM (T)	SNM (mV)	Transistor		Improvement (%)
		MOSFET	FinFET	FinFET
6	HSNM	190	220	13.63
	RSNM	110	130	15.38
10	HSNM	210	270	22.20
	RSNM	210	270	22.20

cells based on FinFET is large while comparing MOSFET-based SRAM. The minimum data retention voltage (DRV) of the proposed SRAM cell is 68 mV.

The performance of the proposed 10T FinFET SRAM cell is compared with state-of the art models such as 7T, TA8T, 9T, PPN10 T, and D2p11T. The PDP of the proposed model is compared with other models, as illustrated in Figure 12.

The PDP of the proposed model is lowest for read operation as well as write operation. TA8T exhibits the maximum PDP of 3.4 nJ in read operation. The proposed model provides 55.85% less PDP than the TA8T method. The second lowest value of 2.17 nJ is provided by PPN10T method which is 30% higher than proposed scheme. The 7T method exhibits the maximum PDP of 1310 nJ in write operation. The proposed model provides 54.04% less PDP than the 7T method. The second lowest value 667 nJ is provided by the TA8T method which is 9.7% higher than proposed scheme. The SNM of the proposed model is compared with other models, as illustrated in Figure 13.

The SNM of the proposed model is highest for read operation as well as hold operation. The proposed scheme exhibits the maximum value of 270 mV for both HSNM and RSNM. The proposed model provides 22 mV more in the case of RSNM and 60 mV more in the case of HSNM when compared to the 7T scheme. The $I_{leakage}$ of the proposed model is compared with other models, as illustrated in Figure 14.

The $I_{leakage}$ of proposed model is 29.439 mA, which is the lowest compared to other methods. The proposed model provides 25.404 mA less than the PPN10T scheme. This indicates that the proposed 10T circuit offers high read stability, low power consumption, and excellent performance. Any innovative topology used to limit read or write PDP while preserving stability may result in a trade-off of increased bitcell access time. The 10T SRAM structure offers several advantages over 6T SRAM, such as improved bitcell stability and a shorter access time. However, it also requires more transistors than the 6T SRAM structure in order to provide these benefits, which can lead to a decrease in the SRAM circuit's density within the CPU. This increased number of transistors can reduce the overall efficiency of the CPU, as the larger area requirement restricts the amount of space available on the chip. Furthermore, the additional areas needed for fabrication can limit the efficiency of the CPU due to the increased overhead. In summary, 10T SRAM

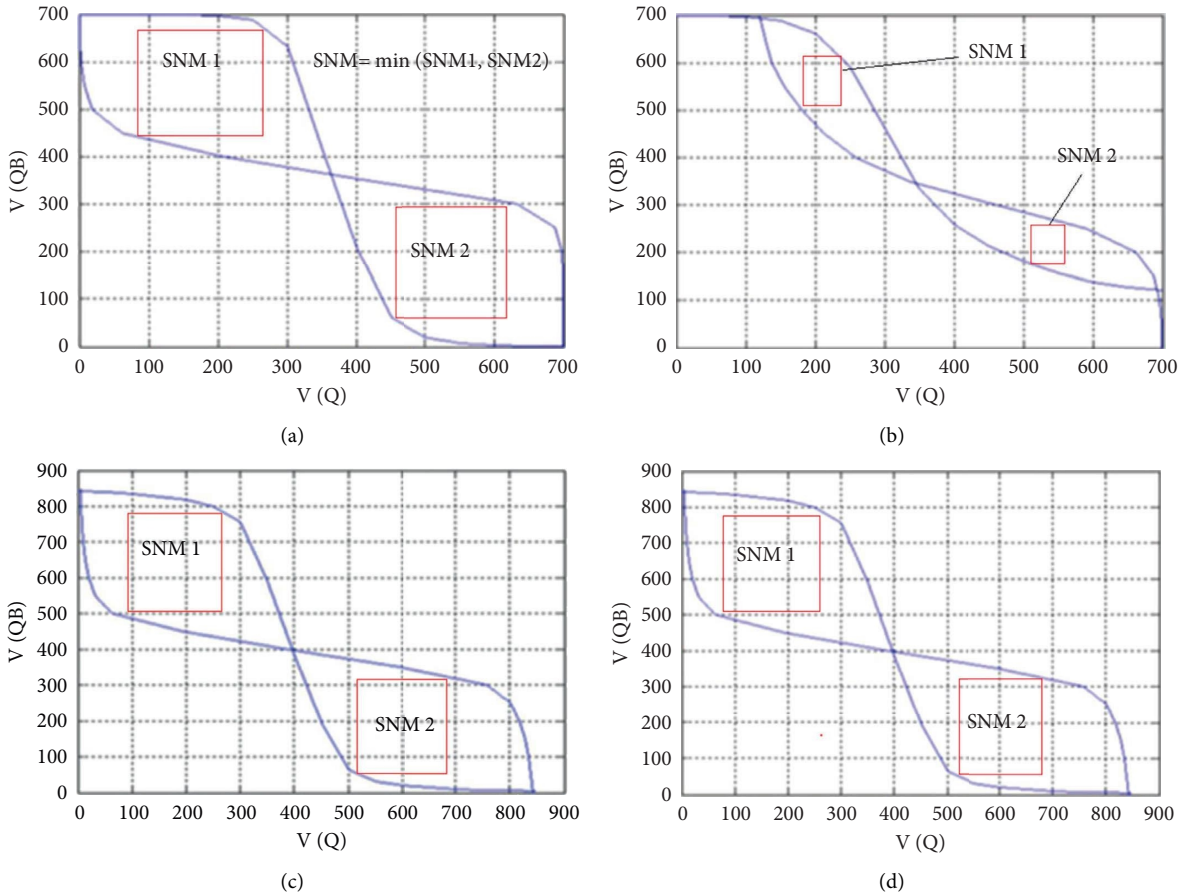

Figure 11: Butterfly curve of SNM: (a) HSNM at 16 nm MOSFET, (b) RSNM at 16 nm MOSFET, (c) HSNM at 16 nm FinFET, and (d) RSNM at 16 nm FinFET 10T SRAM cell.

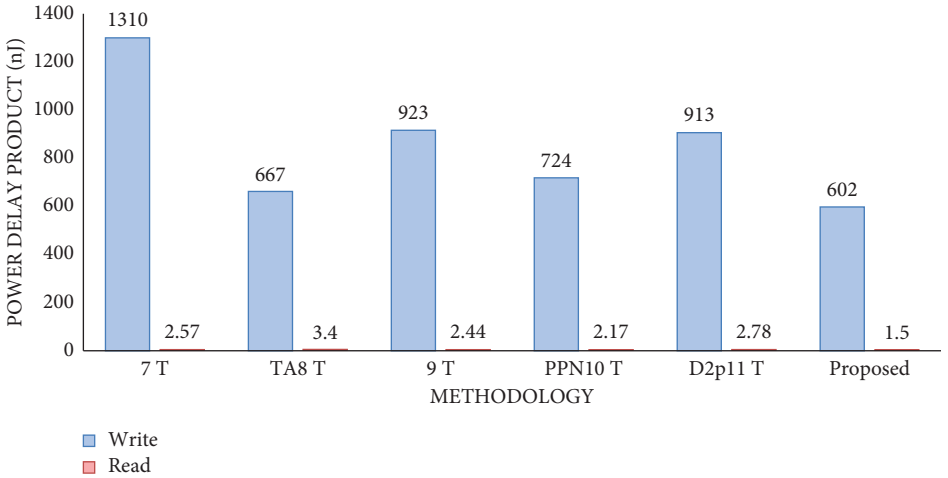

Figure 12: Comparison of PDP.

provides better bitcell stability, reduced access time, and improved read/write capabilities compared to 6T SRAM, but at the cost of decreased SRAM circuit density inside the CPU and greater fabrication costs. Thus, when considering the advantages and disadvantages of both 10T and 6T SRAM structures, designers must carefully evaluate the tradeoff between features and SRAM density before deciding which to use.

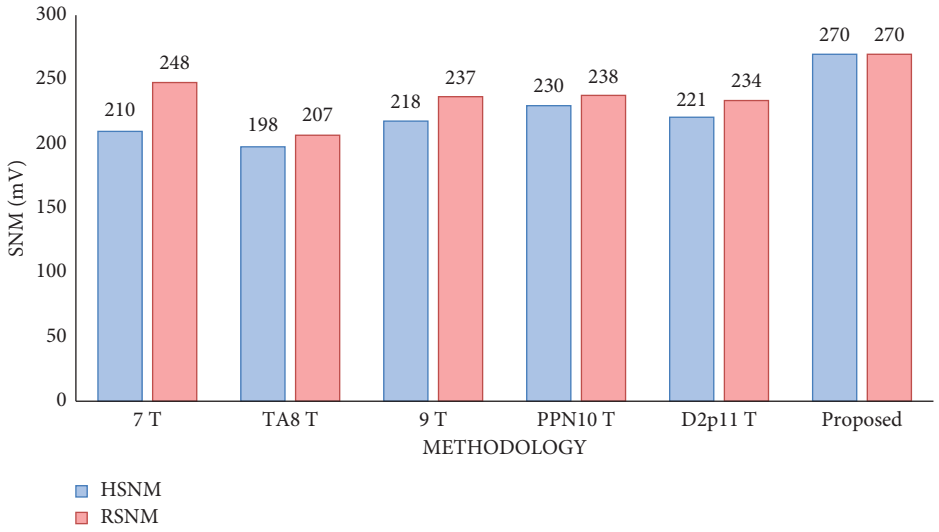

Figure 13: Comparison of SNM.

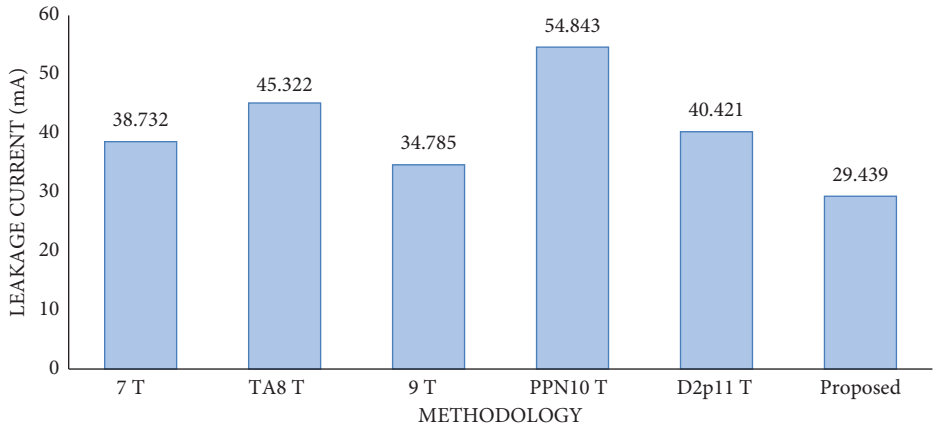

Figure 14: Comparison of leakage current.

5. Conclusion

This paper recommends the usage of a 10T SRAM cell incorporating FinFET for ultra-low dissipation in power along with read and write stability. The developed architecture based on FinFET must run at a higher range of frequencies because of the large I_D and safer operation in the zone of subthreshold. The proposed SRAM cell reduced the PDP and $I_{leakage}$. It improved stability of read operation while comparing with 6T counterpart. This cell is designed with FinFETs at 16 nm technology knot. Various SRAM cells with ultra-low power applications can be created as a result of this research. In contrast with 6T SRAM cell and earlier low power SRAM cells, the proposed cell exhibits significant SNM along with high-speed access. Because of high I_D requirements and its effective operations throughout the region of subthreshold, the characteristic of developed design must function at high frequency. This design can further be utilized to build memory elements as small as 32 nm without the short channel effects (SCE) that affect CMOS technology. In comparison to MOSEFET models, the proposed 10T SRAM based on FinFET offers PDP reductions of 80.80% in write mode and 50.65% in read mode. Both SNM and $I_{leakage}$ have improved by 22.20% and 25.53%, respectively. Future work based on the development of the 10T SRAM cell incorporating FinFET could focus on applying this technology in other ultra-low power applications. Additionally, further research could explore potential use cases of the 10T SRAM cell in the construction of larger memory components such as caches and memories. The area efficiency of the proposed 10T SRAM based on FinFET is higher than that of traditional 6T SRAM and other low-power SRAM cells. Compared to MOSEFET models, it provides an 80.80% PDP reduction in write mode and a 50.65% PDP reduction in read mode.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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