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*Research Article*

# Optimal Design of Voltage Reference Circuit and Ring Oscillator Circuit Using Multiobjective Differential Evolution Algorithm

**Sandeep K. Dash**,[1] **Bishnu Prasad De**,[1] **Pravin K. Samanta**,[1] **Bhargav Appasani**,[1] **Rajib Kar**,[2] **Durbadal Mandal**,[2] **and Nicu Bizon**[3,4,5]

[1]*School of Electronics Engineering, KIIT University, Bhubaneswar 751024, Odisha, India*
[2]*Department of Electronics & Communication Engineering, NIT Durgapur, Durgapur, West Bengal 713209, India*
[3]*Faculty of Electronics, Communication and Computers, University of Pitesti, Pitesti 110040, Romania*
[4]*University Politehnica of Bucharest, Splaiul Independentei Street No. 313, Bucharest 060042, Romania*
[5]*ICSI Energy, National Research and Development Institute for Cryogenic and Isotopic Technologies, 240050 Ramnicu Valcea, Romania*

Correspondence should be addressed to Bhargav Appasani; bhargav.appasanifet@kiit.ac.in

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This paper deals with the optimal design of different VLSI circuits, namely, the CMOS voltage reference circuit and the CMOS ring oscillator (RO). The optimization technique used here is the multiobjective differential evolution algorithm (MDEA). All the circuits are designed for 90 nm technology. The main objective of the CMOS voltage reference circuit is to minimize the voltage variation at the output. The targeted value of the reference voltage is 550 mV. A CMOS ring oscillator (RO) is designed depending on the performance parameters such as power consumption and phase noise. The optimal transistor sizing of each circuit is obtained from MDEA. Each circuit is implemented in SPICE by taking the optimal dimensions of the transistors, and the performance parameters are achieved. The designed voltage reference circuit achieves a reference voltage of 550 mV with 600 nW power dissipation. The reference voltage variation of 8.18% is observed due to temperature variation from −40°C to + 125°C. The MDEA-based optimal design of RO oscillates at 2.001 GHz frequency, has a phase noise of −87 dBc/Hz at 1 MHz offset frequency, and consumes 71 $\mu$W power. This work mainly aims to optimize the MOS transistors' sizes using MDEA for better circuit performance parameters. SPICE simulation has been carried out by using the optimal values of MOS transistor sizes to exhibit the performance parameters of the circuit. Simulation results establish that design specifications are closely met. SPICE results show that MDEA is a better technique for the optimal design of the above-mentioned VLSI circuits.

## 1. Introduction

Circuit sizing is a tedious problem for the IC engineer. Evolutionary techniques are efficient in solving circuit sizing problems. J. H. Holland invented the genetic algorithm (GA) [1]. GA is utilized for op-amp design in [2]. With the help of GA, power dissipation is optimized for an active load differential amplifier [3]. GA-based VLSI circuit partitioning is reported in [4]. The floorplan area is optimized using GA in [5]. A CMOS circuit synthesizer called DARWIN [6] is proposed for op-amp design. Particle swarm optimization (PSO) [7, 8] is a proficient evolutionary method. PSO-based design of op-amp is reported in [9, 10]. PSO is applied for the optimal design of current conveyors [11]. Storn and Price introduced differential evolution (DE) [12]. DE is used for analog circuit synthesis in [13]. DE-based channel routing for the VLSI circuit is proposed in [14]. DE is useful for VLSI floorplanning [15]. A hybrid particle swarm optimization (PSO) method is proposed for the optimization of an operational amplifier [16] and a differential amplifier [17]. In [18], a rule-guided genetic algorithm (RG-GA) is employed to design an operational amplifier. A machine learning-

assisted sizing technique [19] is introduced to design amplifiers and a comparator in analog circuits. Bayesian optimization approaches have been reported for analog circuit sizing in [20, 21]. Deep reinforcement learning [22] is utilized for sizing a two-stage operational amplifier. Various evolutionary optimization techniques [23–28] are applied to the circuit sizing of other analog VLSI circuits. Many optimization problems exhibit a multiobjective nature, and evolutionary approaches prove to be beneficial for solving such problems. In 2003, Babu and Jehan introduced the multiobjective differential evolutionary algorithm (MDEA) [29]. The multiobjective DE [30] is employed to address the power dispatch problem, and the PID controller tuning using a multiobjective DE is discussed in [31]. Several studies on multiobjective numerical optimization have been documented in [32–35]. A CMOS voltage reference circuit is proposed in [36, 37], and a nine-stage ring oscillator circuit is designed in [38, 39].

The paper's contribution is the application of a state-of-the-art algorithm for the optimal design of a voltage reference circuit and a ring oscillator circuit. This article aims to optimize the transistor's dimensions for each circuit for better performance parameters. The paper is written as follows: the optimization problem for each circuit is formulated in Section 2. MDEA is described in the next section. In Section 4, the simulation results are explained. Section 5 concludes the article.

## 2. Optimization Problem Formulation

The CMOS voltage reference circuit is shown in Figure 1, and the nine-stage ring oscillator circuit is shown in Figure 2. MDEA is utilized for the optimal design of these two circuits.

*2.1. Design of a CMOS Voltage Reference Circuit.* For MOSFET, the drain current $I_D$ at the subthreshold region is described as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \times \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right),$$
$$I_0 = \mu C_{OX}(\eta - 1)V_T^2, \tag{1}$$

where $K = W/L$, $\mu$ denotes the carrier mobility, $C_{ox}$ denotes the oxide capacitance/area, $V_T$ denotes the thermal voltage, $V_{TH}$ represents the threshold voltage for MOSFET, and $\eta$ denotes the subthreshold slope factor.

For large values of $V_D$, $I_D$ is not dependent on $V_{DS}$ and is represented by

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right). \tag{2}$$

$V_{GS1}$ in $M_1$ equals the sum of $V_{GS2}$ in $M_2$ and $V_{DSR1}$ in $M_{R1}$.

$$V_{GS1} = V_{GS2} + V_{DSR1}. \tag{3}$$

The current flowing through transistors $M_1$ and $M_2$ is equal to $I_P$. The value of $V_{DSR1}$ is given by

$$V_{DSR1} = \eta V_T \ln\left(\frac{K_2}{K_1}\right). \tag{4}$$

The resistance of the MOS transistor $M_{R1}$ is given by

$$R_{MR1} = \frac{1}{K_{R1}\mu C_{OX}(V_{REF} - V_{TH})}. \tag{5}$$

The current $I_P$ is represented as

$$I_P = K_{R1}\mu C_{OX}(V_{REF} - V_{TH})\eta V_T \ln\left(\frac{K_2}{K_1}\right). \tag{6}$$

The current flowing through $M_4$ and $M_6$ is $3I_P$ and $2I_P$, respectively. The output reference voltage $V_{REF}$ is represented as

$$V_{REF} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7},$$
$$V_{REF} = V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_4 I_0}\right) + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right). \tag{7}$$

$V_{TH}$ and $V_T$ have negative and positive $TC$, respectively; the $V_{REF}$ can be obtained with zero $TC$ by setting the transistor's dimensions.

The design problem is formulated as follows:

(1) Preserve the dimension of current mirror transistors $MC_1$, $MC_2$ and $M_1$, $M_2$.

(2) Preserve the dimension of transistors $MC_3$, $MC_4$, and $MC_5$ for matching purpose.

(3) The current through $MC_3$, $MC_4$, and $MC_5$ must be greater than the leakage currents, i.e., 1 nA.

(4) Preserve the dimension of transistors $M_3$, $M_4$, $M_5$, $M_6$, and $M_7$ for matching purpose.

(5) The optimization problem aims to reduce the variation for the $V_{REF}$ within the temperature range from −40°C to 125°C. The variation of $V_{REF}$ with temperature is represented as

$$Variation_{(V_{REF})} = \frac{\Delta}{V_{REF}} 100,$$
$$\Delta = \max(V_{\max}, V_{\min}),$$
$$V_{\max} = abs\left(\max\left(V_{REF} - V_{T\arg et}\right)_{-40^0C\_to\_125^0C}\right),$$
$$V_{\min} = abs\left(\min\left(V_{REF} - V_{T\arg et}\right)_{-40^0C\_to\_125^0C}\right), \tag{8}$$

where $V_{\max}$ and $V_{\min}$ denote the absolute maximum and minimum of the difference between $V_{\mathrm{REF}}$ and $V_{\mathrm{Target}}$ within the temperature range −40°C to 125°C.

(6) The cost function (CF) is formulated as

$$CF = \text{Variation}_{(V_{REF})} + V_{\mathrm{DD}} I_P. \tag{9}$$

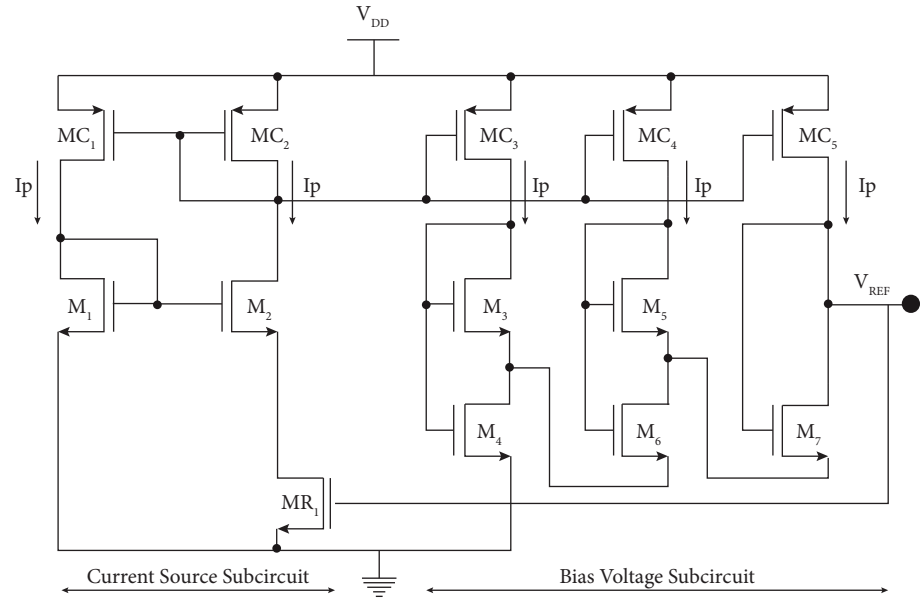


Figure 1: CMOS voltage reference circuit.

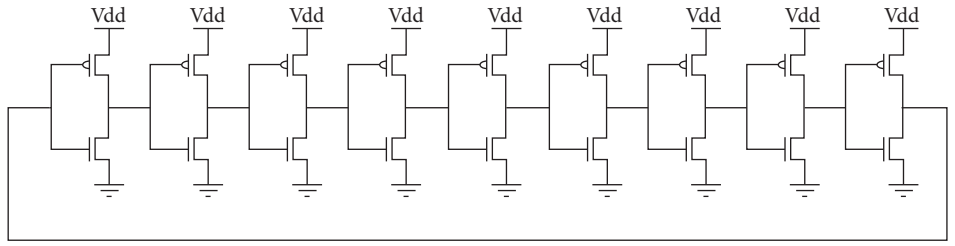


Figure 2: Nine-stage RO circuit.

*2.2. Design of the CMOS Ring Oscillator Circuit.* The nine-stage RO circuit is shown in Figure 2. The oscillation frequency ($f_{osc}$) is defined as

$$f_{osc} = \frac{1}{\eta N\left(t_r + t_f\right)} = \frac{I_D}{\eta N C_{tot} V_{DD}}, \tag{10}$$

where $\eta$ varies between 0.7 and 0.9, $N$ denotes the number of CMOS inverter stages, $I_r$ ($t_f$) denotes the rise (fall) time, $I_D$ is the drain current, $C_{\text{tot}}$ represents the total capacitance, and $V_{DD}$ represents the supply.

The total capacitance $C_{\text{tot}}$ is given by

$$C_{tot} = \frac{5}{2} C_{ox}\left(L_n W_n + L_p W_p\right), \tag{11}$$

where $L_n$ ($L_p$) denotes the length of NMOS (PMOS) and $W_n$ ($W_p$) represents width of the NMOS (PMOS).

The average power dissipation [40] of the RO is represented as

$$P_{avg} = \eta N C_{tot} V_{DD}^2 f_{osc}. \tag{12}$$

The phase noise [40] is defined as

$$L\{\Delta\delta f\} = \frac{8}{3\eta} \frac{kT}{P_{avg}} \frac{V_{DD}}{V_{char}} \frac{f_{osc}^2}{\Delta\delta f^2}, \tag{13}$$

where $V_{char} = \Delta\delta V/\gamma$, $\delta f$ is the offset frequency, $\delta V$ denotes the gate over drive voltage, $T$ represents the absolute temperature, and $k$ denotes the Boltzmann constant, $\gamma = 2/3$

The figure of merit (FOM) is given as

$$FOM = 10\log_{10}\left[L\{\Delta\delta f\} \frac{\Delta\delta f^2}{f_{osc}^2} \frac{P_{avg}}{1mW}\right]. \tag{14}$$

The optimization problem can be represented as follows: (1) minimization of L{$\delta f$}, (2) minimization of the power, and (3) minimize FOM.

The design constraints are given as follows:

$$\begin{aligned} f_{osc} &= 2\,\text{GHz}, \\ W_{n,\min} \le W_n &\le W_{n,\max}, \\ W_{p,\min} \le W_p &\le W_{p,\max}, \\ L_{\min} \le L &\le L_{\max}, \\ L_n &= L_p = L. \end{aligned} \tag{15}$$

The MDEA is applied to get the design parameters for the RO.

Step 1: Initialize $D$ (dimension of optimization problem), $N_p$ (population size), $F$ (scaling factor), CR (crossover rate), and $g_{\max}$ (Maximum iteration cycle)

Step 2:Initialize for $g = 0$ the $D$-dimensional $N_p$ populations as $\vec{x}_{i,g} = \{x_{1,i,g}, x_{2,i,g}, ..., x_{D,i,g}\}$ (where $i = 1, 2, ..., N_P$) within the bounds $\vec{x}_{\min} = \{x_{1,\min}, ..., x_{D,\min}\}$ and $\vec{x}_{\max} = \{x_{1,\max}, ..., x_{D,\max}\}$..

Step 3: for $i = 1$ to $N_p$

{

for $j = 1$ to $D$

{

$x_{i,j} = x_{j,\min} + rnd \times (x_{j,\max} - x_{j,\min},)$

}

}

Step 4: for $g = 1$ to $g_{\max}$

{

for $i = 1$ to $N_p$

{

$\vec{v}_{i,g} = \{v_{1,i,g}, v_{2,i,g}, ..., v_{D,i,g}\}$

$\vec{v}_{i,g} = \vec{x}_{r_1,g} + F(\vec{x}_{r_2',g} - \vec{x}_{r_3',g})$ where $r_1, r_2, r_3 \in \{1, 2, ...., N_p\}; r_1 \neq r_2 \neq r_3 \neq i$

Compute $\vec{u}_{i,g}$ for each $\vec{x}_{i,g}$ where $\vec{u}_{i,g} = \{u_{1,i,g}, u_{2,i,g}, ..., u_{D,i,g}\}$.

$j_{rand} = [\text{rand}(0,1) \text{ x } D]$;

for $j = 1$ to $D$.

{

$$u_{j,i,g} = \begin{cases} v_{j,i,g} \text{if } (\text{rand}_{i,j}(0,1) \leq C_r \text{ or } j = j_{rand}), \\ x_{i,j,g} \text{ otherwise.} \end{cases}$$

}

Determine whether the target vector survives for the next generation.

$$\vec{x}_{i,g+1} = \begin{cases} \vec{u}_{i,g} \text{ if } f(\vec{u}_{i,g}) \leq f(\vec{x}_{i,g}), \\ \vec{x}_{i,g} \text{ otherwise.} \end{cases}$$

}

}

Algorithm 1: MODE Algorithm.

## 3. Multiobjective Differential Evolutionary Algorithm (MDEA)

The multiobjective differential evolution (MODE) algorithm [29–31] is a specialized variant of the differential evolution (DE) algorithm developed to tackle multiobjective optimization problems. By integrating the principles of differential evolution and Pareto dominance, MODE enables the exploration of trade-off solutions that balance conflicting objectives. The following are the key steps involved in the MODE algorithm:

(1) Initialization: An initial population of candidate solutions is generated randomly within the search space.

(2) Mutation: Each individual in the population undergoes mutation, where a mutant solution is created by perturbing the individual using a mutation operator. The mutation operator typically involves the difference between multiple individuals.

(3) Crossover: The mutant solutions are combined with the original individuals to produce trial solutions. The crossover process merges the components of the mutant and original solutions.

(4) Selection: The trial solutions are evaluated, and individuals are selected for the next generation based on Pareto dominance. The selection process compares solutions, determining their superiority or noninferiority relative to others in the population. Dominated solutions are eliminated, while nondominated solutions are retained.

(5) Termination: Steps 2 to 4 are repeated until a termination criterion is met. This criterion may involve a maximum number of generations, the attainment of a specific convergence level, or other predefined stopping conditions.

The MODE algorithm employs a population-based evolutionary search strategy to explore the solution space and discover diverse solutions that represent trade-offs among multiple objectives. Its objective is to approximate the Pareto-optimal front, which comprises the set of nondominated solutions. The algorithmic steps are described as follows: (see Algorithm 1).

Apply the naïve and slow approach [32] to eliminate the dominant solutions from the previous generation.

Output the nondominated solutions.

## 4. Simulation Results and Discussions

The MDEA technique is executed in MATLAB for the analog VLSI circuits depicted in Figures 1 and 2, respectively. Table 1 displays the parameters of MDEA. The optimal transistor dimensions for each circuit are obtained from

Table 1: Parameters for MDEA.

| Parameters | Values |
|---|---|
| $N_p$ | 20 |
| $F$ | 0.5 |
| $CR$ | 0.3 |
| Maximum generation counter ($g_{max}$) | 100 |

MDEA. Cadence is used to simulate the circuits for authentication purposes. A discussion of the results is given below.

*4.1. Simulation Results for the CMOS Voltage Reference Circuit.* The constraints for the first circuit are given as $1\,\mu m \le L \le 20\,\mu m$, $0.1\,\mu m \le W \le 50\,\mu m$, VDD = 1.2 V, VREF = 550 mV, and IP = 100 nA. Table 2 shows the optimal transistor sizing obtained from MDEA. The voltage reference circuit is implemented with these design parameters in Cadence Virtuoso. The variation of VREF with the temperature is displayed in Figure 3 at different process corners such as TT, SF, FS, FF, and SS. The deviation of VREF from the target value of 0.55 V is less than 10% across different process corners. The variation of VREF with respect to temperature and supply voltage for the TT process is shown in Figure 4. It is observed that the reference voltage varies from 0.53 V to 0.6 V for the TT process. The variation of VREF with respect to temperature and supply voltage for the SS process is shown in Figure 5. It is observed that the reference voltage varies from 0.54 V to 0.61 V for the SS process. The variation of VREF with respect to temperature and supply voltage for the FF process is shown in Figure 6. It is observed that the reference voltage varies from 0.52 V to 0.59 V for the FF process. The variation of VREF with respect to temperature and supply voltage for the SF process is shown in Figure 7. It is observed that the reference voltage varies from 0.53 V to 0.61 V for the SF process. The variation of VREF with respect to temperature and supply voltage for the FS process is shown in Figure 8. It is observed that the reference voltage varies from 0.53 V to 0.59 V for the FS process. The temperature is varied from −40°C to 125°C, the supply voltage is from 1 V to 1.4 V for all the processes, and the maximum variation of the reference voltage from the target value is less than 12.2%. Table 3 demonstrates the different performance parameters of the voltage reference circuit. The power dissipation of the voltage reference circuit is 600 nW. It is evident from Figures 4–8 and Table 3 that the voltage reference circuit is very robust for variation against temperature, supply voltage, and different process corners. MDEA shows better results as compared to SCA-mGWO [30].

*4.2. Simulation Results for the CMOS Ring Oscillator Circuit.* Table 4 presents the constraints and optimal design parameters obtained through the application of the multiobjective differential evolutionary algorithm (MDEA). The ring oscillator (RO) circuit is designed using Cadence Virtuoso with the gpdk090 library. The

Table 2: Transistor sizing of the voltage reference circuit.

| Parameters | Values |
|---|---|
| $W_{MC1}$ | 900 nm |
| $L_{MC1}$ | 4 $\mu$m |
| $W_{MC2}$ | 1.73 $\mu$m |
| $L_{MC2}$ | 8 $\mu$m |
| $W_{MC3}$ | 905 nm |
| $L_{MC3}$ | 4 $\mu$m |
| $W_{MC4}$ | 905 nm |
| $L_{MC4}$ | 4 $\mu$m |
| $W_{MC5}$ | 905 nm |
| $L_{MC5}$ | 4 $\mu$m |
| $W_{M1}$ | 797 nm |
| $L_{M1}$ | 4 $\mu$m |
| $W_{M2}$ | 2.88 $\mu$m |
| $L_{M2}$ | 4 $\mu$m |
| $W_{M3}$ | 242 nm |
| $L_{M3}$ | 8 $\mu$m |
| $W_{M4}$ | 153 nm |
| $L_{M4}$ | 12 $\mu$m |
| $W_{M5}$ | 797 nm |
| $L_{M5}$ | 4 $\mu$m |
| $W_{M6}$ | 310 nm |
| $L_{M6}$ | 4 $\mu$m |
| $W_{M7}$ | 2.95 $\mu$m |
| $L_{M7}$ | 4 $\mu$m |
| $W_{MR1}$ | 156 nm |
| $L_{MR1}$ | 8 $\mu$m |

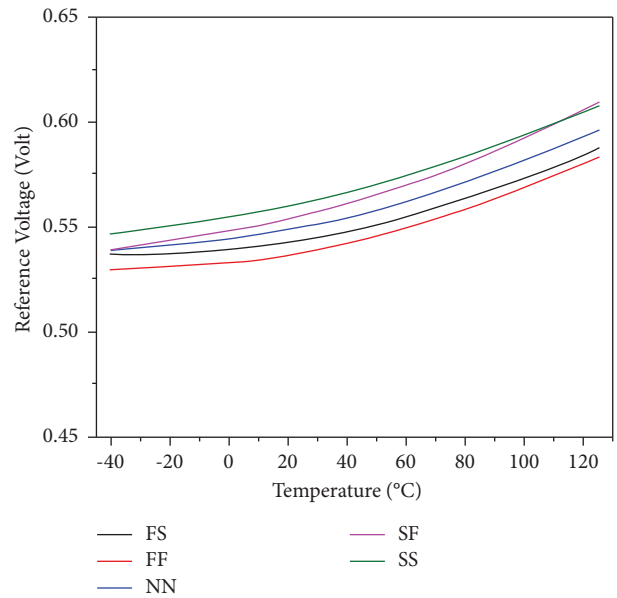


Figure 3: Variation of $V_{REF}$ for different corners.

transient response of the RO is illustrated in Figure 9, showcasing oscillation at a frequency of 2.001 GHz. Figure 10 displays the phase noise plot for the designed RO circuit, revealing a phase noise of −87 dBc/Hz at 1 MHz. The power dissipation plot for the RO circuit is shown in Figure 11, with the optimized circuit dissipating a power of 71 $\mu$W. The achieved figure of merit

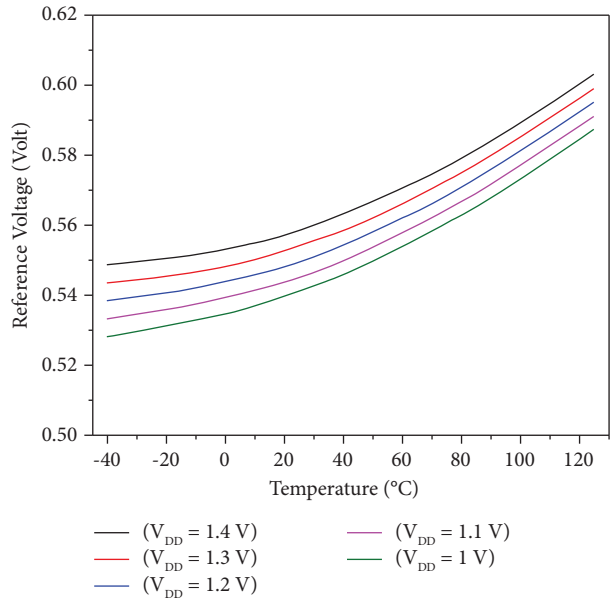


Figure 4: Variation of $V_{REF}$ with temperature and $V_{DD}$ for TT process.

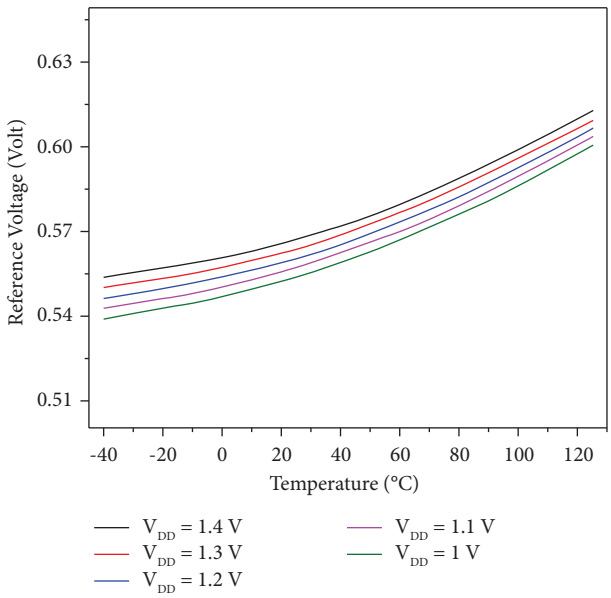


Figure 5: Variation of $V_{REF}$ with temperature and $V_{DD}$ for SS process.

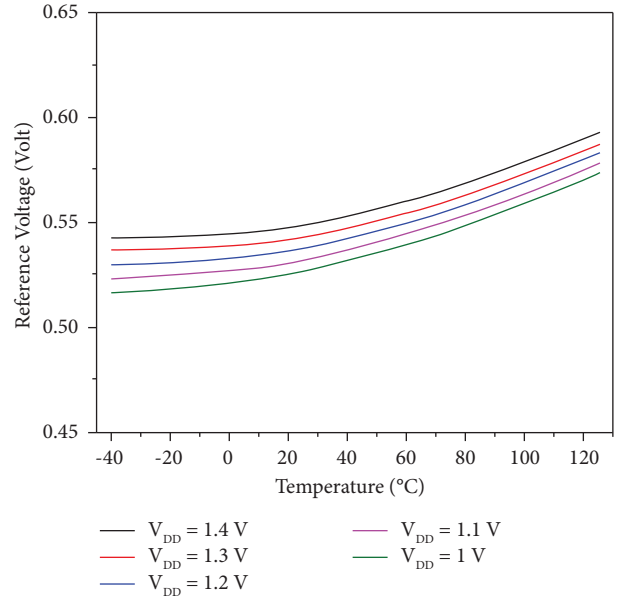


Figure 6: Variation of $V_{REF}$ with temperature and $V_{DD}$ for FF process.

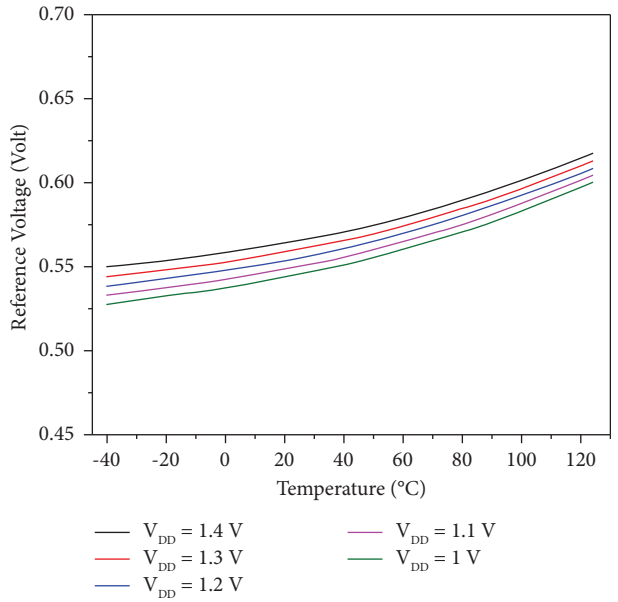


Figure 7: Variation of $V_{REF}$ with temperature and $V_{DD}$ for SF process.

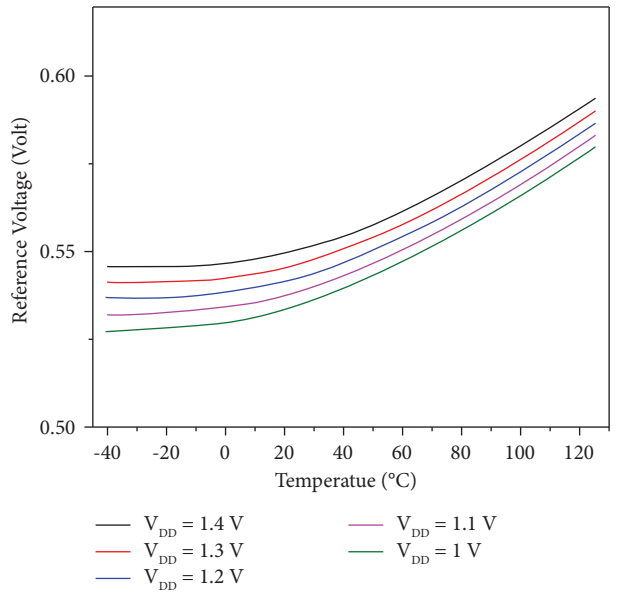


Figure 8: Variation of $V_{REF}$ with temperature and $V_{DD}$ for FS process.

Table 3: Comparison of design performance parameters for the voltage reference circuit.

| Parameters | Values |
|---|---|
| $V_{REF}$ (mV) | 550.01 |
| $V_{\max}$ (mV) | 45 |
| $V_{\min}$ (mV) | 12 |
| $\Delta$ | 45 |
| Variation | 8.18% |
| Power (nW) | 600 |

(FOM) for this design is −164.487 dBc/Hz. In [38], a nine-stage RO circuit was also investigated, operating at a frequency of 2.13 GHz. At this frequency, the power dissipation was reported as 477.7 $\mu$W, and the phase noise was measured as −91.4 dBc/Hz at 1 MHz. The reported FOM in [38] was −16118 dBc/Hz. Comparatively, the MDEA-based design of the RO circuit demonstrates superior performance parameters, as summarized in Table 5.

Table 4: MDEA-based optimal design parameters for RO circuit.

| Design parameters | Upper bound | Lower bound | Optimal values achieved from MDEA |
|---|---|---|---|
| $W_n$ (nm) | 1500 | 100 | 195.715 |
| $W_p$ (nm) | 2000 | 200 | 320.262 |
| $L$ (nm) | 200 | 100 | 170.645 |

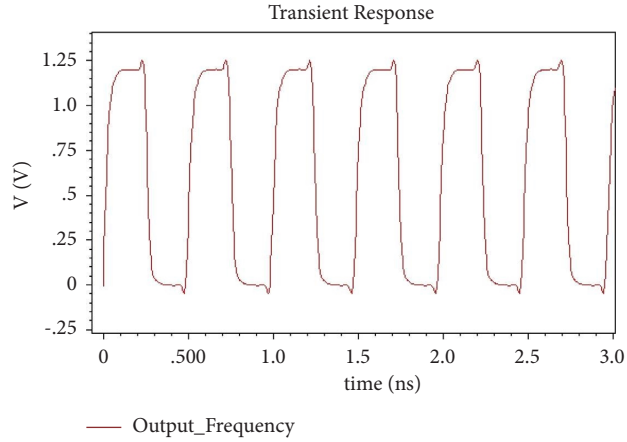


Figure 9: Transient response of the RO.

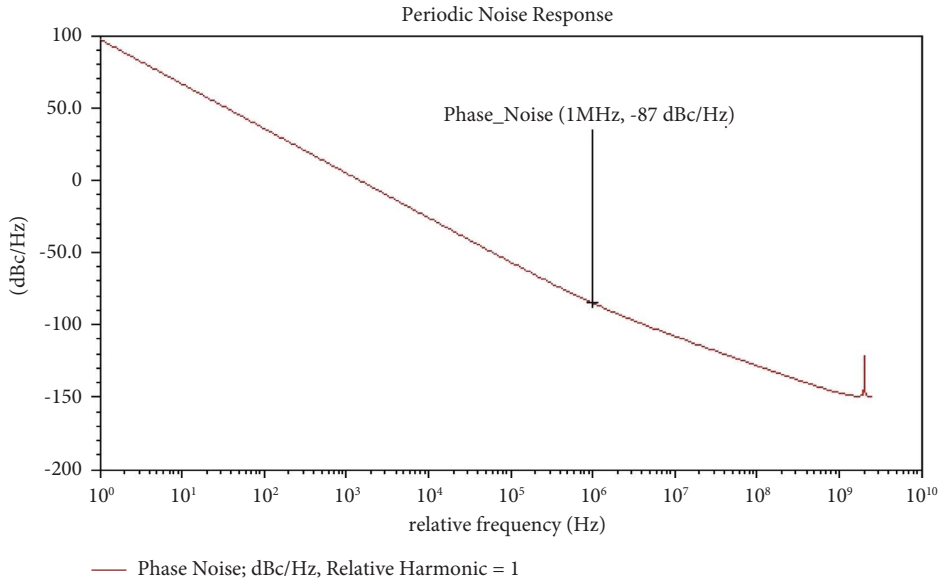


Figure 10: Phase noise plot of the RO.

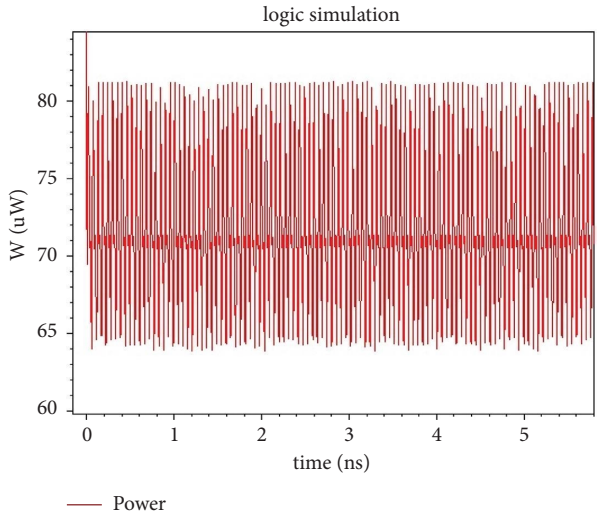


Figure 11: Power dissipation plot of the RO.

Table 5: Performance parameters of the RO circuit.

| Parameters | This work | [38] |
|---|---|---|
| Technology (nm) | 90 | 90 |
| Frequency of oscillation (GHz) | 2 | 2 |
| Oscillation frequency at schematic level (GHz) | 2.001 | 2.1 |
| Optimal power at schematic level (μW) | 71 | 477.7 |
| Optimal phase noise at schematic level @ 1 MHz offset (dBc/Hz) | −87 | −91.4 |
| FOM | −164.487 | −161.18 |

## 5. Conclusion

In this study, the multiobjective differential evolutionary algorithm (MDEA) is employed to achieve optimal designs for CMOS VLSI circuits. By efficiently identifying the optimal design parameters for both circuits, the MDEA enables the reconstruction of each circuit within the Cadence environment. The voltage reference circuit successfully achieves a reference voltage of 550 mV, meeting the targeted specifications. However, it is worth noting that a variation of 8.18% in the reference voltage is observed due to temperature fluctuations ranging from −40°C to + 125°C. The designed ring oscillator (RO) circuit exhibits stable oscillation at a frequency of 2.001 GHz, accompanied by a phase noise of −87 dBc/Hz at an offset frequency of 1 MHz. Additionally, the power consumption of the RO circuit is measured at 71 $\mu$W. Notably, the SPICE simulation results demonstrate that the MDEA-based circuit design fulfills all the required performance parameters. Furthermore, the outcomes obtained through the MDEA approach surpass those reported in previous literature. Thus, the MDEA algorithm proves its efficacy in designing optimal RO and voltage reference circuits.

## Data Availability

The data used to support the findings of this study are included within the article.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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