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Research Article

Comprehensive Analysis of ZVS Operation Range and Deadband Conditions of a Dual *H*-Bridge Bidirectional DC-DC Converter with Phase Shift Control

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This study offers a thorough examination of the zero voltage switching (ZVS) operation range and deadband conditions for a bidirectional DC-DC converter with phase shift control, featuring dual H-bridge. The analysis considers the soft switching range of the DAB converter, accounting for the impact of the headband and the ZVS capacitor. By applying the differential equation of the circuit during deadband time, a sufficient constraint for the input and output bridges can be calculated. The findings indicate that as the output voltage increases, the minimum phase shift value required to achieve ZVS decreases, and expanding the phase shift value will expand the ZVS range and reduce switching losses. The study provides simulation results for various operating conditions, validating the theoretical analysis of the proposed system. In addition, the results furnish information about the circuit behavior during the deadband and waveforms. Finally, MATLAB/SIMULINK verifies the simulation results for different operating stages.

1. Introduction

The double-active-bridge (DAB) converters are highly advantageous compared to other bidirectional-isolated topologies due to their small size, low cost, ease of implementation, and ability to achieve zero-voltage-switching (ZVS) [1–5]. As a result, they have been widely adopted in applications requiring bidirectional power transmission. Previous research on isolated bidirectional DC/DC converters has primarily focused on topology, control strategies, and modeling approaches using classical control theory [6–8]. The literature proposes dual-phase-shift (DPS) control [9] to eliminate reactive power, reduce peak current, and power loss in the DAB converter and determine the on/off state of a simple semiconductor. However, this proposal does not examine the ZVS operating range, which is dependent on factors such as voltage conversion ratios and phase change ratios. The loss of ZVS not only reduces efficiency but also causes electromagnetic interference (EMI) issues [10–12].

The authors of [13] introduced a new hybrid switching modulation approach for an isolated bidirectional DC-DC converter used in a DC microgrid energy storage system. This method combines pulse width modulation and hysteresis current control techniques to achieve zero-voltage switching (ZVS) and improved stability under different operating conditions. Nevertheless, this control strategy has some disadvantages, such as circulating current and

backflow power in the voltage-fed dual-active-bridge converter during heavy load conditions, as highlighted in [14].

In the study of [15], a phase-shifted modulation (PSM) method was introduced to minimize current ripple in a modular multilevel converter of a bidirectional DC-DC converter, even under unstable operating conditions. This method involves adjusting the phase-shift angle between the pulse width modulation (PWM) signals of the half-bridge cells of the modular multilevel converter. Although effective in reducing current ripple, this PSM method is computationally complex due to its optimization problem formulation. In addition, determining the optimal phase-shift angle requires solving a convex optimization problem, which can be time-consuming [16–18]. Despite the effectiveness of various modulation schemes in achieving ZVS over wide load ranges, it remains challenging to achieve full ZVS capability over the entire load range due to the high implementation complexity [19].

The proposed bidirectional DC-DC converter circuit topology is depicted in Figure 1. The converter can operate in two modes, depending on the power flow direction. The converter comprises two H-bridge structured converters, referred to as bridges one and two, which are isolated by a 5 kHz high-frequency transformer. The first H-bridge has four IGBT-diode switches [S_{11}–S_{14}], with two series-connected IGBTs per leg, and a snubber capacitor connected to each of the IGBTs to achieve zero voltage switching and minimize turn-off overvoltage. The second H-bridge operates at low voltage and is configured with four IGBT-diode switches [S_{21}–S_{24}], connected to a small snubber capacitor to minimize switching loss [20, 21].

The converter is bidirectional, and each H-bridge can be primary or secondary depending on the power flow direction. The circuit operates in buck mode when power flows from the high voltage side (HVS) to the low voltage side (LVS) and in boost mode when the power flow is reversed. A deadband is inserted between the interlocked switches in the same bridge to prevent shooting through during commutation, ensuring the reliability of high-voltage and high-power converters [22–31]. However, the deadband may cause waveform distortion and other unexpected transient processes, as depicted in Figure 2. During the deadband, all switches in the same H-bridge module are turned off, including the four switches [S_{11}–S_{14}] on the primary side [24].

This research presents a straightforward theoretical analysis of the steady-state power conditions, the impact of the ZVS capacitor and the deadband on the soft switching operation range of the DAB converter, with varying objectives such as enhancing the ZVS operation range or improving efficiency. The adequate constraints for input and output bridges for soft switching are determined by resolving the differential equation of the circuit during the deadband.

The article is structured as follows. Section 2 provides the operating principle of the proposed DAB bidirectional DC/DC converter. In Section 3, power flow analysis is introduced. Section 4 examines the full-bridge ZVS condition, while Section 5 discusses the converter's behavior during the dead time. Section 6 provides simulation results for the above method. Finally, Section 7 presents the conclusions drawn from the study.

2. Operating Principle of the Proposed a DAB Bidirectional DC/DC Converter

2.1. The Topology of the Proposed Circuit and Control Strategy. The dual active bridge bidirectional converter uses a single-phase-shift control method to regulate power flow between two DC sources, as shown in Figure 2. The primary H-bridge switches (S_{11} and S_{14}) and secondary H-bridge switches (S_{21}–S_{24}) have identical gate signals, with complementary signals for S_{11} and S_{12} having a 50% duty cycle. This generates a voltage ($\pm V_{ab}$) on the primary side of the transformer. Similarly, a voltage ($\pm V_{cd}$) is generated on the secondary side by controlling the switches on the secondary bridge with the same signals as the primary bridge, but with an appropriate phase shift to achieve bidirectional power transfer. The primary voltage is represented by V_{ab}, and the phase shift between the two bridges is denoted by $\mathrm{DT_{hs}}$. The switching frequency is f_s, and T_{hs} is half the switching period, $T_{\mathrm{hs}} = 1/2f_s$. The current i_{Ls} is the sum of the transformer leakage inductance and the auxiliary inductors of the secondary bridge. The equations for a half-cycle are sufficient, given the current waveform's half-wave symmetry in Figure 2.

$$\frac{di_{Ls}(t)}{dt} = \frac{V_{ab}(t) - V_{cd}(t)}{L_s}. \tag{1}$$

L_s is the sum of transformer leakage inductance and auxiliary inductors. ZVS operation was achieved by connecting snubber capacitors parallel to switches. ZVS can be achieved in both leading and full lagging bridges when V_{ab} and V_{cd} change their sign from negative to positive.

2.2. Principle Operation. Based on the on/off state of the switches, there are different operation modes. Figure 3 illustrates the six segments that emerge during each switching cycle. The following assumptions are made in order to simplify the analysis process:

(1) The summation of the transformer leakage inductance and the auxiliary inductor current increases from a negative value at the beginning of the switching cycle to a positive value at the end of the half-switching period

(2) The converter is operating at a steady state

2.2.1. Stage 0 [t_0, t_1]. S_{11} and S_{14} of the first bridge are turned on at this stage. V_{ab} is a positive voltage. The value of i_{Ls} is increasing from a negative to a positive value. S_{11} and S_{14} were turned off, and the current flow through the body diodes D_{11} and D_{14}. Due to this, S_{22} and S_{23} switches will operate under ZVS conditions; the secondary current flows through the body diodes D_2 and D_3, while the current will charge the snubber capacitors C_{21} and C_{24}. The stage will end

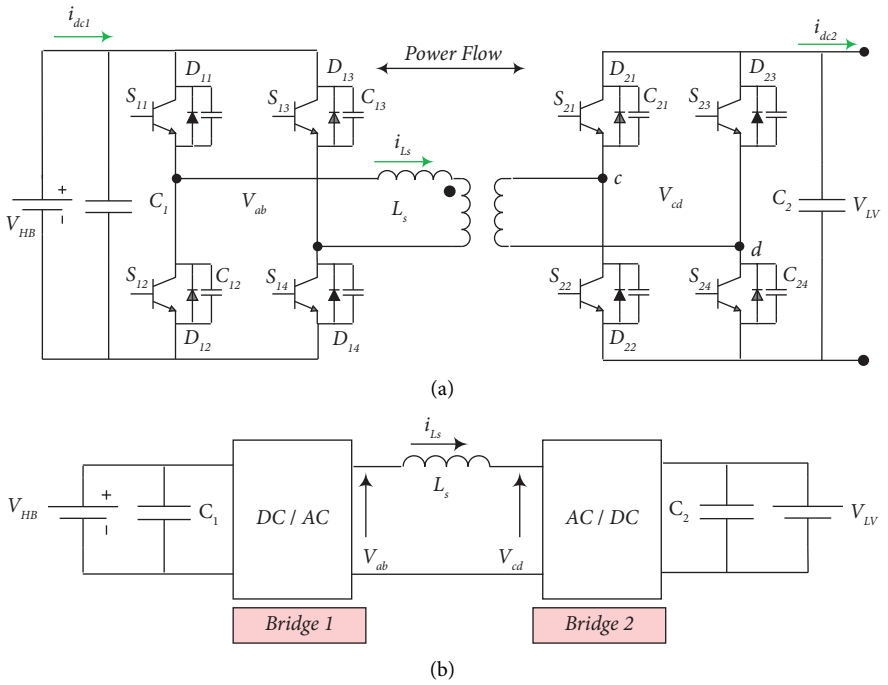


Figure 1: The DAB DC-DC converter: (a) proposed circuit schematic diagram and (b) the equivalent circuit.

when the i_{Ls} current reaches zero (see Figure 3(A)). During this mode, the total dynamic current is

$$i_{Ls}(t) = i_{Ls}(t_0) + \frac{V_{ab} + V_{cd}^{'}}{L_s}(t - t_0); t_0 \le t < t_1, \tag{2}$$

where $V_{cd}^{'}$ is the transformer's secondary voltage generated by the bridge 2, referred primary voltage

2.2.2. Stage 1 $[t_1 - t_2]$. Switches S_{11} and S_{14} are still in the On state, and current flows through them. The current will charge the snubber capacitors of C_{12} and C_{13} and discharge the capacitors of C_{11} and C_{14}. Consequently, the initial voltages of C_{12} and C_{13} are VHB, and those of C_{11}, and C_{14}, are zero. On the secondary side, switches S_{22} and S_{23} are still on, i_{Ls} is greater than 0, and current flows through switches S_{22} and S_{23} (see Figure 3(B)).

2.2.3. Stage 2 $[t_2 - t_3]$. At $t = t_2$, switches S_{22} and S_{23} are turned off due to the snubber capacitors C_{22} and C_{23}, and the dead time stage begins. Secondary currents charge and discharge Snubber capacitors of S_{22}, S_{23}, and S_{21}, S_{24}, respectively. V_{cd} is the voltage across the capacitor, which gets positive from zero.

The voltage of the ZVS capacitor and the inductance current i_{Ls} in this stage is plotted in Figure 4

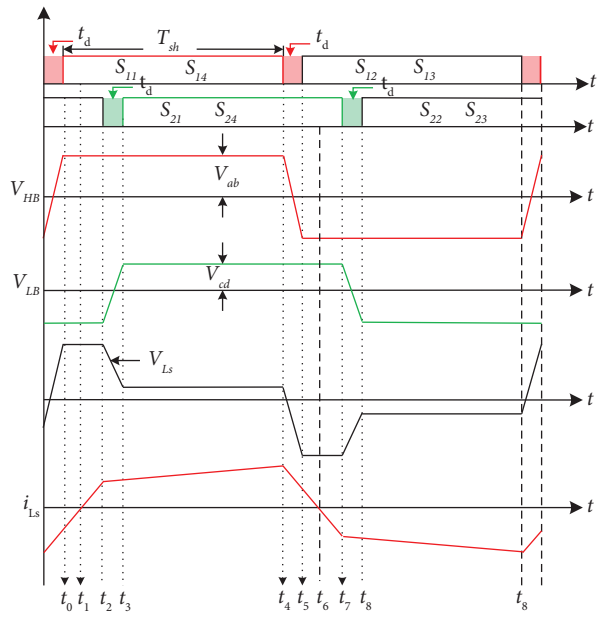


Figure 2: Fundamental operating waveforms of the bidirectional forward converter with single-phase shift control and dead band effect $i_{Ls} < 0$.

Therefore, the voltage of the ZVS capacitor of S_{22} during the deadtime zone can be expressed as follows:

$$V_{ds22}(t - t_2) = \frac{\left[V_{ab}^{'} + V_{cd}\right]}{2} + \frac{\sqrt{\left[z_2 * n * i_{dc2}(t_2)\right]^2 + \left[V_{ab}^{'} + V_{cd}\right]^2}}{2} \sin\left(\omega_2 (t - t_2) - \sigma_2\right), \tag{3}$$

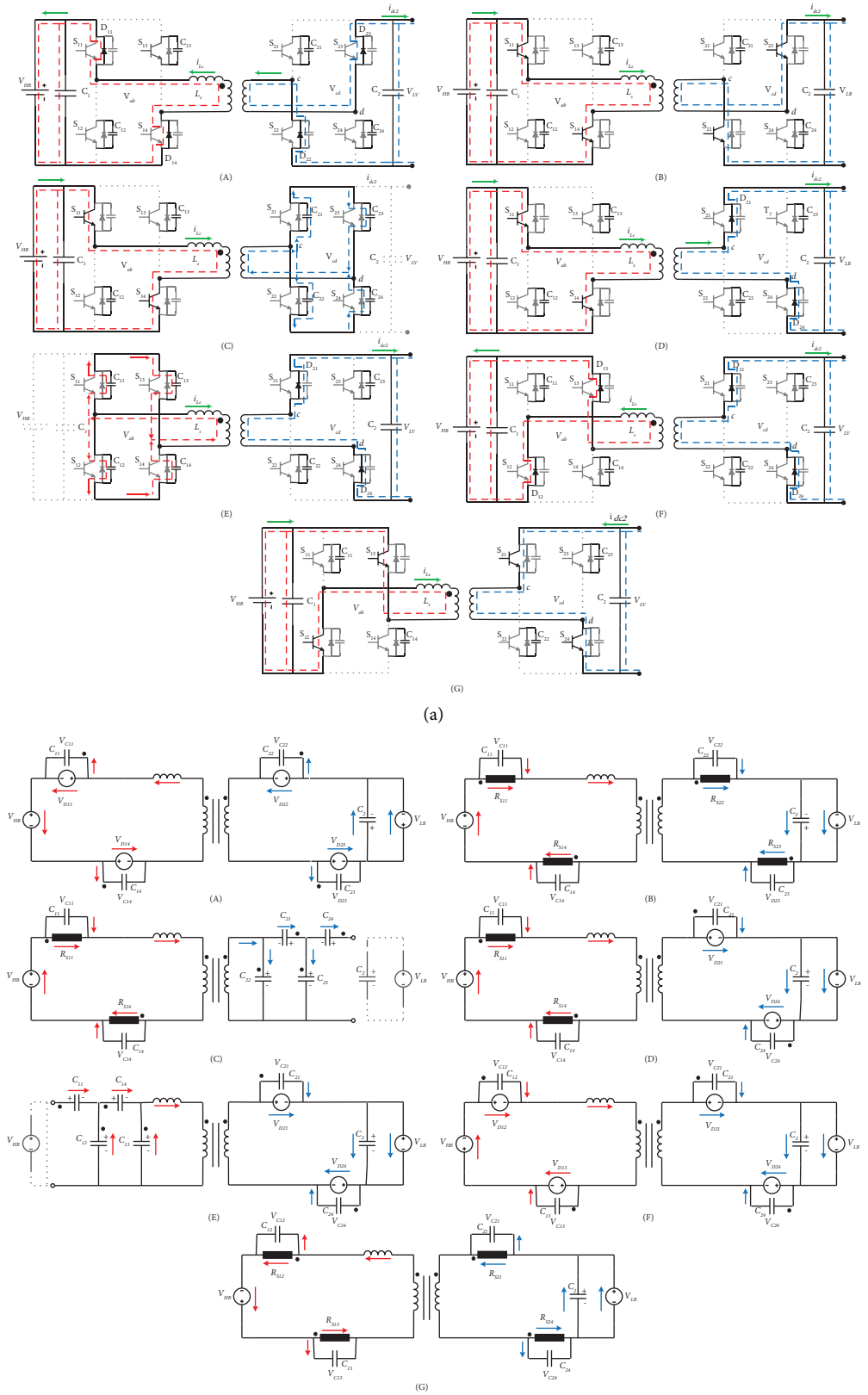


FIGURE 3: (a) Commutation step diagrams during a switching cycle in power flow; (b) equivalent circuits of SPS controlled converter for forwarding operation.

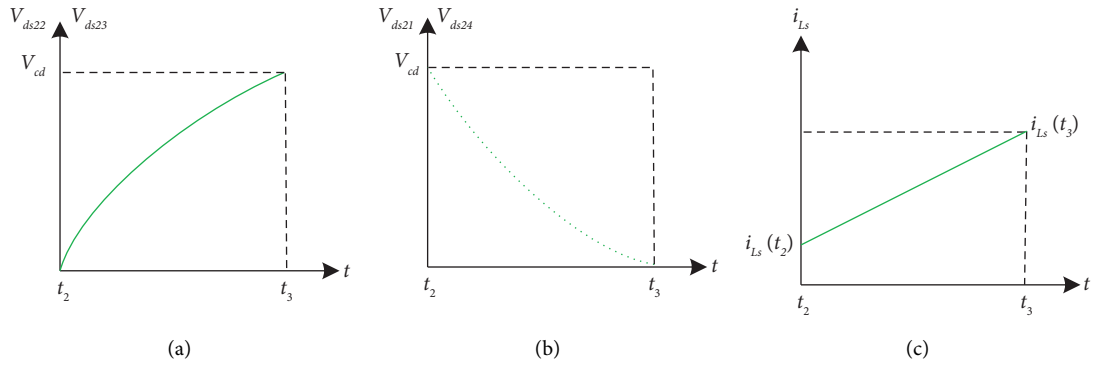


FIGURE 4: The voltage of the ZVS capacitor and the inductance current i_{Ls}: (a) charging the snubber capacitors of S_{22}, S_{23}, (b) discharging the snubber capacitors of S_{21} and S_{24}, and (c) increasing the inductance current.

where

$$\begin{cases} \tan\sigma_2 = \dfrac{V_{ab}^{'} + V_{cd}}{z_2 * n * i_{dc2}(t_2)}, \\ z_2 = n\sqrt{\dfrac{L_s}{C_{ds}}}, \\ \omega_2 = \dfrac{n}{\sqrt{L_s C_{ds}}}, \\ C_{ds} = C_{21} + C_{22}, \end{cases} \tag{4}$$

where V_{ds22} is the voltage across C_{22}, z_2 is the resonant impedance, C_{ds} is the zero-voltage switch capacitor, and ω_2 is the self-oscillating frequency.

The voltage across C_{22} and C_{23} will increase as the voltage across C_{21} and C_{24} continues to decrease, allowing S_{21} and S_{24} to turn on under ZVS conditions. When charging and discharging have been completed to the point where the voltages of C_{21} and C_{24} become zero, while the voltages of C_{22} and C_{23} become V_{cd}, current flows through D_{21} and D_{24} diodes (see Figure 3(C)). The switches S_{21} and S_{24} are turned on after a suitable dead time with zero-voltage switching. Therefore, Table 1 summarized the switches and output capacitance statuses during this stage.

2.2.4. Stage 3 $[t_3, t_4]$. At $t = t_3$, the second bridge's switch S_{21} and S_{24}, will be turned on. Due to $i_{Ls} > 0$, the secondary current will flow through the body diodes D_{21} and D_{24}, which will discharge the capacitors C_{21} and C_{24}. The primary bridges S_{11} and S_{14} remain turned on, and current flows through S_{11} and S_{14} (see Figure 3(D)). During this mode, the i_{Ls} are at their maximum.

$$i_{Ls}(t) = i_{Ls}(t_3) + \frac{V_{ab} - V_{cd}^{'}}{L_s}(t - t_3); t_3 \le t < t_4. \tag{5}$$

2.2.5. Stage 4 $[t_4, t_5]$. At $t = t_3$, the deadtime stage is initiated after switches S_{11} and S_{14} have been turned off. As a result of the stored energy in the leakage inductance L_s, the current continues to flow through the snubber capacitors. As the snubber capacitors C_{11} and C_{14} are being charged, the snubber capacitors C_{12} and C_{13} are being discharged. Thus, the voltage across the primary transformer side V_{ab} decreases from positive to zero while the inductance current i_{Ls} decreases linearly. The equivalent circuit is shown in Figure 3(E). Table 2 summarized the switches and output capacitance statuses during this stage. The leakage inductance L_s resonates with C_{11}, C_{12}, C_{13}, and C_{14} to charge C_{11}, C_{14}, and discharge C_{12} and C_{13}. Therefore, we can express the differential equations as follows:

$$i_{Ls}(t - t_4) = C_{11}\frac{dV_{ds11}(t - t_3)}{dt} + C_{12}\frac{dV_{ds12}(t - t_4)}{dt} = 2C_{ds}\frac{dV_{ds11}(t - t_4)}{dt}, \tag{6}$$

where $V_{ds11}(t)$ and $V_{ds12}(t)$ are the voltages across C_{11}, and C_{12}, respectively, during this stage, and $V_{ds12}(t)$ can be obtained.

$$V_{ds12}(t - t_4) = L_s\frac{di_{dc1}(t - t_4)}{dt} + V_{ab} - V_{cd}^{'}. \tag{7}$$

Table 1: The switches and output capacitance statuses.

Capacitance	Status	Switch	Status
C_{21}	$V_{cd} \longrightarrow 0$	S_{21}	Off
C_{22}	$0 \longrightarrow V_{cd}$	S_{22}	On $\longrightarrow$ off
C_{23}	$0 \longrightarrow V_{cd}$	S_{23}	On $\longrightarrow$ off
C_{24}	$V_{cd} \longrightarrow 0$	S_{24}	Off

Table 2: The switches and output capacitance statuses.

Capacitances	Status	Switch	Status
C_{11}	$0 \longrightarrow V_{ab}$	S_{11}	On $\longrightarrow$ off
C_{12}	$V_{ab} \longrightarrow 0$	S_{12}	Off
C_{13}	$V_{ab} \longrightarrow 0$	S_{13}	Off
C_{14}	$0 \longrightarrow V_{ab}$	S_{14}	On $\longrightarrow$ off

Taking into account that the initial values of $V_{ds12}(0) = -V_{ab}$ and $i_{dc11}(0) = i_{dc11}(t_4)$. From equations (6) and (7), the following equations can be formulated:

$$V_{ds12}(t-t_4) = \left[V_{ab} - V_{cd}^{'}\right] + \left(\sqrt{\left[\sqrt{\frac{L_S}{C_{11}+C_{12}}} i_{Ls}(t_4)\right]^2 + \left[V_{ab} - V_{cd}^{'}\right]^2} \sin\left(\frac{1}{\sqrt{L_s(C_{11}+C_{12})}} + \tan^{-1}\frac{V_{ab} - V_{cd}^{'}}{\sqrt{L_S/C_{11}+C_{12}}\, i_{Ls}(t_4)}\right)\right). \quad (8)$$

Equation (8) can be simplified further to

$$V_{ds12}(t-t_4) = \left[V_{ab} - V_{cd}^{'}\right] + V_{p1}\sin(\omega_1(t-t_4)+\sigma_1), \quad (9)$$

where

$$\begin{cases} C_{ds} = C_{11} + C_{12}, z_1 = \sqrt{\dfrac{L_s}{C_{ds}}}, \tan\sigma_1 = \dfrac{V_{ab} - V_{cd}^{'}}{z_1 i_{dc1}(t_4)}, \\ V_{p1} = \sqrt{\left[z_1 i_{dc1}(t_1)\right]^2 + \left[V_{ab} - V_{cd}^{'}\right]^2}, \\ \omega_1 = \dfrac{1}{\sqrt{L_s(C_{11}+C_{12})}}. \end{cases} \quad (10)$$

The voltage of the ZVS capacitor and the inductance current i_{Ls} in this stage is plotted in Figure 5

i_{Ls} is the inductance current flowing through the snubber capacitors on the primary side and can be expressed as follows:

$$i_{Ls}(t-t_4) = i_{dc1}(t_4)\cos\omega_1(t-t_4) - \frac{V_{ab} - V_{cd}^{'}}{z_1}\sin\omega_1(t-t_4). \quad (11)$$

During this short time, the voltage V_{ds12} and V_{ds13} will decrease, and the Snubber capacitors C_{12} and C_{13} are still being discharged by snubber capacitors C_{11} and C_{14}, while V_{ab} is negatively increasing from zero. Similarly, when $t = t_5$ the ZVS capacitors of S_{11} and S_{14} are fully charged, and the ZVS capacitors of S_{12} and S_{13} are discharged [24].

As a result, the body diodes D_{12} and D_{13} become conductive, setting up conditions for S_{12} and S_{13} to be turned on with ZVS in the following stage. The ZVS capacitor voltage of S_{11} can be expressed using equations (6), (7), and (10).

$$V_{ds11}(t-t_4) = \frac{\left|V_{ab} - V_{cd}^{'}\right|}{2} + V_{P1}\sin(\omega_1(t-t_4)+\sigma_1), \quad (12)$$

where

$$\begin{cases} V_{P1} = \dfrac{\sqrt{\left[z_1 i_{Ls}(t_4)\right]^2 + \left[V_{ab} - V_{cd}^{'}\right]^2}}{2}, \\ \tan\sigma_1 = \dfrac{V_{ab} - V_{cd}^{'}}{z_1 i_{Ls}(t_4)}. \end{cases} \quad (13)$$

In Figure 6, several variations of $V_{ds11}(t)$ are plotted versus values of the ZVS capacitor at $V_{HB} = 270V, V_{LB} = 28V$ and $L_s = 460\mu H$ according to the dead time during this stage. The maximum value of V_{ds11} decreases as the capacitor size increases. As a result, V_{ds11} has a lower peak value than V_{HB} when $C_{ds} = 0.45nF$ and $C_{ds} = 0.5nF$. For the ZVS to operate correctly, the peak capacitor voltage must be obtained during the deadband [6].

2.2.6. Stage 5 $[t_5, t_6]$. At the beginning, S_{12} and S_{13} are ON, and S_{11} and S_{14} are OFF. Transformer leakage inductance and auxiliary inductors flow into the load through D_{21} and D_{24}, while primary current flows through D_{12} and D_{13}. At $t = t_6$, the secondary side current decreases from positive to zero. There is zero voltage turn-on for active switches, and no turn-on loss exists (see Figure 3(F)).

2.2.7. Stage 6 $[t_6, t_7]$. At $t = t_6$, switches S_{12} and S_{13} are still on, while switches S_{11} and S_{14} are off. Charges on C_{12} and C_{13} will discharge through S_{12} and S_{13}. The primary current will flow through S_{12}, S_{13}, while the negative current of the transformer leakage inductance will flow through S_{21} and S_{24}. Therefore, S_{21} and S_{24} will be turned off at $t = t_6$ (see Figure 3(G)).

During this period, No switching occurs at t_6. It is a short time interval only to illustrate the conversion of current flow from the D_{12} andD_{13} mode to the S_{12} and S_{13} mode. Therefore, the current will discharge the snubber capacitors of C_{12} and C_{13} and charge C_{11} and C_{14}.

Figure 7 depicts the circuit operation when one leg of bridge one consisting of S_{11} and S_{12} operates with zero voltage switching (ZVS). As shown in Figure 2, the current is positive before the deadband time and flows into S_{11}, as seen

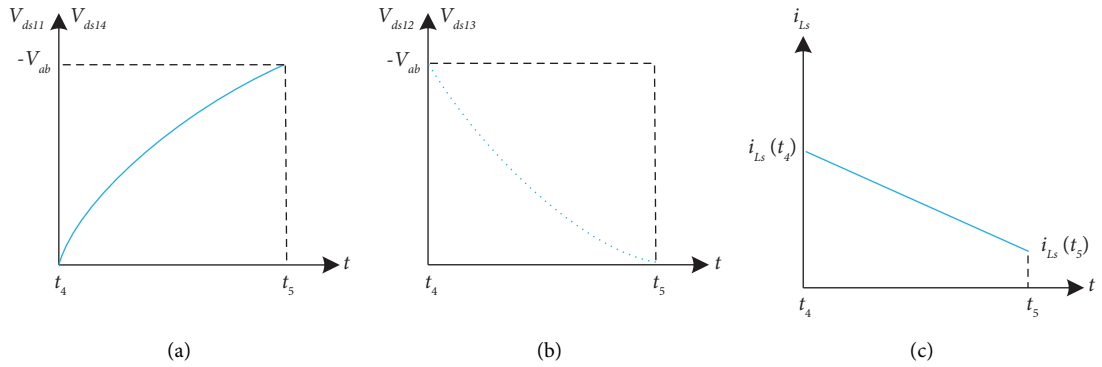


FIGURE 5: The voltage of the ZVS capacitor and the inductance current i_{Ls} (a) charging the snubber capacitors of S_{11}, S_{14}, (b) discharging the snubber capacitors of S_{12}, S_{13}, and (c) decreasing the inductance current.

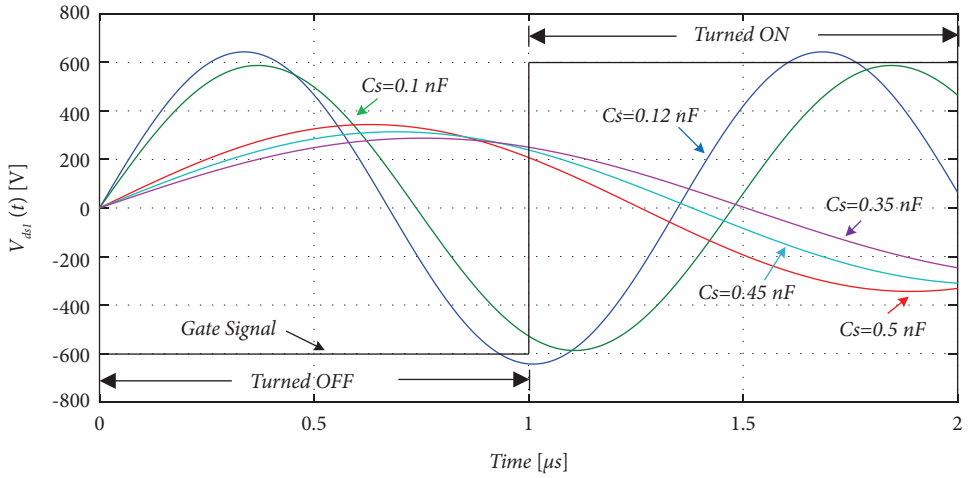


FIGURE 6: Relationship between $V_{ds11}(t)$ and ZVS capacitor.

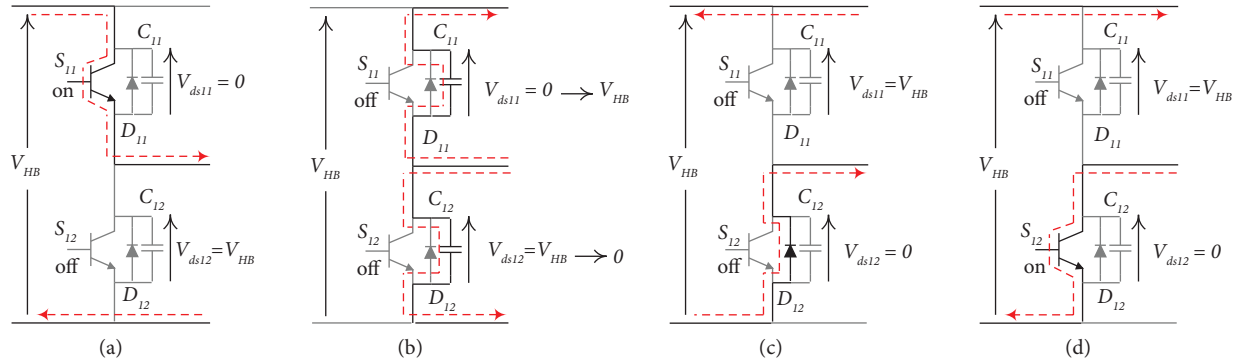


FIGURE 7: ZVS on a leg in bridge one: (a) before the dead time starts, (b) the dead time starts (rapid charging/discharging of C_{11} and C_{12}), (c) diode freewheeling, and (d) after the dead time, the current polarity changes.

in Figure 7(a). After S_{11} turns off, the deadband time starts. As shown in Figure 7(b), C_{11} charges from zero to VHB, while C_{12} discharges from VHB to zero. Once C_{12}'s discharge process is complete, the current freewheels through D_{12}. Providing a gating signal at the point when D_{12} is conducting enables S_{12} to turn on with ZVS, as shown in Figure 7(d), as the current in D_{12} decreases to zero and alternates its polarity.

The circuit modes when S_{11} and S_{12} operate at ZVS are depicted in Figure 8. During this time interval, prior to the turn-on of S_{11}, the current is negative, as shown in Figure 2, and the switching voltages are illustrated in Figure 8(a). Deadband time initiates once S_{11} is turned off. As seen in Figure 8(b), the current flowing in commutates to the snubber capacitors, where C_{11} discharges from VHB to zero, and C_{12} charges from zero to VHB. Once the charging and

discharging are complete, the current freewheels through commutates to the diode D_{11}, where it is negative, as shown in Figure 8(c). As turn-on gate signals are provided to S_{11}, it begins to conduct at zero voltage once the current alternates its polarity, as illustrated in Figure 8(d). Similarly, ZVS can be employed for visualizing other switches.

3. Power Flow Analysis

The power transfer can be controlled by adjusting the phase shift between the transformer's primary voltage V_{ab} and secondary voltage V_{cd} [32]. In buck mode, power flows from Bridge 1 to Bridge 2 at a voltage conversion ratio of $k < 1$. The polarity of the V_{ab} and V_{cd} changes from negative to positive as shown in Figure 2. Thus, under steady-state conditions, the average value of the DC current at the bridge 2 i_{cd2} must be zero. Based on figure $t_2 = DT_{sh}, t_4 = T_{sh}, t_7 = (1+D)T_{sh}, k = V_{ab}/nV_{cd}$ and $f_s = 1/(2T_{sh})$. The expression of the inductance current can be obtained. Table 3 summarizes the inductor current steady-state expressions for forwarding power flow directions.

Moreover, $i_{Ls}(t_0) = -i_{Ls}(t_4)$ and $i_{Ls}(t_2) = -i_{Ls}(t_7)$. From the above condition, we can express i_{Ls} at time t_0, t_2, t_4, and t_7 as follows:

$$\begin{cases} i_{Ls}(t_0) = \dfrac{V_{cd}^{'}}{4f_sL_s}(1-2D-k), \\ i_{Ls}(t_2) = \dfrac{V_{cd}^{'}}{4f_sL_s}[1-k(1-2D)], \\ i_{Ls}(t_4) = -\dfrac{V_{cd}^{'}}{4f_sL_s}(1-2D-k), \\ i_{Ls}(t_7) = -\dfrac{V_{cd}^{'}}{4f_sL_s}[1-k(1-2D)]. \end{cases} \tag{14}$$

Therefore, the average input current can be expressed as

$$I_{\text{ave}} = \frac{1}{T_{hs}}\int_0^{T_{hs}} i_{Ls}(t)\mathrm{d}t = \frac{V_{cd}^{'}}{2f_sL_s}D(1-D). \tag{15}$$

Consequently, the transmission power controlled by SPS can be expressed as a function of the feeding voltage as follows:

$$P_O = V_{HB} * I_{\text{ave}} = \frac{V_{ab}V_{cd}^{'}}{2f_sL_s}D(D-1). \tag{16}$$

The equation (16) indicates that the powers are directly proportional to the phase shift ratio of the two bridges D. By employing a single-phase shift control, one can represent the normalized transmission power in the following manner:

$$P_{\text{nor}} = \frac{P_o}{P_{\max}} = 4D(1-D), \tag{17}$$

where $P_{\max}$ is the maximum power of the converter. Therefore,

$$P_{\max} = \frac{V_{cd}^{'}V_{ab}}{8f_sL_S}. \tag{18}$$

Referring to Figure 2, the maximum inductor current ($I_{\max} = i_{Ls}(t_4)$) can be expressed as

$$I_{\max} = i_{Ls}(t_4) = (2D+k-1)\frac{V_{cd}^{'}}{4f_sL_s}. \tag{19}$$

When the converter operates at full load and the minimum value of the input, while the input current has a maximum value, therefore, under these conditions, the current stress can be determined as follows:

$$I_{\text{stress}} = I_{\max}\big|_{k<1} = \frac{V_{cd}^{'}}{4f_sL_s}(2k_{\max}D_{\max}+1-k_{\max}). \tag{20}$$

Equation (20) shows that the current stress of the converter is a function of the maximum phase shift, the maximum value of the voltage ratio, and the value of leakage inductance in the SPS control mode.

Figure 9 shows the output power as a function of the phase shift angle. The maximum power is achieved at a phase shift angle of ($\pi/2$), as evident from the graph, indicating that equation (16) has reached its maximum and zero transmission power points. In addition, increasing the phase shift ratio results in higher transmission power values. During power transmission in the forward direction, the source-side bridge leads to the load-side bridge, while in reverse mode, the loading side bridge leads to the source side bridge. Figure 9(d) depicts the relationship between current stress and phase shift at different voltage conversion ratios in SPS control under full load. The graph indicates that, with a constant shift ratio D, current stress decreases as the voltage conversion ratio k is reduced. Therefore, it is recommended to decrease the voltage conversion and phase shift ratio as much as possible to minimize the converter's current stress, reduce losses, and improve efficiency [24, 27].

4. Full Bridge ZVS Condition

4.1. Zero Voltage Switching Limits. According to the above-given transition analysis, to ensure full ZVS operation, the inductor current should be negative at (t_0) and positive at t_2 and t_4. In order to achieve ZVS in both leading and lagging full bridges, i_{Ls} (t_2) and i_{Ls} (t_4) must be greater than zero. However, to realize ZVS at $t = t_0$, the leakage inductance energy should be greater than the amount of energy required to charge and discharge the output capacitors in the leading bridge. Therefore, the leakage inductance current can be written as follows:

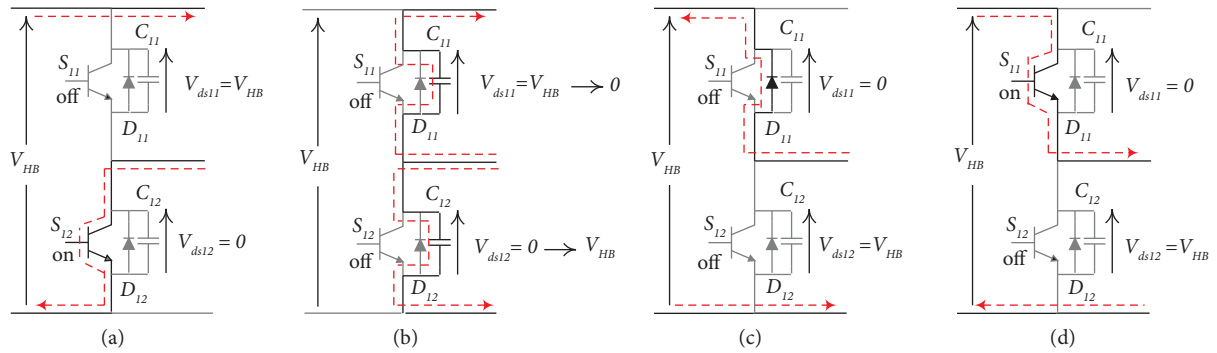


Figure 8: ZVS turn on of S_{11}: (a) before the dead time starts, (b) after dead time starts, (c) diode freewheeling, and (d) after the dead time, the current polarity changes.

Table 3: Inductor current expression during different intervals.

Intervals	Inductor current
$t_1 \le t < t_2$	$i_{Ls}(t_2) = i_{Ls}(t_0) + DT_{hs}/L_s(V_{ab} + V_{cd}')$
$t_3 \le t < t_4$	$i_{Ls}(t_4) = i_{Ls}(t_2) + (1-D)T_{hs}/L_s(V_{ab} - V_{cd}')$
$t_6 \le t < t_7$	$i_{Ls}(t_7) = i_{Ls}(t_4) - DT_{hs}/L_s(V_{ab} + V_{cd}')$
$t_7 \le t < t_8$	$i_{Ls}(t_8) = i_{Ls}(t_7) - (1-D)T_{hs}/L_s(V_{ab} - V_{cd}')$

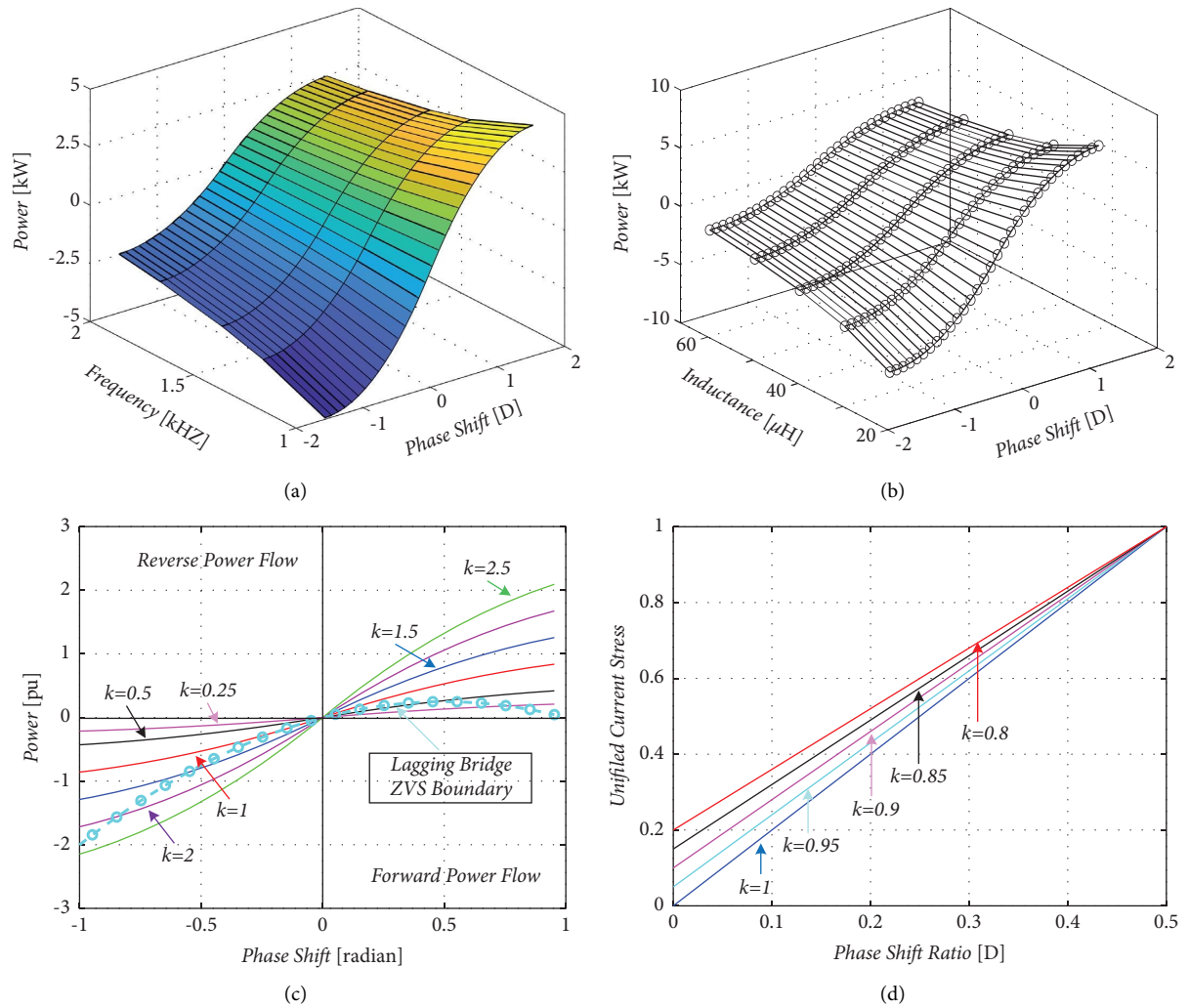


Figure 9: (a) Dependency of the output power on operating phase shift and leakage inductance for DAB converter. (b) A dependency of the output power on operating phase shift frequency for DAB converter. (c) Output power characterization A versus phase shift ratio of the DAB. (d) Effect of phase shit ratio on the current stress under full load condition.

$$\begin{cases} i_{Ls}(t_0) = -\dfrac{nV_{cd}^{'}}{4f_sL_s}(2D + k - 1), \\ i_{Ls}(0) \le 0; i_{Ls}(t_0) = -i_{Ls}(t_2), \\ f_s = \dfrac{1}{2T_{sh}}, V_{ab} = V_{LB}, V_{cd}^{'} = nV_{HB}. \end{cases} \tag{21}$$

Due to the symmetry of the leakage inductance current $i_{Ls}(t_0) = -i_{Ls}(t_2)$, equation (19) describes the maximum inductor current. As $i_{Ls}(0) \le 0$, by equation (21), we can write the equation as follows:

$$D \ge \frac{k-1}{2k}, k \ge 1, \tag{22}$$

where $k = (V_{LB}/nV_{HB})$ is the voltage conversion between the output voltage on the primary side of the converter and the input voltage, equation (22) shows that when $k \ge 1$, there is a requirement of D to realize ZVS of the leading bridge. Regarding the lagging leg bridge, to achieve ZVS operation (power transfer from the high voltage side to the low voltage side), the current of the leakage inductance must be positive.

$$\begin{cases} i_{Ls}(t_2) = \dfrac{V_{cd}^{'}}{4f_sL_s}(2D - k + 1), \\ i_{Ls}(t_2) \ge 0; t_2 = DT_{sh}. \end{cases} \tag{23}$$

Since $i_{Ls}(DT_{sh}) \ge 0$, equation (23) can be presented in the following form:

$$D \ge \frac{1-k}{2}. \tag{24}$$

The normalized load resistance R_L can be obtained as

$$R_L = \frac{V_{HB}}{i_{dc2}}. \tag{25}$$

In equation (24), i_{cd2} represents output current and D is required to achieve ZVS of the lagging bridge when $k \le 1$. Furthermore, when $k \ge 1$, the lagging bridge is usually achieved, which is the limiting condition for ZVS. Whenever $k = 1$, ZVS is fulfilled for any value of D. The above analysis can be summarized in Table 4.

Figure 10(a) displays the Zero Voltage Switching (ZVS) region of the DAB converters based on equations (22) and (24), where the phase shift is represented on the x-axis, and the relationship between the output and input voltages is shown on the y-axis. The bold curves indicate the operating zone of the DAB converter under ZVS conditions. When $k = 1$, complete control of ZVS is achievable. However, under light load conditions where $k \ne 1$, the ZVS region diminishes. The operational phase shift is determined by the intersection of the k line and the load line R_L. Increasing the phase shift leads to a larger ZVS region and lower switching loss but higher reactive current value and conduction loss, while decreasing the phase shift produces the opposite effect.

Table 4: The constraint of ZVS for the leading and lagging bridge.

	Mode of operation	$k = 1$	$k \ge 1$	$k \le 1$
Leading bridge	Input	Fulfilled	$D \ge k - 1/2k$	Fulfilled
Lagging bridge	Output	Fulfilled	Fulfilled	$D \ge 1 - k/2$

Figure 10(b) plots the phase shift and ZVS boundaries of the input and output bridges against the voltage gain ratio for different values of the ZVS capacitor. It can be observed that as the ZVS capacitor increases, the ZVS region decreases.

To expand the operating range of ZVS, it is necessary to select the maximum feasible values for L_{seq} and D_{max}. The theoretical maximum D value is 0.5, but the output power's nonlinearity is more severe for a value of D close to 0.5 because the output power's evolution with D is parabolic [9]. Therefore, the maximum value of the phase shift and leakage inductance is determined by the maximum transmission power as follows:

$$P_{max} = \frac{V_{LB}V_{HB}^{'}(1 - D_{max})D_{max}T_{sh}}{L_{seq}}. \tag{26}$$

A phase shift and the power at which ZVS is lost in the converter can be estimated using the following equations:

$$\begin{cases} D_{ZVS} = \dfrac{2nk\sqrt{L_{seq}C_s}}{T_{hs}} + \dfrac{1-k}{2}, \\ P_{ZVS} = \dfrac{V_{LB}V_{HB}^{'}(1 - D_{ZVS})D_{ZVS}T_{hs}}{L_{seq}}. \end{cases} \tag{27}$$

4.2. Required Dead times. As mentioned in the transition above, the leakage inductance current must be sufficient to complete the charging and discharging of the capacitor. To achieve ZVS, the dead time must be longer than the voltage capacitor connected in parallel across the switch discharging from the DC input voltage to zero V. As a result, the resonance occurs. During stage 4 [t_4, t_5], the voltage across C_{12} and C_{13} decreases to zero and is completely discharged at $t = t_5$, D_{12} and D_{13} are conducive naturally. Moreover, the voltage of S_{12} and S_{13} is also clamped to zero, and ZVS is achieved when switches S_{12} and S_{13} are turned on at this time. In order to ensure that S_{12} and S_{13} will turn ON with ZVS, a dead time is necessary between the turn-off of S_{11} and S_{14} and the turn-on of S_{12} and S_{13}. To ensure that D_{12} and D_{13} are conducting before turning ON S_{12} and S_{13} should be larger than the time of discharging C_{12} and C_{13}. Accordingly, the dead-time t_{dead} can be described as follows:

$$t_{dead} > t_{45}. \tag{28}$$

After the leakage inductance current i_{Ls} discharges C_{12}, C_{13} completely, the body diodes D_{12}, D_{13} will be conductive, resulting in an increase in voltage across V_{ds11} and V_{ds14}

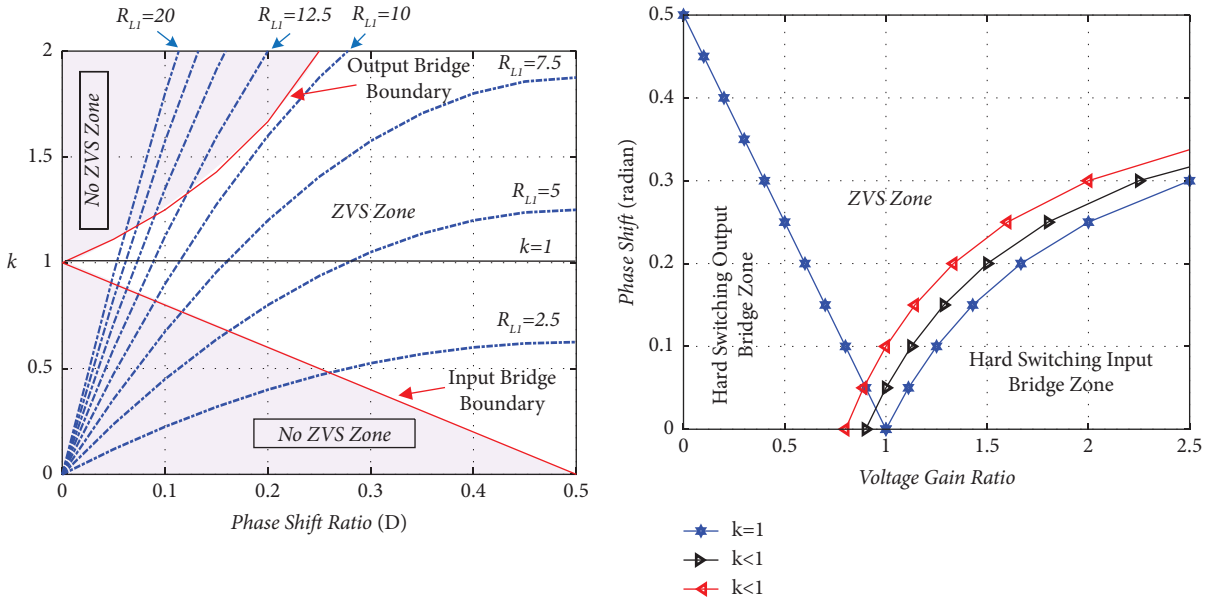


FIGURE 10: (a) ZVS zone in leading and lagging DAB converter, R_L is load resistance; (b) phase shift and ZVS boundaries under the different value of voltage gain ratio.

equal to the input DC voltage V_{HB}. According to equation (11), the following equation can be derived:

$$\frac{V_{ab} - V_{cd}}{2} + V_{P1} \sin\left(\omega_1 (t - t_4) + \sigma_1\right) \geq V_{HB}. \tag{29}$$

Based on Figure 2, the leakage inductance current must be greater than zero during the whole dead band $[t_4, t_5]$. This condition can be expressed as follows:

$$i_{Ls}(t_4) \geq 0. \tag{30}$$

According to (22), condition (30) can be presented in the following form:

$$\frac{V_{cd}}{4 f_s L_s}\left(2D\frac{V_{ab}}{V_{cd}} - \frac{V_{ab}}{V_{cd}}\right) \geq 0. \tag{31}$$

Furthermore, the minimum value of the current i_{Lsmin} is required to achieve zero voltage switching at $t = t_5$, ensuring that the voltage across S_{11} and S_{14} reaches and equal to the input DC voltage V_{HB}. Consequently, the inductance current i_{Ls} decreases linearly, as shown in Figure 2. Hence, at $t = t_4$, the $i_{Ls} = i_{Ls}(t_4)$; V_{ds11} and $V_{ds14} = 0$, V_{ds12} and $V_{ds13} = V_{HB}$. Therefore, at $t = t_5$, V_{ds11} and $V_{ds14} = V_{HB}$; V_{ds12} and $V_{ds13} = 0$, and $i_{Ls} = i_{\text{Lsmin}}$. The magnitude of $i_{dc1}(t_4)$ should be greater than i_{Lsmin} so that the inductance current will fully charge the snubber capacitors C_{11} and C_{14} while the voltage across S_{11} and S_{14} reaches the input DC voltage V_{HB}. Therefore, we say:

$$W_{\text{tran}} = \frac{L_s i_{Ls_{\min}}^2}{2}. \tag{32}$$

W_{tran} represents the amount of energy transferred, assuming no loss occurs at the circuit. ZVS operates under the condition that $V_{HB} = DV_{ds}$ during this stage, therefore

$$W_{\text{tran}} = 2C_{ds} V_{HB} n V_{LB}. \tag{33}$$

The following expression can be obtained by comparing (32) and (33):

$$i_{Ls_{\min}} = \frac{2\sqrt{V_{HB} n V_{LB}}}{z}. \tag{34}$$

The magnitude of $i_{dc1}(t_4)$ should be greater than i_{Lsmin} in order to ensure that the inductance current fully charges the snubber capacitors C_{11} and C_{14} while the voltage across S_{11} and S_{14} reaches the input DC voltage V_{HB}. Due to this,

$$i_{Ls}(t_4) > i_{Ls_{\min}}. \tag{35}$$

If equation (29) is not satisfied, the $i_{dc1}(t_2)$ amount is smaller than i_{dc1min}. As a result, the C_{11} and C_{14} are not charged up to V_{HB}, while the C_{12} and C_{13} are not discharged to zero. Therefore, the zero voltage switching operation cannot be achieved. The efficiency will decrease as a result of switching loss. Accordingly, the voltage of S_{12} can be expressed as follows:

$$V_{ds12} = V_m \cos\omega_1 t - \frac{z_1 |i_{dc1}(t)|}{2} \sin\omega_1 t. \tag{36}$$

Thus,

$$\begin{cases} V_m = \dfrac{(V_{HB} + V_{LB}')(V_{HB} - V_{LB}')}{2}, \\ z_1 = \sqrt{\dfrac{L_S}{C_{ds}}}, \end{cases} \tag{37}$$

where t is the time after the dead time started. At the end of the dead time $t = t_5$, $V_{ds12}(t_5)$ is not zero because $i_{Ls}(t_4) < i_{Lsmin}$. C_{12} is shorted out and discharges rapidly from $V_{ds12}(t_5)$ to zero. C_{11} suddenly charges from $V_{HB} - V_{ds12}(t_5)$ to V_{HB}. During dead time, the S_{11} voltage must reach V_{HB} to ensure S_{12} will turn on with ZVS. Accordingly,

$$V_{ds11}(t - t_4) = \frac{V_{HB} - V_{LB}'}{2} + V_{P1}\sin(\omega_1(t - t_4) + \sigma_1) \geq V_{HB}. \tag{38}$$

Formulas (10) and (13), as well as (36) and (38), can be used to determine sufficient restrictions for input bridge ZVS operation:

$$\left|i_{Ls}\,|_{t=t_4}\right| > \frac{2V_{HB}\sqrt{k}}{z_1}, \tag{39}$$

$$\sin^{-1}\left(\frac{V_{HB} + V_{LB}'}{\sqrt{(V_{HB} - V_{LB}')^2 + (z_1 * i_{dc1}(t_4))^2}}\right) - \tan^{-1}\left(\frac{V_{HB} - V_{LB}'}{z_1 * i_{dc1}(t_4)}\right) \leq \omega_1 t_{\text{dead}}. \tag{40}$$

Formula (39) guarantees that the amount of L_s is sufficient to fully charge the zero-voltage switching capacitor of switch S_{11}. Conversely, during the deadband, formula (40) ensures that V_{ds11} across S_{11} reaches the input DC voltage V_{HB}. As a result, the minimum value of the deadband zone or the maximum value of the ZVS capacitor can be limited [31].

A sufficient constraints output bridge requires the voltage V_{ds22} across S_{22} to reach the output DC voltage V_{LB} during the headband. Consequently,

$$\tan^{-1}\left(\frac{V_{HB}' + V_{LB}}{z_2 * n * i_{dc2}(t_2)}\right) + \sin^{-1}\left(\frac{V_{HB}' + V_{LB}}{\sqrt{[z_2 * n * i_{dc2}(t_2)]^2 + [V_{HB}' + V_{LB}]^2}}\right) \leq \omega_1 t_{\text{dead}}. \tag{41}$$

5. Behaviour of Converter during the Deadtime

Figure 11 illustrates a simulation of the switching waveforms during the operational states. When the time reaches $t = t_0$, the HV bridge enters its deadtime phase, causing the AC inductor current to flow from the active switches to the opposite antiparallel diode pair. This leads to the primary H-bridge being ahead of the secondary H-bridge, resulting in no phase shift error being detected [33, 34].

As a consequence, when the dead time commences at $t = t_1$, the output voltage of the LV bridge remains unchanged in polarity. The AC inductor current flowing in the anti-parallel diode of the LV bridge prevents the switching transition from altering the transmission path.

Since the phase shift error (D_{db}) is caused by the current that slews during the deadtime period, an expression that describes the slew time (D_s) can be derived [33]. Also, since the AC inductor current is cyclic and half-wave symmetric, the positive peak current and the negative peak current have the same magnitude ($|i(t_0)| = |i(t_4)|$). This means that by setting ($i(t_4) = -i(t_0)$), a method for deriving this expression is presented in [34], an expression for D_s can be solved for both the leading and lagging switching alternatives as

$$D_s = D_c - \frac{\pi}{2}\frac{V_{HB} - V_{LB}}{V_{HB}} - \frac{V_{LB}}{V_{HB}}D_{DT}, \tag{42}$$

where D_c represents the commanded phase shift, and D_{DT} is the deadtime period in radians. From the slew time equation (42), the phase shift error D_{db} is determined by first identifying the converter operating condition. This is necessary because the phase shift error augments the applied phase shift when the HV bridge leads the LV bridge and reduces it when the HV bridge lags the LV bridge. This allows D_{db} to be determined based on D_s. The relationship between D_s and D_{db} is therefore summarized in Table 5.

6. Simulation Results

MATLAB Simulink was used to simulate the circuit schematic shown in Figure 1 in order to verify the previous theoretical considerations. Table 6 contains the specifications and parameters of the system.

The simulation outcomes for the gating signals and steady-state operation waveforms in the buck mode at 5 kW rated power and a high-frequency transformer are demonstrated in Figure 12, which is consistent with the waveform simulated in Figure 2. The primary voltage of the transformer, the output voltage of the secondary bridge, the

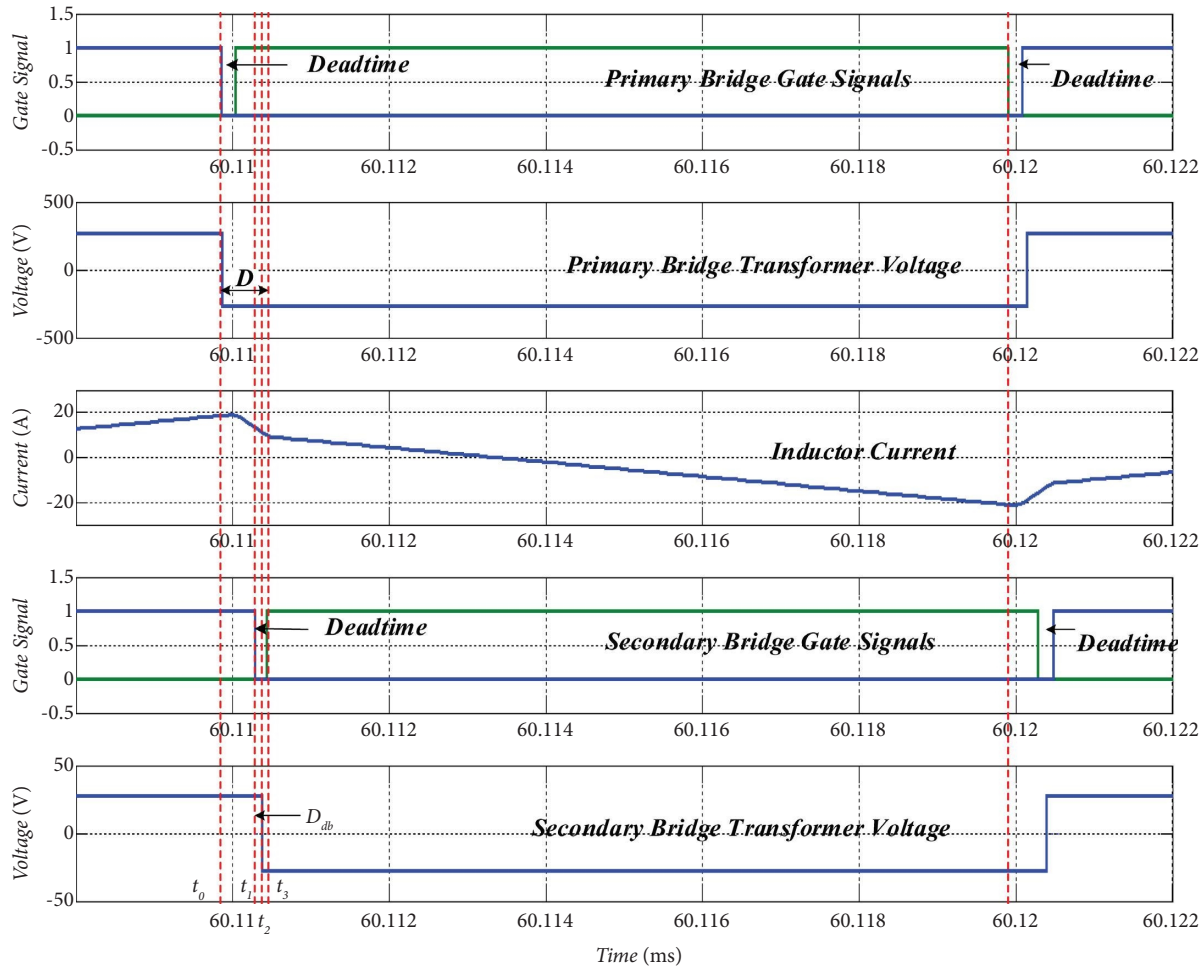


Figure 11: Deadtime effect—the primary H-bridge leads the secondary H-bridge.

Table 5: The relationship between D_s and D_{DT}, and the phase shift error effect.

	$V_{HB} > V_{LB}'$		$V_{HB} < V_{LB}'$	
	Condition	Phase shift error	Condition	Phase shift error
Primary H-bridge leads the secondary H-bridge	$D_s > D_{DT}$	0	$D_s < 0$	0
	$0 < D_s < D_{DT}$	$D_{DT} - D_s$	$0 < D_s < D_{DT}$	$-D_s$
	$D_s < 0$	D_{DT}	$D_s > D_{DT}$	$-D_{DT}$

Table 6: Main proposed circuit parameters.

Parameter descriptions	Symbol	Value
Output voltage	V_{LB}	28–35 V
Input voltage	V_{HB}	270 V
Rated power	P	5 kW
Total snubber capacitor	C_{ds}	0.1 nF
Total DAB inductance	L_s	460 μH
Transformer turns ratio	n	9.6

voltage across an inductor, and the inductor current all exhibit the same attributes as the fundamental operating waveform of the bidirectional forward converter depicted in Figure 2.

Figure 13(a) shows waveforms of the gate signals G_1 and G_2 applied to S_{11} and S_{12}, V_{ds11} and V_{ds12} are the voltages across S_{11} and S_{12}, respectively, and i_{Ls}. It can be seen that the currents $i_{Ls} > 0$ and $i_{Ls} < 0$ during the turn-on instants of S_{12} and S_{11}, respectively. The zoomed views of S_{12} and S_{11} when turned On are shown in Figures 13(b) and 13(c), respectively. The S_{11} starts to turn OFF at $t = \tau_\alpha$. For $t \le \tau_\alpha$, V_{ds11} and V_{ds12} are zero and 270 V, respectively (see Figure 13(c)). It can be observed that after $t = \tau_\alpha$, V_{ds12} decreases until it equals zero, while V_{ds11} increases linearly to 270 V. When $t = \tau_{\alpha 1}$, the S_{12} will turn on. In addition, before $t = \tau_{\alpha 1}$, $V_{ds12} = 0$, and i_{Ls} is positive at $t = \tau_{\alpha 1}$. Therefore, D_{12} conducts from $t = \tau_{\alpha 1}$ to $t = \tau_{\alpha 2}$. The switch S_{12} conducts from $t > \tau_{\alpha 2}$ as i_{Ls} become negative. It can be seen from Figure 13(c) that $V_{ds12} = 0$ at $t = \tau_{\alpha 1}$, indicating the ZVS turn-on conduction of S_{12}. Similarly, as can be seen from Figure 13(b), i_{Ls} become positive concerning $t > \tau_{\beta 1}$, so after $t = \tau_{\beta 2}$, S_{11} begins to conduct at zero voltage $V_{ds1} = 0$.

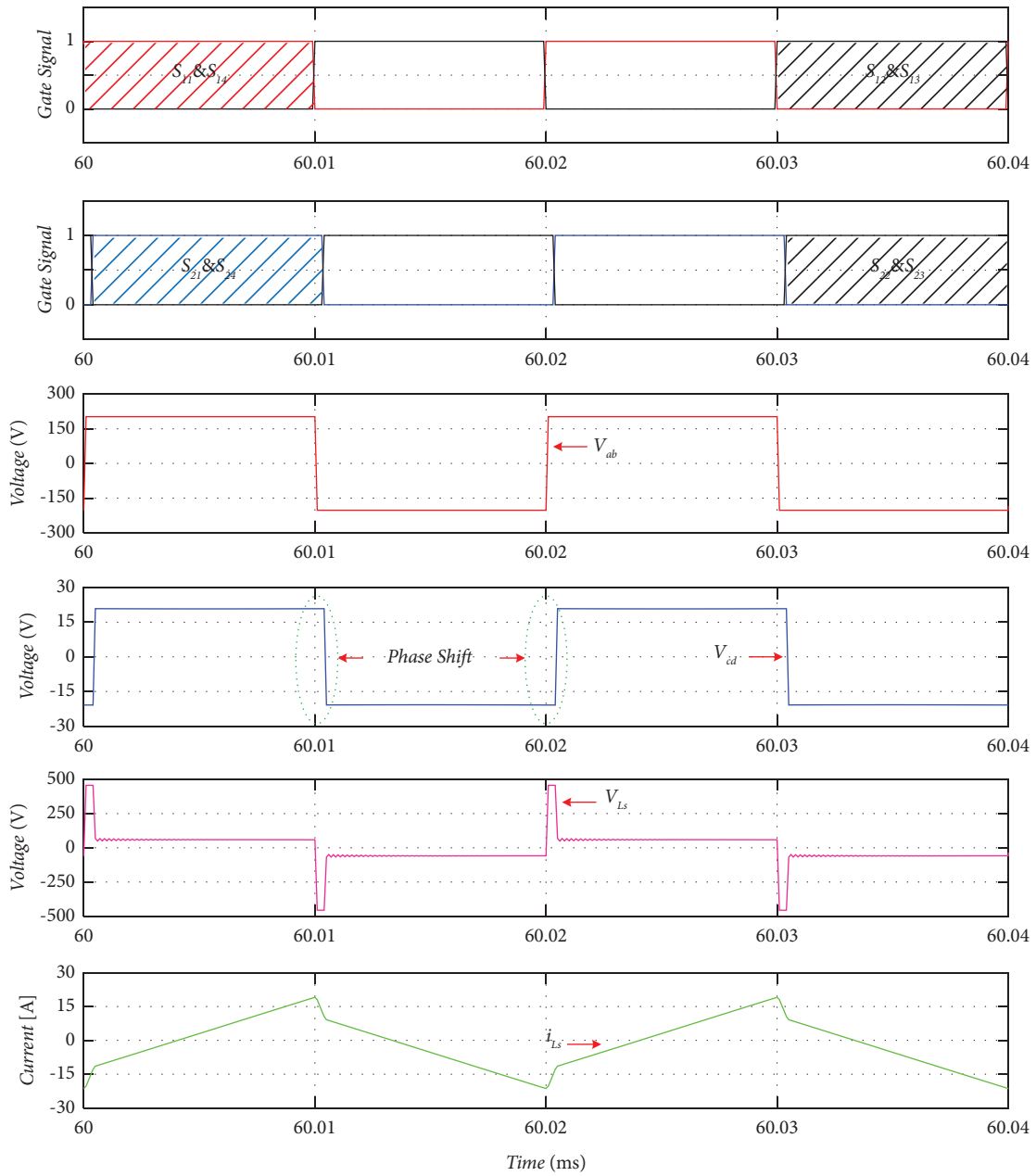


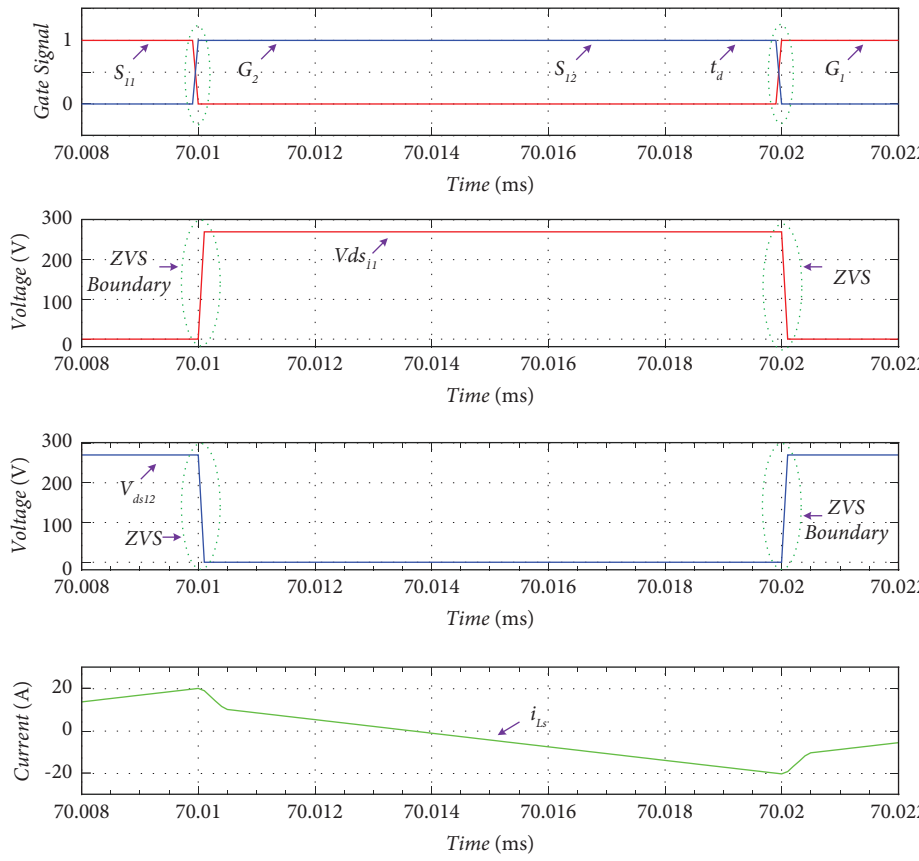
FIGURE 12: Simulation of the DAB for the proposed circuit: from top to bottom: gating signal for bridge one switches, gating signal for bridge two switches, circuit waveforms of V_{ab}, V_{cd}, and V_{Ls}, respectively, and inductor current i_{Ls}.

Similarly, you can predict the ZVS operation of the bridge-2 converter.

Figure 14 depicts a comparison between the simulation results of this study and a previous one [8], in terms of the minimum phase shift needed for the input and output bridges to meet the necessary and sufficient constraints for various output voltages. The graph demonstrates that for the lagging bridge, the minimum phase shift required to achieve ZVS decreases as the output voltage increases. On the other hand, for the leading bridge, as the output voltage increases, the minimum phase shift required to achieve ZVS increases. As a result, increasing the phase shift can widen the ZVS range and reduce switching losses, but it can also increase reactive current and conduction losses. Conversely, reducing the phase shift can lead to the opposite results. Therefore, to achieve a successful design, it is crucial to evaluate the trade-off between these factors.

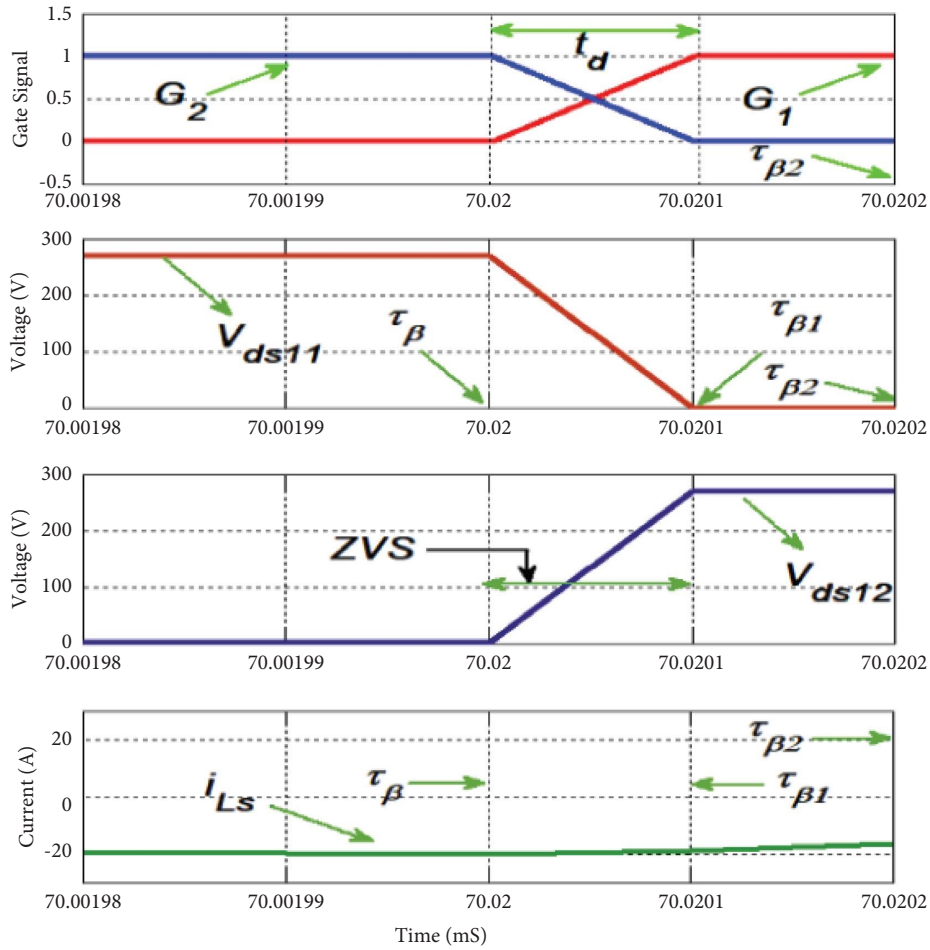
The boundaries for zero voltage switching (ZVS) are presented in Figure 15, where the power handled by the converter is depicted on the x-axis. By selecting a value of K that is marginally above 1, the operating range of the converter with ZVS can be substantially expanded.

Table 7 shows the comparison simulation results of the value of the phase shift and the power at which ZVS is lost in the leading and lagging bridge between this paper and compared reference paper [8] for different values of the output voltage. Using the value of k equal to 1, the ZVS operation will be lost approximately at 0, 400 and 750 W



(a)

Figure 13: Continued.



(b)

Figure 13: Continued.

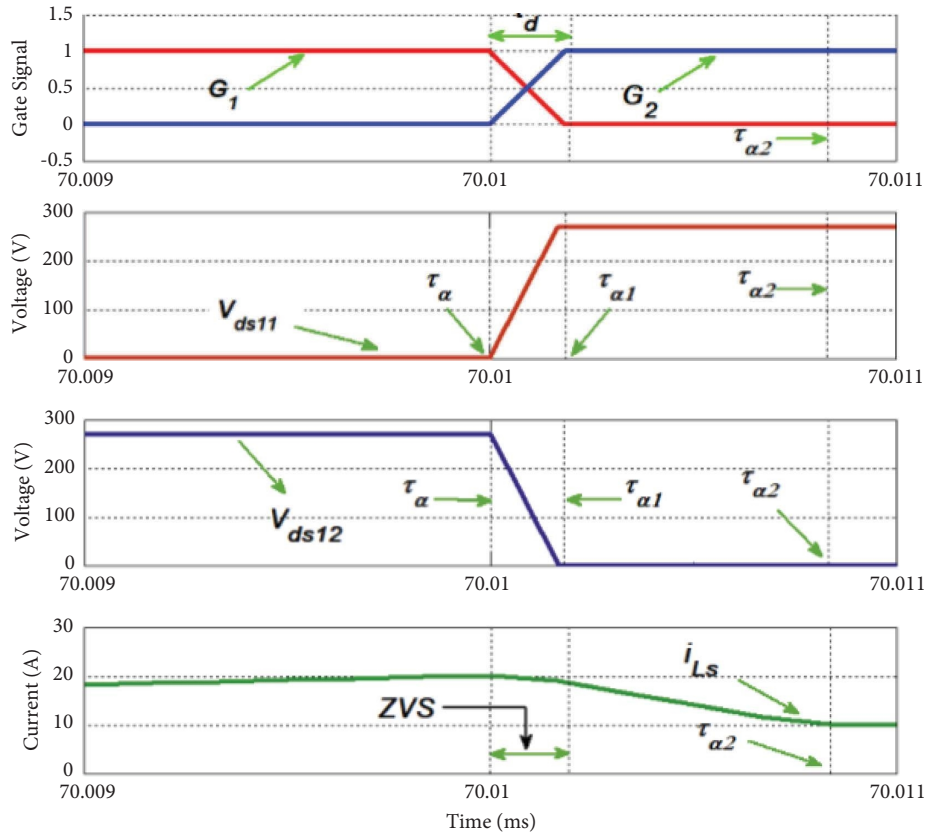


Figure 13: Impact of dead time on the primary bridge and ZVS turn-on operation of the switches S_{11} and S_{12} of the DAB.

Table 7: Comparison of the simulation results of this paper and reference paper [8].

		Simulation results in [8] Output voltage (V_{LB})			Simulation results in this paper Output voltage (V_{LB})		
		20 V	28 V	35 V	20 V	28 V	35 V
Leading bridge	D_{ZVS}	0	0.0167	0.02	0.0125	0.016	0.04
	P_{ZVS} (W)	0	400	750	100	400	1000
Lagging bridge	D_{ZVS}	0.054	0.049	0.025	0.0125	0.016	0.04
	P_{ZVS} (W)	3200	2150	1250	1700	740	250

when the sufficient boundaries to operate with D_{ZVS} are 0, 0.0167, and 0.02, respectively, for the leading bridge (input bridge). While the ZVS operation will be lost approximately for the lagging bridge at 3200, 2150, and 1250 W, when the sufficient boundaries to operate with D_{ZVS} are 0.054, 0.049, and 0.025, respectively, for the reference paper [8] (see Figures 14(a) and 15(a) and Table 6). Furthermore, as can also be seen from the Figures 14(b) and 15(b) and Table 6, ZVS operation will be lost approximately at 100, 400, and 1000 W when D_{ZVS} are 0.0125, 0.016, and 0.04 for the leading bridge. While the ZVS operation will be lost approximately for the lagging bridge at 1700, 740, and 250 W, when the sufficient boundaries to operate with D_{ZVS} are 0.0125, 0.016, and 0.04, respectively. Moreover, the operating range using ZVS can greatly increase when the k value is slightly larger than one.

When the phase shift of a dual active H-bridge bidirectional DC-DC converter is increased, the duration of overlap between upper and lower switches is reduced, leading to a decrease in switching losses. However, increasing the phase shift also causes an increase in conduction losses and reactive current, as the switching devices are subjected to higher voltage stress, resulting in increased conduction losses. In addition, the increase in reactive current results in losses from the converter's reactive components. This can cause a decrease in the efficiency of the converter. Figure 16 illustrates power efficiency curves that vary with load variation, and the efficiency is significantly low under light load conditions due to ZVS being under the RMS phase current. The RMS currents through the switches determine conduction losses. Under heavy load conditions, the converter is highly efficient because the circulating current decreases, resulting in low conduction losses.

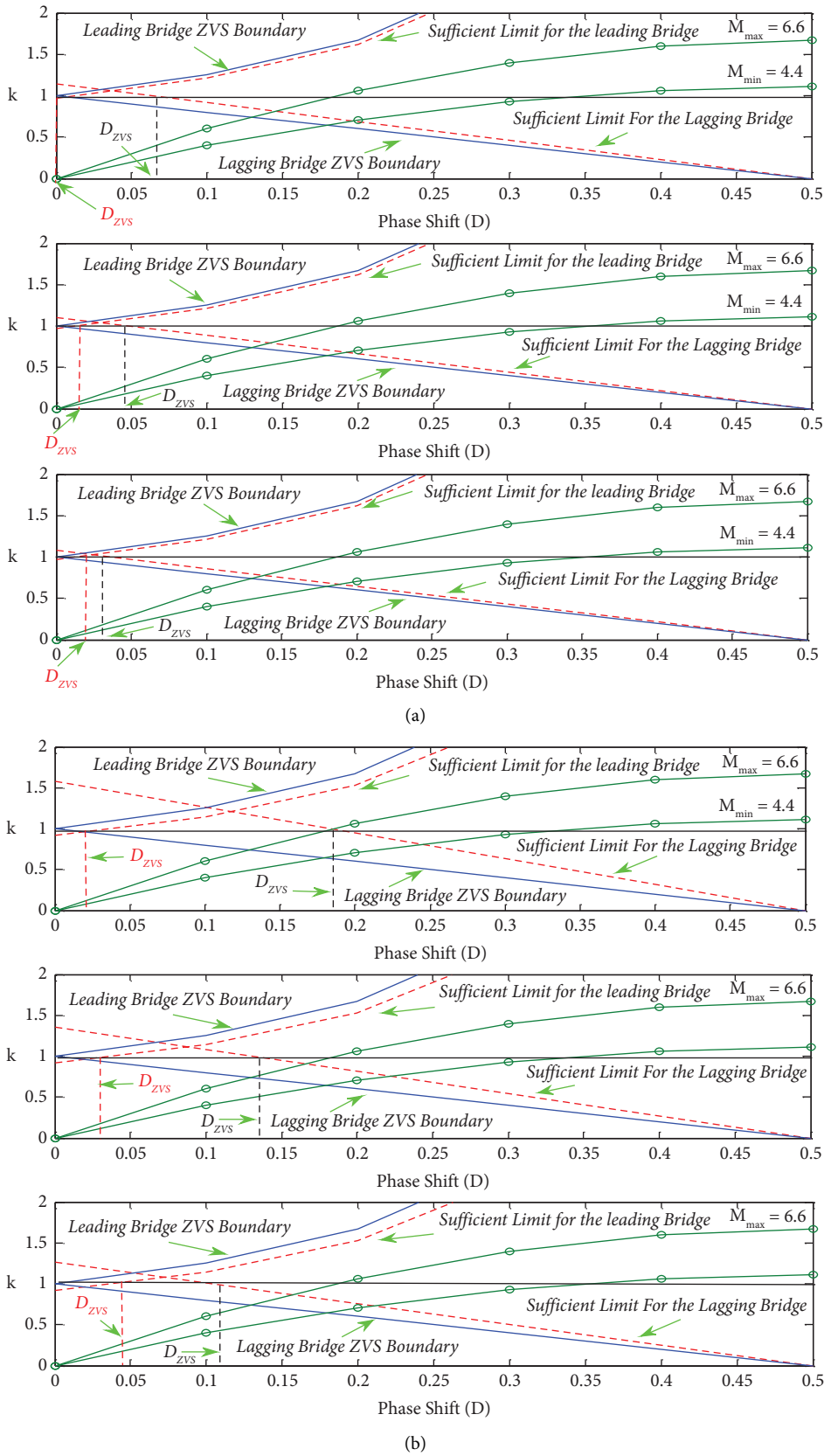


Figure 14: A simulation comparison of the necessary and sufficient constraints to achieve ZVS for input and output bridge under different output voltage between this paper and [8] using D as the x-axis. From top to bottom, V_{LB} = 20 V, 28 V, and 35 V, respectively. (a) Paper [8]; (b) this paper.

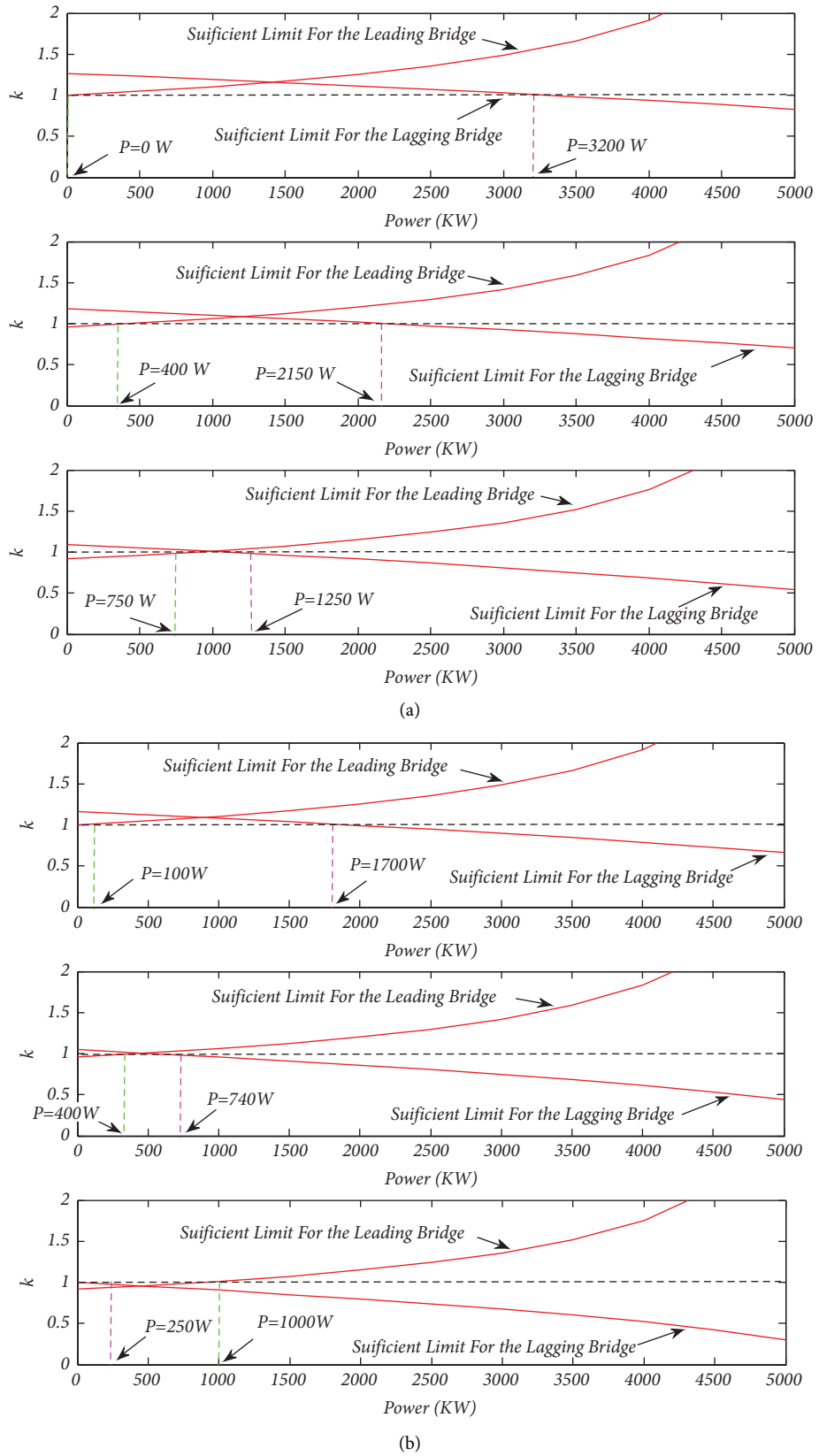


FIGURE 15: Sufficient constraints to achieve ZVS for input and output bridge under different output voltage between this paper and [8] using the power as the x-axis. From top to bottom, $V_{LB} = 20$ V, 28 V, and 35 V, respectively. (a) Paper [8]; (b) this paper.

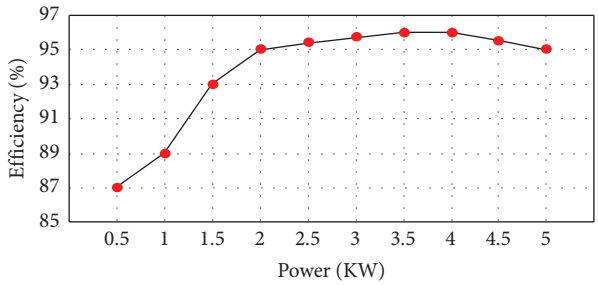


Figure 16: Efficiency of DAB from 0.5–5 kW.

7. Conclusions

This article presents a detailed theoretical analysis of the steady-state power conditions, the impact of the ZVS capacitor, and the deadband on the soft switching operation range of the DAB converter with phase shift control. The simulation results are in agreement with the theoretical analysis. The adequate conditions for achieving ZVS are calculated for both the input and output bridges, and the boundaries of sufficient conditions for ZVS operation are plotted. A comparison of sufficient constraints between our proposed system and previous studies is provided, indicating that our proposed restrictions are more accurate. The study shows that as the output voltage increases, the minimum phase shift value required to achieve ZVS decreases. Increasing the value of D expands the ZVS range and reduces switching losses, as noted in [9].

Abbreviations

ZVS: Zero voltage switching
DC: Direct current
DAB: Dual active bridge
DPS: Dual phase shift
IGBT: Insulated gate bipolar transistor
HVS: High voltage side
LVS: Low voltage side
SPS: Single phase shift
D: Phase shift
D_s: Slew time
D_{db}: Phase shift error
D_c: Commanded phase shift
D_{DT}: Deadtime period in radians.

Data Availability

The data used to support the study are included in the paper.

Conflicts of Interest

The authors declare that there are no conflicts of interest.

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