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Research Article

Electronically Tunable Grounded and Floating Capacitance Multipliers Using a Single Active Element

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A capacitance multiplier is an active circuit designed specifically to increase the capacitance of a passive capacitor to a significantly higher capacitance level. In this paper, the use of a voltage differencing differential difference amplifier (VDDDA), an electronically controllable active device for designing grounded and floating capacitance multipliers, is proposed. The capacitance multipliers proposed in this study are extremely simple and consist of a VDDDA, a resistor, and a capacitor. The multiplication factor (K_c) can be electronically controlled by adjusting the external bias current (I_B). It offers an easy way of controlling it by utilizing a microcontroller for modern analog signal processing systems. The multiplication factor has the potential to be adjusted to a value that is either less than or greater than one, hence widening the variety of uses. The grounded capacitance multiplier can be easily transformed into a floating one by utilizing Zc-VDDDA. PSpice simulation and experimentation with a VDDDA realized from commercially available integrated circuits were used to test the performance of the proposed capacitance multipliers. The multiplication factor is electronically adjustable, ranging in approximation from 0.56 to 13.94. The operating frequency range is approximately three frequency decades. The realization of the lagging and leading phase shifters using the proposed capacitance multiplier is also examined and proven. The results reveal that the lagging and leading phase shifts are electronically tuned via the multiplication factor of the proposed capacitance multipliers.

1. Introduction

The invention of integrated circuits (ICs) has led to a significant development in worldwide technological advances, particularly in electrical, electronic, and communication systems. In the last half-century, there has been a persistent focus on research and development in integrated circuit design, especially in analog signal processing systems. Many techniques have been proposed in analog circuit design, where most approaches involve the combination of active devices alongside passive components, such as resistors or capacitors. The utilization of passive inductors in circuit design is widely considered less favored due to their large size and the difficulties associated with adjusting the inductance value. Hence, employing capacitors in the design of analog signal processing circuits that involve frequency is deemed more suitable. A capacitor with a large capacitance value is needed in many applications, including low-frequency filters [1, 2], sample and hold circuits [3], locked-in amplifiers [4], and sensor applications [5]. Variable capacitors are also fundamental devices in a wide range of wireless telecommunication systems, including voltage-control oscillators, tunable filters, matching circuits, and phase shifters [6]. Although the process of fabricating a capacitor within an integrated circuit is possible [6, 7], the high-value on-chip capacitors result in significant chip area

occupation, high absolute tolerances, and restricted capacitance adjustability [1, 2, 8]. In order to handle the concerns mentioned above, the implementation of an active circuit known as the capacitance multiplier is employed. This active circuit combines a passive capacitor and/or a passive resistor. It has been designed to emulate the behavior of a significantly larger capacitor using a smaller capacitor. The parameter of the capacitance multiplier called the multiplication factor (K_c) is normally adjustable. When it is used instead of the passive capacitor in circuit designs, the parameters of these circuits, such as the cutoff frequency, the oscillation frequency, and the phase shift, are consequently tunable.

The synthesis of electronically adjustable analog circuits is increasingly appealing in contemporary analog signal processing systems. Microcomputers or programmable devices are commonly utilized to provide intelligent and autonomous control of circuits. In recent times, there has been a surge in the popularity of employing active building blocks (ABBs) for the synthesis of analog circuits [9–12]. This trend can be attributed to the significant advantages it offers in terms of simplicity, flexibility, and versatility. Combining an ABB with just a few passive components, such as capacitors or resistors, gives several analog circuits with superior performance characteristics. Furthermore, using active components with high input and low output impedances during voltage-mode circuit synthesis can eliminate the need for additional voltage buffers at the input and output stages. Additionally, some ABBs with electronically controllable properties are essential for modern circuits, as stated above. Numerous analog circuits employing electronically controllable analog ABBs have been presented in the existing body of scholarly research. The voltage differencing differential difference amplifier (VDDDA) [13] is a contemporary and flexible analog building block that exhibits adaptability and versatility in various circuit designs for analog signal processing. This device integrates the characteristics of an operational transconductance amplifier (OTA) with electronic control and a differential difference amplifier (DDA) with low-output impedance and unity gain. As a result, the transconductance of VDDDA can be adjusted electronically by utilizing an external direct current bias current. The circuit parameters of the VDDDA-based system can be electrically controlled, including the current or voltage gain, cutoff or oscillation frequency, quality factor, and bandwidth. Moreover, it is common practice in circuit synthesis to include an integrator and passive simulator while incorporating a subtractor or adder. Hence, the existence of the DDA within VDDDA presents significant benefits in expediting the synthesis procedure. Moreover, the VDDDA exhibits a high impedance at both the input-voltage and output-current terminals while maintaining a low impedance at the output-voltage terminal.

Several implementations of capacitance multipliers using different ABBs have been reported in published works [14–54]. These utilized ABBs include operational amplifier (opamp), operational transconductance amplifier (OTA), voltage buffer, current conveyor (CCII), voltage-to-current transducer (VCT), current operational amplifier (COA), current-controlled conveyor transconductance amplifier (CCCTA), modified current-feedback operational amplifier (MCFOA), voltage and current gain second generation current conveyor (VCG-CCII), differential voltage current conveyor transconductance amplifier (DV-CCTA), tunable four-terminal floating nullor (TFTFN), current control differential difference current conveyor (CCDDCC), dual-X second-generation current conveyor (DXCCII), voltage differencing current conveyor (VDCC), current follower transconductance amplifier (CFTA), fully balanced voltage differencing buffered amplifier (FB-VDBA), voltage differencing inverting buffered amplifier (VDIBA), current differencing transconductance amplifier (CDTA), current feedback operational amplifier (CFOA), third-generation current conveyor transconductance amplifier (CCIIITA), voltage conveyor (VCII), differential voltage buffer (DVB), operational transresistance amplifier (OTRA), current follower differential input transconductance amplifier (CFDITA), and VDDDA. There are two classifications of ABB-based capacitance multipliers: grounded ones [14, 16–18, 20–22, 24, 27, 28, 33, 37–41, 43–53] and floating ones [15, 18, 19, 23, 25, 26, 29–32, 34–36, 40, 42, 46, 54], as indicated in Table 1. Simple structures with a single ABB were proposed in [14, 20, 24, 28–31, 40, 42, 45, 49, 52, 53], unlike the capacitance multiplier in [15–19, 21–27, 32–41, 43, 44, 46–48, 50, 51, 54], which uses different kinds and more than one ABB. The resistor-less circuits were realized in [16, 18, 19, 23, 26, 27, 29–33, 35, 37, 41, 45, 46, 51, 53], but using more than one resistor was needed for the capacitance multipliers realized in [14, 15, 20–22, 24, 25, 28, 34, 36, 38, 40, 43, 44, 47–50, 52, 54]. The multiplication factor of the proposed capacitance multipliers in references [14, 15, 20–22, 24, 25, 28, 36, 38, 40, 43, 47, 49, 50, 54] cannot be electronically adjusted. In the given references [16, 20, 21, 24, 33, 36–38, 40–43, 49, 50, 52, 53], the inability to adjust the multiplication factor to a value greater or less than one limits its widespread applicability. A recent grounded capacitance multiplier using one VDDDA, one MOS transistor, and one capacitor was proposed [51]. The multiplication factor can be electronically tuned to be greater or less than one. However, the multiplication factor is inversely proportional to the bias current, which implies that setting the bias current to a low value will result in a high multiplication factor, thereby distorting the OTA's output signal (in VDDDA). Moreover, this grounded capacitance multiplier structure is not easy to modify as a floating type. The results of this comparison study are summarized in Table 1 (Figures 1 and 2).

This paper proposes grounded and floating capacitance multipliers with an electronic tuning of the multiplier factor. The paper covers the following topics: a description of the circuit principle is shown in Section 2, including an overview of VDDDA, proposed electronically controllable capacitance multipliers, and the effect of nonideal properties of VDDDA. Section 3 presents the results of circuit simulations using the PSpice program and the prototype experiment. Section 4 demonstrates the application examples of the capacitance multipliers and their experimental results in the lagging and leading phase

Table 1: Comparison of existing capacitance multipliers using ABBs.

Ref.	ABB	$R+C$	Floating/grounded	Electronic tune	K_c can be set to be greater or less than one	Supply (V) and power consumption (mW)	Testing	Technology
[14]	1 opamp	3 + 1	Grounded	No	Yes	NA	Experiment	IC
[15]	4 CCII	2 + 1	Floating	No	Yes	NA	NA	NA
[16]	2 OTA and 1 buffer	0 + 1	Grounded	Yes	No	NA	Experiment	IC
[17]	1 OTA and 2 buffers	1 + 1	Grounded	Yes	Yes	NA	Experiment	IC
[18]	2 OTA and 1 opamp	0 + 1	Grounded	Yes	Yes	NA	Experiment	IC
	2 OTA, 1 opamp, and 1 buffer	0 + 1	Floating	Yes	Yes	NA	Experiment	IC
[19]	4 VCT	0 + 1	Floating	Yes	Yes	±5 and NA	Both Sim. and Exp.	CD4007 CMOS
[20]	1 CCII	2 + 1	Grounded	No	No	NA	Simulation	1.2 μm CMOS
[21]	1 CCII and 1 COA	2 + 1	Grounded	No	No	±1.5 and NA	Simulation	0.5 μm CMOS
[22]	2 CCII	2 + 1	Grounded	No	Yes	5 and NA	Simulation	1.2 μm CMOS
[23]	4 CCCII	0 + 1	Floating	Yes	Yes	±2.5 and NA	Simulation	BJT
[24]	1 AD844 (Cir. I and II)	2 + 1	Grounded	No	No	NA	Experiment	IC
	2 AD844 (Cir. III)	2 + 1	Grounded	No	No	NA	Experiment	IC
[25]	2 DO-CCII	2 + 1	Floating	No	Yes	±2.5 V and NA	Simulation	BJT AT and T
[26]	1 DVCC and 2 CCCII	0 + 1	Floating	Yes	Yes	±2.5 and 7.3	Simulation	BJT AT and T
[27]	2 CCCTA	0 + 1	Grounded	Yes	Yes	±1.5 and 0.82	Simulation	BJT AT and T
[28]	1 MCFOA	2 + 1	Grounded	No	Yes	±1.5 and 0.52	Both Sim. and Exp.	0.25 μm CMOS and IC
[29]	1 VCG-CCII	0 + 1	Floating	Yes	Yes	2 and 0.7	Simulation	0.35 μm CMOS
[30]	1 DV-CCTA	0 + 1	Floating	Yes	Yes	±1.5 and 0.48	Simulation	BJT AT and T
[31]	1 TFTFN	0 + 1	Floating	Yes	Yes	±10 and NA	Simulation	BJT and IC
[32]	3 CCDDCC	0 + 1	Floating	Yes	Yes	±1.25 and NA	Simulation	0.25 μm CMOS
[33]	1 DXCCI and 2 MOS	0 + 1	Grounded	Yes	No	±1.65 and 0.2	Simulation	0.35 μm CMOS
[34]	2 VDCC	2 + 1	Floating	No	Yes	±0.9 V and NA	Simulation	0.18 μm CMOS
[35]	2 FB-VDBA	0 + 1	Floating	Yes	Yes	±1 and NA	Simulation	0.35 μm CMOS
[36]	2 DVCC	2 + 1	Floating	No	No	±0.75 and 1.29	Simulation	0.13 μm CMOS
[37]	1 VDIBA and 1 MOS	0 + 1	Grounded	Yes	No	±0.75 and 5.27	Simulation	0.25 μm CMOS
[38]	1 CCII and 1 buffer	2 + 1	Grounded	No	No	±0.9 V and NA	Experiment	0.18 μm CMOS
[39]	2 VDBA	1 + 1	Grounded	Yes	Yes	±0.75 and 1.57	Simulation	CMOS 0.25 μm
[40]	1 CDTA*	1 + 1	Grounded	Yes	No	NA	Experiment	0.7 μm CMOS
	1 CDTA**	2 + 1	Grounded	No	No	NA	Experiment	0.7 μm CMOS
	1 CDTA and 1 DVB***	1 + 1	Floating	Yes	No	NA	Experiment	0.7 μm CMOS
	1 CDTA and 1 DVB****	2 + 1	Floating	No	No	NA	Experiment	0.7 μm CMOS
[41]	2 VDBA	0 + 1	Grounded	Yes	No	±0.75 and 0.75	Simulation	0.25 μm CMOS
[42]	1 FB-VDBA	1 + 1	Floating	Yes	No	±0.75 and 7.4	Simulation	0.25 μm CMOS
[43]	2 CFOA	2 + 1	Grounded	No	No	±0.75 and NA	Both Sim. and Exp.	0.35 μm CMOS and IC

Table 1: Continued.

Ref.	ABB	$R+C$	Floating/grounded	Electronic tune	K_c can be set to be greater or less than one	Supply (V) and power consumption (mW)	Testing	Technology
[44]	2 CFOA	2 + 1	Grounded	No	Yes	±0.9 and 223	Both Sim. and Exp.	IC
[45]	1 CCIIITA	0 + 1	Grounded	Yes	Yes	±1.5 and 0.97	Both Sim. and Exp.	CMOS 0.18 μm and IC
[46]	1 DVB and 1 ECCII	0 + 1	Grounded	Yes	Yes	±5 and 360	Experiment	IC
	1 DVB, 1 ECCII, and 1 VGA	0 + 1	Floating	Yes	Yes	±5 and 540	Experiment	IC
[47]	2 OTRA and 1 buffer	2 + 1	Grounded	No	Yes	±0.9 and 0.83	Simulation	0.18 μm CMOS
[48]	2 CFTA	2 + 1	Grounded	Yes	Yes	±0.75 and NA	Both Sim. and Exp.	0.13 μm CMOS and IC
[49]	1 ICFOA	2 + 1	Grounded	No	No	±1.25 and 0.024	Both Sim. and Exp.	0.18 μm CMOS and IC
[50]	2 VCII	2 + 1	Grounded	No	No	±1.65 and 1.5	Both Sim. and Exp.	0.35 μm CMOS and IC
[51]	1 VDDDA and 1 MOS	0 + 1	Grounded	Yes	Yes	±0.9 and 0.67 ±5 and NA	Both Sim. and Exp.	0.18 μm CMOS and IC
[52]	1 CFDITA	2 + 1	Grounded	Yes	No	±1.25 and NA	Both Sim. and Exp.	0.18 μm CMOS and IC
[53]	1 MO-VDTA	0 + 1	Grounded	Yes	No	±0.9 and 0.42 ±12 and NA	Both Sim. and Exp.	0.18 μm CMOS and IC
[54]	2 ICFOA	2 + 1	Floating	No	Yes	±1.25 and 1.49 ±6 and NA	Both Sim. and Exp.	0.18 μm CMOS and IC
This work	1 VDDDA	1 + 1	Grounded	Yes	Yes	±5 and 201	Both Sim. and Exp.	IC
	1 Zc-VDDDA	1 + 1	Floating	Yes	Yes	±5 and 257	Both Sim. and Exp.	IC

NA indicates that information is not available.

shifters. Finally, Section 5 summarizes the overall content of this paper.

2. Principle of the Proposed Circuit

2.1. Overview of VDDDA. The voltage differencing differential difference amplifier (VDDDA) is a recent active component that is effectively employed for synthesizing and designing analog signal processing circuits [13]. The VDDDA comprises an operational transconductance amplifier (OTA) and a unity-gain differential difference amplifier (DDA), endowing it with many advantageous characteristics. The OTA section offers several advantages, namely, an expanded frequency range of operation, electronic controllability, and precise parameter adjustment capabilities. Moreover, the DDA demonstrates a high impedance at input voltage terminals, a low impedance at output voltage terminals, and the capacity to execute mathematical computations. Figure 3(a) displays the block diagram of the VDDDA. The diagram depicted in Figure 3(b) represents the VDDDA's equivalent circuit, and internal construction based on commercially available ICs is shown in Figure 3(c) [55].

VDDDA contains high impedance terminals, v_+, and v_-, at the OTA section, similar to z, n, and p terminals at the VDU section, as depicted in Figures 3(a) and 3(b). The voltage difference between the v_+ and v_- terminals is transferred to the current at the z terminal through the transconductance, g_m. A direct current bias imposed externally and defined as I_B directly relates to this transconductance. The voltage present at the low output voltage terminal, w, is produced by converting the voltage differential between the z, n, and p terminals. The following matrix equation can be used to model the port characteristic equation for an ideal VDDDA [13]:

$$\begin{pmatrix} i_+ \\ i_- \\ i_z \\ i_n \\ i_p \\ v_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 1 & 0 \end{pmatrix} \begin{pmatrix} v_+ \\ v_- \\ v_z \\ v_n \\ v_p \\ i_w \end{pmatrix}. \quad (1)$$

As shown in Figure 3(c), the VDDDA in this design is implemented utilizing the commercial ICs LT1228 [56] and AD830 [57]. g_m for this VDDDA's structure is given by [56]

$$g_m = \frac{I_B}{3.87V_T}. \quad (2)$$

V_T in equation (2) represents thermal voltage. As indicated by equation (2), g_m is temperature dependent. At room temperature, $g_m \cong 10I_B$. g_m may be regulated electronically by adjusting the bias current I_B. This implies that a microcomputer or microcontroller can easily control circuits based on the LT1228.

2.2. Proposed Grounded Capacitance Multiplier. The proposed grounded capacitance multiplier is depicted in Figure 3. It is constructed of a single VDDDA, a single grounded resistor, and a single floating capacitor. IB, or the bias current, is used to adjust the transconductance gain of the VDDDA electronically. Although the proposed circuit requires a floating capacitor, the metal-oxide-metal (MOM), double poly (poly1-poly2), or metal-insulator-metal (MIM) capacitor processes can be used to fabricate the floating capacitor [58]. Based on equation (1), a circuit analysis can be performed to determine the grounded capacitance multiplier's input impedance (the ratio of v_{in} to i_{in}), which is defined as

$$Z_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} = \frac{1}{\text{sg}_m\text{RC}}. \quad (3)$$

So, from equation (3), it is clear that the proposed circuit realizes a grounded capacitor, and the equation of the equivalent capacitance is given by

$$C_{\text{eq}} = g_m\text{RC}. \quad (4)$$

From equation (4), the multiplication factor (K_C) is given by

$$K_C = g_mR = 10I_BR. \quad (5)$$

It is found from equations (4) and (5) that the original capacitance (C) is multiplied by the multiplication factor, K_C, which is electronically controlled via the bias current, I_B. Additionally, the multiplicand can be varied to be greater or less than one.

2.3. Modification as the Floating Capacitance Multiplier. It is well known that the floating type of passive element provides a better winding application than the grounded one. So, the grounded capacitance multiplier designed in Figure 4 is modified to obtain the floating type, as depicted in Figure 1(a). The proposed floating capacitance multiplier consists of a single z-copy VDDDA, a single grounded resistor, and a single floating capacitor. The z-copy VDDDA possesses characteristics identical to VDDDA in all aspects except for the addition of the z-copy terminal. The magnitude of the current at the z-copy terminal is equal to the magnitude of the current at the z-terminal, but they flow in opposite directions. Figure 1(b) illustrates the internal construction of the z-copy VDDDA realized from the commercially available integrated circuits.

Routine procedures analyze the circuit in Figure 1(a) and identify the input impedance as follows:

$$Z_{\text{in}} = \frac{v_{\text{in1}} - v_{\text{in2}}}{i_{\text{in1}}} = \frac{v_{\text{in2}} - v_{\text{in1}}}{i_{\text{in2}}} = \frac{1}{\text{sg}_m\text{RC}}. \quad (6)$$

So, from equation (6), it is clear that the proposed circuit realizes a floating capacitor, and the equations of the equivalent capacitance and the multiplication factor of the floating capacitance multiplier are the same as the grounded one.

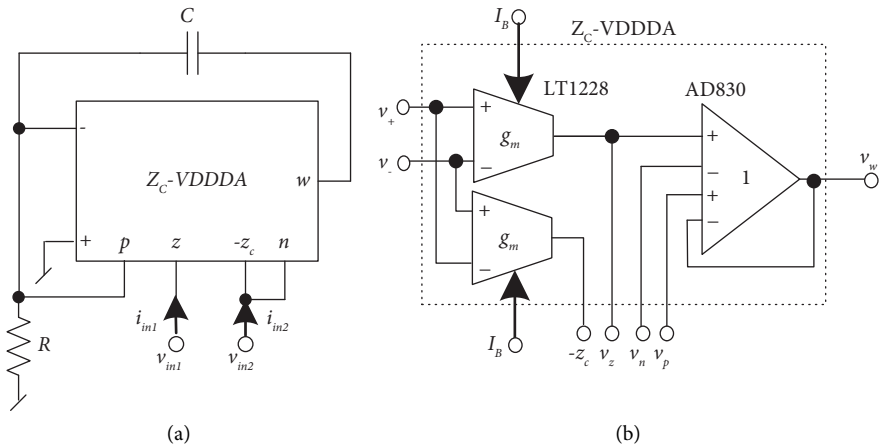


Figure 1: (a) Proposed floating capacitance multiplier and (b) internal construction of Z_C-VDDDA.

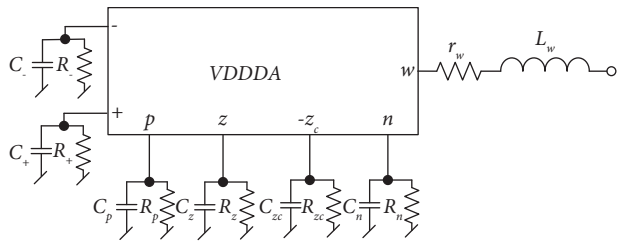


Figure 2: VDDDA equivalent circuit with parasitic capacitance and resistance [55].

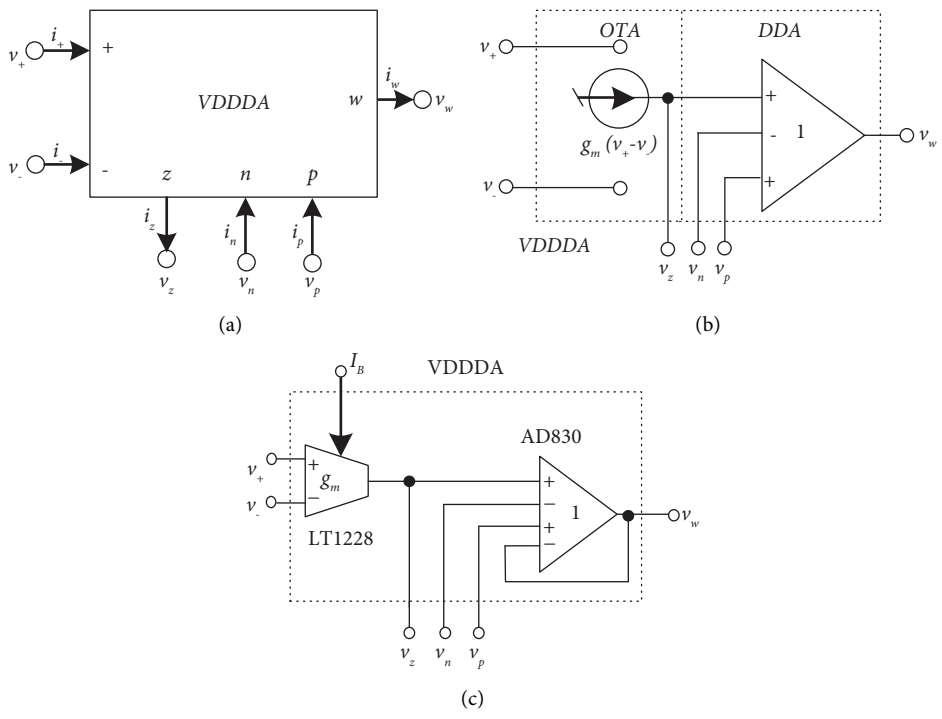


Figure 3: (a) VDDDA symbology and (b) an equivalent representation and (c) internal construction of the VDDDA.

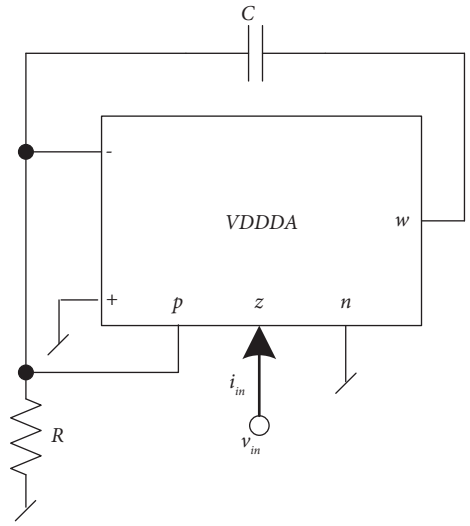


Figure 4: Proposed grounded capacitance multiplier.

2.4. Effect of Voltage Gain Errors. The nonideal characteristics of the VDDDA may impact the performance of the proposed capacitance multipliers. Hence, this section will examine and analyze these nonideal scenarios. To begin with, we will examine the voltage gain errors that occur in the VDU stage of the VDDDA. The VDDDA characteristic with the voltage gain errors is defined by [13]

$$\begin{pmatrix} i_+ \\ i_- \\ i_z \\ i_n \\ i_p \\ v_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \beta_z & -\beta_n & \beta_p & 0 \end{pmatrix} \begin{pmatrix} v_+ \\ v_- \\ v_z \\ v_n \\ v_p \\ i_w \end{pmatrix}. \tag{7}$$

In this context, the symbol β_z represents the voltage gain error between the z and w terminals, β_n represents the voltage gain error between the n and w terminals, and β_p represents the voltage gain error between the p and w terminals. Due to these mistakes, the input impedance of the proposed grounded capacitance multiplier is the same as the input impedance at port v_{in2} of the proposed floating capacitance multiplier, where port v_{in2} is grounded. This can be shown mathematically as

$$Z_{\text{in}}^* = Z_{\text{in1}}^* \mid_{v_{\text{in2}}=0} = \frac{1}{s\beta_z g_m \text{RC}} + \frac{1}{\beta_z g_m} - \frac{\beta_p}{\beta_z g_m}. \tag{8}$$

The input impedance at port v_{in2} of the proposed floating capacitance multiplier, where port v_{in1} is grounded, can be given by

$$Z_{\text{in2}}^* \mid_{v_{\text{in1}}=0} = \frac{1}{s\beta_z g_m \text{RC}} + \frac{1}{\beta_z g_m} - \frac{\beta_n}{\beta_z g_m}. \tag{9}$$

The last two nonideal terms $(1/\beta_z g_m - \beta_p/\beta_z g_m)$ in equation (8) and $(1/\beta_z g_m - \beta_n/\beta_z g_m)$ in equation (9) appear to be the resistance connected in series with the capacitance. These nonideal terms will affect the workability of the proposed capacitance multipliers in the high-frequency region.

2.5. Effect of Parasitic Elements. Next, we will examine the impact of parasitic impedances on the input and output terminals of the VDDDA. The parasitic impedances present in the circuit include the parallel capacitance (C_+) and resistance (R_+) at the v_+ terminal, the parallel capacitance (C_-) and resistance (R_-) at the v_- terminal, the parallel capacitance (C_z) and resistance (R_z) at the z terminal, the parallel capacitance (C_n) and resistance (R_n) at the n terminal, the parallel capacitance (C_p) and resistance (R_p) at the p terminal, the parallel capacitance (C_{zc}) and resistance (R_{zc}) at the z-copy terminal (for Z_c-VDDDA), and the series resistance (r_w) and inductance (L_w) at the low output impedance w terminal as depicted in Figure 2 [55]. For standard VDDDA, there is no z-copy terminal, so the parasitic capacitance C_{zc} and resistance R_{zc} are neglected.

At high frequencies, the operation of the proposed circuits is limited by the parasitic capacitances C_-, C_p, and the parasitic resistance, r_w. The operation frequency of the proposed circuits caused by these parasitic elements is determined by

$$f_{\text{op}} \ll \frac{1}{2\pi\sqrt{C\left(C_- + C_p\right)\left(R//R_-//R_p\right)r_w}}. \tag{10}$$

Equation (10) reveals a noteworthy discovery: to ensure that the proposed circuits may function effectively at higher frequencies, it is crucial to adjust the capacitance factor through the transconductance g_m. It is advisable to use a resistor R with a low value to maximize the operational frequency. If the operational frequency of the proposed circuits is less than equation (10), the parasitic capacitances C_- and C_p's effects are ignored. So, the input impedance of the proposed grounded capacitance multiplier and the input

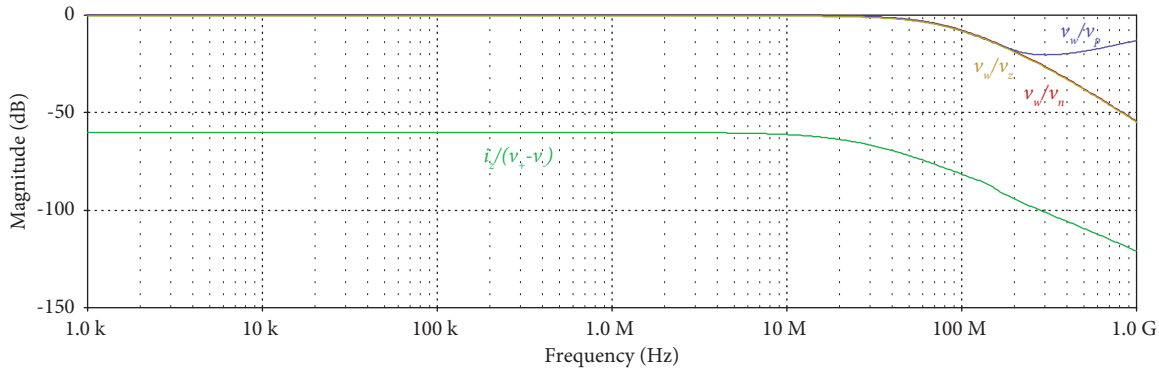


Figure 5: Simulated AC analyses of VDDDA.

impedance at port v_{in1} of the proposed floating capacitance multiplier (where port v_{in2} is grounded) can be shown mathematically as

$$Z_{in}^{*} = Z_{in1}^{*} \mid_{v_{in2}=0} = \left\{ \frac{1}{\mathrm{sCg}_m\left(R//R\_//R_p\right)} + \frac{sL_w}{g_m\left(R//R\_//R_p\right)} + \frac{r_w}{g_m\left(R//R\_//R_p\right)} \right\} // \frac{1}{\mathrm{sC}_z} // R_z. \tag{11}$$

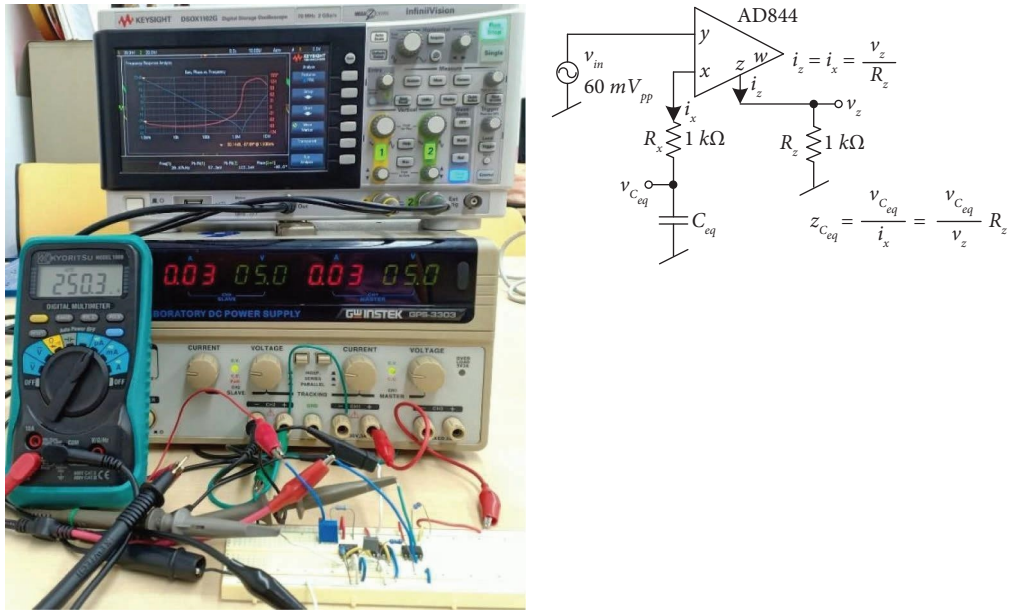
The input impedance at port v_{in2} of the proposed floating capacitance multiplier, where port v_{in1} is grounded, can be given by

$$Z_{in1}^{*} \mid_{v_{in1}=0} = \left\{ \frac{1}{\mathrm{sCg}_m\left(R//R\_//R_p\right)} + \frac{sL_w}{g_m\left(R//R\_//R_p\right)} + \frac{r_w}{g_m\left(R//R\_//R_p\right)} \right\} // \frac{1}{s\left(C_{zc} + C_n\right)} // R_{zc} // R_n. \tag{12}$$

Equations (11) and (12) reveal that the term in the blanket is the series of capacitance, inductance, and resistance, which is parallel with C_z and R_z for the grounded one and C_{zc}, C_{zn}, R_{zc}, and R_n for the floating one. Equations (11) and (12) align with the study findings discussed in references [59, 60]. The parasitic resistances R_z, R_{zc}, and R_n influence the operation of the proposed capacitance multipliers at low frequencies, according to equations (11) and (12). In contrast, at high frequencies, they are affected by the parasitic inductance L_w.

3. Simulation and Experimental Results

In this section, the grounded and floating capacitance multipliers were tested with the help of the PSpice program and a prototype experiment. The internal schemes of the VDDDA and Z_c-VDDDA were made with commercially available integrated circuits (ICs): the LT1228 and the AD830, as shown in Figures 1(b) and 3(c), respectively. In the simulation, the PSpice macromodels of the LT1228 and AD830 discrete components were employed. The circuits were biased with ±5 VDC power supplies. The performance of the VDDDA was simulated using AC analysis, and the results are shown in Figure 5. The bias current was chosen to be $I_B = 100\,\mu$A, leading to a g_m value of approximately 0.962 mA/V. The voltage gain errors β_z, β_p, and β_n are 0.993, 0.995, and 0.993, respectively. The −3 dB frequency voltage gains of v_w/v_z, v_w/v_p, and v_w/v_n are 59.01 MHz, 57.54 MHz, and 59.01 MHz, respectively. Figure 6(a) depicts the experimental setup for testing the proposed capacitance multipliers. The circuit shown in Figure 6(b) was utilized to assess the magnitude and phase characteristics of the input



(a) (b)

Figure 6: (a) Experimental setup and (b) impedance testing circuit [51].

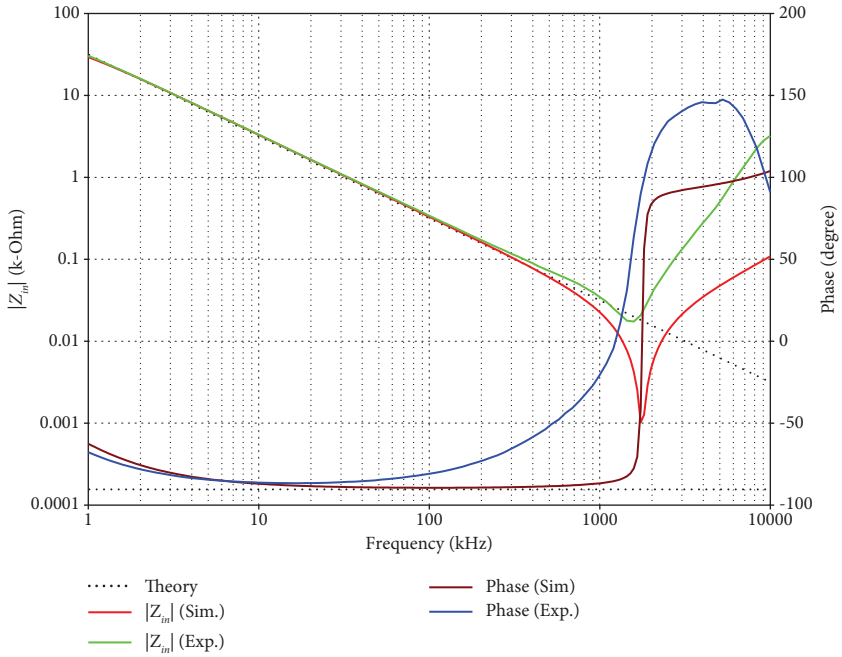


Figure 7: The magnitude and phase response of Z_{in} obtained from the grounded capacitance multiplier.

Table 2: The tested results of the grounded capacitance multiplier at $f = 20$ kHz.

Parameters	Theory	Simulation	Experiment
Z_{in} (kΩ)	1.59	1.65	1.66
Phase (degree)	−90.00	−88.45	−86.54
Kc	5.00	4.82	4.79

impedance in the proposed grounded and floating capacitance multipliers, which were obtained from [51]. This circuit uses AD844 as an active component.

The purpose of the circuits is to achieve a multiplication factor, K_C, of 5. This is accomplished by configuring the circuits (both grounded and floating types) with an I_B value of 250 μA, corresponding to a transconductance (g_m) of

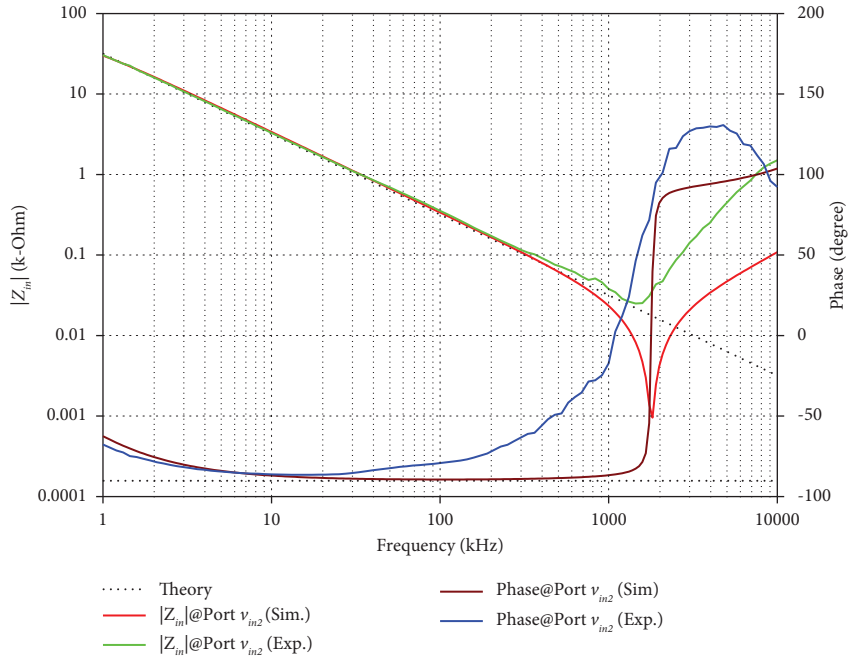


Figure 8: The magnitude and phase response of Z_{in2} obtained from port v_{in2} ($v_{in1} = 0$) of the floating capacitance multiplier.

Table 3: The tested results of the floating capacitance multiplier (only port v_{in2}) at $f = 20$ kHz.

Parameters	Idea	Simulation	Experiment
Z_{in2} (kΩ)	1.59	1.61	1.65
Phase (degree)	−90.00	−88.51	−86.38
Kc	5.00	4.94	4.80

2.5 mS. The bias currents were fine-tuned using the bias resistor (R_B). In order to achieve this, the variable bias resistors were connected between the bias terminal (pin 5) of the LT1228 integrated circuits (ICs) and the ground. The selection of the capacitor and resistor was made with a value of $C = 1$ nF and $R = 2$ kΩ. Figure 7 displays the magnitude and phase response of the input impedance obtained from the grounded capacitance multiplier. In a valid frequency range, the experimental magnitude of the input impedance shows an inverse relationship with frequency. On the other hand, the phase response stays close to −90 degrees. The ideal, simulated, and experimental values of Z_{in}, phase, and K_c are summarized in Table 2. These values were evaluated explicitly at a frequency of 20 kHz. The power consumption of the grounded capacitance multiplier was measured by the utilization of the PSpice program and experimental measurements, resulting in power values of 201 mW and 225 mW, respectively.

Because the input impedance at port v_{in1} of the proposed floating capacitance multiplier (where port $v_{in2} = 0$) is the same as the input impedance of the proposed grounded capacitance multiplier, only the input impedance at port v_{in2} of the proposed floating capacitance multiplier was tested. Figure 8 displays the magnitude and phase response of the input impedance obtained from port v_{in2} of the floating capacitance multiplier. The ideal, simulated, and experimental values of Z_{in}, phase, and K_c of the floating capacitance multiplier are summarized in Table 3. The power consumption of the floating capacitance multiplier, as determined through simulation and experimentation, was found to be 257 mW and 293 mW, respectively.

The results of multiplication factor-tuning are illustrated in Figure 9. In this result, the I_B values were manipulated at 50 μA, 125 μA, and 250 μA. The remaining active and passive element values remain unchanged, as previously stated. With these I_B values, the experimental capacitance multiplier factors were obtained as 1.11, 2.59, and 4.79, respectively. The result depicted in Figure 9 demonstrates the electronic adjustability of the capacitance multiplier factor, as indicated in equation (5). Sweeping the bias current I_B from 20 μA to 800 μA produced a variation in the experimental multiplication factor that ranged from 0.56 to 13.94. The corresponding results, along with the theoretical evaluations, are shown in Figure 10. To analyze the effect of variations in passive components on the proposed grounded capacitance multiplier, a Monte Carlo analysis was conducted using a 10% deviation in passive elements. Figures 11(a) and 11(b) display the magnitude and phase responses of the input impedance after 100 runs, respectively.

4. Application Examples

In this section, phase shifters with lagging and leading phases are designed as application examples. The proposed grounded capacitance multiplier was utilized for the lagging phase shifter depicted in Figure 12(a), while the proposed floating capacitance multiplier was employed for the leading phase shifter illustrated in Figure 12(b). The equations of the lagging and leading phase shifters are, respectively, given by

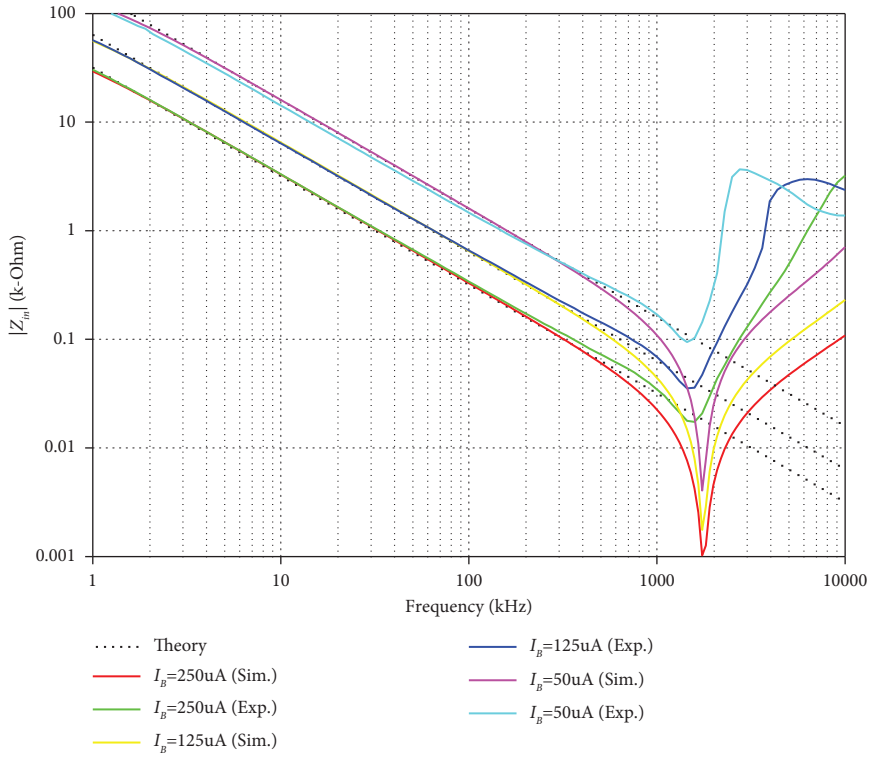


Figure 9: The magnitude of Z_{in} for different I_{B} values.

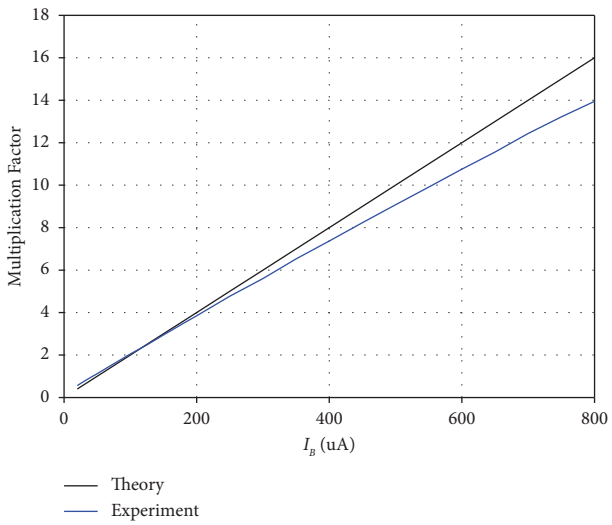


Figure 10: The experimental multiplication factor versus I_{B}.

$$\theta_{\text{lag}} = -2\tan^{-1}\left(2\pi f R_2 C_{\text{eq}}\right), \tag{13}$$

and

$$\theta_{\text{lead}} = 180 - 2\tan^{-1}\left(2\pi f R_2 C_{\text{eq}}\right). \tag{14}$$

Substituting C_{eq} in equation (4) into equations (13) and (14), the equations of the lagging and leading phase shifters, respectively, became

$$\theta_{\text{lag}} = -2\tan^{-1}\left(20\pi f R_2 \text{RCI}_B\right), \tag{15}$$

and

$$\theta_{\text{lead}} = 180 - 2\tan^{-1}\left(20\pi f R_2 \text{RCI}_B\right). \tag{16}$$

It is seen from equations (15) and (16) that the phase shift is electronically controlled by I_B.

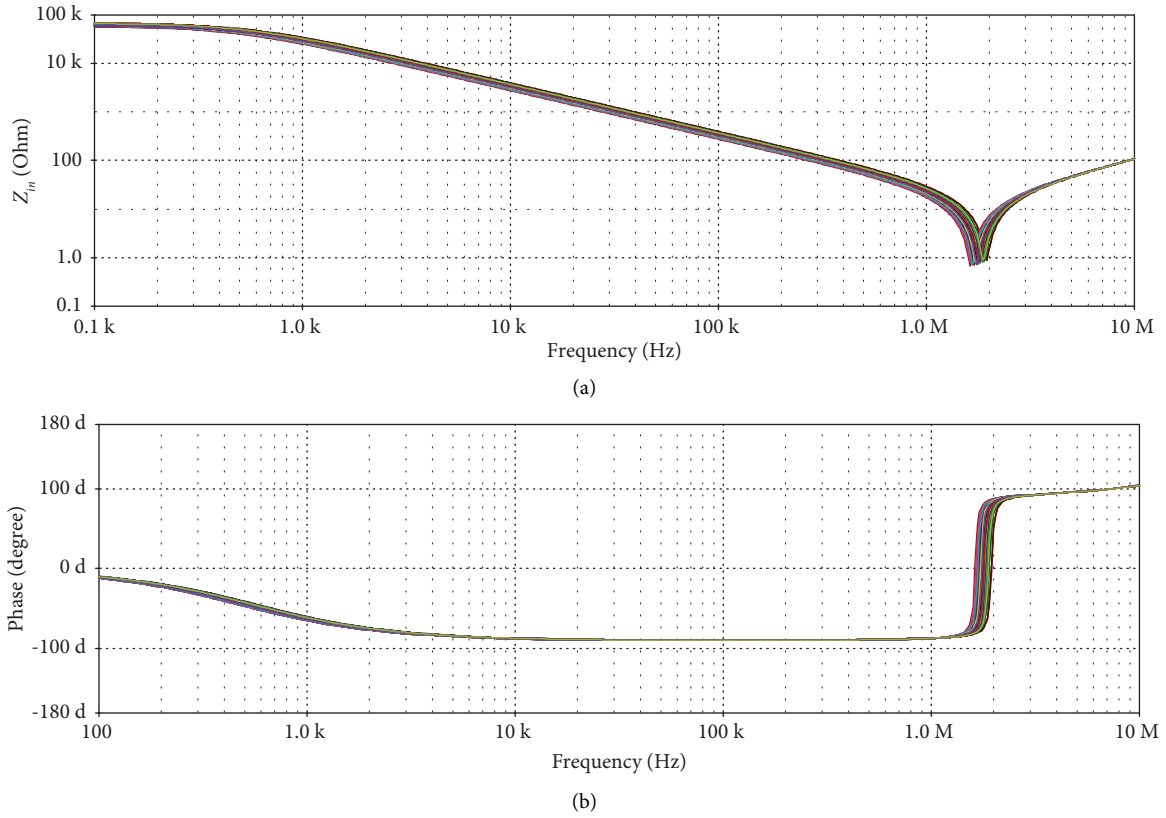


Figure 11: A Monte Carlo analysis with 100 running for 10% passive elements changes (a) magnitude (b) phase.

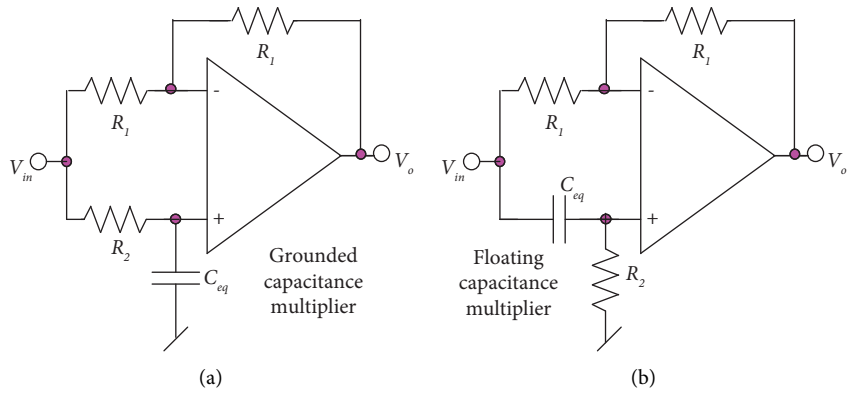


Figure 12: (a) The lagging phase shifter and (b) the leading phase shifter.

The lagging phase shifter using the proposed grounded capacitance multiplier depicted in Figure 12(a) was experimentally tested with ±5 VDC power supplies. The LF351 opamp was employed. The selection of the active and passive elements was made with a value of $I_B = 150\,\mu$A, $C = 1$ nF, $R = 2\,$kΩ (in capacitance multiplier), $R_1 = 2\,$kΩ, and $R_2 = 0.33\,$kΩ. Figure 13 displays the gain and phase response of the lagging phase shifter. Within an acceptable frequency range, the measured and simulated voltage gains are around 0 dB, while the measured and simulated phase shifts with respect to frequency range from 0 degrees to approximately −120 degrees. When the frequency is higher than 300 kHz, the measured and simulated responses significantly differ from the expected responses. This is due to the parasitic element and the opamp's gain bandwidth. The output voltage of the lagging phase shifter is demonstrated in Figure 14, where a sinusoidal input waveform with 50 mVp-p at 200 kHz was applied. The measured voltage gain is 0.905 (9.5% error), and the measured phase shift is −103.3 degrees (0.87% error). The electronic controllability of the lagging phase shift by varying the bias current (50 μA, 100 μA, and 150 μA) is depicted in Figure 15. With these I_B values, the experimental phase shifts at $f = 100\,$kHz were obtained as −24.96°, −44.57°, and −61.91°, respectively. The result

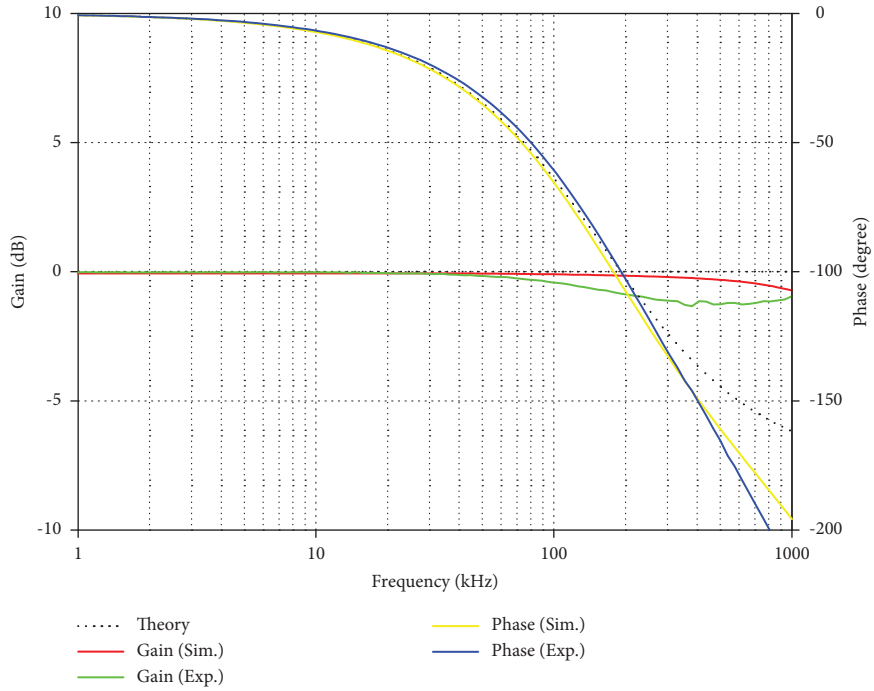


Figure 13: The gain and phase response of the lagging phase shifter.

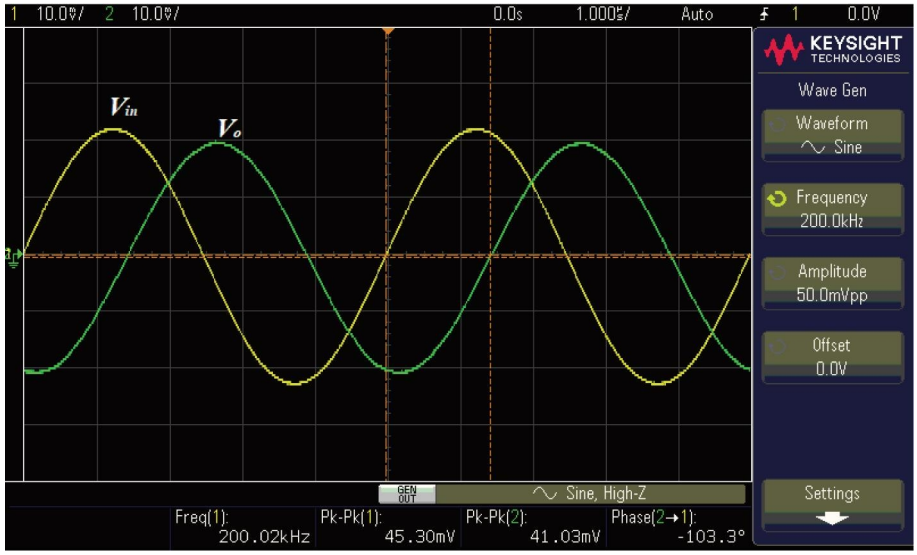


Figure 14: Measured input and output waveforms of the lagging phase shifter.

depicted in Figure 13 demonstrates the electronic adjustability of the lagging phase shift, as indicated in equation (15).

The leading phase shifter was also experimentally tested. The active and passive element selection was the same as the lagging phase shifter, except $R_2 = 0.47\,\text{k}\Omega$. Figure 16 displays the gain and phase response of the leading phase shifter. Within an acceptable frequency range, the experimental and simulated voltage gains of the leading phase shifter are around 0 dB, while the experimental and simulated leading phase shifts with respect to a frequency range from 180 degrees to approximately 35 degrees. When the frequency is higher than 300 kHz, the measured and simulated responses significantly differ from the expected responses. This is due to the parasitic element and the opamp's gain bandwidth. The output voltage of the leading phase shifter is demonstrated in Figure 17, where a sinusoidal input waveform with 50 mVp-p at 200 kHz was applied. The experimental voltage gain is 0.905 (5.19% error), and the experimental leading phase shift is 57.2 degrees (2.83% error). The electronic controllability of the leading phase shift by varying the bias current is depicted in Figure 18. With these $I_B I_B$ values, the experimental leading phase shifts at $f = 100\,\text{kHz}$ were obtained as 145.40°, 119.81°, and 99.12°, respectively. The result

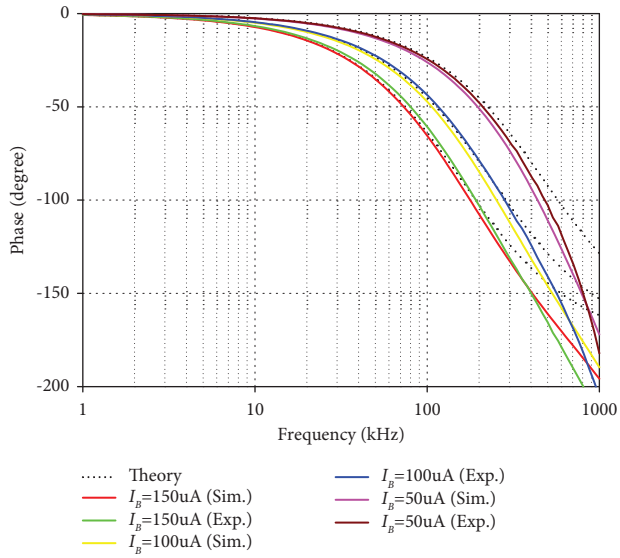


Figure 15: The lagging phase tuning by I_B.

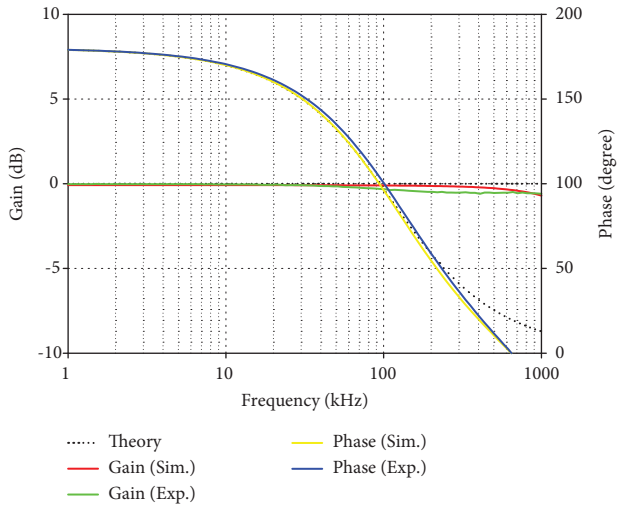


Figure 16: The gain and phase response of the leading phase shifter.

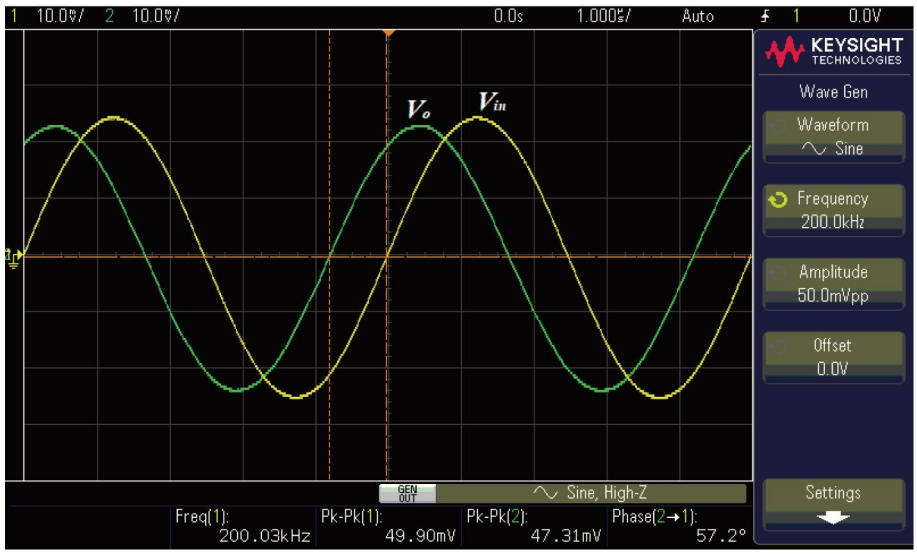


Figure 17: Measured input and output waveforms of the leading phase shifter.

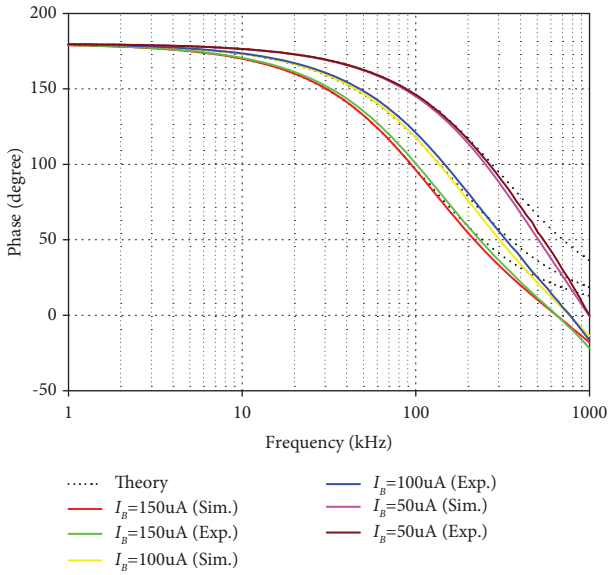


Figure 18: The leading phase tuning by I_B.

depicted in Figure 16 demonstrates the electronic adjustability of the lagging phase shift, as indicated in equation (16).

5. Conclusions

This paper proposes grounded and floating capacitance multipliers. The proposed circuits have a simple structure using a single VDDDA as an active element with one resistor and one capacitor. The floating one is slightly modified from the grounded one by using the Zc-VDDDA, which contains two Z terminals with an opposite-direction current. The multiplication factor of the proposed circuits is electronically adjusted via the bias current. The effect of nonideal VDDDA's properties included voltage and current tracking errors, and parasitic elements were also studied. These nonideal properties had an impact on the proposed circuits' operational frequency range and the accuracy of the capacitance multiplier factor. The parasitic resistances R_z, R_{zc}, and R_n influence the operation of the proposed capacitance multipliers at low frequencies, according to equations (11) and (12). In contrast, at high frequencies, they are affected by the parasitic inductance L_w. The validity of the proposed capacitance multipliers was verified through the PSpice simulation and experiment using VDDDA built up from the commercially available ICs. The multiplication factor can be electronically adjusted and ranges approximately between 0.56 and 13.94. The working frequency range reaches nearly three decades. With ±5 V power supplies, the measured power consumption of the grounded and floating capacitance multipliers is 225 mW and 293 mW, respectively. Additionally, the application examples, such as the lagging and leading phase shifters using the proposed circuits, and their experimental verification were designed and verified to confirm the workability of the proposed capacitance multipliers.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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