Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2011, Article ID 792759, 11 pages
doi:10.1155/2011/792759

Research Article

Modeling and Simulation of Special Shaped SOI Materials for the Nanodevices Implementation

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Received 30 December 2010; Accepted 4 May 2011

Academic Editor: Shaogang Hao

In the industrial chain of the nanomaterials for electronic devices, a main stage is represented by the wafer characterization. This paper is starting from a standard SOI wafer with 200 nm film thickness and is proposing two directions for the SOI materials miniaturization, indexing the static characteristics by simulation. The first SOI nanomaterial is a sub-10 nm Si-film with a rectangular shape. The influence of the buried interface fixed charges has to be approached by the distribution theory. The second proposal studies the influence of the vacuum cavity in a "U" shaped SOI nanofilm. In all cases, with rectangular or "U" shape film, the simulations reveal transfer characteristics with a maximum and output characteristics with a minimum for sub-10 nm thickness of the SOI film.

1. Introduction

The modeling of the classical devices [1] or novel nanodevices [2] improves the design and explains some phenomena experimentally encountered [3].

In the SOI structures, two oxide-semiconductor interfaces exist with specific associated charges. Conventional models ignore the charges situated at the buried oxide-substrate interface, being focused just on the front and back channels conduction in the silicon film. All these fixed charges, expressed in electrons per cm^2, are physically spread into a small volume that becomes significant in ultra-thin films. This paper presents a suitable model for the flat-band voltage, based on the δ-distribution strings, which include this bottom interface. Hence, the model accuracy increases in the SOI nanofilms materials, accordingly with our theory and numerical simulations. The electrons confinement effect is continuing to be studied in "U" shape SOI films. Whether the conduction channel occurs at the film bottom, the upper part of the SOI film was removed, monitoring the static characteristics of some SOI-MOSFETs.

This paper proposes two directions for the electrical characterization of the nano-SOI (silicon on insulator) materials, by simulation of the electrical characteristics of some devices. The first class of the studied SOI transistors has a rectangular film shape. In this case, the effect of the buried interface fixed charges is modeled with the distribution theory [4, 5].

The classical HTA SIMOX (high temperature annealing separation by implanted oxygen), technology offers SOI wafers with 200 nm Si-film on 400 nm BOX with fixed charges in the range $Q_{ox} = 10^{10} \div 10^{12}$ e/cm^2, [6]. This charge is located in a shallow oxide slice. An SOI device has the interfaces: I_1-Si-film/BOX, I_2-BOX/Substrate, and eventually the upper interface I_0-gate oxide/Si-film; see Figure 1. The classical model strongly insists on the electric charges from I_0 and I_1 interfaces, [7]. In fact, all these fixed charges are physically spread into a small volume. In ultra-thin oxide structures, this kind of charge must be modeled as a bulk charge density [8].

This paper emphasizes that the effect of a fixed charges about 10^{12} e/cm^2, at the bottom interface I_2 could be neglected in a classical SOI-MOSFET with 200 nm Si/400 nm BOX sizes, while it is the main charge in a nano-SOI-MOSFET with 10 nm × 10 nm × 10 nm Si/10 nm × 10 nm × 10 nm BOX.

Transforming 10^{12} e/cm^2 in 10^{-2} e/nm^2 = 1 electron per 10 nm × 10 nm that means that the back interface

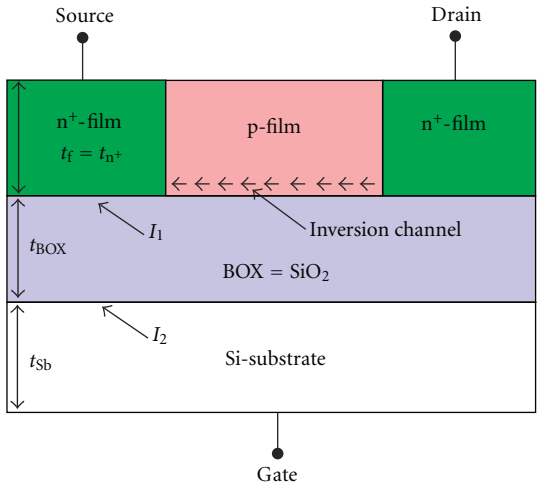

Figure 1: The current flow in a cross-section of a rectangular SOI-MOSFET, with SOI film thickness less than 200 nm.

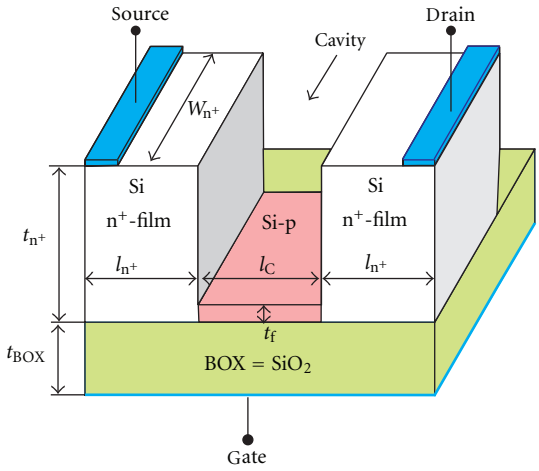

Figure 2: The conceptual architecture of the nanotransistor with a cavity, with SOI film thickness less than 10 nm.

I_2 (Si/BOX) is charged with one indivisible elementary charge. A model with a discontinuous function escapes from the integration operation. Just the Dirac distribution can correctly describe it as a bulk charge density.

Beside to the strong effect of the buried interface charge on the current through a SOI nanotransistor, the current confinement is modulated by the shape of the SOI material, in sub-10 nm Si-film devices, [9]. The influence of the vacuum cavity on the static characteristics, in a "U" shape nanotransistor, was the second direction of study for this paper; see Figure 2.

The notations from Figures 1 and 2 are t_{n+}: the Si-n$^+$ region thickness, t_f: the Si-p film thickness, t_{BOX}: the buried oxide (BOX) thickness, t_{Sb}: the Si-substrate thickness, l_{n+}: the Si-n$^+$ region length, l_C: the cavity length, and W_{n+}: the Si-n$^+$ region width.

The joint of both subjects will be finally motivated by similar output characteristics with minimum and transfer

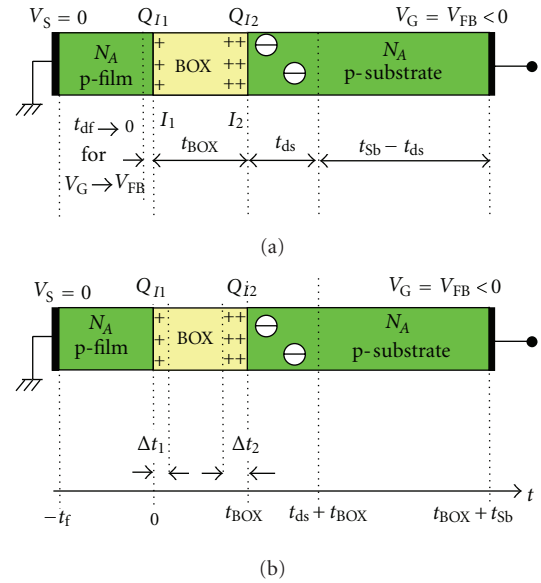

Figure 3: A segment of SOI structure with localization of interface charges (a) with Q_{I1}, Q_{I2} as sheet charge density and (b) with Q_{I1}, Q_{I2} scattered onto the $\Delta t_1, \Delta t_2$ thicknesses.

characteristics with maximum, both for rectangular shape sub-10 nm or "U" shaped SOI films.

2. The Analytical Model with Distributions

Firstly, the characterization of the back interface of a nano-SOI-MOSFET, using the pseudo-MOS transistor technique [10], will be presented. This is a dedicated transistor for the in situ electrical characterization, working like an upside down SOI-MOSFET controlled by the back gate, [11]. All unprocessed SOI wafers contain a pseudo-MOS transistor with two metals in contact with the semiconductor layer, as source and drain. The substrate acts like the gate contact in a classical SOI-MOSFET, Figure 1. One key parameter that contains information about the back interface charge is the flat band voltage, V_{FB}, [12]. This parameter is extracted from the measured I_D-V_{GS} curves or directly from simulations with its definition.

In order to be focused just on the fixed interface charge density, others effects like interface traps, mobile ionic charge and metal semiconductor work function are neglected in the analytical model and in simulations.

The SOI structure associated with the pseudo-MOS transistor is modeled. Identical doping concentrations in film and substrate, N_A, are considered to avoid the film-substrate work function in the flat-band voltage expression.

The source and drain are grounded, while the gate is biased at V_{FB} voltage, Figure 3(a). By Poisson's equation integration, the flat-band voltage V_{FBC} is computed by the classical method [13]

$$V_{FBC} = -\frac{Q_{I1}}{\varepsilon_{ox}} \cdot t_{BOX} - \frac{(Q_{I1} + Q_{I2})^2}{2\varepsilon_{Si} q N_A}, \quad (1)$$

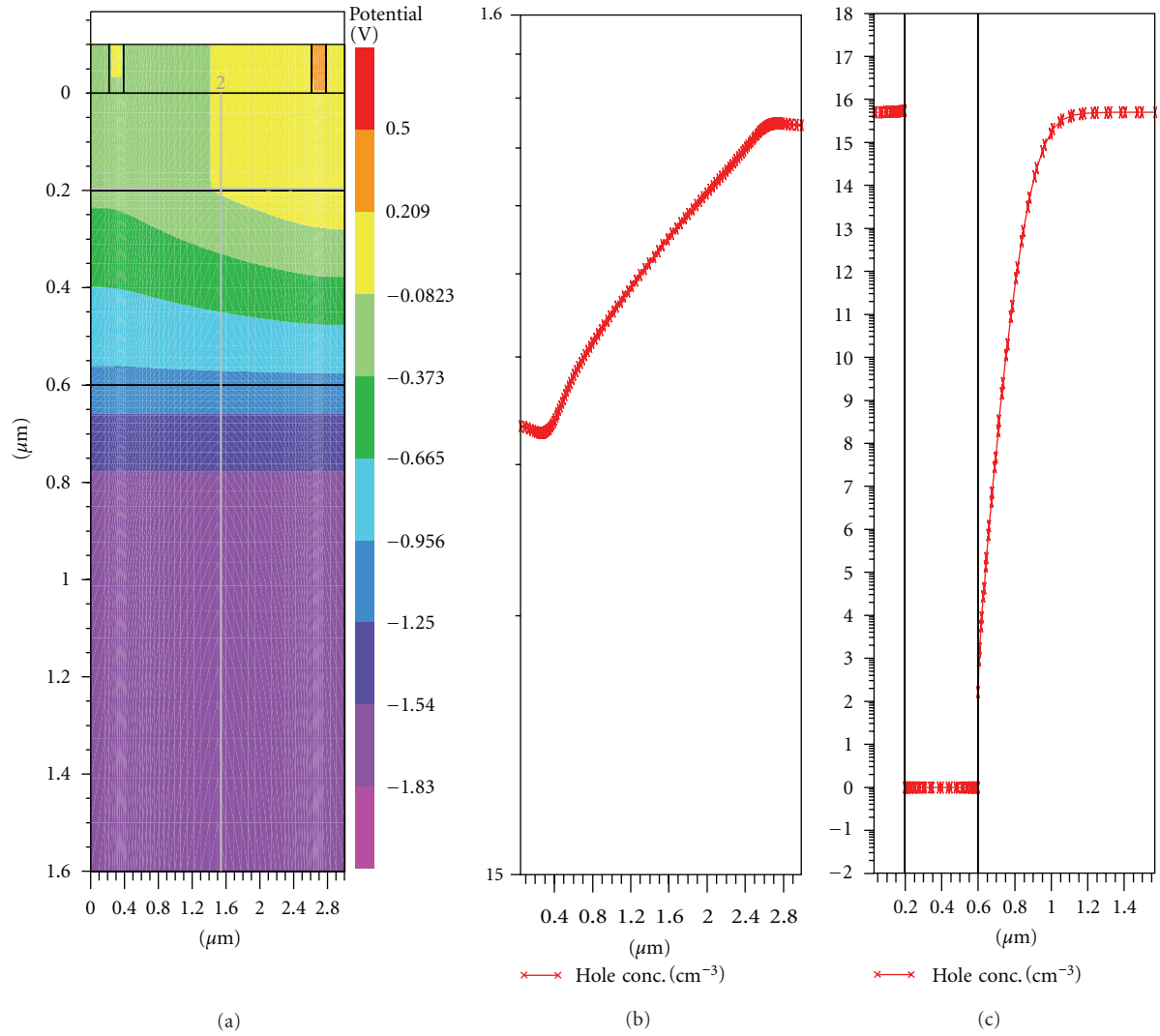

FIGURE 4: (a) The potential distribution in the 200 nm SOI structure; (b) the holes concentration across the structure; (c) the holes concentration along the structure.

where t_{BOX} is the buried oxide thickness, ε_{Si}, ε_{ox}, respectively, are the dielectric permittivity of silicon and oxide, V_{FBC} is the classical flat-band voltage given by the condition of the potential zeroing in the entire SOI film. The depleted film thickness $t_{df} \to 0$ for $V_G \to V_{FB}$, Q_{I1}, Q_{I2} are, respectively, the sheet charge densities from the upper and buried interface and the last term, $V_{FB\text{-}Sb}$ models the substrate depletion on distance t_{ds} in Figures 3(a) and 3(b) presents the interface charges scattered into smalls volumes, as a real situation, both in micro- or nano-SOI structures. Hence, a relationship between surface charge density Q_I and the bulk electric charge density q_V for whatever I_1 or I_2 interface is

$$Q_I = \lim_{\Delta t \to 0} \int_0^{\Delta t} q_V \cdot dt = \lim_{\Delta t \to 0} q_V \cdot \Delta t, \tag{2}$$

where Δt is interpreted as a spreading coefficient. The surface charge Q_I was spread into an infinitesimal volume: $\Delta t \cdot S$, with $\Delta t \to 0$ and $q_V = \text{ct}$, S being the area. If q_V is modeled with a function like this

$$q_V = \begin{cases} q_S, \text{expressed in e/cm}^3, & \text{for } t = 0, \\ 0, & \text{for } t \in \Re - \{0\}, \end{cases} \tag{3}$$

where q_S is a real number associated with $Q_I/\Delta t$. Then, Q_I becomes zero, accordingly with (2), escaping from the integration operation. In order to obtain Q_I finite in (2), q_V must tend to ∞, considering $\Delta t \to 0$. But this is a δ distribution. On the horizontal axis Ot, along the SOI structure from Figure 2(a), the bulk charge density can be written with the Dirac distribution

$$q_V(t) = Q_{I1} \cdot \delta_0(t) + Q_{I2} \cdot \delta_{t_{BOX}}(t). \tag{4}$$

The electric field distribution is expressed as a Heaviside distribution after the first integration. The potential imposes a second integration that is difficult in distribution terms.

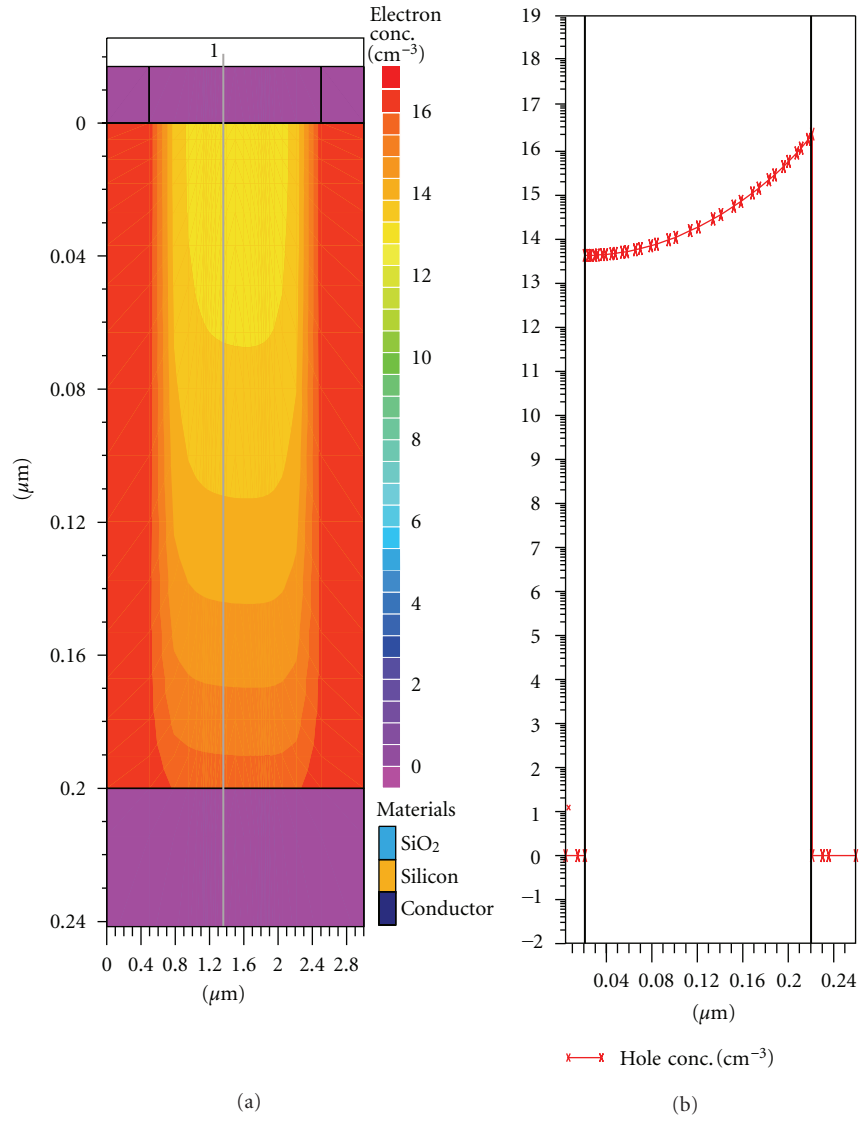

FIGURE 5: Detail in film for the electron concentration rised for a positive gate voltage.

Due to this reason, is preferred a model based on δ-generator strings. The functional analysis demonstrated that Dirac distribution is the limit of the following string of regulates distribution, pulse-type [14]

$$D_{t_i}(t) = \begin{cases} \dfrac{1}{\Delta t_i}, & \text{for } t \in [t_i, t_i + \Delta t_i], \\ 0, & \text{for } t \notin [t_i, t_i + \Delta t_i], \end{cases} \tag{5}$$

where t_i is the spatial coordinate for Q_{Ii}, $i = 1$ or 2 and $\Delta ti \longrightarrow 0$ $(\forall i)$ represent the spreading coefficients for Q_{I1}, Q_{I2}; see Figure 2(b). Now, the bulk electric charge distribution can be written with δ-generators string

$$q_V(t) = Q_{\text{I1}} \cdot D_0(t) + Q_{\text{I2}} \cdot D_{t_{\text{BOX}}}(t). \tag{6}$$

The string $D_{ti}(t)$ has the advantage of being an integrable function. The integral $\int_{-\infty}^{\infty} D_{ti}(t)dt$ gives 1 like δ distribution. The convergence toward δ-distribution is successfully fulfilled for $\Delta t_i \to 0$. In the old SOI technologies, $\Delta t_i = 20\,\text{nm} = 2 \cdot 10^{-8}$ m [15], but in the ultimate stage of nanotechnologies, Δt_i could reach the atomic sizes— $\Delta t_i \approx 0.3\,\text{nm} = 3 \cdot 10^{-10}$ m, closer to zero, [16]. Hence, our model is more accurate for nanodevices. After two integration operations of the Poisson's equation, the following potential drops result:

$$\begin{aligned} &\text{For } t \in (-t_f, 0) \longrightarrow \Phi_{\text{film}} = 0, \\ &\text{For } t \in (0, \Delta t_1) \longrightarrow \Phi_{\Delta t_1} = -\frac{Q_{I1}}{2\varepsilon_{\text{ox}}} \cdot \Delta t_1, \\ &\text{For } t \in (\Delta t_1, t_{\text{BOX}} - \Delta t_2) \\ &\qquad \longrightarrow \Phi_{\text{BOX}} = -\frac{Q_{I1}}{\varepsilon_{\text{ox}}} \cdot (t_{\text{BOX}} - \Delta t_1 - \Delta t_2), \\ &\text{For } t \in (t_{\text{BOX}} - \Delta t_2, t_{\text{BOX}}) \\ &\qquad \longrightarrow \Phi_{\Delta t_2} = -\frac{Q_{I1}}{\varepsilon_{\text{ox}}} \cdot \Delta t_2 - \frac{Q_{I2}}{2\varepsilon_{\text{ox}}} \cdot \Delta t_2. \end{aligned} \tag{7}$$

Adding the previous voltages, Φ_{film}, Φ_{BOX}, $\Phi_{\Delta t1}$, $\Phi_{\Delta t2}$—the potentials drops, respectively, over film, neutral oxide, and Δt_1 and Δt_2 regions from the buried oxide, with the potential drop over the depleted substrate, $V_{\text{FB-Sb}}$, the complete flat-band voltage expression with distribution terms, V_{FBC}, is

$$V_{\text{FBD}} = -\frac{Q_{I1}}{\varepsilon_{\text{ox}}} \cdot \left(t_{\text{BOX}} - \frac{\Delta t_1}{2}\right) - \frac{Q_{I2}}{2\varepsilon_{\text{ox}}} \cdot \Delta t_2 - \frac{(Q_{I1} + Q_{I2})^2}{2\varepsilon_{\text{Si}} \cdot qN_A}. \quad (8)$$

If the spreading coefficients are approximated with zero ($\Delta t_{1,2} = 0$), the new model (8) becomes the conventional model (1). The validity of the new model (8) will be discussed in the next paragraph, in comparison with classical model (1).

3. The Simulation Results for the SOI Structure with 200 nm Thickness

In this paragraph, the previous models (1) and (8) are tested using Atlas simulations of a pseudo-MOS transistor integrated on a SOI wafer with 200 nm Si-p-film and 400 nm buried oxide. The constructive data were [17]: $t_{n+} = 0.2\,\mu$m, $t_{\text{BOX}} = 0.4\,\mu$m, $t_{\text{Sb}} = 1\,\mu$m, the doping concentrations in film and substrate is $N_A = 2 \times 10^{15}\,\text{cm}^{-3}$.

The applied voltages were $V_D = 0\,\text{V} \cdots + 4\,\text{V}$, $V_S = 0\,\text{V}$ and $V_G = 0\,\text{V} \cdots -3\,\text{V}$ in order to estimate the simulated flat-band voltage that must be applied on gate.

Figure 4(a) presents the potential distribution and the holes concentration in an intermediate situation at $V_G = -1.8\,\text{V}$, through the structure with 200 nm Si-film thickness. A negative gate bias induces a holes crowding in the p-type film. Near drain, where V_{GD} is higher than V_{GS}, the holes reached $p = 8 \times 10^{15}\,\text{cm}^{-3}$ and near source $p = 4 \times 10^{15}\,\text{cm}^{-3} > 2 \times 10^{15}\,\text{cm}^{-3} = N_A$, Figure 4(b). From the longitudinal holes distribution can be observed the holes concentration decreasing in the substrate; see Figure 4(c). This simulation proves the substrate depletion effect.

Figure 5 presents the electron concentration in the same structure with 200 nm film thickness. A positive gate bias induces an electron inversion channel in p-type film (e.g., $n|_{y=0.2\mu\text{m}} = 10^{16}\,\text{cm}^{-3} > 5 \cdot 10^{15}\,\text{cm}^{-3} = N_{A\text{-film}}$); see Figure 5.

Atlas takes into account the interface electric charge by the statements

$$\begin{aligned} &\text{Interface } y_{\min} = 0.1 \quad y_{\max} = 0.5, \quad \text{QF} = 5e10, \\ &\text{Interface } y_{\min} = 0.5 \quad y_{\max} = 0.8, \quad \text{QF} = 1e12. \end{aligned} \quad (9)$$

The metal semiconductor work function was zero for the source, drain, and gate contacts, defined as "neutral". The simulated flat-band voltage value, V_{FBS} was searched accordingly with the theoretical definition. For $V_S = 0\,\text{V}$, the V_G voltage was searched so that the potential in the film bottom becomes zero.

Figure 6 presents the potential distribution between source and gate, after Atlas running. Initially, the potential distribution was extracted for $V_{GS} = 0\,\text{V}$ in order to observe the potential bending in the absence of some external electrical voltages due to the interface charges densities Q_{I1} and Q_{I2}. In this case, the potential at the film bottom reaches +0.28 V at $x = 0.2\,\mu$m; see Figure 6. Then, the gate voltage was increased so that the potential at the coordinate $x = 0.2\,\mu$m decreases to 0 V. This occurs for $V_{GS} = -1.95\,\text{V}$ in Figure 6 consequently; $V_{\text{FBS}} = -1.95\,\text{V}$.

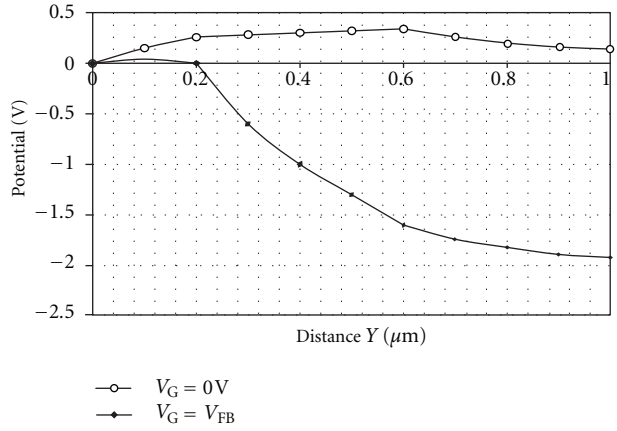

Figure 6: The potential distribution in the 200 nm structure between source and gate.

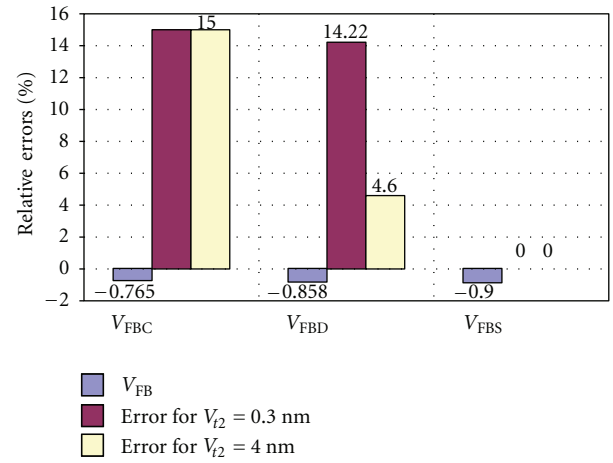

Figure 7: The flat-band voltages: $V_{\text{FBS}} = -1.95\,\text{V}$, $V_{\text{FBC}} = -1.77\,\text{V}$, and $V_{\text{FBD}} = -1.93\,\text{V}$, besides to the relative errors for V_{FBC}, V_{FBD} in respect with V_{FBS}.

On the other hand, the classical model (1) provides a fix value $V_{\text{FBC}} = -1.77\,\text{V}$ and the new model (8) based on the distribution generation strings gives $V_{\text{FBD}} = -1.93\,\text{V}$, fitting the spreading coefficients to $\Delta t_1 = 0.5\,\text{nm}$ and $\Delta t_2 = 7\,\text{nm}$.

All these results are briefly shown in Figure 7, where the old model (1) gives 9.3% error, while the new model (8) can adjust the error to 1.03%.

A comparison of the simulated parameter V_{FBS} with a measured flat-band voltage, V_{FBM}, is possible, monitoring the transfer characteristics of the pseudo-MOS transistor made on the SOI wafer with 200 nm Si-p-film and 400 nm buried oxide, [17]. In order to extract the flat-band voltage,

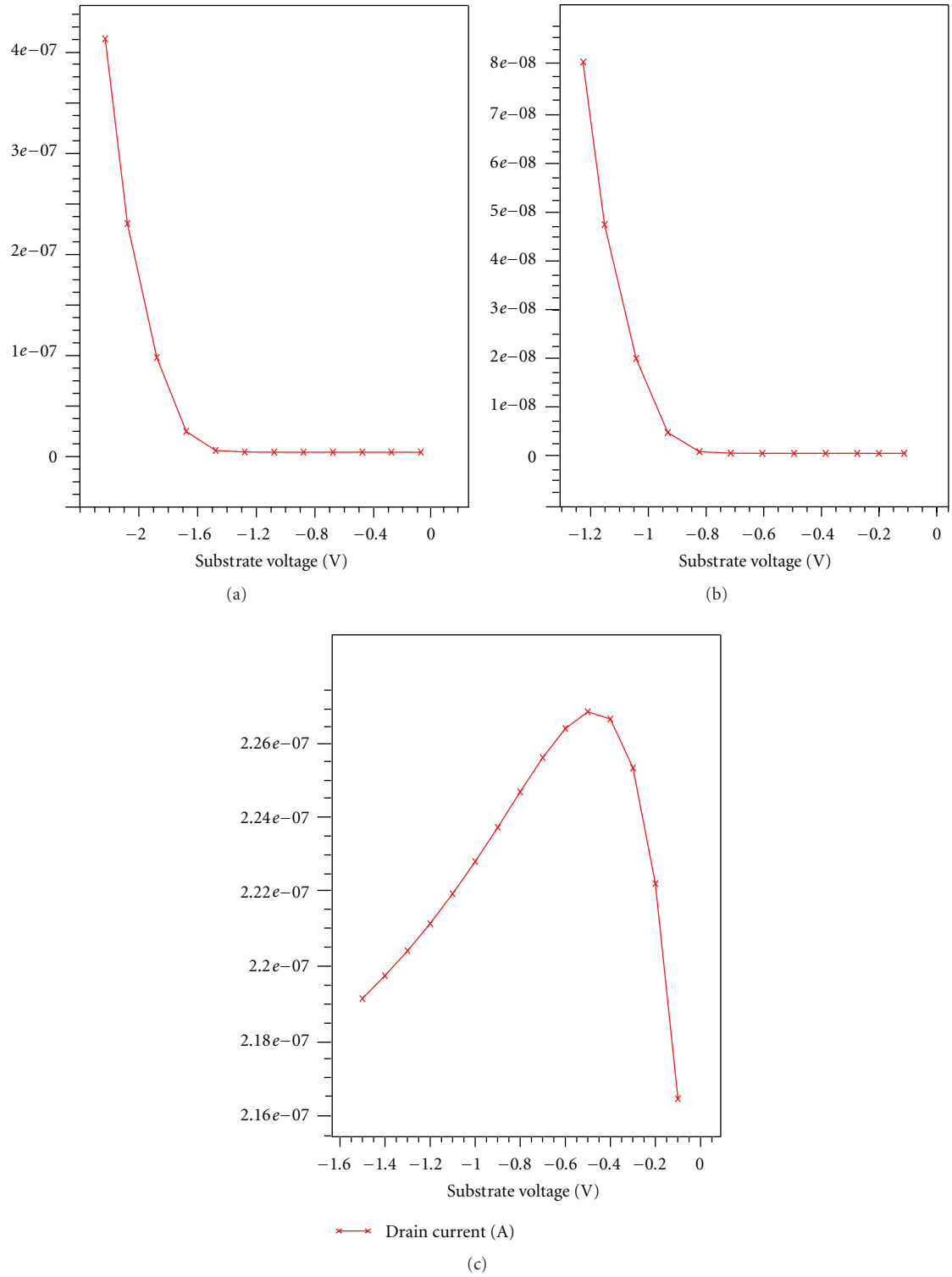

FIGURE 8: The I_D-V_{GS} characteristics for (a) 50 nm (b) 10 nm and (c) 2 nm thickness of the semiconductor SOI film.

the source was grounded, while the drain was maintained at +0.3 V, and the gate voltage was varied from −5 V up to +5 V in order to induce the flat-band conditions in the device. From the transfer characteristics, the measured flat-band voltage results: $V_{FBM} = -2.16$ V for p-type film and +4.25 V for n-type film, [17, 18]. In our case, the closest values to the experimental parameter, $V_{FBM} = -2.16$ V, are the simulated and distribution model: $V_{FBS} = -1.95$ V and $V_{FBD} = -1.93$ V. Obviously, the classical model (1), $V_{FBC} = -1.77$ V, loses the accuracy, neglecting the buried oxide interface. However, the

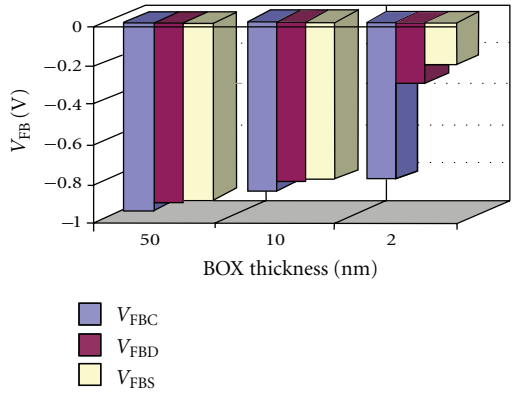

FIGURE 9: The flat-band voltages: V_{FBS}, V_{FBC}, and V_{FBD}, besides to the relative errors for V_{FBC}, V_{FBD} in respect to V_{FBS}, for t_f = 50, 10, and 2 nm.

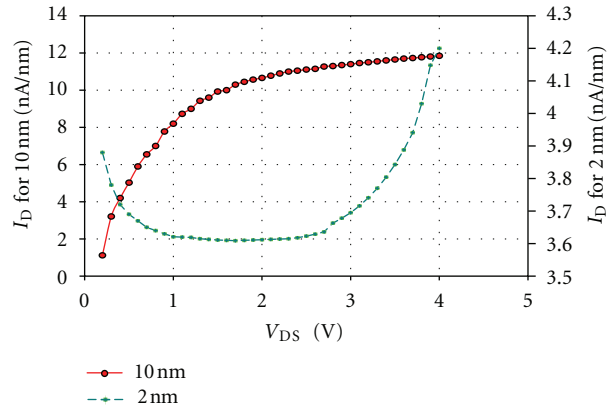

FIGURE 10: The I_D-V_{DS} characteristics at V_{GS} = 3 V and rectangular shape of the SOI film with 10 nm and 2 nm thickness.

discrepancy among experiments, simulations, and analytical values is still small at 200 nm film thickness and is predictable to becomes consistent for sub-20 nm films.

4. Simulation Results for Sub-10 nm Rectangular SOI Structures with Interface Charges

The investigation of the nano-SOI-MOSFETs is continuing with the downscale of the film thicknesses: for Si-film from 200 nm to 50 nm, 10 nm, and 2 nm and for BOX layer from 400 nm to 50 nm, 10 nm, and 4 nm. The doping concentrations are $N_A = 5 \times 10^{15}\,\text{cm}^{-3}$ both in film and substrate. The interface electric charge densities are $Q_{I1} = 5 \times 10^{15}\,\text{e/cm}^2$ and $Q_{I2} = 10^{12}\,\text{e/cm}^2$.

The simulated transfer characteristics show the evolution of the I_D-V_{GS} curves from: (a) 50 nm, (b) 10 nm, (c) 2 nm thickness of the semiconductor SOI film; see Figure 8. The typical characteristic shape of a standard SOI-MOSFET is fulfilled till 10 nm. From these curves, the simulated flat-band voltage can be extracted, as the voltage that opens the accumulation channel and produces the current increases: $V_{FBS} = -0.9\,\text{V}$ for 50 nm structure and $V_{FBS} = -0.8\,\text{V}$ for 10 nm structure. Under this value, an I_D-V_{GS} curve with a maximum occurs, probably due to the electrons confinement effect. The simulated flat-band voltage cannot be still extracted from the I_D-V_{GS} curve.

In order to check these assessments, the output characteristics are also investigated, to observe the typical effect of transistor. Figure 8 comparatively presents the I_D-V_{DS} curves for different semiconductor SOI thickness: 10 nm and 2 nm. The typical shape with saturation occurs till 10 nm film thickness. For sub-10 nm the characteristics takes atypical shape with minimum, Figure 8 for t_f = 2 nm.

A comparison among the simulated, classical, and distribution flat-band voltage for t_f = 50 nm, 10 nm, and 2 nm is available in Figure 9, besides to the error versus the V_{FBS}. This analysis proofs that the model (8) with distributions is closer to the simulations than the classical model (1), which provides higher errors at lower thicknesses.

Figure 10 comparatively presents the output characteristics when the drain-source voltage was increased from 0 V up to +5 V, at a constant V_{GS}, for two nanosizes of the SOI film.

Besides to the model with distribution accuracy, the prior simulations of the statics characteristics highlights classical shape of characteristics for $t_f > 10$ nm and atypical shape for $t_f < 10$ nm.

Another direction of the SOI nanotransistors investigation is related to a special shape of the SOI film. Taking into account that the current occurs only at the Si-film bottom, results that the 90% from the upper Si-film region does not participate to conduction. Hence, this Si-film region was removed in next simulations, obtaining a SOI nanotransistor with a cavity or "U" shaped.

5. Simulation Results for Sub-10 nm Special Shaped SOI Nanotransistor without Interface Charges

In the simulations, the constructive data were those described in the paragraph 4. The aim of this paragraph is to highlight only the special shape effect of the semiconductor on the static characteristics.

The main physical effects included as "nanoeffects" were band to band tunnelling, Fowler-Nordheim tunnelling, Fermi distribution, including in the MODEL statement the following parameters: BBT, FNORD, and FERMI. Figure 11 presents the total current vectors in a structure with $t_{n+} = 7$ nm, $t_f = 1$ nm, and $t_{BOX} = 10$ nm, at $V_{DS} = 4$ V, $V_{GS} = 3$ V, besides to the electrons concentration in the channel region. The vectors through the vacuum (emphasised by dotted line), proved the tunnel effect.

In Figure 12 family of curves I_D-V_{GS} for $y_{film} = 200$ nm, 10 nm, 1 nm, and 0.3 nm are presented. These curves have a maximum for $y_{film} \leq 1$ nm, like SET transistor [19] or atypical nanodevices [20].

Figure 13 shows the curves I_D-V_{DS} at $V_{GS} = 3$ V. The shape of the I_D-V_{DS} curves with a minimum proves the tunnel effect, [21].

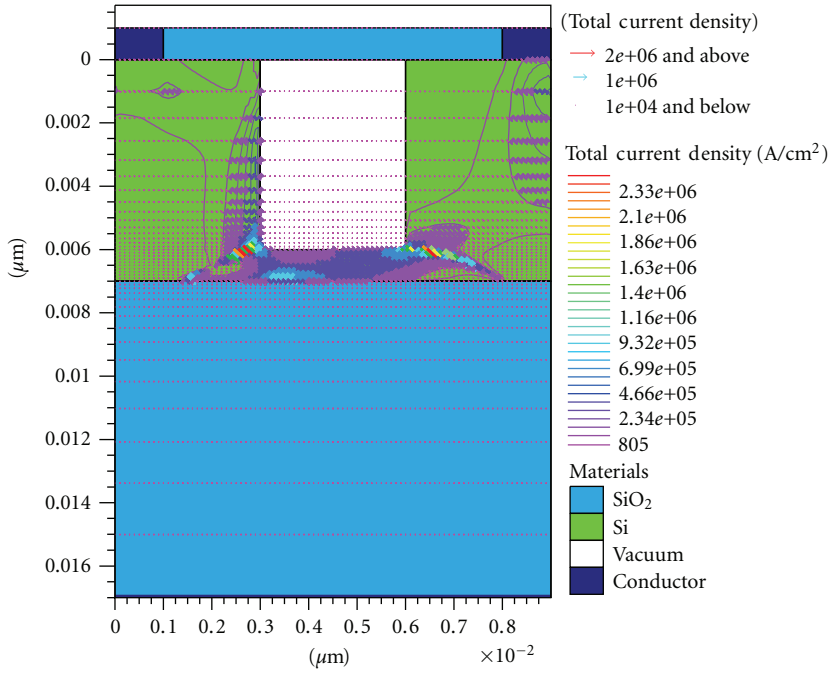

Figure 11: Total current vectors in the 1 nm transistor.

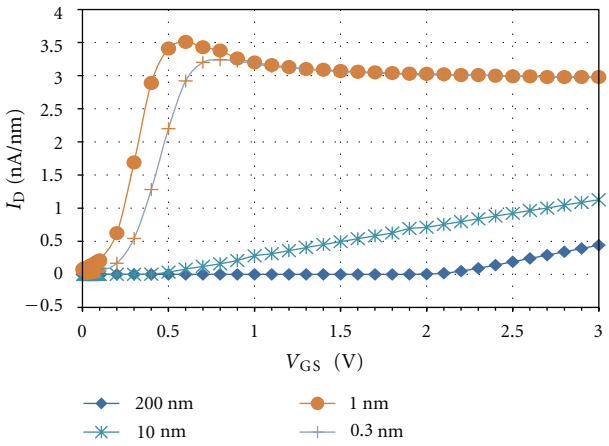

Figure 12: The I_D-V_{GS} transfer characteristics.

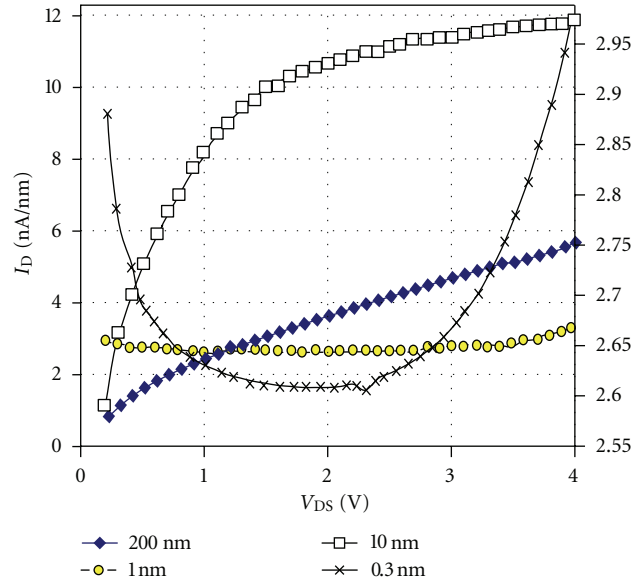

Figure 13: The I_D-V_{DS} output characteristics.

Figure 14 presents the global potential distribution (left) and a detail of the electron concentration (right) for the 0.3 nm structure with cavity, biased at a high drain voltage in this last case: $V_S = 0$ V, $V_G = 3$ V, and $V_D = 4$ V.

In this case, the saturation occurred, and an unbalanced electron distribution can be seen in the film $1.1 \cdot 10^{16}$ cm^{-3} in the source region, $7 \cdot 10^{15}$ cm^{-3} in the channel near the source, $2 \cdot 10^{15}$ cm^{-3} in the channel near the drain, and decrease up to $1.4 \cdot 10^{15}$ cm^{-3} in the drain, region at the film bottom; see Figure 14.

6. Possible Set Implementation

The single electron devices (SEDs) tend to become the main rivals for the sub-50 nm classical CMOS devices [22]. Advantages of SED's are low-power dissipation, ultra-high-density of integration, a natural technology evolution inspired from miniaturized CMOS processes, and hence reasonable costs.

The simulations suggest the SET (single electron transistor) like behavior of the SOI nanotransistor with cavity for sub 1 nm film thickness. The electrons must be transferred from source to drain one by one [23].

As in the case of SOI-MOSFETs, a positive gate bias induces an electron inversion channel in the p-type film.

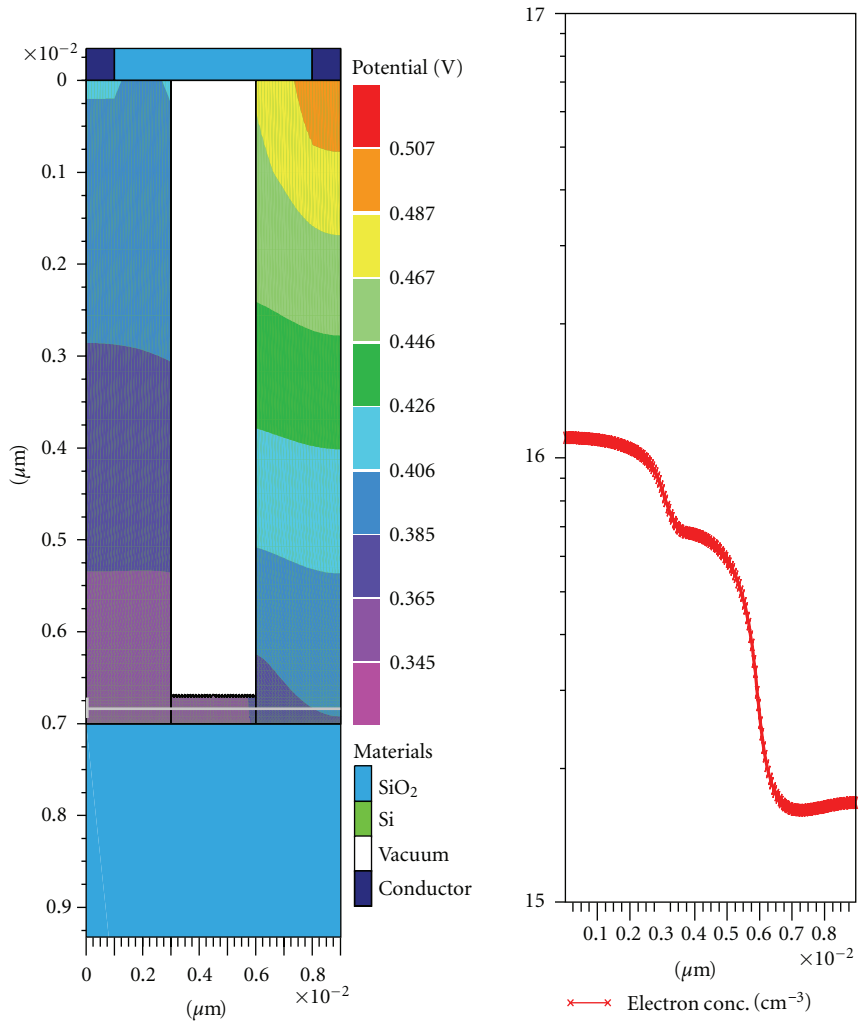

FIGURE 14: The potential and the electron concentration in the 0.3 nm structure.

The DC analysis used the following voltages: $V_G = 3\,V$, $V_D = 0.1\,V$, $V_S = 0\,V$. The nanoeffects were simulated taking into account the Fowler-Nordheim tunneling and the Fermi distribution, using in the MODEL statement the following parameters: FNORD, FERMI: models conmob srh auger fermi fldmob fnord print, meaning: constant mobility, Shockley-Read-Hall and Auger recombination model and mobility attenuation with lateral field. For electron concentration study in the inversion channel, the drain voltage was maintained at 0.1V and the gate voltage was increased from 0 V to +3 V with a 0.05 V step. Despite of the very thin p film, a high electron concentration occurs in the channel at $V_{GS} = +3\,V$, as is shown in Figure 15. With V_{DS} increasing, the current arise as a superposition, when the source-drain vacuum is tunneled.

However, the device is in strong inversion at this gate voltage, because $n_{channel} = 2 \times 10^{20}\,cm^{-3} > 5 \times 10^{15}\,cm^{-3} = N_{A-film}$. The electron concentration in the 0.3 nm p-type SOI film is: $n_{channel} = 2 \times 10^{20}\,cm^{-3} = 0.2\,nm^{-3} \approx 1$ electron per channel volume, V, Figure 16. The channel volume is $V = 0.3\,nm \times 3\,nm \times 6\,nm = 5.4\,nm^3$. Then, the electrons transport, from source to drain, is one by one. Therefore, the SET principle is satisfied.

7. Conclusions

This paper presented a nanotransistor with silicon on insulator structure in different situations. When the film thickness varied between 200 nm to 10 nm the electrical characteristics preserve the classical shape. When the film thickness varied from 1 nm to 0.3 nm and a cavity occurs above the film, the device presents atypical electrical characteristics I_D-V_{GS}, having a maximum like the SET transistor. The shape of the I_D-V_{DS} curves with a minimum proves the presence of the tunnel effect. The electron transport in the p-film is one by one, proving the Single Electron Technology for our proposed SOI nanotransistor.

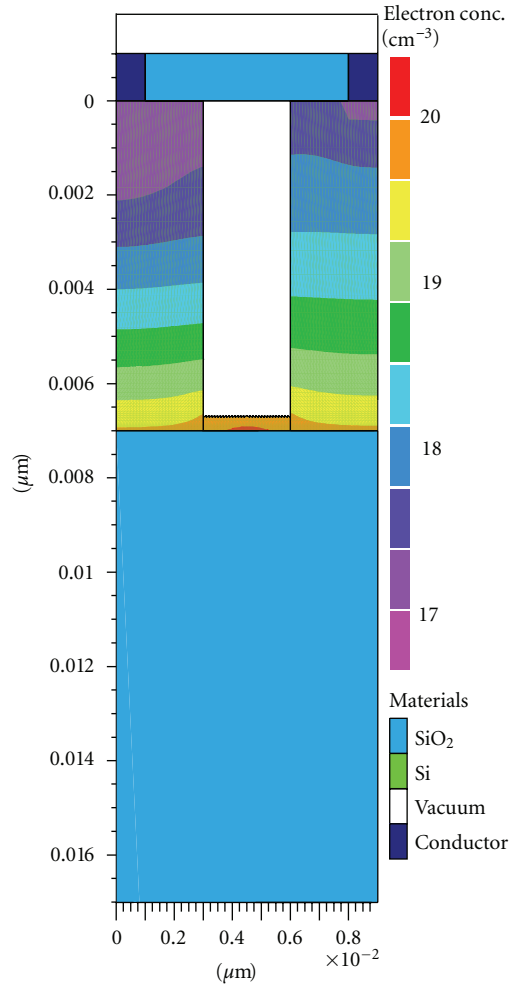

Figure 15: The electron concentrations in 0.3 nm SET: global.

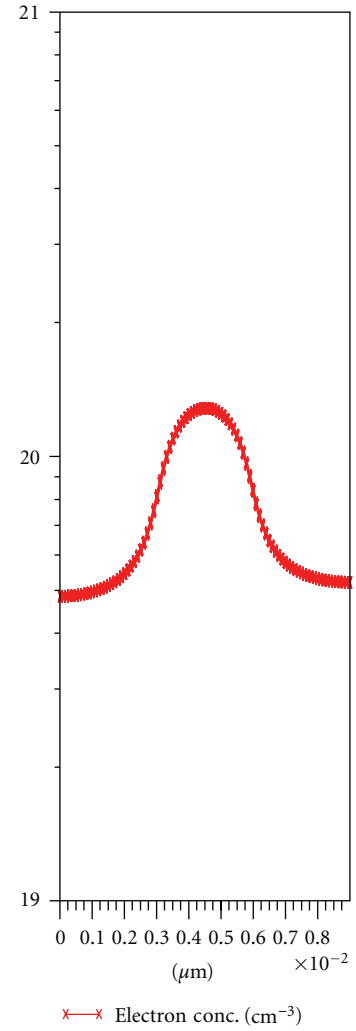

Figure 16: The electron concentrations in the 1 nm transistor-a detail in a cross-section.

Also, the new model with distribution presented in this paper, improves the flat-band voltage modeling of the SOI nanostructures, introducing new fitting parameters: $\Delta t_{1,2}$—the spreading coefficients. However, neither the presence or absence of the interface charge $Q_{I1,2}$ is defining for the atypical shape of the transfer characteristics, because the curves with maximum arose both in rectangular SOI film with Q_{I2} both in "U" shape SOI film without Q_{I2}; the only conditions was to exist a ultra-thin SOI film under 2 nm.

The simulations revealed that the SOI nanotransistor with a thinner film in the channel body represents a solution for the SET's implementation, with possible applications in industry like digital ULSI, invertors with SET, memories with SEM-single electron memory, and communications cells [24].

These simulations and the model with the distribution represent an important chapter in the devices design—a key stage during the industrial manufacturing.

Acknowledgment

The work has been cofunded by the Sectorial Operational Program Human Resources Development of the Romanian Ministry of Labor, Family, and Social Protection through the Financial Agreement nos. POSDRU/89/1.5/S/62557 and PNII-62063-12095.

References

[1] H. Murray, P. Martin, and S. Bardy, "Taylor expansion of surface potential in MOSFET: application to Pao-Sah integral," *Active and Passive Electronic Components*, vol. 2010, Article ID 268431, 11 pages, 2010.

[2] S. A. Mahmoud, S. M. Al-Shomar, and A. A. Akl, "Electrical characteristics and nanocrystalline formation of sprayed iridium oxide thin films," *Advances in Condensed Matter Physics*, vol. 2010, Article ID 518209, 6 pages, 2010.

[3] J. Pretet, S. Monfray, S. Cristoloveanu, and T. Skotnicki, "Silicon-on-nothing MOSFETs: performance,short-channel

effects, and backgate coupling," *IEEE Transactions on Electron Devices*, vol. 51, no. 2, pp. 240–245, 2004.

[4] D. N. Vizireanu, "Quantized sine signals estimation algorithm for portable DSP based instrumentation," *International Journal of Electronics, Taylor & Francis*, vol. 96, no. 11, pp. 1175–1181, 2009.

[5] N. Quijano and K. M. Passino, "The ideal free distribution: theory and engineering application," *IEEE Transactions on Systems, Man and Cybernetics, Part B*, vol. 37, no. 1, pp. 154–165, 2007.

[6] A. A. J. Al-Douri, M. F. A. Alias, A. A. Alnajjar, and M. N. Makadsi, "Electrical and optical properties of Ge_xSi_{1-x}:H thin films prepared by thermal evaporation method," *Advances in Condensed Matter Physics*, vol. 2010, Article ID 428739, 8 pages, 2010.

[7] J. Benson, N. V. D'Halleweyn, W. Redman-White et al., "A physically based relation between extracted threshold voltage and surface potential flat-band voltage for MOSFET compact modeling," *IEEE Transactions on Electron Devices*, vol. 48, no. 5, pp. 1019–1021, 2001.

[8] C. Ravariu, A. Rusu, F. Babarada, and F. Ravariu, "Discrepancies of the flat-band voltage models revealed by simulations in sub-50 nm SOI films," in *Proceedings of the 15th IASTED International Conference on Applied Simulation and Modelling (ASM '06)*, pp. 141–144, Rhodes, Greece, June 2006.

[9] C. Ravariu, A. Rusu, M. D. Profirescu, and F. Ravariu, "A nano-transistor with a cavity," in *Proceedings of the 8th IEEE International Conference on Nanotechnology*, vol. 1, chapter 4, pp. 111–114, Anaheim, Calif, USA, 2005.

[10] S. Sato, K. Komiya, N. Bresson, Y. Omura, and S. Cristoloveanu, "Possible influence of the Schottky contacts on the characteristics of ultrathin SOI pseudo-MOS transistors," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, p. 1807, 2005.

[11] C. Ravariu, A. Rusu, F. Ravariu, D. Dobrescu, and L. Dobrescu, "Alternative methods of parameters extraction based on the pseudo-MOS technique," in *Proceedings of the 24th IEEE International Conference on Microelectronics (MIEL '04)*, pp. 249–252, Nis, Serbia, 2004.

[12] C. Ravariu, A. Rusu, F. Udrea, and F. Ravariu, "Simulation results of some diamond on insulator nano-MISFETs," *Diamond and Related Materials*, vol. 15, no. 2, pp. 777–782, 2006.

[13] C. Ravariu, F. Babarada, A. Rusu, and F. Ravariu, "More accurate models of the interfaces oxide ultra-thin SOI films," *AIP Conference Proceedings*, vol. 893, pp. 3–4, 2007, ISI electronic Journal, under the American Institute of Physics AIP auspices.

[14] O. Stanasila, *Special Mathematics*, ALL Publishing, Bucharest, Romania, 2001.

[15] G. A. Brown, H. H. Hosack, K. Joyner, and W. A. Krull, "Integrity of gate oxides formed on SIMOX wafers," in *Proceedings of the IEEE International SOI Conference*, p. 73, October 1994.

[16] "CEA-Leti makes a R&D 20 nm fully depleted SOI process," *EUROSOI Newsletter*, vol. XXVI, October 2010.

[17] C. Ravariu, A. Rusu, and F. Ravariu, "Parameters extraction from some experimental static characteristics of a pseudo-MOS transistor," *Scientific Bulletin Journal Series C*, vol. 70, no. 1, pp. 29–34, 2008.

[18] D. N. Vizireanu, "A simple and precise real-time four point single sinusoid signals instantaneous frequency estimation method for portable DSP based instrumentation," *Measurement*, vol. 44, no. 2, pp. 500–502, 2011.

[19] S. Mahapatra, A. M. Ionescu, and B. Banerjee, "A quasi-analytical SET model for few electron circuit simulation," *IEEE Electron Device Letters*, vol. 23, no. 6, pp. 366–368, 2002.

[20] S. M. Rezaul Hasan, "Transition frequencies and negative resistance of inductively terminated CMOS buffer cell and application in MMW LC VCO," *Active and Passive Electronic Components*, vol. 2010, Article ID 542406, 11 pages, 2010.

[21] C. Ravariu, A. Rusu, A. Bondarciuc et al., "Modeling and simulation of a nanostructure for a single electron technology implementation," in *Proceedings of the 5th International Mediterranean Modelling Multiconference*, pp. 312–315, Briatico, Italy, September 2008.

[22] C. J. Singh, K. C. Kumar, S. Gope, J. Basu, S. Sarkar, and S. Kumar, "Single electron device based automatic tea vending machine," in *Proceedings of the IET-UK International Conference on Information and Communication Technology in Electrical Sciences (ICTES '07)*, pp. 891–896, Chennai, Tamilnadu, India, December 2007.

[23] H. Inokawa, Y. Takahashi, K. Degawa, T. Aoki, and T. Higuchi, "A single-electron-transistor logic gate family and its application—part II: design and simulation of a 7-3 parallel counter with linear summation and multiple-valued latch functions," in *Proceedings of the 34th International Symposium on Multiple-Values Logic (ISMVL '04)*, pp. 269–274, 2004.

[24] R. M. Udrea and D. N. Vizireanu, "Quantized multiple sinusoids signal estimation algorithm," *Journal of Instrumentation*, vol. 3, article P02008, pp. 1–7, 2008.