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Research Article

Temperature-Dependent Physical and Memory Characteristics of Atomic-Layer-Deposited RuO_x Metal Nanocrystal Capacitors

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Physical and memory characteristics of the atomic-layer-deposited RuO_x metal nanocrystal capacitors in an n-Si/SiO_2/HfO_2/RuO_x/Al_2O_3/Pt structure with different postdeposition annealing temperatures from 850–1000°C have been investigated. The RuO_x metal nanocrystals with an average diameter of 7 nm and a highdensity of $0.7 \times 10^{12}/cm^2$ are observed by high-resolution transmission electron microscopy after a postdeposition annealing temperature at 1000°C. The density of RuO_x nanocrystal is decreased (slightly) by increasing the annealing temperatures, due to agglomeration of multiple nanocrystals. The RuO_3 nanocrystals and Hf-silicate layer at the SiO_2/HfO_2 interface are confirmed by X-ray photoelectron spectroscopy. For post-deposition annealing temperature of 1000°C, the memory capacitors with a small equivalent oxide thickness of ~9 nm possess a large hysteresis memory window of >5 V at a small sweeping gate voltage of ±5 V. A promising memory window under a small sweeping gate voltage of ~3 V is also observed due to charge trapping in the RuO_x metal nanocrystals. The program/erase mechanism is modified Fowler-Nordheim (F-N) tunneling of the electrons and holes from Si substrate. The electrons and holes are trapped in the RuO_x nanocrystals. Excellent program/erase endurance of 10^6 cycles and a large memory window of 4.3 V with a small charge loss of ~23% at 85°C are observed after 10 years of data retention time, due to the deep-level traps in the RuO_x nanocrystals. The memory structure is very promising for future nanoscale nonvolatile memory applications.

1. Introduction

Memory devices with a low program/erase voltage operation and a better scalability with excellent endurance/retention are required for future nanoscale high-performance flash memory applications. According to the International Technology Roadmap for Semiconductors (ITRS) on a 20 nm technology node [1], the scaling of tunneling oxide thickness is one of the key issues for conventional floating gate memory devices. Recently, many nanocrystals with the advantages of many energy levels as well as high charge-trapping probability, high-speed with a low program/erase voltage operation, high scalability potential, excellent endurance, and data retention, and so forth, have been reported [2–10]. Due to higher density of states around the Fermi level, discrete charge storage in the nanocrystals and stronger coupling with conduction channel, the thickness of tunneling oxide can be reduced for metal or metal oxide nanocrystal memory devices. To solve the scaling problems, high-κ tunneling barriers such as HfO_2, and Al_2O_3 are also reported by many researchers. The metal nanocrystals embedded in high-κ tunneling barriers with high thermal stability (~1000°C) are needed in future nanoscale nonvolatile memory applications, that can follow the conventional complementary-metal-oxide-semiconductor (CMOS) process line. Recently, the TiN nanocrystal memory devices were reported with process temperatures of 1000°C [7] and ~1050°C [10]. Due to the high melting point (~1200°C [11]) and high work function (Φ_m > 4.7 eV) of ruthenium oxide (RuO_x) materials, this nanocrystal can be also used as a charge-storage node in nanoscale flash memory device applications. Furthermore, the RuO_x material can be deposited

by atomic-layer-deposition (ALD), which will be useful in future applications. In this study, annealing dependence of the atomic-layer-deposited RuO_x nanocrystals embedded in the high-κ HfO_2/Al_2O_3 layers in an n–$Si/SiO_2/HfO_2/RuO_x/Al_2O_3$/Pt memory structure has been investigated. After post-deposition annealing (PDA) temperature ranges from 850–1000°C, the Hf-silicate layer at the SiO_2/HfO_2interface is formed. The memory devices with a low voltage operation (<5 V) and good memory characteristics are obtained after a high PDA of 1000°C.

2. Experimental and Methods

n-Type Si (100) substrate with a doping of $1 \times 10^{17}/cm^3$ was cleaned by an RCA process. To remove native oxide from the Si surface, the wafer was dipped in HF solution. After cleaning Si wafers, the tunneling oxide (SiO_2) with a nominal thickness of 3 nm was grown by a rapid thermal oxidation (RTO) process at a substrate temperature of 1000°C for 15 s. The oxygen gas (O_2) was used for oxidation. The high-κ HfO_2 film with an as-deposited thickness of 2 nm was grown for a wetting layer by ALD. The high-κ HfO_2 film can be used as a part of tunneling oxide. The stack tunneling oxide layers are SiO_2 and HfO_2 films, which can also improve memory performance. Then, the RuO_x metal layer with an as-deposited thickness of ~2 nm was grown by ALD using a diethyl-cyclopentadienyl ruthenium [$Ru(EtCp)_2$] precursor at a substrate temperature of 350°C. The precursor temperature was 100°C. The high-κ Al_2O_3 film with a thickness of 20 nm was deposited *in situ* for a blocking oxide by ALD. The H_2O precursor was used for oxygen content. The description of the deposition of high-κ and metal oxide films by ALD can be found in our previous study [12]. To form the RuO_x nanocrystals from a RuO_x nanolayer, a PDA process with the temperature ranges from 850 to 1000°C for 1 min in N_2 (90%) + O_2 (10%) gas mixtures by a rapid thermal annealing (RTA) process was performed. To maintain the quality of the high-κ Al_2O_3 film during the RTA process, a small amount (10%) of oxygen gas was used during the annealing process. For comparison, the pure Al_2O_3 film as a charge-trapping layer was also deposited on a SiO_2/Si substrate. The thickness of the Al_2O_3 film was 20 nm. The Al_2O_3 charge-trapping layer was annealed at 900°C for 1 min. in N_2 ambient by the RTA process. A platinum (Pt) metal gate electrode with a gate area of $1.12 \times 10^{-4}\,cm^2$ was fabricated by using a shadow mask. A schematic view of the RuO_x metal nanocrystal capacitors is shown in Figure 1. The RuO_x metal nanocrystals are embedded in the high-κ HfO_2/Al_2O_3 films. Table 1 shows the thicknesses and electrical characteristics of the RuO_x nanocrystal memory capacitors. To confirm the size and microstructure of the RuO_x nanocrystals, high-resolution transmission electron microscopy (HRTEM) with an operating voltage of 300 kV and a resolution of 0.17 nm was carried out. To investigate the chemical bonds of Si–O, Hf–O, Ru–O, and Al–O signals, X-ray photo-electron spectroscopy (XPS) was performed. Memory characteristics such as capacitance-voltage (C-V) hysteresis, current density-voltage (J-V), retention, and endurance, and so forth, were investigated using an HP 4284A LCR meter and HP 4156C semiconductor measurement analyzer.

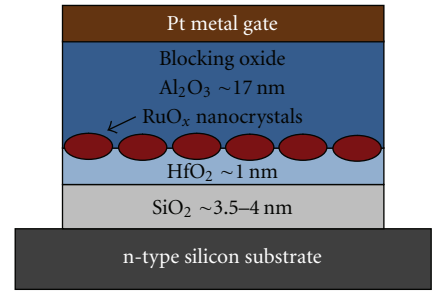


Figure 1: Schematic view of the RuO_x nanocrystal memory capacitor after the annealing process.

3. Results and Discussion

The thicknesses of the as-deposited dielectric layers are verified by cross-sectional HRTEM images, as shown in Figure 2(a). The as-deposited film is investigated for comparison. The thicknesses of SiO_2, HfO_2, RuO_x, and Al_2O_3 layers are 3, 2, 2, and 20 nm, respectively, for the as-deposited film. The RuO_x metal layer shows crystalline, while both high-κ HfO_2 and Al_2O_3 films appear amorphous in nature. The elemental compositions of all layers are observed by energy dispersive X-ray spectroscopy (EDS) with a spot size of 0.5 nm in a diameter and a spacial resolution of ~1 nm (Figure 2(b)). The numbers indicated on the EDS spectra correspond to the numbers on the TEM image. The peak elemental compositions of hafnium (Hf), ruthenium (Ru), oxygen (O) and aluminum (Al) atoms are 23.6, 3.5, 60.3, and 37.5 at %, respectively. It is estimated that the SiO_2, HfO_2 and Al_2O_3 films are closely stoichiometric for the as-deposited one. After annealing at 850°C (sample: S1), the RuO_x nanolayer displayed the nanocrystals (Figure 2(c)). The peak elemental compositions of the Hf, Ru, O, and Al atoms are 24.5, 17.7, 59.5 and 39.9 at %, respectively (Figure 2(d)). The atomic concentration of Ru is increased from 3.5 at % to 17.7 at % after the annealing process. It is speculated that this higher atomic concentration of Ru after the annealing process may be due to both Ru-rich nanocrystal formation, and higher thickness from 2-3 nm. Furthermore, the atomic concentrations of Si and Hf atoms at a beam position of 4 are 33.2 and 13.5 at %, respectively, for the annealed memory capacitors, and those values are 29.9 and 6 at % for the as-deposited capacitor. Enhanced Si and Hf atoms at the SiO_2/HfO_2 interface can be explained by diffusion of Hf and Si atoms after the annealing process. This is due to the Hf-silicate ($HfSi_xO_y$ or simply HfSiO) formation at the SiO_2/HfO_2 interface, which has been also confirmed by subsequent XPS measurement later. The atomic concentrations of Al and Hf at a beam position of 6 are 8.1 and 24.7, respectively, for the annealed memory capacitors, while those values are 6.1 and 24 for the as-deposited capacitors. The atomic concentrations are enhanced (slightly) after the annealing process. It indicates

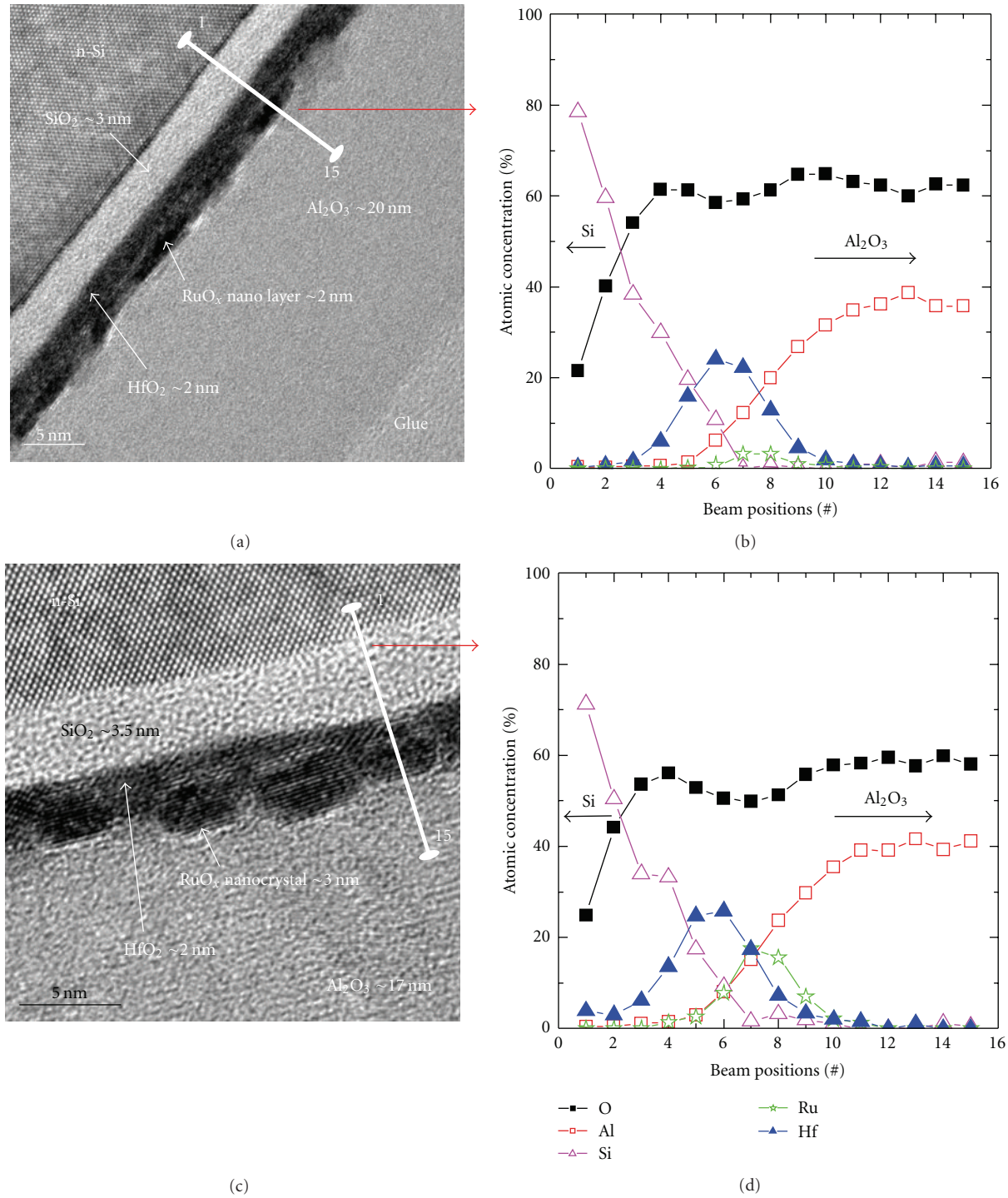


FIGURE 2: (a) HRTEM image of RuO_x nanolayer; (b) atomic concentration profiles by EDX from TEM image (a); (c) HRTEM image of RuO_x nanocrystals at PDA 850°C; (d) atomic concentration profiles by EDX from TEM image (c) in an n–Si/SiO_2/HfO_2/RuO_x/Al_2O_3/Pt structure. The beam positions are indicated as shown in the HRTEM images.

that the Hf and Al atoms are also diffused after the annealing process which can also form $HfAl_xO_y$ at the HfO_2/Al_2O_3 interface or in the vicinity of the RuO_x nanocrystals. The thicknesses of SiO_2, HfO_2, and Al_2O_3 layers are found to be 3.5, 1, and 17 nm, respectively (Figure 3(a)). The thickness of RuO_x nanocrystal is approximately 3 nm. Total physical thickness of the stack tunneling oxides including SiO_2, HfSiO, and HfO_2 layers is 4.5 nm, which is one of the important key areas to improve the memory characteristics. The thickness of SiO_2 layer is slightly (0.5 nm) increased

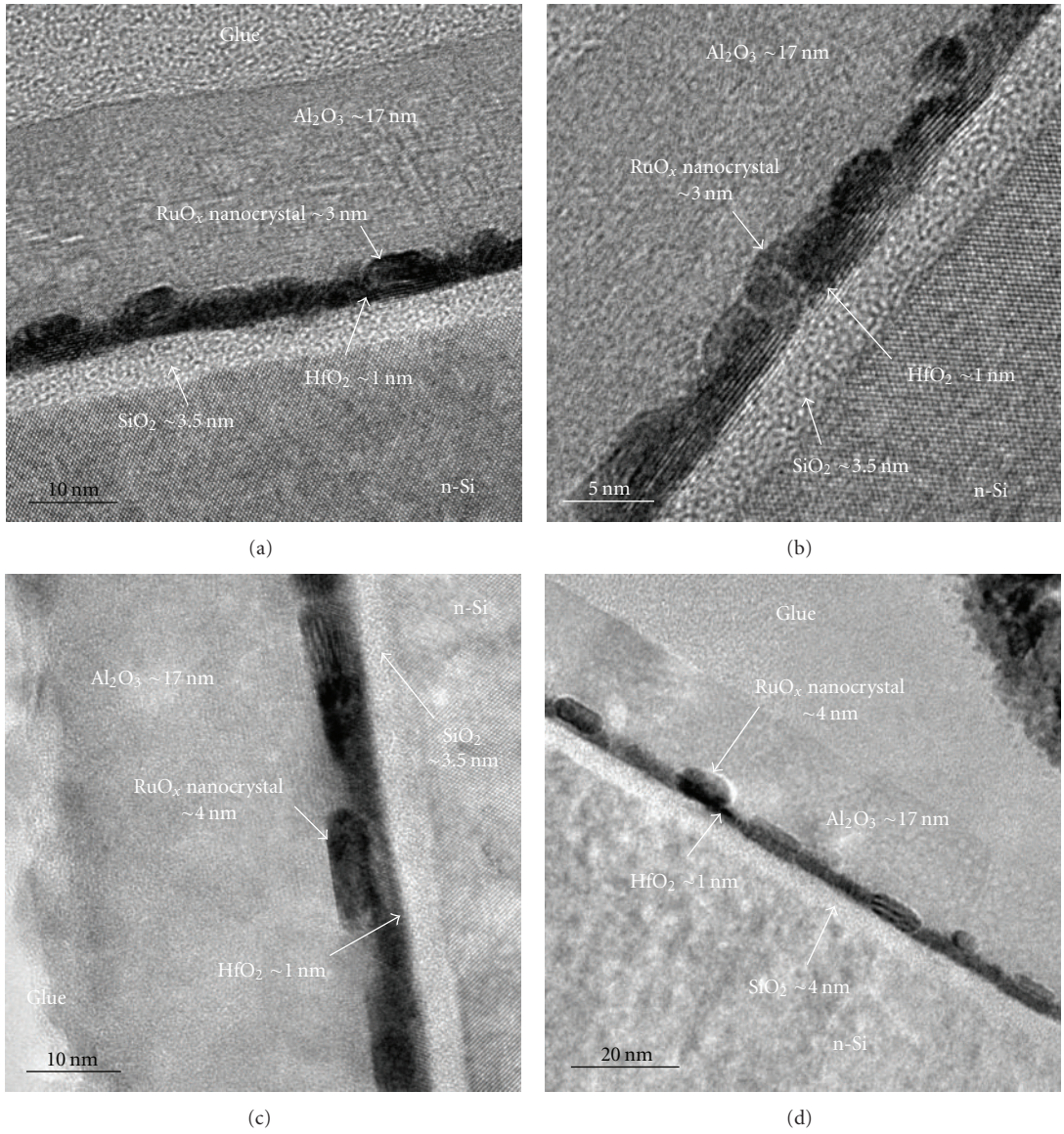


Figure 3: HRTEM images with different post-deposition annealing temperatures from (a) 850°C; (b) 900°C; (c) 950°C; (d) 1000°C in an n-Si/SiO_2/HfO_2/RuO_x/Al_2O_3/Pt capacitor.

Table 1: Thickness and characteristics of all memory capacitors after the annealing process.

Memory capacitors	PDA (°C)	SiO_2 (nm)	HfO_2 (nm)	RuO_x (nm)	Al_2O_3 (nm)	Memory window at ±5 V	Memory window at ±7 V	Breakdown voltage (V)
S1	850	3.5	1	3	17	1.8 V	4.0 V	−15
S2	900	3.5	1	3	17	8.0 V	11.1 V	−14
S3	950	3.5	1	4	17	7.5 V	10.8 V	−14
S4	1000	4.0	1	4	17	5.2 V	8.6 V	−13.4

compared to that of the as-deposited one. The thicknesses of HfO_2 and Al_2O_3 films are reduced (2-1 nm and 20–17 nm) compared to that of the as-deposited one, due to both the nanocrystal formation and densification of the films. All of the films including HfO_2, RuO_x, and Al_2O_3 show crystalline after the annealing process. The thickness of SiO_2 is increased (3.5–4 nm) by increasing the annealing temperatures from 850°C to 1000°C (Figure 3 and Table 1), due to both the oxygen diffusion and HfSiO formation at the SiO_2/HfO_2 interface. The thickness of SiO_2 layer including HfSiO film

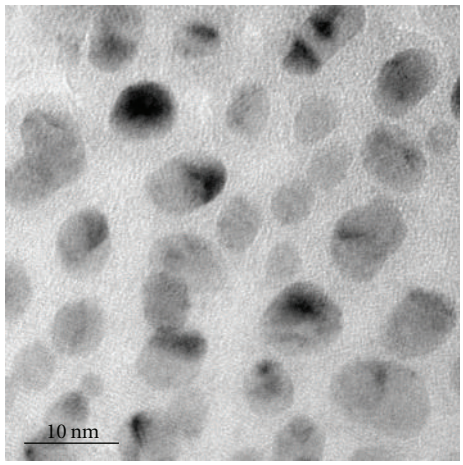


FIGURE 4: Plane view TEM image of the RuO_x metal nanocrystals in an n-$Si/SiO_2/HfO_2/RuO_x/Al_2O_3$/Pt memory capacitor at PDA 850°C. Isolated RuO_x nanocrystals are observed clearly.

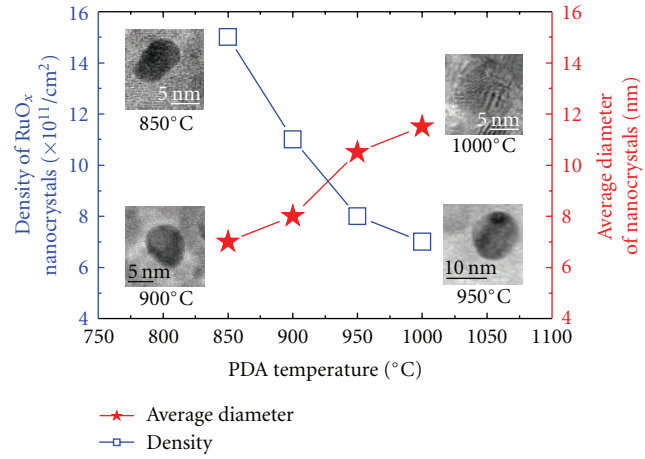


FIGURE 5: Variation of diameter and density of the RuO_x metal nanocrystals with different annealing temperatures from 850–1000°C. A single RuO_x nanocrystal is shown in the inset for each annealing temperature.

is approximately 4 nm at a PDA of 1000°C. The thickness of stack tunneling oxide including SiO_2, HfSiO, and HfO_2 layers nm is approximately 5 nm. It is expected that the thickness of the HfSiO layer is about 0.5–1.0 nm. The thickness (~3 nm at 850°C to ~4 nm at 1000°C) and average diameter (~7 nm at 850°C to ~11.5 nm at 1000°C) of the RuO_x metal nanocrystals are also increased with an increasing in the annealing temperature up to 1000°C (sample: S4), due to the agglomeration or nanotwin formation after high temperature process. The Si and metal nanotwin formations after the annealing process were also reported by Wang et al. [13]. Figure 4 shows a plane-view TEM image of the RuO_x nanocrystals in an n–$Si/SiO_2/HfO_2/RuO_x/Al_2O_3$/Pt memory structure at a PDA of 850°C (sample: S1). The RuO_x nanocrystals are observed clearly. The average diameter is approximately 7 nm, which is larger than that of the cross-sectional TEM image in Figure 2(c) (diameter: ~4 nm) due to the different crystal orientations or image captured at different positions. The nanocrystals are like a circular disk and the diameters are varied from 4–10 nm. Figure 5 shows the diameter and density of the RuO_x metal nanocrystals with different annealing temperature ranges from 850°C–1000°C. The density of the RuO_x nanocrystals is calculated from the plane-view TEM images. The density of the RuO_x metal nanocrystals is high: 1.5×10^{12}/cm^2 at a PDA of 850°C; 0.7×10^{12}/cm^2 at a PDA of 1000°C. A single RuO_x nanocrystal with different annealing temperatures is also shown in the inset of Figure 5. At a PDA of 1000°C, the nanocrystals are difficult to observe clearly on a plane-view TEM image because of crystalline Al_2O_3 film. It suggests that the density of the RuO_x metal nanocrystals decreases (slightly) with increasing the annealing temperatures due to the agglomeration of multiple nanocrystals. The nanocrystal sizes are varied from 4–10 nm, 4–12 nm, 4–17 nm, and 5–18 nm for the PDAs of 850°C, 900°C, 950°C, and 1000°C, respectively (data not shown). The average diameters are from 7–11.5 nm for the annealing temperatures at 850°C to 1000°C. The nanocrystal size distribution is broad with increasing the annealing temperature. However, the memory characteristics are very promising for future nanoscale nonvolatile memory applications. Furthermore, the compositions of the RuO_x metal nanocrystals are explained by XPS below.

Figure 6(a) shows the Ru3*d* spectra with different annealing temperatures. The RuO_x metal nanocrystals show the Ru$3d_{5/2}$ and Ru$3d_{3/2}$ doublets. At a PDA of 850°C (sample: S1), the peak binding energies of the Ru$3d_{5/2}$ and Ru$3d_{3/2}$ electrons are 281.7 eV and 285.9 eV, respectively. The peak binding energies are quite similar 281.7–281.5 eV for the Ru$3d_{5/2}$ electrons, and 285.9–285.7 eV for the Ru$3d_{3/2}$ electrons, with increasing annealing temperatures from 850–1000°C. The peak fittings of the Ru$3d_{5/2}$ core level electrons are performed by Shirley background subtraction and Gaussian/Lorentzian functions at a PDA of 1000°C (Figure 6(b)). The RuO_3 peak is located at 281.5 eV. A negligible intensity of the RuO_2 and RuO_4 peak is observed. The binding energy peak positions and the separation between the doublets (4.0–4.2 eV) indicate the presence of the RuO_x nanocrystals. Zhang et al. [14] reported that the peak binding energies of the Ru$3d_{5/2}$ electrons for Ru and RuO_2 elements were 280.6 eV and 281.6 eV, respectively. Kaga et al. [15] reported that the peak binding energies of the Ru$3d_{5/2}$ electrons are 280 eV for the Ru, and 280.8 eV for the RuO_2 films. Basically, the RuO_3 element is almost unchanged up to an annealing temperature of 1000°C due to the high thermal stability of the RuO_x nanocrystals in the memory capacitors.

Figure 7(a) shows the Hf4*f* peaks with different annealing temperatures. The peaks are located at the Hf$4f_{7/2}$ and Hf$4f_{5/2}$. These Hf4*f* doublet peaks originate from the pure HfO_2 or Hf-silicate film. The peak binding energies are 17–16.7 eV for the Hf$4f_{7/2}$ electrons, and 18.6–18.4 for the Hf$4f_{5/2}$ electrons with different annealing temperatures from 850–1000°C (samples: S1–S4). The shift of the Hf peak toward higher binding energy is attributed to both the formation of the Hf-silicate and Hf-aluminate films, which

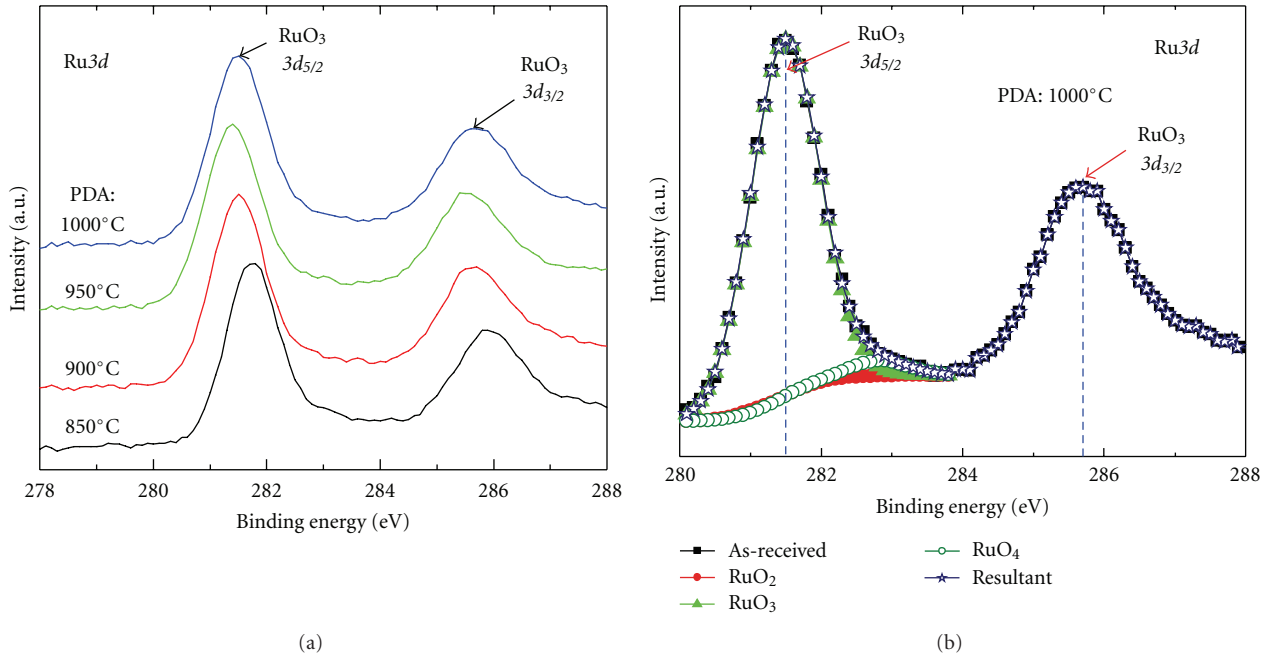


Figure 6: (a) XPS spectra of the Ru*3d* electrons with different annealing temperatures from 850–1000°C; (b) Ru*3d* electrons at a PDA of 1000°C is deconvoluted.

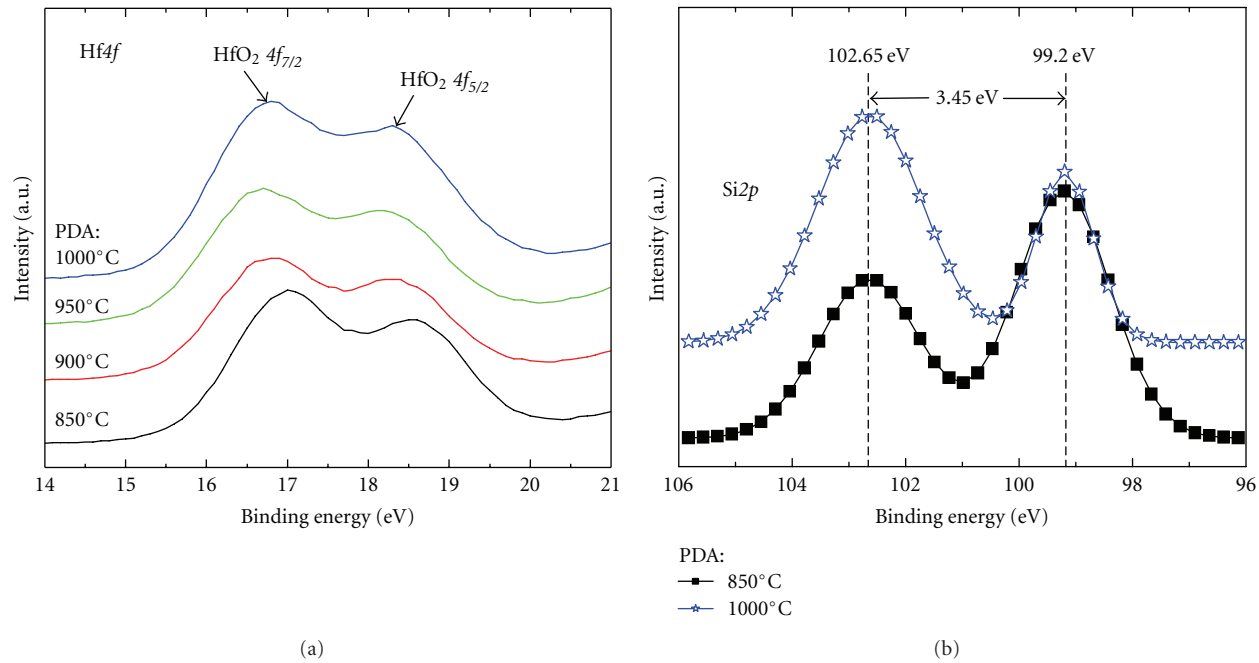
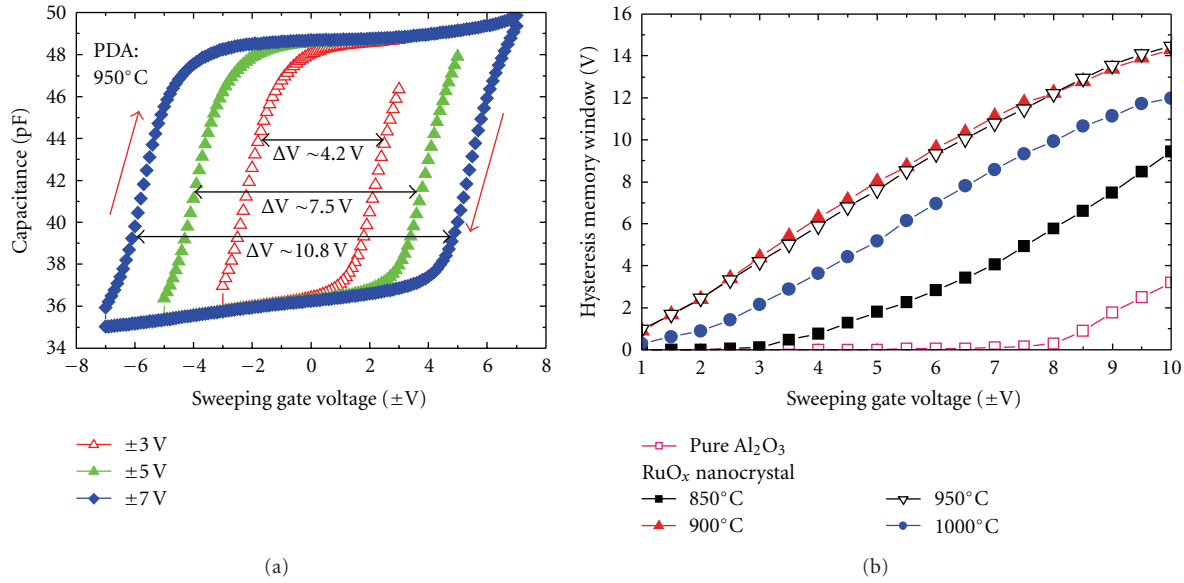


Figure 7: (a) XPS spectra of the Hf*4f* electrons with different annealing temperatures from 850–1000°C; (b) XPS spectra of the Si*2p* electrons at the PDA of 850°C and 1000°C.

is ~0.3 eV higher than that of pure HfO_2 film (16.7 eV [16]). Figure 7(b) shows the Si*2p* core-level electrons with different annealing temperatures (samples: S1 & S4). An additional peak shift with respect to the Si*2p* core-level spectra (99.2 eV) at the interfacial layer of the HfO_2/SiO_2 structures is ~3.45 eV with different annealing temperatures of 850°C and 1000°C. A lower Si*2p* binding energy shift with respect to SiO_2 (~4.2 eV) indicates that the interfacial layer is composed with the Hf atoms or formed Hf-silicate compound. It is believed that this Hf-silicate layer is at the SiO_2/HfO_2 interface or HfO_2 layer itself a HfSiO layer. Furthermore, the SiO_2 peak (~102.65 eV)



(a) (b)

FIGURE 8: (a) *C-V* hysteresis characteristics with different sweeping gate voltages at a PDA of 950°C; (b) a *C-V* hysteresis memory window versus sweeping gate voltages with different annealing temperatures from 850–1000°C. A high-κ Al_2O_3 charge-trapping layer is also shown for comparison.

intensity in Si*2p* spectra increases at a PDA of 1000°C. It implies that the thickness of the tunneling oxide layer is increased with increasing PDA temperature. The Al-O binding energies located at 74.7–74.5 eV with different annealing temperatures are observed (data not shown). The peak binding energies of O*1s* spectra are 532.4–532.2 eV for different annealing temperatures, suggesting the Al_2O_3 film. Due to the RuO_x metal nanocrystals embedded in the high-κ HfO_2/Al_2O_3 films, the improved charge storage characteristics can be expected with a low voltage operation that is explained below.

Clockwise capacitance-voltage (*C-V*) hysteresis characteristics of the RuO_x metal nanocrystal memory capacitors with different sweeping gate voltages (V_g) at a PDA of 950°C (sample: S3) are shown in Figure 8(a). The *C-V* measurement frequency was 1 MHz. Both hold and delay times were 0.1 s during *C-V* measurement. A hysteresis memory window of $\Delta V \approx 4.2$ V at a small sweeping gate voltage of $V_g = \pm 3$ V is observed. The hysteresis memory window increases by increasing the sweeping gate voltages. Due to the high density of the RuO_x metal nanocrystals, a large memory window of $\Delta V \approx 10.8$ V at a sweeping gate voltage of $V_g = \pm 7$ V is obtained. The electron- (or hole-) trapping density under positive and negative gate voltages can be calculated using this equation below:

$$N_{\text{electron (hole)}} = \frac{\Delta V_{\text{FB}} \cdot C_{Al_2O_3}}{q \cdot \Phi}, \quad (1)$$

where ΔV_{FB} ($=V_{\text{FB}} - V_{\text{FBN}}$) is the gate voltage shift under external gate voltage, V_{FB} is the flat-band voltage. V_{FBN} is the neutral V_{FB} where no hysteresis memory window is observed under a small sweeping gate voltage, $C_{Al_2O_3}$ is the capacitance of the blocking oxide [17], "Φ" is the gate area, and "q" is the electronic charge. A neutral flat-band voltage (V_{FBN}) is +0.05 V under a gate voltage of ±0.5 V (data not shown). A high C_{total} is 48.72 pF, which is very useful for the nanoscale flash memory device applications. The capacitance of the $C_{Al_2O_3}$ is ~75.8 pF by using dielectric permittivity of ~13 of the Al_2O_3 films [18]. The values of V_{FB} are 1.5, 3.1, and 4.5 V under sweeping gate voltages of +3 V → −3 V, +5 V → −5 V, and +7 V → −7 V, respectively, while those values are −2.7 V, −4.4 V, and −6.3 V under the sweeping gate voltages of −3 V → +3 V, −5 V → +5 V, and −7 V → +7 V, respectively. Considering the $V_{\text{FBN}} = +0.05$ V, and using (1), the high electron-trapping densities are calculated ~6.12×10^{12}, 1.29×10^{13}, and 1.86×10^{13} cm^{-2} under the gate voltages of +3 V, +5 V and +7 V, respectively. The high hole-trapping densities are also calculated ~1.12×10^{13}, 1.83×10^{13}, and 2.64×10^{13} cm^{-2} under the gate voltages of −3 V, −5 V, −7 V, respectively. It suggests that the hole-trapping density is higher than that of the electron-trapping density, which is explained as follows. Gibbs free energies of the HfO_2, RuO_3, and Al_2O_3 materials are −1010.75, −40.875, and −1582.3 kJ/mol at 300 K, respectively. The HfO_2, and Al_2O_3 films will be easily oxidized than the RuO_3 films. It suggests that the oxygen gathering (O^{2-}) could be observed in the HfO_2 and Al_2O_3 films and oxygen deficiency could be observed inside the RuO_x films. It suggests that the RuO_x nanocrystals are like a core-shell structure, that is, Ru-rich is inside the nanocrystal and oxygen-rich is outside the nanocrystal. So annular region of the nanocrystals will be oxygen-rich, where Hf or Al atoms will be mixed with Ru atoms. So the oxygen vacancy (positive-type defects) could be realized inside the nanocrystal and oxygen-rich (negative-type defects) could be realized on the boundary of the nanocrystal. As a consequence, the positive-type defects can trap the electrons and the negative-type defects can trap the holes. It is expected that the area covered by the annular

region of the nanocrystals should be larger than the core area of the nanocrystals. It is believed that the holes will be trapped in the annular region while the electrons will be trapped in the core region of the nanocrystals. Considering the nanocrystal density of $0.8 \times 10^{12}\,\text{cm}^{-2}$ at a PDA of 950°C, one RuO_x nanocrystal can trap 23 electrons and 33 holes under the gate voltages of +7 V and −7 V, respectively. The hysteresis memory windows as well as electron- (or hole-) trapping density can be varied with sweeping gate voltages and different annealing temperatures, as shown in Figure 8(b). A large hysteresis memory window of the RuO_x metal nanocrystal memory capacitors at different annealing temperatures is observed compared to that of the pure Al_2O_3 charge-trapping layers in a Pt/Al_2O_3 (20 nm)/SiO_2 (3 nm)/Si structure, due to charge-trapping in the RuO_x nanocrystals. The memory capacitors with an as-deposited RuO_x metal layer in an n–Si/SiO_2/HfO_2/RuO_x/Al_2O_3/Pt structure have been also fabricated for comparison. According to our capacitor design, the metal gate electrode (Pt) is deposited by using shadow mask. It indicates that the device-to-device isolation is observed by metal gate electrode only but the RuO_x metal layer is continuous. For the as-deposited RuO_x film, the *C-V* characteristics could not be observed from our CV measurement system and the system shows OVERLOAD. Then the capacitors have been annealed from 600–1000°C. The *C-V* characteristics are observed from the PDAs of 800–1000°C. At PDA of <800°C, the *C-V* characteristics could not be measured. It suggests that the electric field could not pass inside the RuO_x metal layer, resulting in no *C-V* characteristics. At the PDA of >800°C, the RuO_x nanocrystals have been formed and the metal layer becomes discrete, resulting in the electric field pass through the RuO_x nanocrystal boundary. In this case, the *CV* system could measure *C-V* characteristics. On this point, the temperature of the metal nanocrystal formation can be monitored, which is also important for other metal nanocrystal formation process. The nanocrystal formation temperature depends on the thickness of the metal nanolayer, deposition process, and material itself. A memory window of the pure Al_2O_3 charge-trapping layer is increased (slightly) after sweeping gate voltages of ±7 V. After the annealing process, the Al_2O_3 grain boundaries can be formed and the charges can be trapped on the grain boundary sites. The thickness of tunneling oxide (SiO_2) is increased (3 nm to 4 nm) at the SiO_2/Al_2O_3 interface after the high-temperature annealing process. Due to both the thicker tunneling oxide and the large conduction band offset ($\Delta E = (E_c)_{\text{Si}} - (E_c)_{\text{Al}_2\text{O}_3} = 4.05\,\text{eV} - 1.25\,\text{eV} = 2.8\,\text{eV}$) between the Si and Al_2O_3 conduction layers, a large operation voltage of 7 V is needed to trap charges in the Al_2O_3 charge-trapping layers. On the other hand, a small operation voltage of <|7 V| is needed for the RuO_x metal nanocrystal memory capacitors, due to the negative conduction band offset ($\Delta E = (E_c)_{\text{Si}} - (E_F)_{\text{RuO}_x} = 4.05\,\text{eV} - 4.7\,\text{eV} = -0.65\,\text{eV}$) between the Si and RuO_x nanocrystals. The work function of RuO_x layer is ~4.7 eV. It indicates that the charge trapping probability in the RuO_x nanocrystals will be enhanced when compared to that observed for the pure Al_2O_3 charge trapping layers. The hysteresis memory window increases with increasing the sweeping gate voltages up to ±10 V. If the operation voltage is less than |7 V| then the charge-trapping can be only observed in the RuO_x nanocrystals. If the operation voltage is higher than that of |7 V| then the charge-trapping can be observed in both of the RuO_x nanocrystals and Al_2O_3 charge-trapping layers. Under a sweeping gate voltage of ±5 V, the hysteresis memory windows are 1.8, 8.0, 7.5, and 5.2 V for the PDA of 850°C, 900°C, 950°C, and 1000°C, respectively. Those values are 4.0, 11.1, 10.8, and 8.6 V under a sweeping gate voltage of ±7 V (Figure 8(b) and Table 1). Even though the high-density RuO_3 nanocrystals are observed at a PDA of 850°C but the smallest memory window is observed as compared to that observed for other high temperature annealing processes. It may be due to both the higher equivalent oxide thickness (EOT = 8.9 ± 0.5 nm), as shown in Figure 9, and the unwanted defects remained in the RuO_3 nanocrystals at low annealing temperature (850°C). The EOT decreases (slightly) with increasing PDA up to 950°C, due to densification of the layers. But the EOT is increased at a PDA of 1000°C due to a thicker stack tunneling oxide (~5 nm). A minimum EOT of 7.9 ± 0.5 nm is observed at a PDA of 950°C. The memory window at 1000°C is also lower as compared to that of both annealing temperatures of 900°C and 950°C due to the higher EOT, the lower density of the RuO_x nanocrystals and higher leakage current, which will be discussed below. At a PDA of 900°C and 950°C, a large hysteresis memory window of >14.0 V is observed under a sweeping gate voltage of ±10 V due to both the lower EOT (7.9 ± 0.5 nm) and the RuO_x nanocrystals composed with RuO_2 and RuO_3 elements (data not shown). A memory window of 0.9 V is also observed under a small sweeping gate voltage of ±1 V. The large memory window and high electron- (or hole-) trapping density of the memory devices under a low voltage operation can be used in future multi-level-charge (MLC)-trapping flash memory device applications, which has been explained below.

The *C-V* hysteresis indicates that the charge can be trapped in the RuO_x nanocrystals under a small positive gate voltage and the trapped charges can be erased under a small negative gate voltage. The electric fields across layer-by-layer under the external gate voltages (V_g) can be explained below. Considering the memory device under programming mode, the stack voltage, V_{stack} ($=V_{\text{g}} - V_{\text{FBN}} - \psi_s$) across the memory structure can be written by

$$V_{\text{stack}} = V_{\text{SiO}_2} + V_{\text{HfO}_2} + V_{\text{RuO}_x} + V_{\text{Al}_2\text{O}_3}, \tag{2}$$

where ψ_s is the surface potential at the SiO_2/Si interface, V_{SiO_2} is the voltage across the SiO_2 tunneling layer (i.e., SiO_2 and HfSiO), V_{HfO_2} is the voltage across the HfO_2 layer, V_{RuO_x} is the voltage across the RuO_x nanocrystal layer, and $V_{\text{Al}_2\text{O}_3}$ is the voltage across the blocking oxide (Al_2O_3). The V_{FBN} is about +0.05 V for our device. The surface potential can be written as

$$\psi_s = \frac{kT}{q} \ln \frac{N_D}{n_i}, \tag{3}$$

where k ($=1.38 \times 10^{-23}$ J/K) is the Boltzmann's constant, T (=300 K) is the absolute temperature, N_D ($1 \times 10^{17}\,\text{cm}^{-3}$) is

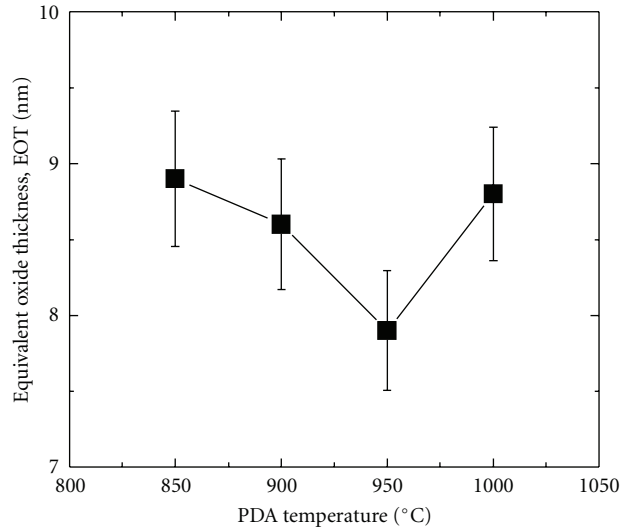


FIGURE 9: Equivalent oxide thickness (EOT) versus different annealing temperatures.

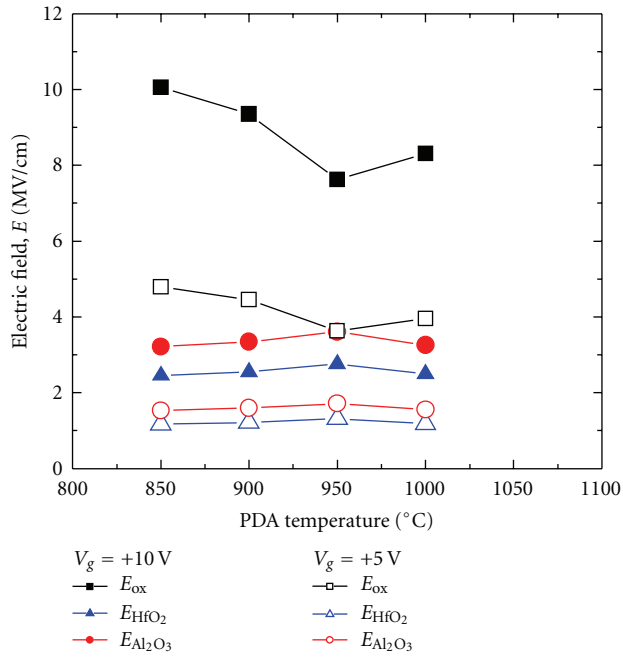


FIGURE 10: Electric fields across different layers versus different annealing temperatures and different gate voltages.

the doping density in n-type Si, n_i (=1.45 × 10^{10} cm^{-3}) is the intrinsic carrier concentration of Si. Using those above values, the ψ_s is 0.41 V. From Gauss's law of electrostatics on layer-by-layer structure, the boundary condition can be written as follows:

$$\varepsilon_{SiO_2} \cdot E_{SiO_2} = \varepsilon_{HfO_2} \cdot E_{HfO_2} = \varepsilon_{RuO_x} \cdot E_{RuO_x} = \varepsilon_{Al_2O_3} \cdot E_{Al_2O_3}. \quad (4)$$

The ε_{SiO_2}, ε_{HfO_2}, ε_{RuO_x}, and $\varepsilon_{Al_2O_3}$ are the relative permittivities of the SiO_2, HfO_2, RuO_x nanocrystal, and Al_2O_3 layers, respectively. The E_{SiO_2}, E_{HfO_2}, E_{RuO_x}, and $E_{Al_2O_3}$ are the

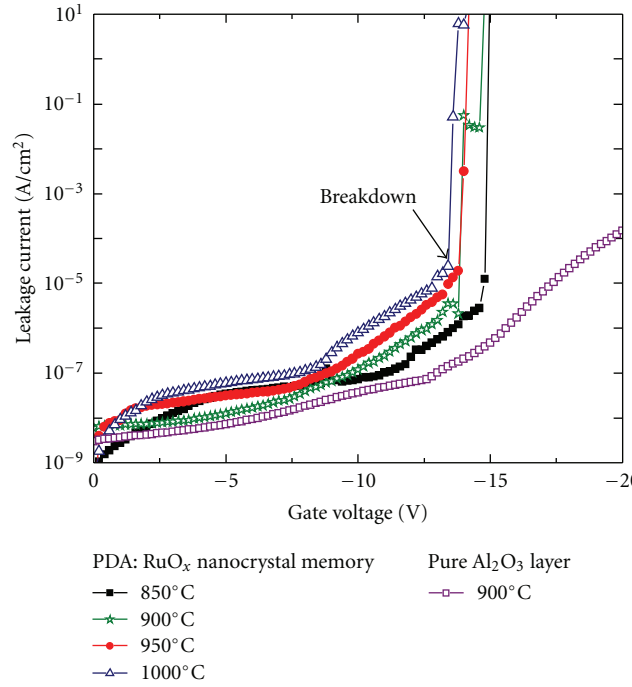


FIGURE 11: Leakage current with different annealing temperatures.

electric fields across the SiO_2, HfO_2, RuO_x nanocrystal, and Al_2O_3 layers, respectively. The electric fields across the SiO_2, HfO_2, and Al_2O_3 layers can be obtained from (2) and (4),

$$E_{SiO_2} = \frac{V_{SiO_2}}{t_{SiO_2}} = \left[t_{SiO_2} + \varepsilon_{HfSiO} \cdot \left\{ \frac{t_{HfO_2}}{\varepsilon_{HfO_2}} + \frac{t_{RuO_x}}{\varepsilon_{RuO_x}} + \frac{t_{Al_2O_3}}{\varepsilon_{Al_2O_3}} \right\} \right]^{-1} \cdot V_{stack}, \quad (5)$$

$$E_{HfO_2} = \frac{V_{HfO_2}}{t_{HfO_2}} = \left[t_{HfO_2} + \varepsilon_{HfO_2} \cdot \left\{ \frac{t_{SiO_2}}{\varepsilon_{SiO_2}} + \frac{t_{RuO_x}}{\varepsilon_{RuO_x}} + \frac{t_{Al_2O_3}}{\varepsilon_{Al_2O_3}} \right\} \right]^{-1} \cdot V_{stack}, \quad (6)$$

$$E_{Al2O3} = \frac{V_{Al_2O_3}}{t_{Al_2O_3}} = \left[t_{Al_2O_3} + \varepsilon_{Al_2O_3} \cdot \left\{ \frac{t_{SiO_2}}{\varepsilon_{SiO_2}} + \frac{t_{HfO_2}}{\varepsilon_{HfO_2}} + \frac{t_{RuO_x}}{\varepsilon_{RuO_x}} \right\} \right]^{-1} \cdot V_{stack}, \quad (7)$$

where the t_{SiO_2}, t_{HfO_2}, t_{RuO_x}, and $t_{Al_2O_3}$ are the thicknesses of the SiO_2, HfO_2, RuO_x nanocrystal, and Al_2O_3 layers, respectively. Total series capacitance (C_{total}) at accumulation region can be written as

$$\frac{1}{C_{total}} = \frac{t_{SiO_2}}{\varepsilon_{SiO_2}.\varepsilon_0.A} + \frac{t_{HfO_2}}{\varepsilon_{HfO_2}.\varepsilon_0.A} + \frac{t_{RuO_x}}{\varepsilon_{RuO_x}.\varepsilon_0.A} + \frac{t_{Al_2O_3}}{\varepsilon_{Al_2O_3}.\varepsilon_0.A}, \quad (8)$$

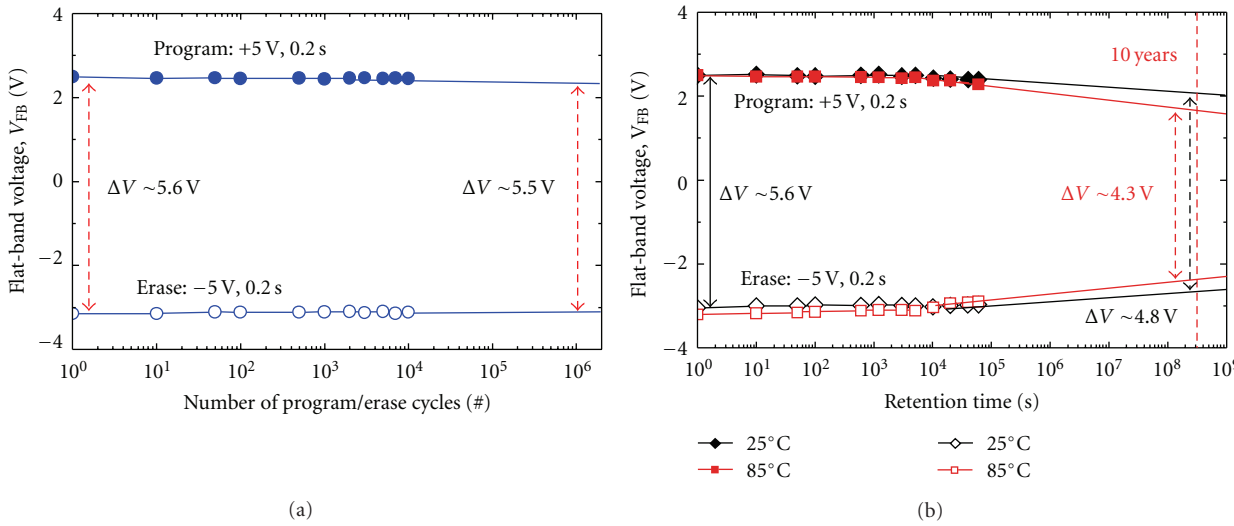


FIGURE 12: (a) Program/erase endurance; (b) retention characteristics of the RuO_x metal nanocrystal memory capacitors at a PDA of 1000°C.

where ε_0 (=8.85 × 10^{-14} F/cm) is the free space permittivity. The values of C_{total} are 43.43, 45.2, 48.72, and 43.92 pF for the PDA of 850°C, 900°C, 950°C, 1000°C, respectively. Considering the series capacitances using (8) and thicknesses (Table 1) of layer by layer for all annealing temperatures, the relative permittivity values of the Al_2O_3, HfO_2, and RuO_x layers are 13, 17, and 40, respectively [18–21]. The higher relative permittivity of the Al_2O_3 film is due to the crystallization or RuO_x diffusion into the Al_2O_3 film during a high-temperature annealing process. The different crystal orientation including metal-doped Al_2O_3 film or nanograin formation of the high-κ Al_2O_3 films may also cause higher permittivity of the film. The values of effective permittivity of the SiO_2 layer are found to be 4.15, 4.65, 6.15, and 5.1 for the PDA of 850°C, 900°C, 950°C, 1000°C, respectively. The effective permittivity of the tunneling oxide (SiO_2) is higher than that of a pure SiO_2 layer (ε_{SiO_2} = 3.9). It suggests that the Hf-silicate layer at the HfO_2/SiO_2 interface is formed after the annealing process, due to the Hf and Si atom diffusion which is also explained by EDX and XPS analyses. Using those relative permittivity values in (5), (6), and (7), the electric fields have been calculated under positive gate voltages of V_g = +10 V or +5 V on the Pt gate electrode. The electric fields versus PDA temperatures are plotted as shown in Figure 10. The electric field across the SiO_2 layer (E_{SiO_2}) is higher than 8 MV/cm under an operation voltage of +10 V for all annealing temperatures. Under a gate voltage of +5 V, the E_{SiO2} is ~4 MV/cm. It indicates that the modified Fowler-Nordheim (F-N) tunneling mechanism plays a role to trap electron in the RuO_x nanocrystals. The electric field across the HfO_2 layer is smaller ~2 MV/cm but the conduction band offset [$\Delta E = (E_c)_{Si} - (E_c)_{HfO_2}$ = 4.05 eV − 2.35 eV = 1.7 eV] between the Si and HfO_2 conduction layers is also smaller. The electrons can be tunneled easily through the HfO_2 layer. The electric field is decreased (slightly) with increasing the PDA temperature, due to the higher thickness and permittivity of the SiO_2layer. It is noted that the electric field across the high-κ Al_2O_3 layers is much smaller than the electric field across the SiO_2 layer. In this case, the electrons are tunneled through the tunneling oxide layer and the charges are trapped in the RuO_x metal nanocrystals under a low voltage operation. When we apply the negative gate voltage on Pt gate electrode then the electric field across the tunneling oxide layer (E_{SiO_2}) is also higher than that of the blocking oxide layer ($E_{Al_2O_3}$). First, the trapped electrons will be tunneled back from the RuO_x nanocrystals to the Si conduction layer. Second, the holes will be tunneled from the Si valence band to the RuO_x nanocrystals. So, the large memory window is observed due to the electron and hole traps under positive and negative gate voltages, respectively, on the gate electrode.

Figure 11 shows the variation of leakage current density with different annealing temperatures. The leakage current density of the RuO_x nanocrystal memory capacitors is higher than that of the pure Al_2O_3 charge-trapping layers due to the RuO_x nanocrystal formation. The leakage current increases with increasing the PDA temperatures, due to the nanocrystal formation and outdiffusion of RuO_x metal into the high-κ Al_2O_3 blocking oxide. Furthermore, the crystallization of the Al_2O_3 film can also play a role to increase leakage current. The formation of crystallites may result in increased leakage currents along grain boundaries of the Al_2O_3 films after high temperature annealing process. The breakdown voltage of the RuO_x nanocrystal memory capacitors decreases with increasing the PDA temperatures, due to higher leakage current. It is also believed that the hysteresis memory window at a PDA of 1000°C is lower as compared to that of 950°C, due to a higher leakage current. It implies that the hysteresis memory window can be limited by gate leakage or backtunneling current, and also by design of memory structure.

Figure 12(a) shows the excellent program/erase endurance characteristics under a small program/erase voltage of ±5 V and a pulse width of 200 ms for a PDA of 1000°C.

An initial memory window is 5.6 V and it is 5.5 V after extrapolation of 10^4 cycles. A small memory window loss of ~2% is observed after 10^6 cycles. Figure 12(b) shows the variation of the flat-band voltage with retention time at a PDA of 1000°C. The program/erase voltage is ±5 V and pulse width is 200 ms. To read the data (i.e., V_{FB}) with elapsed time under programming/erasing conditions, the capacitance is measured at a read voltage of 0.1 V and the capacitance transferred to the V_{FB}. An initial memory window is 5.6 V, and it is 4.8 V at a room temperature (RT: 25°C) and 4.3 V at 85°C after extrapolation of 10 years data retention. A small charge loss of ~14% at RT (~23% at 85°C) is observed after 10 years of retention time. A small charge loss and large memory window of the RuO_x nanocrystal memory capacitors under a small program/erase voltage of ±5 V are due to both the deep-level charge trap in the RuO_x nanocrystals and the thicker (~5 nm) tunneling oxide layer at a PDA of 1000°C, which is very useful for future nanoscale nonvolatile memory applications.

4. Conclusions

The RuO_x metal nanocrystals in n–Si/SiO_2/Hf-silicate/HfO_2/RuO_x/Al_2O_3/Pt capacitors with different annealing temperatures from 850–1000°C have been investigated by using HRTEM, EDX, and XPS measurements. An average diameter of the RuO_x metal nanocrystals increases from 7–11.5 nm and the density decreases from $1.5 - 0.7 \times 10^{12}\,cm^{-2}$ with increasing PDA temperatures from 850°C to 1000°C, due to agglomeration of multiple nanocrystals. The isolated nanocrystals are observed by plane-view TEM images. Due to the diffusion of the Si and Hf atoms at the HfO_2/SiO_2 interface during the annealing process, the Hf-silicate layer is confirmed by both XPS and electrical measurements. The RuO_x metal nanocrystals with a high-density ($>1 \times 10^{12}/cm^2$), large memory window (>5 V) at a small gate voltage operation (<5 V), and a small EOT (~9.0 nm) are obtained. A good endurance of $\sim 10^6$ cycles and a large memory window of ~4.3 V with a small charge loss of ~23% at 85°C after extrapolation of 10-year data retention are obtained, which can be useful in future low voltage operated nanoscale nonvolatile memories.

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