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Review Article

Technical Solutions to Mitigate Reliability Challenges due to Technology Scaling of Charge Storage NVM

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Charge storage nonvolatile memory (NVM) is one of the main driving forces in the evolution of IT handheld devices. Technology scaling of charge storage NVM has always been the strategy to achieve higher density NVM with lower cost per bit in order to meet the persistent consumer demand for larger storage space. However, conventional technology scaling of charge storage NVM has run into many critical reliability challenges related to fundamental device characteristics. Therefore, further technology scaling has to be supplemented with novel approaches in order to surmount these reliability issues to achieve desired reliability performance. This paper is focused on reviewing critical research findings on major reliability challenges and technical solutions to mitigate technology scaling challenges of charge storage NVM. Most of these technical solutions are still in research phase while a few of them are more mature and ready for production phase. Three of the mature technical solutions will be reviewed in detail, that is, tunnel oxide top/bottom nitridation, nanocrystal, and phase change memory (PCM). Key advantages and reported reliability challenges of these approaches are thoroughly reviewed in this paper. This paper will serve as a good reference to understand the future trend of innovative technical solutions to overcome the reliability challenges of charge storage NVM due to technology scaling.

1. Introduction

Charge storage nonvolatile memory (NVM), that is, standard floating gate (FG) and nitride-based charge trap flash (CTF) memory, has always been at the heart of the evolution of IT mobile devices, for example, tablet, cell phone, digital camera, and so forth. The future outlook of charge storage NVM is getting brighter as the world's technological per-capita capacity to store information has roughly doubled every year and projected to create up to 2.5 quintillion bytes of data everyday as of 2012 [1, 2]. This indicates the insatiable demand for bigger storage space, and lower cost per bit continues to rise for flash memory in the future. The persistent effort to achieve bigger memory space at lower cost was driven by Moore's law of cost reduction through technological scaling [3–6]. Conventional technology scaling that typically scales down the physical dimensions of charge storage NVM came into fruition through the advancement in lithography techniques as the main driving force [3]. As shown in Figure 1, technology trend of charge storage NVM predicted by International Technology Roadmap for Semiconductors (ITRS) 2011 revealed that the floor space of charge storage NVM continues to shrink, and by 2015, flash memory is predicted to be scaled to 16 nm [2]. Beyond 30 nm, this continuous aggressive scaling of charge storage NVM is fast approaching NVM device's fundamental limit or its practical limit in considering the balance between economic gain and investment required to resolve issues that arise from scaling [5]. Technological scaling of charge storage NVM has unveiled many critical reliability issues related to device characteristics, for example, charge loss (CL), charge gain (CG), and random telegraph noise (RTN) exhibited through threshold voltage (V_t) shift and broadening of memory cell, neighboring bit interference (i.e., disturb phenomenon), cell-to-cell coupling interferences, and severe short channel effects.

Increase in cell-to-cell interference and decrease in gate coupling ratio have been highlighted as the two main

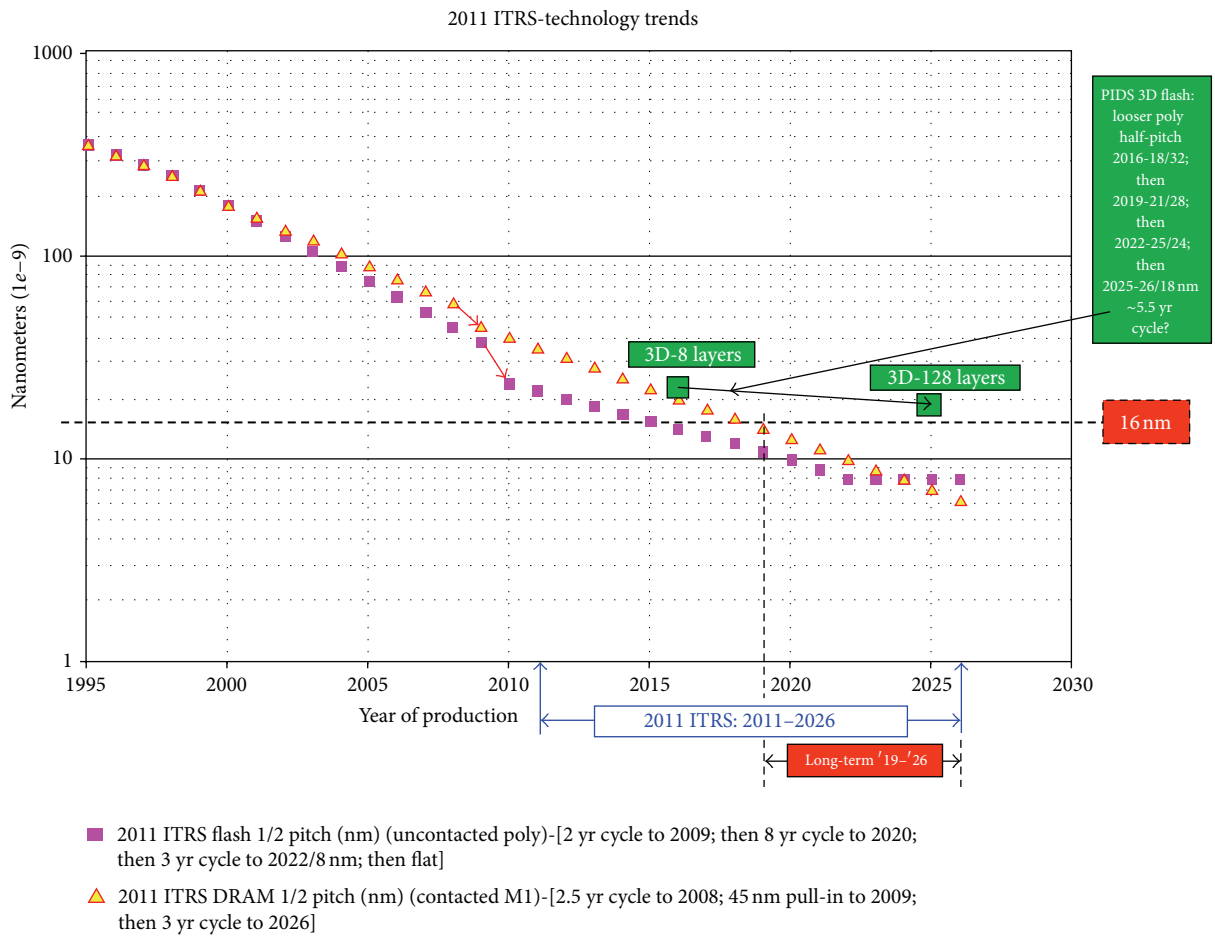


Figure 1: Technology scaling trend of 2011 ITRS [2].

technology barriers to develop memory technology of sub-40 nm and less [4, 5, 7–14]. Furthermore, technological scaling of physical dimension for memory cell alone will not be able to completely overcome these reliability issues. Kinam et al. have proposed and emphasized that further technology scaling should be complemented with novel mitigation approaches to extend the dominance of charge storage NVM in semiconductor market [4–14]. Many researchers have dedicated their research work on these novel approaches to extend the longevity of charge storage NVM devices beyond 30 nm. These novel approaches include (1) novel flash cell structures [4, 15–19], for example, Hemi-Cylindrical FET (HCFET) and FinFET; (2) new lithography process technologies, for example, improvement in patterning techniques to realize 20 nm structures [20]; (3) novel materials in charge storage layer, for example, phase change memory (PCM) [21–37], magnetic random access memory (MRAM) [6], and nanocrystal [38–59]; (4) tunnel barrier engineering, for example, VARIable Oxide Thickness (VARIOT) [60–63], and implementation of high-k dielectric [64, 65], for example, HfO_2; (5) enhancement of flash memory system by integrating complex compensation schemes through implementing embedded flash controllers [7]; (6) improvement made on error correction code (ECC) algorithm [7]; and (7) innovative way to stack flash cell, for example, high density 3D stack NAND flash and cross point memories. As transistor based charge storage NVM approaching fundamental limits of NVM characteristics soon, these technical solutions or combination of them could be the key in future development of charge storage NVM. Thus, thorough studies and understanding of these technical solutions are required.

This paper is focused on providing comprehensive review on research findings on reliability challenges and technical solutions to mitigate device characteristics issues that stem from technology scaling of charge storage NVM. In Section 2, reliability challenges resulted from technology scaling of charge storage NVM are reviewed. In Section 3, an overview of viable technical solutions is reviewed. These technical solutions consist of tunnel barrier engineering, novel flash cell structures, and emerging NVM technologies that quickly evolve from research phase to production, for example, PCM. Among the technical mitigation methods, three of the mature technical solutions are discussed in detail, that is, tunnel oxide nitridation, nanocrystal memory, and PCM. Based on comprehensive work done by research groups on these three mitigation methods, key advantages and critical reliability challenges are reviewed. Section 4 reviews tunnel oxide nitridation in detail and assesses the

intricate changes of implementing top/bottom nitridation to endurance/retention performance of charge storage NVM. In Sections 5 and 6, intricate research findings of emerging NVM technologies, that is, nanocrystal and phase change memory (PCM), are reviewed, respectively. These novel NVM technologies may eclipse standard FG flash memory as the main driving force to sustain the growth of semiconductor market due to its superior scalability. Section 7 wraps up our review. Our thorough review in this paper can be served as good reference to understand recent research findings on the reliability challenges of charge storage NVM that stems from technology scaling and technical solutions (in research phase or in production) to mitigate device characteristic issues of charge storage NVM.

2. Reliability Challenges of Technology Scaling for Charge Storage NVM

To achieve larger memory space with lower cost per bit, relentless cost saving effort was aggressively pursued through reduction in physical dimension of charge storage NVM as shown in Figure 1. Recent publications have reported that further scaling beyond 30 nm has resulted in critical reliability challenges. These challenges on device characteristics of charge storage NVM include cell level V_t instability issues, array level V_t instability issues due to cell-to-cell interference, RTN, and so forth. These mechanisms yielded read failures through broadening and shifting of V_t distribution of memory cells that impact the memory window (MW). Table 1 summarizes crucial reliability challenges faced by charge storage NVM and critical findings based on comprehensive work done by many researchers.

3. Overview of Viable Technical Solutions

Throughout the technology scaling trend of charge storage NVM, there are two main obstacles to breakthrough to reach the next technology nodes, that is, limitation on lithography process and device characteristics (as reviewed in Table 1). Optical lithography techniques have been improved to extend the longevity of optical lithography tools to sub-30 nm [66]. Double patterning techniques or especially self-aligned spacer double patterning (SADP) technique are best suited to develop 20 nm structures to extend 193 nm immersion lithography processes [20] while anticipating next generation extreme UV (EUV) tools. Furthermore, it has been implemented in volume manufacturing of high density NAND devices. For reliability challenges on device characteristics issues due to technology scaling, the key strategy as proposed by many researchers is to replace conductive floating gate (FG) with compact discrete charge trapping layer [4, 6, 9, 11, 66] to enable further physical dimension scaling of memory cell which is not possible for FG flash memory. To further mitigate the reliability challenges due to technology scaling as reviewed in Table 1, there are many viable technical solutions proposed by researchers to overcome device characteristics issues due to continuous technology scaling. These proposed technical solutions are summarized in Table 2 as shown next.

As shown in Table 2, the viable technical mitigation solutions can be categorized to tunnel barrier engineering (TBE), novel flash cell structure, and emerging NVM technologies. To further enhance the endurance and retention performance of tunnel dielectric of charge storage NVM, TBE was implemented by modulating the electrical properties of tunnel dielectric through several major techniques, that is, (1) nitridation at top/bottom interfaces of tunnel oxide layer [67–82]; (2) implementation of novel VARIOT concept [60–63]; and (3) replacement of conventional oxide layer with high-k dielectric material [64, 65]. Tunnel oxide nitridation is performed by incorporating optimized nitrogen concentration at top/bottom tunnel oxide layer of charge storage layer through thermal nitridation and chemical/physical nitridation process techniques to enhance reliability performance of charge storage NVM devices [67]. Implementation of novel VARIOT concept involves two-layer dielectric stack with a combination of low-k/high-k or three-layer dielectric stack with a combination of low-k/high-k/low-k to regulate tunnel barrier height and achieve enhancement in endurance/retention characteristics of charge storage NVM devices [60–63]. Combinational approaches of tunnel oxide nitridation and bandgap engineering have exhibited excellent endurance performance for NAND flash memory [63].

In order to enhance the reliability performance and scalability of flash memory, high-k materials are employed to substitute oxide layer of interpoly dielectric stack of FG flash memory or tunnel oxide layer of nitride based CTF and FG flash memory [64, 65]. Novel flash cell structures were proposed by researchers to address the severe short channel effects and scalability of standard FG flash memory. In order to surmount critical reliability challenges in device issues that stem from technology scaling, several exploratory and interesting flash cell structures such as FinFET [16–19, 110] and HCFET [15] are studied. Kwak et al. have reported that HCFET exhibited excellent enhancement in subthreshold swing and off current when compared to planar type NVM cell structure [15]. Thus, this shows that HCFET provides superior short channel effects over planar type NVM cell structure [15]. On the other hand, another type of cell structure, namely, FinFET, is also actively under study for its superior reliability performance [16–19]. Figure 4 shows the TEM cross section of sub-40 nm Bandgap-Engineered (BE) SONOS NVM devices of (a) near planar and (b) FinFET structure [19]. Implementation of FinFET structure in charge storage NVM devices has shown excellent short channel control characteristics and scalability as compared to planar type cell structure [16–19]. Comparing the near planar structure, FinFET structure shows superior resistance to body effect as well as drain induced barrier lowering (DIBL) effect as a result of the capability of gate control [17, 19]. FinFET structure based NVM exhibited superior memory window (MW) based on post P/E cycled V_t distribution data and good feasibility to implement multilevel cell (MLC) which requires stringent control on V_t distribution width [17, 19]. As shown in Figure 5, Lue et al. have reported that novel buried channel FinFET BE-SONOS NVM exhibited excellent P/E endurance characteristics with no significant MW closure or V_t roll up [18]. However, implementation of complex cell geometry

Table 1: Overview of major reliability challenges due to technology scaling of charge storage NVM.

	Reliability challenges due to technology scaling of charge storage NVM	References
1	V_t distribution broadening and shifting due to cell level V_t instability mechanisms, such as charge loss, charge gain, and RTN. These mechanisms exacerbated along technology scaling	[83–96]
2	Neighboring bit interference (disturb phenomenon) that inadvertently alters V_t of neighboring cell while erase/program/read on an other memory cell	[97–99]
3	FG interference to adjacent memory cell of standard FG flash memory	[100]
4	Decrement in tolerable loss of electrons in storage layer due to shrinkage in cell's dimension as shown in Figure 2	[9]
5	Program interference caused by cell-to-cell interference of adjacent word line	[101]
6	Adjacent bit line cell interference due to RTN on 32 nm NAND flash	[102]
7	Limitation on thickness of tunnel oxide layer > 8 nm for FG flash memory to prevent severe defect assisted charge leakage or Flash-SILC	[103–107]
8	Limitation on gate coupling ratio of GCR > 0.6 for control gate to properly regulate the channel for FG flash memory	[106]
9	Edge word line disturb exhibited by FG NAND memories	[108]
10	Variability effect of V_t distribution of nanoscale NAND memories	[109]
11	Cell-to-cell coupling interference ratio was found to be inversely proportional to design rules of 2D memory structure that includes FG and charge trap flash (CTF) structures; as shown in Figure 3, 2D memory structure will hit the design limit for coupling interference ratio of 5 at approximately 16 nm	[8]

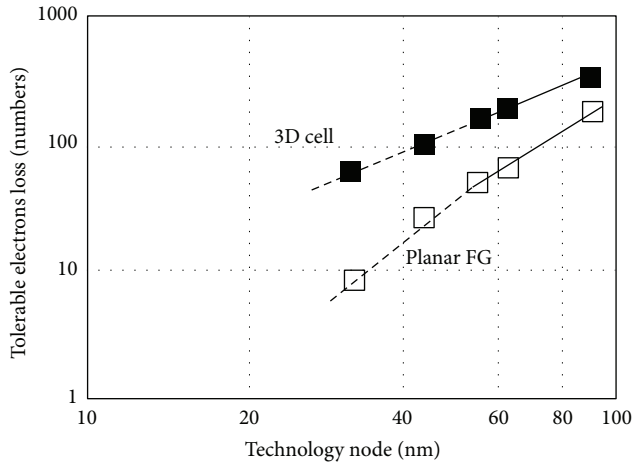


Figure 2: Number of tolerable electrons losses as a function of technology node [9].

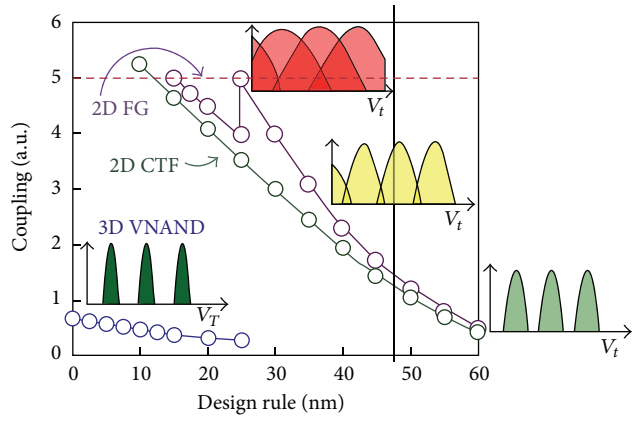
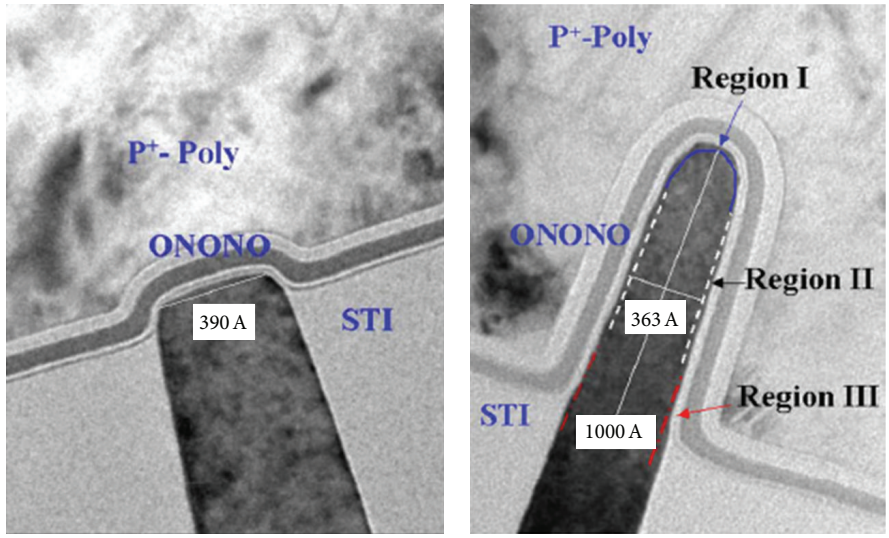
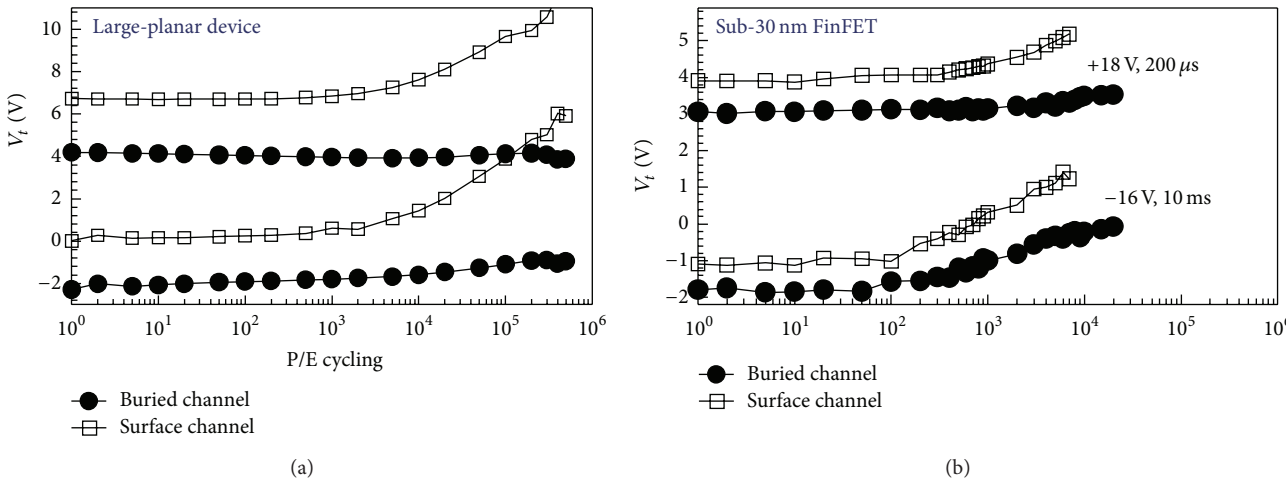


Figure 3: Cell-to-cell coupling interference ratio inversely proportional to design rules of 2D structures [8].



(a) near-planar (b) FinFET

Figure 4: TEM cross section of (a) near-planar, and (b) FinFET structure of sub-40 nm BE-SONOS NVM devices [19].



(a) (b)

Figure 5: Evolution program and erase V_t along increment of program/erase (P/E) cycling for both FinFET and planar structure NVM devices. Buried channel FinFET based NVM device showed superior endurance characteristics as compared to planar structure up to 500 K P/E cycles [18].

of FinFET structure and program/erase optimization faces several hurdles to overcome which requires greater study before FinFET based NVM technology could roll out from the research lab to be ready for production [17–19].

On the other hand, extensive research effort has been put into understanding and developing exploratory NVM technologies such as PCM, MRAM, nanocrystal, and RRAM into mature technology that is ready for production. Among the various exploratory NVM technologies, several NVM technologies such as PCM, MRAM, and RRAM have been thoroughly researched to enable the transition from charge based NVM technology to noncharge based NVM technology. The research on noncharge based NVM technologies heavily concentrated on the innovation in search of new materials to be applied as new charge storage layer. Even though each of these technical mitigation methods are elucidated separately, but research of combinational mitigation methods is carefully studied for the potential improvements in reliability performance [17–19, 47]. In Sections 4, 5, and 6, each of these three mature technical solutions was reviewed in detail, that is, top/bottom nitridation of tunnel oxide, nanocrystal quantum dot memory, and PCM.

4. Tunnel Oxide Nitridation

Tunnel oxide nitridation has long been a topic of great interest as one of the mitigation methods to enhance the reliability of tunnel oxide. This is of great significance for charge storage NVM when there are many reliability issues that arise due to charge traps generated under high electric field of applied FN-tunneling mechanism as summarized in

Table 2: Summary of viable technical solutions to mitigate device characteristic issues of charge storage NVM.

Categories of mitigation techniques	Mitigation techniques	Purposes	References
Tunnel barrier engineering	Tunnel oxide top/bottom nitridation	To enhance endurance and retention performance of tunnel oxide of flash memory	[67–82]
	VARIable Oxide Thickness (VARIOT)	To implement multilayer dielectric stacks with combination of high-k and low-k dielectrics to enhance either endurance speed or retention performance	[60–63]
	Implementation of high-k dielectrics	To replace interpoly ONO dielectric stack of standard FG flash memory or tunnel oxide of CTF with high-k dielectrics to enhance reliability performance, for example, HfO_2, Al_2O_3, and HfAlO	[64, 65]
Novel flash cell structure	Hemi-Cylindrical FET (HCFET)	To reduce severe short channel effect of small dimension beyond sub-40 nm as compared to planar standard FG flash	[4, 15]
	FinFET	Offer better scalability and better short channel effect as compared to planar structure of standard FG flash	[16–19]
Emerging NVM technologies	Phase change memory (PCM)	Utilizes electrical properties of chalcogenide based material to store data. Offers better scalability than standard FG flash with program/erase and retention performance rivals standard FG flash	[21–37]
	Magnetoresistive random access memory (MRAM)	Utilizes the resistance change of Magnetic Tunnel Junction (MTJ) to store data which is determined by the magnetic directions of two electrodes made of ferromagnetic material	[6]
	Nanocrystal	Utilizes mutually isolated quantum dots as charge storage node in control oxide layer to replace conductive FG for further dimension scaling	[38–59, 81, 82]
	Resistive RAM (RRAM)	Relies on the ability to switch to different resistance states by applying sufficient voltage across the structures. RRAM consists of simple oxide or complex oxide or transition metal oxide structures	[6, 66, 110]

Table 1. The incorporation of nitrogen into tunnel oxide of charge storage NVM through many nitridation schemes (as shown in Figure 6) can enhance the reliability performance of tunnel oxide of charge storage NVM [67–80]. Major advantages of tunnel oxide nitridation include (1) increase in immunity towards FNstress that translates to larger memory window (MW); (2) increase in resistance towards V_t instability induced by irradiation of high energy particles, such as gamma rays [81]; and (3) effective barrier to prevent the penetration of boron or any impurities from polysilicon (FG) to tunnel oxide layer [70, 77]. Nonetheless based on the recent published literature, tunnel oxide nitridation induces critical V_t instabilities, for example, quick electron detrapping (QED) and random telegraph signal (RTS) [77, 79].

Based on the published literatures, there are two main nitridation methods, that is, bottom nitridation [67–69, 71–76, 78–80] and top nitridation [70, 77] that will be discussed in this section. Bottom nitridation of tunnel oxide is done by incorporating nitrogen in the oxide located near to the channel of charge storage NVM cell [68, 69, 71–76, 78–80]. This method enhances the endurance characteristics through selective substitution of Si–N bond onto dangling bond of Si–O near to SiO_2/Si interface [68]. However, the incorporation of excess Si–N bonds in bulk oxide increases the probability of defect-related breakdown [68]. As shown in Figure 7(a), V_t shift of various tunnel oxynitrides was plotted as a function of program/erase (P/E) cycle counts [68]. It shows that tunnel oxynitrides exhibit wider memory window (MW) as compared to conventional dry oxide after extensive P/E cycling [68, 76] as shown in Figure 7(b). For this improvement in endurance characteristics on tunnel oxynitrides, Kim et al. attributed this to reduction in electron trapping in high nitrogen concentration oxide [68]. Kim et al. also reported that increment in nitrogen content improves

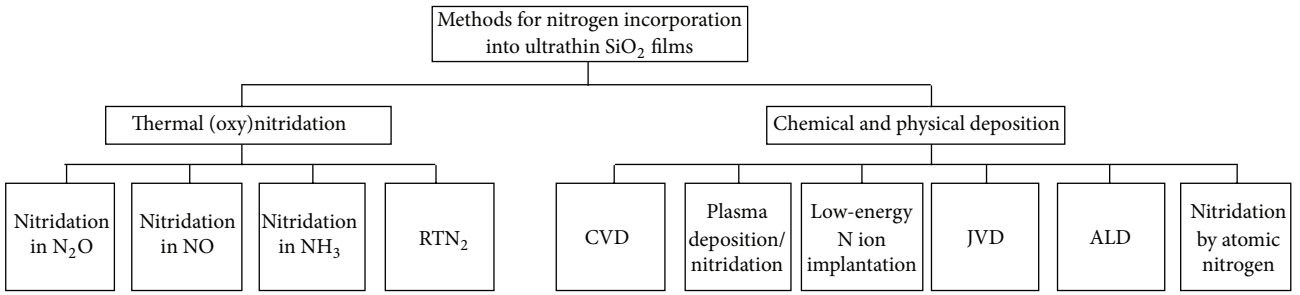


Figure 6: Viable nitridation methods for ultrathin SiO_2 films [67].

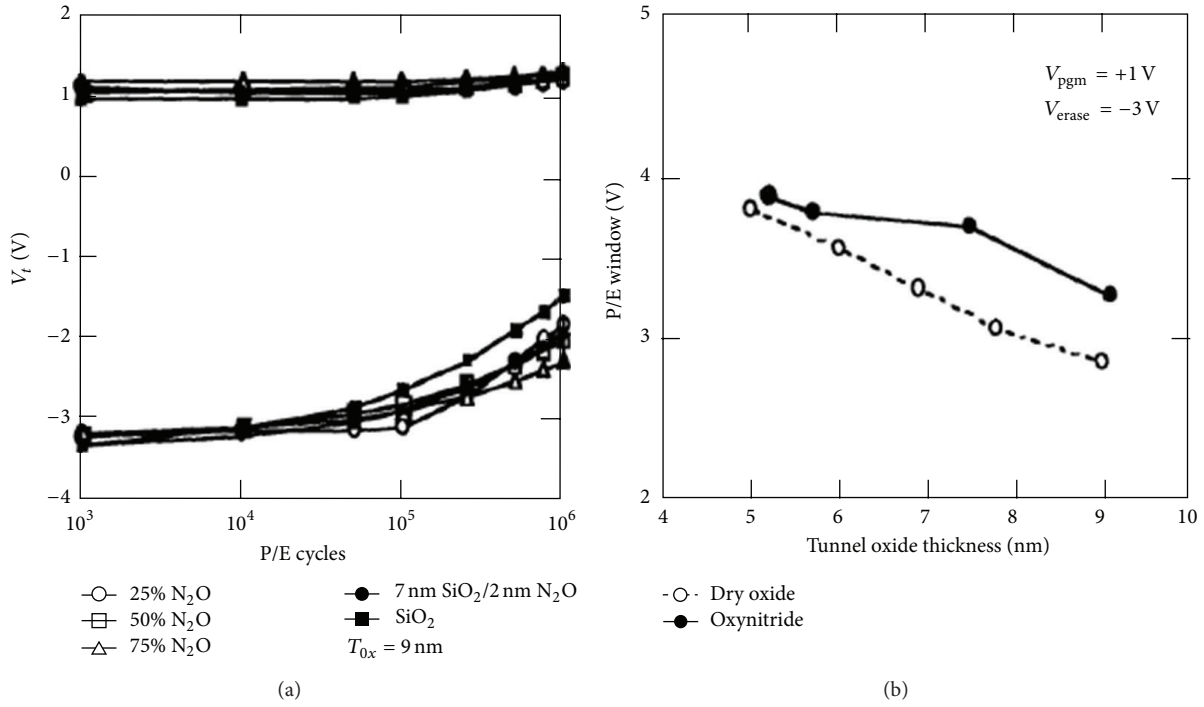


Figure 7: (a) V_t shift of various tunnel oxynitrides as a function of P/E cycle counts [68]; (b) memory window (MW) after 10^6 P/E cycle as a function of tunnel oxide thickness [68].

endurance characteristics and reduces MW closure, but it increases the probability of defectrelated breakdown which may cause retention issue [68, 77, 79, 80]. Lee et al. [80] reported that tunnel oxide nitridation yields large quick electron detrapping (QED) and random telegraph noise (RTN) for fresh device due to increment in defect density through incorporation of nitrogen content in tunnel oxide.

On the other hand, top nitridation of tunnel oxide is typically done by forming a silicon oxynitride (SiON) layer between floating gate (FG) and tunnel oxide [70, 77] through rapid thermal nitridation with ammonia (NH_3) anneal and decoupled plasma nitridation [70, 77]. Similar tradeoff between endurance and retention performance of nitrided charge storage NVM was reported in a recent study [77]. Figure 8(a) shows the normalized ΔV_t of various top nitridation (TN) profile plotted as a function of P/E cycle count [17]. Evidently, it shows that higher nitrogen concentration in TN profile yields larger ΔV_t which means more charges are trapped. Figure 8(b) shows curves of normalized ΔV_t of different TN profile after P/E cycling and after 32 hours bake at 85°C [77]. After bake, normalized ΔV_t slightly reduces for TN-A and TN-B profile, but normalized ΔV_t exacerbates for maximum concentration of TN-C. Based on this intriguing behavior, Kim et al. suggested that TN layer may introduce deep energy traps, and thus, appropriate nitrogen content in TN-A and TN-B profile could cause fewer charges to detrap. However, further increment in nitrogen concentration causes more charges to be trapped due to increase in defect density. The defect generation may surmount the deep energy trap effect and cause higher ΔV_t shift [77]. Kim et al. have attributed the improvement in endurance and retention characteristics of nitrided oxide layer to the substitution of distorted yet stable Si–O bonds in tunnel oxide layer with relatively stronger Si–N bonds to relieve the interface strain [77, 79, 82].

As a summary, the reliability performance of nitrided tunnel oxide depends heavily on the specific nitridation schemes and distribution of nitrogen concentration with

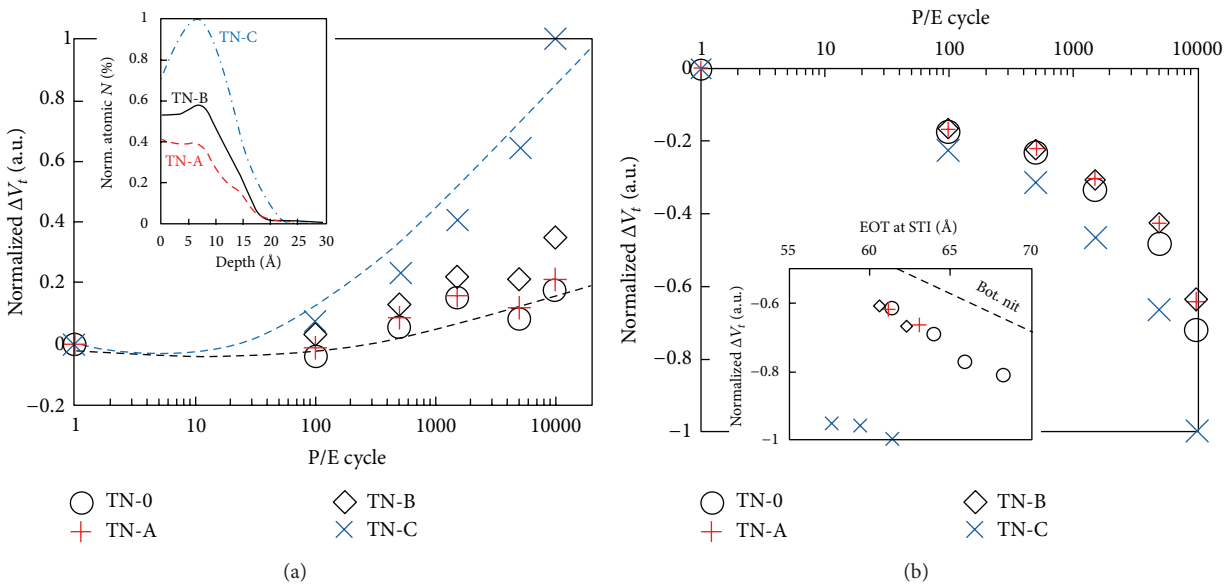


FIGURE 8: (a) Normalized ΔV_t is plotted as a function of P/E cycle for each TN profile. (b) Normalized ΔV_t after bake at each P/E cycle for each top nitridation profile. ΔV_t is normalized by the maximum value of TN-C, and N% is normalized by maximum concentration of TN-C. TN-0 shown in this figure indicates no TN [77].

consideration of the tradeoff between endurance and retention behavior [68–82]. Optimal bottom nitridation on SiO_2/Si interface does enhance endurance performance while fine-tuned top nitridation on FG/SiO_2 can improve retention performance of charge storage NVM. Optimal nitridation process is needed to balance out the tradeoffs and obtain best reliability performance of nitrided NVM devices. The primary advantage of tunnel oxide nitridation is that enhancement in endurance and retention behavior of tunnel oxide can be done by leveraging existing Si material in CMOS compatible fabrication process. This approach yielded cost effectiveness in fabrication. The concern of this approach is that meticulous and precise control in optimal nitridation scheme is required to achieve desired reliability performance of charge storage NVM.

5. Nanocrystal Memory

Discrete silicon nanocrystal NVM was proposed by Tiwari et al. in 1995 [38, 39] as a potential alternative to standard FG flash memory [38–59] as remedy to conflicting requirements of tunnel oxide that stems from incessant technology scaling. To improve program/erase speed and reduce operating voltage, thinner tunnel oxide of FG flash memory is desirable to allow fast and efficient transfer of charges in and out of FG. At the same time, the tunnel oxide isolation between FG and silicon substrate has to be sufficient to meet data retention criterion of 10 years typical for industrial applications. Thus with discrete nanocrystal NVM as alternative, scaling of tunnel dielectric is feasible to achieve lower operating voltage, faster program/erase/read speed, and desirable charge retention time. As comprehensively reported by Chang et al. in [40], the most common techniques to form nanocrystals as quantum storage dots are self-assembly, precipitation, and chemical reaction. Among these three techniques, precipitation and chemical reaction are found to be more robust in controlling the size and density of nanocrystals [40].

As shown in Figure 9, silicon nanocrystal NVM replaces conductive polysilicon floating gate charge storage layer of standard flash memory with discrete and mutually isolated charge storage nodes in silicon nanocrystals distributed in control oxide layer [38–41]. Each nanocrystal or "dot" stores few electrons in the control oxide layer, and collectively, these charges will modulate the channel conduction of each memory cell. Due to the nature of distributed discrete charge storage, nanocrystal NVM exhibits excellent inherent immunity towards defects assisted charge leakage through defects in tunnel oxide that critically limits the scaling of tunnel oxide below 8 nm for standard FG flash memory [103–107]. Thus, tunnel oxide of silicon nanocrystal can be further scaled down below 8 nm with consideration for the tradeoff between operating voltage, speed, and charge retention time.

The recent published literature have shown popular trend in implementing combinations of technical mitigation methods as illustrated in Table 2 to better achieve program/erase characteristics and enhance retention performance in the form of larger memory window (MW). As reported by Qian et al., nitridation was performed on silicon nanocrystals as shown in Figure 10 [47]. This approach yielded larger MW, faster programming speed, and improved retention performance [47]. Typical quantum dots used in nanocrystal NVM are based on silicon material, but metal nanocrystals, that is, germanium, Au, Gd_2O_3, and other refractory metals, are also proposed and researched [40, 47, 56–58]. For better endurance and retention performance as compared to conventional silicon nanocrystal NVM, Kim et al. reported that SiGe dots with HfO_2 as tunnel dielectric exhibited desirable balance of low voltage operations and

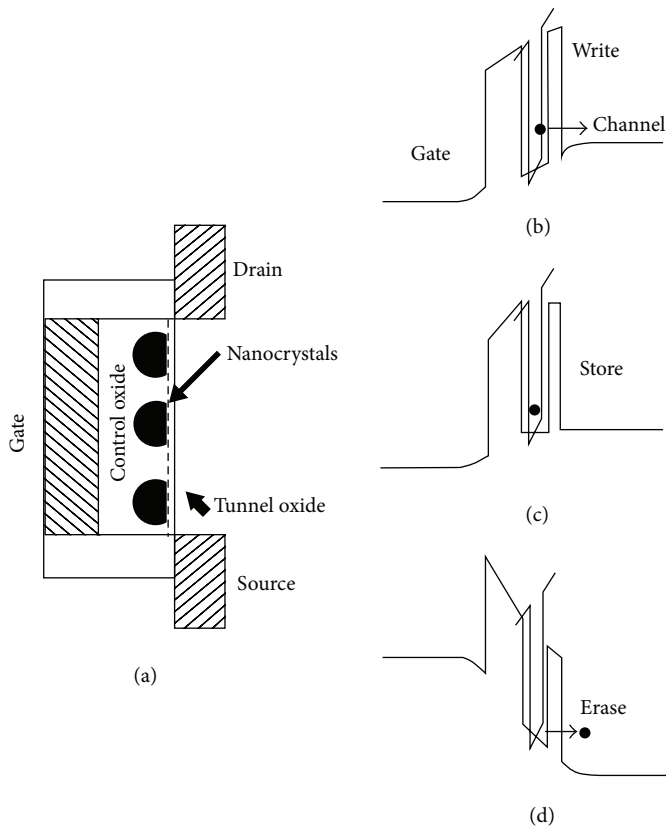


FIGURE 9: (a) Schematic cross section of silicon nanocrystal NVM; (b) band diagram during charge injection through program operation; (c) band diagram during charge retention; (d) band diagram during charge removal through erase operation [38, 39].

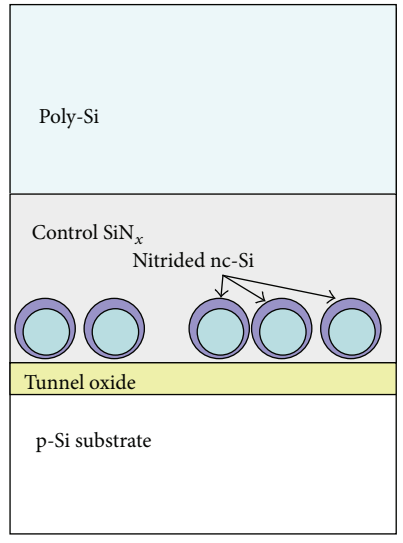


FIGURE 10: Nitridation was performed onto silicon nanocrystals that reside in silicon nitride layer to further enhance its reliability performance [47].

good endurance/retention performance as compared to SiGe dots with conventional SiO_2 as tunnel dielectric [47]. On the other hand, Wang et al. reported the use of Au and Gd_2O_3 nanocrystals based NVM which exhibited ultrafast program/erase characteristics, disturb-free behavior and multilevel cells capability [58]. For typical multilevel cells, disturb-free behavior is critical to clearly distinguish V_t levels of all bits in the same NVM cell. As shown in Figure 11, Lin and Chien reported that HfO_2 based nanocrystals NVM exhibited better P/E characteristics and retention

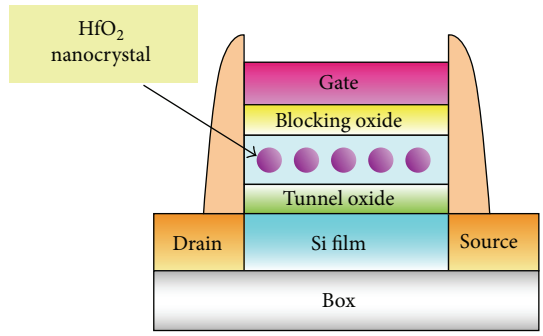


Figure 11: Novel HfO_2 based nanocrystal NVM proposed to achieve enhanced P/E characteristics and retention performance as compared to FG based NVM devices [56].

performance as compared to conventional FG based NVM [56]. However due to the complexity process implementing these proposed novel combinational approaches, manufacturability of these nanocrystals NVM devices in production environment is still a huge challenge to overcome.

Uniform charge injection mechanisms were used to transport charges into and out from nanocrystals, such as direct tunneling [38–41]. Band diagrams during charge injection, retention and removal are shown in Figures 9(b), 9(c), and 9(d), respectively [38, 39]. The dynamics of charge transport and retention mainly depend on quantum confinement effect and coulomb blockade effect [38, 39, 43]. When an electron is injected and retained in nanocrystal, the nanocrystal is charged up by $q^2/2C_{tt}$ with C_{tt} representing the nanocrystal capacitance that depends on its size, thickness of tunnel oxide, and thickness of control oxide layer [38, 39, 43]. The charged-up nanocrystal will hence reduces the electric field across the tunnel oxide which then reduces the tunneling current density during program operation [43]. She and King reported that this coulomb blockade effect has its pros and cons [43]. The salient advantage of this coulomb blockade effect is its effectiveness to impede electrons to tunnel through at low electric field (low gate voltage), and this effectively enhances the immunity of nanocrystal NVM towards flash memory disturb [43]. However, coulomb blockade effect negatively impacts programming speed and retention time [43]. To improve programming speed, larger nanocrystals are desirable to achieve fast and high tunneling current during programming operation. Since the nanocrystals are charged up after programming operation, there is significant tendency for the electrons in the nanocrystals to tunnel back to channel. She and King also reported that quantum confinement energy becomes significant because the dimensions of nanocrystals are in nanometer range [43]. Thus, this causes the conduction band of nanocrystal to shift upwards while the conduction band offset between nanocrystal and surrounding control oxide layer reduces [43]. Careful considerations of coulomb blockade effect, quantum confinement effect, and typical 10 years data retention requirement are required to determine the size and density of nanocrystals and the thickness of tunnel oxide. Furthermore, based on TCAD simulations done on nanocrystals, Gasperin et al. reported that width, number, size, and positions of nanocrystals can impact the charge localizations of nanocrystal memory cells which then impact the program window in subthreshold as well as linear region [54].

As compared to conventional charge storage NVM, for example, standard FG flash memory and nitride based CTF NVM, there are two potential leakage paths, that is, vertical leakage path through intrinsic direct tunneling (DT) and extrinsic defect assisted tunneling of SILC as shown in Figure 12. Based on comprehensive modeling work done by Monzio Compagnoni et al. in [53], retention time was modeled and calculated as a function of nanocrystal spacing. As shown in Figure 13, direct tunneling (DT) becomes dominant discharge mechanism for large a_D while LT dominates at smaller a_D region below t_1. Monzio Compagnoni et al. reported that minimum a_D of 3.7 nm is sufficient to fulfill 10 years data retention requirement [53]. Therefore, larger spacing between nanocrystals is able to effectively suppress lateral tunneling and improves data retention performance [42, 49, 53]. For nanocrystals with typical diameter of 6 nm and density of $N_D = 3 \times 10^{11}$ cm^{-2}, Monzio Compagnoni et al. reported that minimum tunnel oxide thickness of 4.2 nm is required to fulfill 10 years data retention requirement [45, 53]. As a summary, Tables 3(a) and 3(b) summarize the salient advantages and critical challenges of typical nanocrystal NVM as compared to standard FG flash memory with the corresponding literature references.

6. Phase Change Memory (PCM)

Phase change memory (PCM) or also known as ovonic unified memory is one of the promising emerging NVM that has been developed for the past 10 to 15 years and made it into production. Furthermore, PCM emerges as one of the mature mitigation alternatives to conventional charge storage NVM. PCM primarily depends on the characteristic of chalcogenide material to switch to amorphous or crystalline phases through heat controlled by amplitude and timing of electric pulses in a typical PCM memory array [23]. The most common chalcogenide material used in PCM is $Ge_2Sb_2Te_5$ (GST) material. In PCM terminology, if GST switches to amorphous state which yielded high resistance, the PCM cell is in reset state. On the other hand, if GST switches to crystalline state which yielded low resistance, the PCM cell

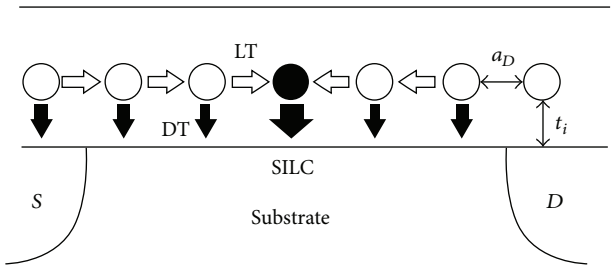


FIGURE 12: Schematic diagram of vertical leakage path (through direct tunneling (DT) and SILC) and lateral tunneling (LT). a_D is the lateral spacing between each nanocrystal. t_1 is the tunnel oxide thickness [45].

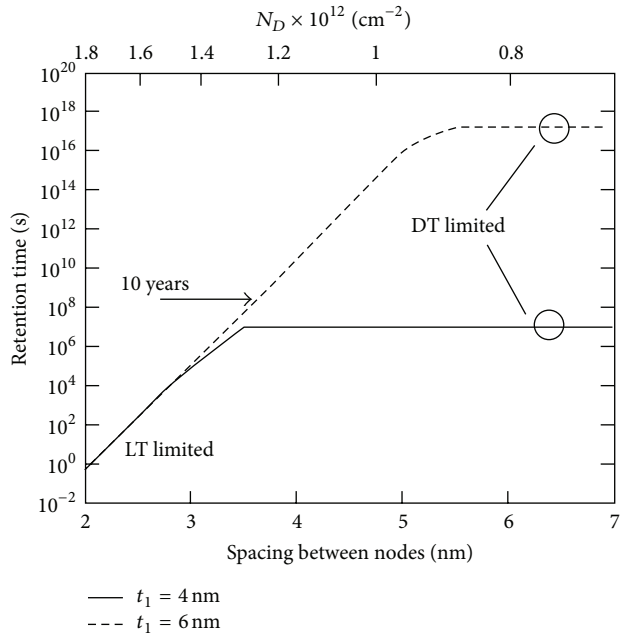


FIGURE 13: Calculated retention time as a function of spacing between nanocrystals, a_D with density of nanocrystals set at $N_D = 1.2 \times 10^{12}$ cm^{-2} [45].

is in set state. The difference between set and reset states of chalcogenide material is the atomic order and electron trap density that yielded several order differences in low field resistance [21, 22].

Figure 14(a) shows typical schematic cross section of PCM cell [21]. PCM consists of top/bottom contact, GST layer with "mushroom" shape active region and resistor that acts as "heater" to heat up the active region of GST layer. Figure 14(b) illustrates the electrical current pulse shapes issued during set/reset/read operations [56]. During reset operation, a huge electrical current pulse for a short period of time is issued to melt the active region and convert it from crystalline phase to amorphous phase. On the other hand, during set operation, a moderate electrical current pulse was issued for a sufficient time period to heat up the active region to a distinct temperature between melting and crystalline temperature. This distinct temperature is used to convert the active region of GST material from amorphous phase to crystalline phase. The read operation is done by issuing a small electrical current pulse to measure out the resistance of the PCM cell. The voltage drop across the cell should be lower than the threshold voltage of PCM cell to inhibit destructive read operation that may alter the data content [21, 22].

Figure 15 shows the current-voltage (I-V) measurement of PCM cell in amorphous and crystalline states during read/set/reset operations [21]. Threshold voltage (V_t) represents the condition in which the conductivity in amorphous phase changes from high resistance state (or off state) to low resistance state (or dynamic on state) [21, 25]. Below V_t indicated in Figure 15, the resistance of amorphous state is much higher as compared to crystalline state. The amorphous state exhibits electronic threshold voltage switch effect that reduces the resistance of amorphous state to be comparable to crystalline state. This enables set operation to be carried out successfully. Figure 15 also indicates that reset operation of typical PCM cell consumes the most power to melt the active region of GST material. Set operation is the key limit for operating speed of PCM as shown in Figure 14(b).

PCM is one of the production-ready emerging NVM technologies with potential capability of multilevel cell operation as shown in the recent literature. The main attractiveness of PCM is its scalability to sub-20 nm, and recent study

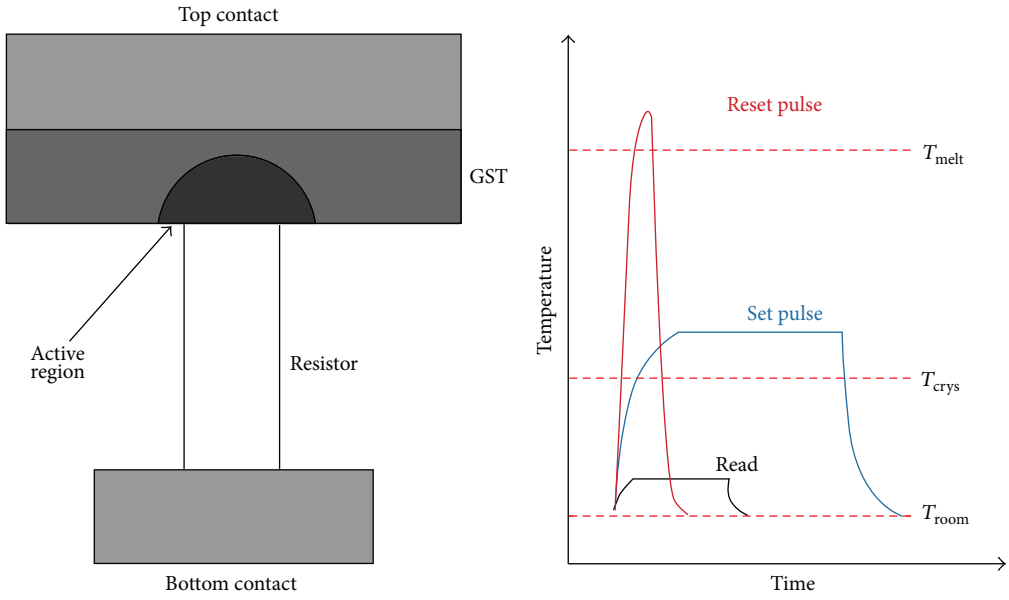


FIGURE 14: (a) Schematic cross section of PCM cell [21]; (b) schematic of set/reset/read pulse shapes of typical PCM [21].

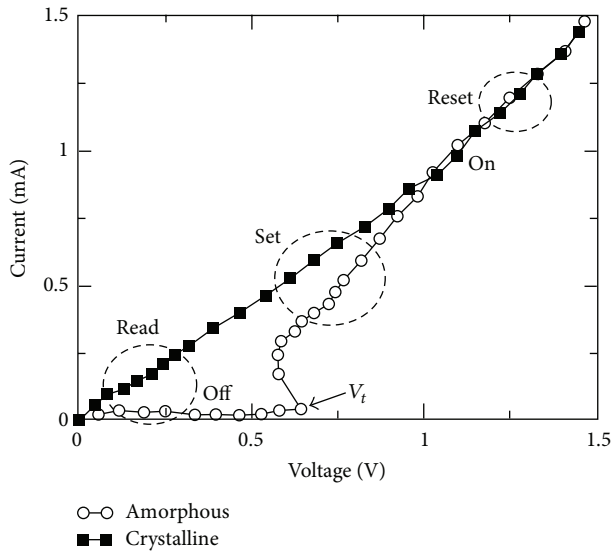


FIGURE 15: I-V measurement of PCM cell in amorphous and crystalline phases [21].

has shown that no significant intrinsic retention issue was found on 10 nm technology node [37]. With direct write technology, PCM does not require any erase operation prior to writing data into the memory cell which is similar to DRAM. Fast read/write at low write/read operating voltage coupled with good data retention and superior endurance performance as compared to standard FG flash memory make PCM very attractive in semiconductor industry. Since PCM is chalcogenide based, studies have reported that PCM is immune to charge based radiation effects which is a genuine reliability concern for charge storage NVM. Table 4 summarizes the key attributes of PCM.

Table 5 summarizes recent research findings on reliability issues of PCM. Based on comprehensive work done by Bae et al., physical origins of endurance failures were investigated. There are three types of endurance failures as reported by Bae et al., that is, stuck reset, stuck set, and tail bits with low resistance originating from reset distribution due to composition changes of GST film in active region [29]. Another key challenge of PCM is to ensure that sufficient thermal isolation is placed on the adjacent cells during reset operations to inhibit thermal disturbance effect [27, 28]. Increase in temperature due to thermal disturbance causes reduction in V_t drift and reset resistance [27, 28]. Similar to discrete charge storage NVM, current fluctuations in PCM are impacted by RTN effect [24]. Fugazza et al. have reported that RTN effect on PCM originates from the fluctuation traps located within the amorphous GST material [24]. Since

Table 3: (a) Key advantages of nanocrystal NVM as compared to standard FG flash memory. (b) Critical challenges of nanocrystal NVM.

(a)

	Key advantages of nanocrystal NVM	References
1	Excellent inherent immunity to trap assisted tunneling of SILC through defects in tunnel oxide	[38–43]
2	Tunnel oxide thickness can be further scaled down below 8 nm (critical limitation for standard FG flash memory)	[41–53]
3	Low operating voltage, fast write and erase speed	[38, 39, 41–44]
4	Multiple bit storage	[51, 58]
5	Eliminate floating gate interference especially for ultradense NAND flash memory	[52]
6	Leverage existing Si material technology and CMOS compatible process	[41–53]
7	Simpler device structure which yielded fewer process steps that further reduce fabrication costs	[40, 52]
8	Superior tolerance to radiation effects as compared to standard FG flash memory	[55, 58]
9	Nitrided silicon nanocrystal NVM has shown larger memory window and faster program speed	[47]

(b)

	Critical challenges of nanocrystal NVM	References
1	Nanocrystals are not fabricated through lithography process; thus variability in fabrication process is critical towards memory properties of nanocrystal NVM	[40–42, 50]
2	Concern on charge leakage through surrounding oxide if thinning of surrounding oxide continues and density of nanocrystals increases	[40, 41, 50, 52–54]
3	Optimal nanocrystal memory performance requires formation of nanocrystals of optimal size and density and preserving them during subsequent processing steps	[40, 41, 43–45, 50, 52, 54]
4	Impact of charge localization of nanocrystals to operating window	[54]

Table 4: Key advantages of PCM.

	Key attributes of PCM	References
1	Scalable to sub-20 nm; new study shows no significant intrinsic retention issue for PCM at 10 nm	[31, 37]
2	Low random access read latency at ~50 ns, fast write performance at ~100 ns, good data retention >10 years, low write and read operating voltage, direct write technology that requires no erase prior to write operation, and good endurance performance at 10^9 cycles	[21, 28–30]
3	As compared to charge storage NVM, chalcogenide based NVM is immune to charge based radiation effects	[35, 36]
4	Multilevel cell operation capability	[34]

Table 5: Key reliability challenges of PCM.

	Reliability challenges of PCM	References
1	Reported endurance failures of PCM are stuck reset of set state (open due to void generated at interface between GST and bottom electrode contact), the stuck set of reset state (small voids spread over the active region that block heat from bottom electrode contact), and tails bit with low resistance from the reset distribution	[29]
2	Thermal disturbance effect on V_t and resistance during reset operation. [21] reported that increase in temperature due to thermal disturbance decreases V_t drift and reset resistance	[27, 28]
3	RTN effect found on PCM. Dependency of current fluctuation on programmed resistance was confirmed through experimental work and numerical model	[24]
4	Structural relaxation (SR) effect induce V_t shift as a function of annealing time. This indicates the data stability depends on the SR effect for amorphous phase of PCM	[25, 26]

PCM relies on resistance contrast between amorphous and crystalline phases of chalcogenide material, data stability of PCM was reported to depend on structural relaxation process that yielded temperature accelerated time evolution of electrical properties of active region of chalcogenide material. Based on extensive work done by Ielmini et al. and Lavizzari et al., reliability of PCM is mainly attributed to the metastable nature of amorphous phase that can be impacted by structural relaxation process [25, 28]. As a summary, PCM is an excellent mitigation alternative to charge storage NVM that faces imminent steep reliability challenges due to further technological scaling per Moore's law. Key advantages

of PCM are its superior endurance/retention performance, better scalability without significant reliability issues, and immunity towards extrinsic irradiation effects.

7. Conclusion

In order to quench the insatiable demand for bigger storage space with lower cost per bit, the persistent effort of technology scaling of memory cell dimension has been driven by Moore's law. However, technology scaling of memory cell dimension alone is not able to surmount the challenges faced by charge storage NVM, especially on device characteristic issues. Further technology scaling is recommended to be complemented with innovative mitigation techniques. In this paper, critical reliability challenges of charge storage NVM with emphasis on device characteristic issues have been reviewed. Overall technical mitigation approaches to overcome fundamental device characteristic issues of charge storage NVM have been discussed. Key advantages and reliability challenges of tunnel oxide nitridation, nanocrystal based NVM, and PCM have been carefully reviewed in this paper. These three mitigation approaches are topics of great interest among researchers to extend the dominance of flash memory in semiconductor NVM industry.

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