Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2014, Article ID 342478, 9 pages
http://dx.doi.org/10.1155/2014/342478

Research Article

Improving the Microstructure and Electrical Properties of Aluminum Induced Polysilicon Thin Films Using Silicon Nitride Capping Layer

Min-Hang Weng,[1] Cheng-Tang Pan,[2] Chien-Wei Huang,[2] and Ru-Yuan Yang[3]

[1] *Medical Devices and Opto-Electronics Equipment Department, Metal Industry Research and Development Center, Kaohsiung City 821, Taiwan*
[2] *Department of Mechanical & Electromechanical Engineering, National Sun Yat-sen University, Kaohsiung 804, Taiwan*
[3] *Graduate Institute of Materials Engineering, National Pingtung University of Science and Technology, Pingtung 912, Taiwan*

Correspondence should be addressed to Ru-Yuan Yang; ryyang@mail.npust.edu.tw

Received 23 January 2014; Accepted 30 May 2014; Published 26 June 2014

Academic Editor: Alireza Talebitaher

We investigated the capping layer effect of SiN_x (silicon nitride) on the microstructure, electrical, and optical properties of poly-Si (polycrystalline silicon) prepared by aluminum induced crystallization (AIC). The primary multilayer structure comprised Al (30 nm)/SiN_x (20 nm)/a-Si (amorphous silicon) layer (100 nm)/ITO coated glass and was then annealed in a low annealing temperature of 350°C with different annealing times, 15, 30, 45, and 60 min. The crystallization properties were analyzed and verified by X-ray diffraction (XRD) and Raman spectra. The grain growth was analyzed via optical microscope (OM) and scanning electron microscopy (SEM). The improved electrical properties such as Hall mobility, resistivity, and dark conductivity were investigated by using Hall and current-voltage (I-V) measurements. The results show that the amorphous silicon film has been effectively induced even at a low temperature of 350°C and a short annealing time of 15 min and indicate that the SiN_x capping layer can improve the grain growth and reduce the metal content in the induced poly-Si film. It is found that the large grain size is over 20 μm and the carrier mobility values are over 80 cm^2/V-s.

1. Introduction

Recently, polycrystalline silicon (poly-Si) films fabricated on glass or plastic substrates have attracted much attention because of their applications in optic-electrical devices such as thin-film transistors (TFTs) [1], sensors, thin film solar cells, and active matrix organic light-emitting diode (AMOLED). The reason is that the mobility of the polycrystalline silicon (poly-Si) thin film is 10 to 100 times greater than that of the amorphous silicon (a-Si) thin film which has the mobility value less than 1 cm^2/V-s [2]. Conventional solid phase crystallization (SPC) of a-Si thin film needs a relatively high process temperature larger than 800°C and a long processing time. However, the average grain size of poly-Si was small in the range of 1-2 um and a poor crystal quality was obtained through SPC method [3]. A low-temperature polysilicon (LTPS) is the polycrystalline silicon film formed by subsequent low-temperature crystallization of amorphous silicon (a-Si). Usually, there are two common methods for fabrication of LTPS film such as excimer laser annealing (ELA) [4] and metal induced crystallization (MIC) [5–21]. The ELA method is currently used as a low-temperature manufacturing approach; however it needs expensive equipment to be implemented.

Generally, MIC method is studied for the fabrication of the LTPS film. Many different metals can be used, such as Pd [5], Au [6], and Al [7–19]. The aluminum induced crystallization (AIC) fabrication is one of the MIC methods with the advantages of a low annealing temperature less than 577°C [7–10] and large grain sizes [11–13]. However, since the reaction of the Al and a-Si is fast, residual Al metal in the induced poly-Si film as the traps results in a decrease in carrier mobility. Moreover, it is difficult to control the

distribution of the residual Al metal so that the grain size during the grain growth is abnormal [7, 8]. However, the performance of devices fabricated on poly-crystalline silicon strongly depends on grain size because grain boundaries also usually act as traps and recombination centers for carriers [7].

It was reported that the use of capping layer could control the lateral growth of poly-Si through lateral thermal gradients. Formerly, there were different patterned capping layers such as SiO_2, SiN_x, and metal capping layers [14] used on the a-Si to reduce metal contamination and obtain a clean and smooth surface [15]. For example, Choi et al. demonstrated a Ni-induced crystallization of a-Si through a SiN_x capping layer [14] annealed in a rapid thermal annealing system. However, the properties of the LTPS using AIC with the capping layer have not been reported. Additionally, SiN_x usually acts as an antireflection layer in solar cell device and then a metal layer such as Ag or Al is deposited on the antireflection layer (SiN_x). After firing, the metal such as Ag or Al will diffuse through SiN_x layer to react with Si to form an ohmic contact. Therefore, we expected that the Al film is deposited on the capping layer and diffuses through the capping layer to form the seeds in a-Si thin film for crystallization. In this paper, we investigated the capping layer (silicon nitride, SiN_x) effect on the microstructure, electrical, and optical properties of poly-Si prepared by the AIC method.

2. Experiment

Hydrogenated amorphous silicon (a-Si:H) and SiN_x layers were sequentially deposited on indium tin oxide (ITO) coated glass by plasma-enhanced chemical vapor deposition (PECVD) equipment. Figure 1(a) shows the experimental procedure of this study for poly-Si thin films using AIC with the capping layer. The thickness of a-Si:H was 100 nm and the deposition parameters for the RF power, chamber pressure, substrate temperature, N_2, and SiH_4 flow rates were controlled at 100 W, 300 mTorr, 350°C, 1140 sccm, and 30 sccm, respectively. The thickness of SiN_x layer was 20 nm and the deposition parameters for the RF power, chamber pressure, substrate temperature, NH_3, N_2, and SiH_4 flow rate were controlled at 20 W, 300 mTorr, 350°C, 30 sccm, 450 sccm, and 25 sccm, respectively. Then, 30 nm thick aluminum film was deposited on the SiN_x layer using sputter system and the parameters for the DC power, chamber pressure, substrate temperature, and Ar flow rate were controlled at 1000 W, 2×10^{-6} Torr, 25°C, and 5 sccm, respectively. When the aluminum deposition process was finished, the specimen was cut into small pieces and annealed at 350°C for 15, 30, 45, and 60 minutes in an N_2 atmosphere. After annealing, the Al layer was first removed using wet selective etching solution and the etchants consist of phosphoric acid, nitric acid, and acetic acid. The SiN_x layer was then removed in the reactive ion etch (RIE) system. The expected transformation procedure for AIC of a-Si:H films on the ITO coated glass substrate is shown in Figure 1(b).

The prepared samples were analyzed for evaluating the influence of AIC process with capping layer. The crystallinity and morphology characteristics were analyzed by using X-ray diffraction (XRD, machine type: Bruker D8 Advance) and Raman (machine type: Horiba HR80) analysis. Optical microscopy (OM, machine type: Olympus BX-51) and scanning electron microscope (SEM, machine type: Jeol-6700) were used to observe the morphology of the film surface. Hall measurement (machine type: Ecopia HMS-3000), four-point measurement (machine type: Jandel HM21), and current-voltage measurement (I-V, machine type: HP4145B) were used to observe the electrical properties of the prepared samples. UV-Vis spectrometer (machine type: Thermo Evolution-300) was used to measure the reflection and absorption coefficient of the prepared samples in the wavelength range of 200–400 nm.

Table 1: The crystalline size and crystallinity of the poly-Si thin films using AIC with the capping layer for different annealing time.

	Time (min)			
	15	30	45	60
Crystallinity size (D, nm)	13.1	17.8	19.8	20.8
Crystallinity (X_c, %)	72	74	74	73

3. Results and Discussion

3.1. Crystallite Structure. XRD analysis was performed on these induced samples in order to confirm if the samples are crystallized silicon after annealing and etching of Al and SiN_x. Figure 2 illustrates the XRD of the poly-Si thin films using AIC with capping layer on the ITO coated glass substrate with the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min. The highest peaks were around $2\theta = 28.5^\circ$ and correspond to Si (111) which indicates that the crystallization of a-Si:H is obtained in the AIC specimens even for the low annealing temperature of 350°C with annealing time of 15, 30, 45, and 60 min, respectively. In addition, the peak of Si (220) is enhanced for the long annealing time, indicating that the well crystallization can be obtained in the longer annealing time. The crystalline size is calculated by the Scherrer equation [16]:

$$D = \frac{K\lambda}{\Delta(2\theta)\cos\theta}. \quad (1)$$

D is crystalline size, K is constant, λ is X-ray wavelength, $\Delta(2\theta)$ is full width at half maximum (FWHM), and θ is diffraction angle. The crystalline sizes were 13.1, 17.8, 19.8, and 20.8 nm, as shown in Table 1, for the poly-Si thin films with the annealing time of 15, 30, 45, and 60 min, respectively.

Figure 3 illustrates the Raman spectra of the poly-Si thin films using AIC with the capping layer annealed at a low temperature of 350°C with the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min. It is known that the Raman spectra of the amorphous silicon, polycrystalline silicon, and single crystal silicon are located around 480 cm^{-1}, 500~515 cm^{-1}, and 520 cm^{-1}, respectively [8]. The Raman spectra of the prepared poly-Si thin films with different annealing time all appeared around 510 cm^{-1} to the 520 cm^{-1}, indicating that the amorphous thin films on the ITO coated glass substrate have been induced successfully at a low temperature of 350°C even at a short annealing time of 15 min.

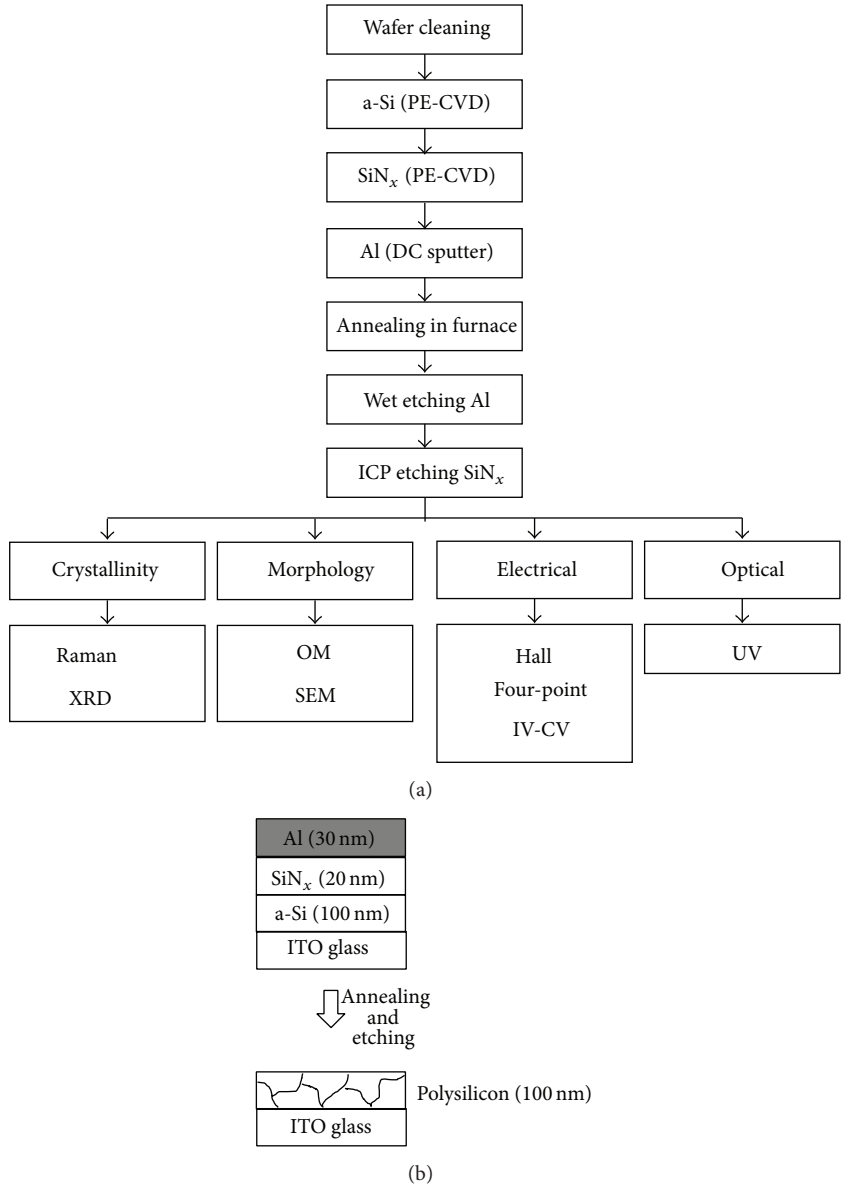


Figure 1: (a) The experimental procedure of this study for poly-Si thin films using AIC with the capping layer and (b) transformation procedure for aluminum induced crystallization of a-Si:H films on the ITO coated glass substrate.

To further calculate the crystallinity fraction of the induced samples for different annealing time, the curve fitting of the Raman spectra shall be used as shown in Figure 4. The Raman spectra can be divided into three spectra regions for amorphous silicon, polycrystalline silicon, and single crystal silicon. The crystallinity fraction X_c of the induced samples for the different annealing time is calculated by (2), and the meaning of I_a, I_m, and I_c is the intensity of Raman shift on 480 cm^{-1}, 500~515 cm^{-1}, and 521 cm^{-1}, respectively [5–7]. Consider

$$X_c = \frac{I_m + I_c}{I_a + I_m + I_c}. \quad (2)$$

Table 1 shows the crystallinity ratios of the induced poly-Si thin films using AIC with the capping layer for different annealing time. It is found that the crystallinity ratios for all films are around 73% and independent of the annealing times. The process parameters of the annealing temperature of 350°C and the annealing time of 15 min are suitable to induce the amorphous silicon film to be poly-Si film in this study. For the solar cell application, the crystallinity ratio of 73% is desired. If one desires more crystallization of silicon thin film, it is suggested that the Al thickness shall be thick or the silicon nitride layer should not be introduced. However, it will cause more residual Al concentration to decrease the grain size and Hall mobility as discussed later [7].

3.2. Surface Morphology. Figure 5 illustrates optical microscope (OM) images of the poly-Si thin films using AIC with

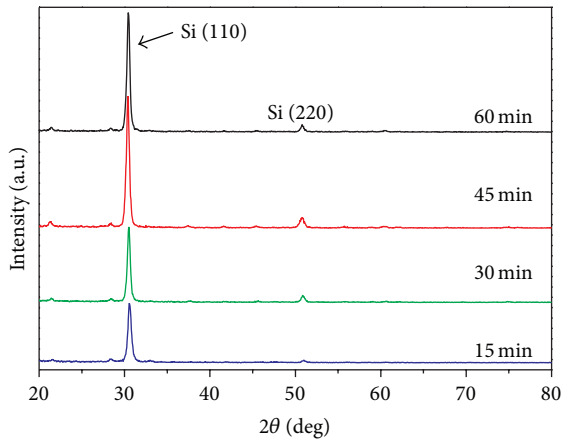


Figure 2: The XRD of the poly-Si thin films using AIC with the capping layer for the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min.

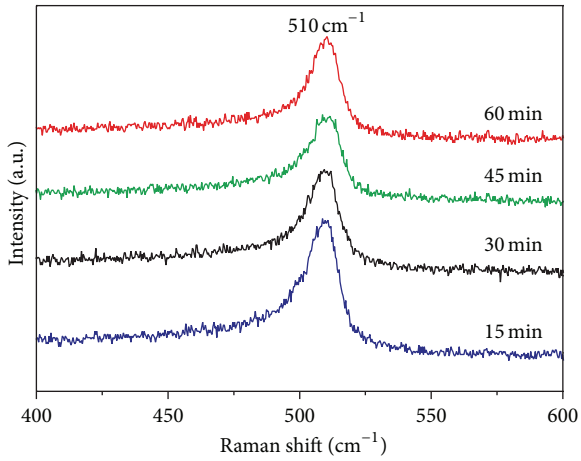


Figure 3: The Raman spectra of the poly-Si thin films using AIC with the capping layer for the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min.

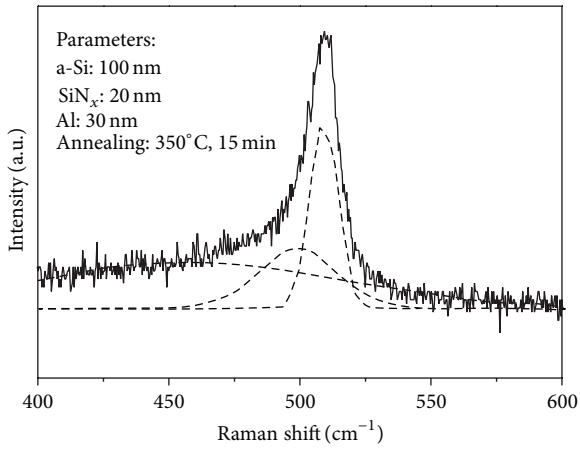


Figure 4: Curve fitting of the Raman spectra for the poly-Si thin films using AIC with the capping layer, wherein the Raman spectra can be divided into three spectra for a-silicon (480 cm^{-1}), polysilicon (500 cm^{-1}) and single-silicon (521 cm^{-1}).

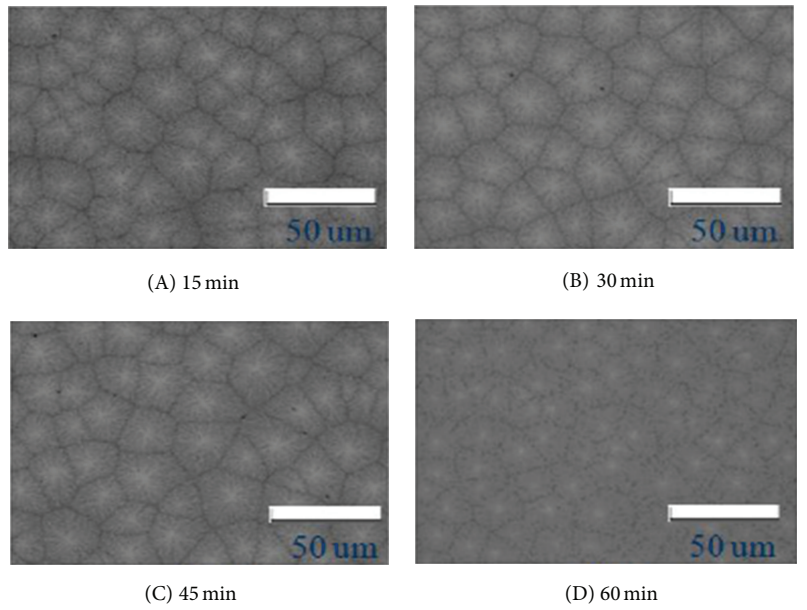
the capping layer for different annealing time. It is clearly observed that the grain sizes are growing when the annealing time increases. In order to show the difference of grain size between the AIC with and without the capping layer, the poly-Si thin films on the ITO coated glass substrate using AIC but without the capping layer for the annealing time of 120 min was also prepared and its OM image was shown in Figure 5(b). The bright spots in each grain of Figure 5(a) are believed to be the nucleation sites [17]. It was reported that the difference in intensity/color between the nucleation center and other portions of a grain is attributable to the difference of refractive index in the two regions of the grain [13]. The average grain sizes $\overline{G}$ of the sample were estimated directly from the OM using the linear intercept method described by the formula [17]:

$$\text{Average grain size}, \overline{G} = 1.56\overline{L}, \tag{3}$$

where $\overline{L}$ is the average grain boundary intercept length of a series of random lines on the OM image. Figure 5(c) shows the variation of average grain size of the poly-Si thin film using AIC specimens. The average grain sizes are around 18.5, 21, 18, and 17.5 μm for the annealing time of 15, 30, 45, and 60 min, respectively. It is also observed that the poly-Si thin film using AIC, but without, the capping layer has the grain size of 6 μm even with the annealing time of 120 min. Namely, the grain size of the poly-Si thin films with the capping layer is three times larger than that without the capping layer. The reason is explained as follows. The Al induced crystallization starts with formation of Si nuclei within the Al layer at the Al/a-Si interface [12]. Then, the Si grains keep growing laterally only until they touch adjacent grains and from a continuous poly-Si film [9]. The capping layer is used in this study to decrease the diffusion rate of Al atoms from Al layer to react with a-Si 9 at the Al/a-Si interface. Therefore, the nucleation sites at the Al/a-Si interface with the capping layer are lower than those without the capping layer, thus enhancing the Si grain to grow laterally.

The result shows that the grain size of the poly-Si thin film induced by AIC is significantly affected by the distance between adjacent nucleation sites. Namely, reducing the density of nucleation sites is a key factor for growing large grains. Thus, using the capping layer of SiN_x between the Al and a-Si thin film actually reduces the density of nucleation sites so as to grow the large grains.

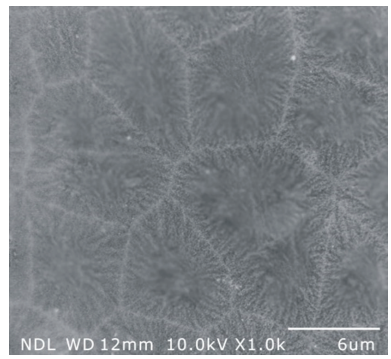
Figure 6 shows SEM images of the poly-Si thin films using AIC with the capping layer for the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min. No cracks were observed by SEM to ensure that grain boundaries observed by optical microscopy are not cracks in the silicon films. Moreover, the subgrains are clearly observed in the SEM images and the subgrains sizes are around 100 nm to 150 nm for the annealing time from 15 to 60 min. The subgrains sizes estimated from the SEM images are larger than the crystal sizes calculated from the XRD results. It is known that the difference between the average crystalline size and subgrain size determined from XRD and SEM data resulted from the fact that the SEM measurement is more sensitive to the surface structure and the XRD data is sensitive to the structure of the film itself [14].



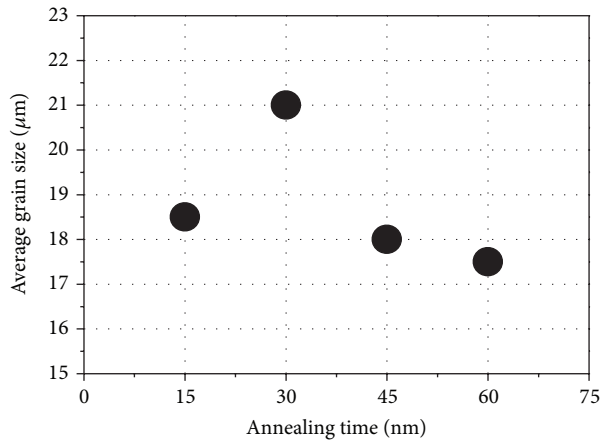
(A) 15 min (B) 30 min

(C) 45 min (D) 60 min

(a)

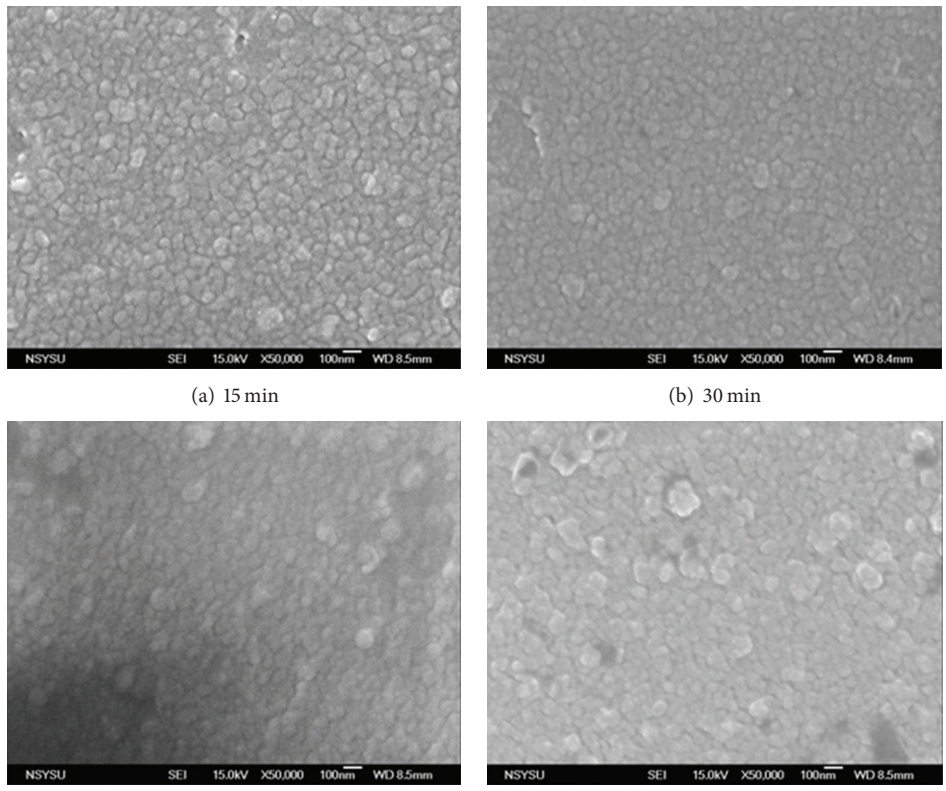


(b)



(c)

Figure 5: OM images of the poly-Si thin films (a) using AIC with the capping layer for the annealing time of 15, 30, 45, and 60 min and (b) using AIC without the capping layer for the annealing time of 120 min; and (c) the variation of average grain sizes of the poly-Si thin films using AIC with the capping layer.



(a) 15 min (b) 30 min

(c) 45 min (d) 60 min

Figure 6: SEM images of the poly-Si thin films using AIC with the capping layer for annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min.

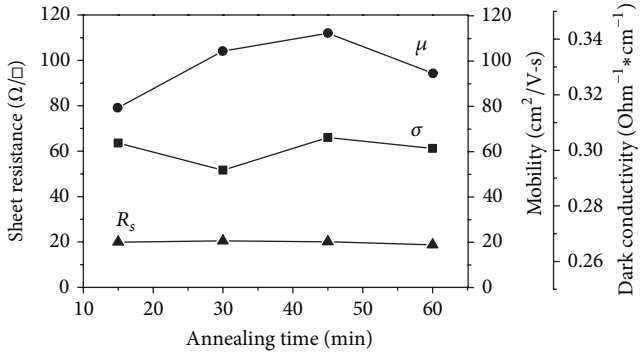


Figure 7: Mobility, dark conductivity, and sheet resistance of the poly-Si thin films using AIC with the capping layer for different annealing time.

3.3. Electrical Properties. Figure 7 shows mobility (μ), dark conductivity (σ_d), and sheet resistance (R_s) of the poly-Si thin films using AIC with the capping layer for the different annealing time. First, the mobility (μ) and sheet resistance (R_s) of the ITO are 35 cm^2/V-s and 15 Ω/squ, respectively. Although the poly-Si thin films using AIC with the capping layer are coated on ITO glass, under this structure, the measured mobility is around 82, 105, 112, and 92 cm^2/V-s, the dark conductivity is within 0.29~0.31 Ω-cm^{-1}, and the sheet resistance is all around 20 Ω/squ for the annealing time is 15, 30, 45, and 60 min, respectively. Table 2 summarizes the electrical properties of the prepared poly-Si thin films using AIC with the capping layer and compared them with those in the previous works using conventional AIC without the capping layer. It is clearly found the electrical properties of poly-Si thin films are much improved by using the proposed method, that is, the AIC with the capping layer. The mobility is much improved due to the increased grain size as compared with the previous work, since a large grain size has a few grain boundaries and thus reduces the scattering effect from the defect of the grain boundary. Since the resistivity (ρ) is reversal to the conductivity (σ) and the resistivity of the prepared poly-Si thin films is calculated within 3.2~3.4 Ω-cm, the values of resistivity indicate that it is also suitable to be used as the semiconductor material.

Moreover, the carrier concentration (n) can be calculated in an order of 10^{16}/cm^3 according to the following equation [7]:

$$\sigma = q\mu n, \tag{4}$$

where q is 1.6×10^{-19} Coul. Thus, the carrier concentration of the induced poly-Si using the proposed AIC with the capping layer is much lower than those of the previous works since the residual Al metal is not easy to be removed in the traditional AIC without the capping layer. According to the Nast et al. study [9], they emphasized that the number of metal concentrations affects the value of mobility in the MIC

Table 2: The electrical properties of the poly-Si thin films using AIC with the capping layer.

	Al (nm)	a-Si (nm)	Substrate	Annealing temperature (°C)	Annealing time (min)	Mobility (μ, cm^2/V-s)	Sheet resistance (Rs, Ω/□)	Grain size (um)
Kim et al. [6]	200	96	Glass	550	10~40	N/A	4500~5000	N/A
Nast et al. [7]	500	500	Glass	350~500	30	60~70	N/A	N/A
Nast et al. [9]	450~500	500	Glass	500	5~60	56.3	820	N/A
Widenborg et al. [19]	250~450		Glass	400	30	N/A	800~4000	N/A
Our results	30	100	ITO Glass	350	15~60	80~112	19~21	17~21

process. In the Sohn et al. study [15], they indicated the low metal concentration of polysilicon in the MIC process with capping layer than without capping layer. However, the film still has the metal content.

When considering the sheet resistance (R_s) of the poly-Si thin films, the typical formula (5) is as follow [6, 7, 19]:

$$R_s = \frac{\rho}{d}, \tag{5}$$

where d is the film thickness. If we use this formula to calculate the sheet resistance (R_s) of the prepared poly-Si thin films, the sheet resistance (R_s) is around 4000~5000 Ω/sq, which is much higher than our measured results, but is very similar to those of the previous works, as shown in Table 2. The reason is explained as follows. The previous works were done on the glass and obtain their sheet resistance (R_s) with the value within 4000~5000 Ω/sq, which is similar to our calculated sheet resistance (R_s). However, the prepared poly-Si thin films are formed on the ITO coated glass, and it is believed that the low resistance of the ITO can reduce the sheet resistance (R_s) of the prepared poly-Si thin films as the results we measured.

3.4. Optical Properties. Figure 8 shows the optical energy gaps of the poly-Si thin films using AIC with the capping layer annealed at a low temperature of 350°C with the annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min using Taucs plot. The optical energy gap (Eg) of the films can be further calculated from the transmission spectra using (6), which assumes a direct transition between the edges of the valence and the conduction band. The relationship between the absorption coefficient α and the photon energy $h\nu$ can be given as in [22]:

$$(\alpha h\nu)^2 = A\left(h\nu - \mathrm{Eg}\right), \tag{6}$$

where α was estimated from the transmittance data, A is a constant depending on the materials properties, and $(\alpha h\nu)^2$ is a function of $h\nu$. By extrapolating $\alpha = 0$ from the linear region of "Tauc" plots, the calculated values of the optical energy gaps for the prepared poly-Si thin films in this study were closed to 1.1 eV.

Figure 9 illustrates the reflection spectra of the poly-Si thin films using AIC with the capping layer for different annealing time. It was reported that for intrinsic monocrystalline silicon, two prominent maxima peaks at the wavelength of 274 nm and 365 nm in the reflectance spectrum

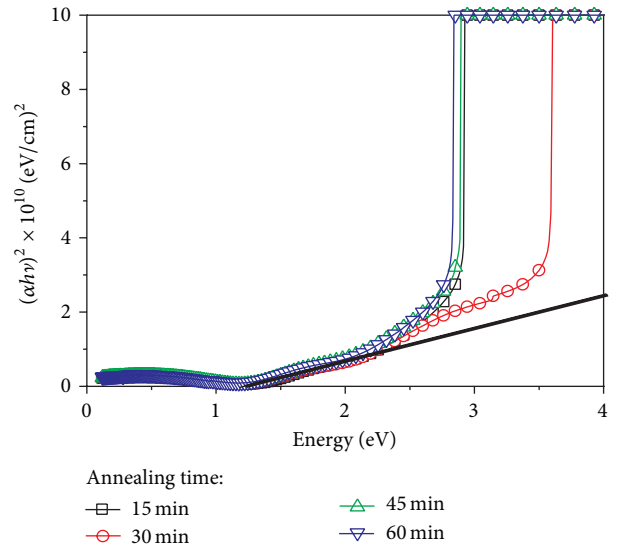


Figure 8: Taucs plots for the poly-Si thin films using AIC with the capping layer for annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min.

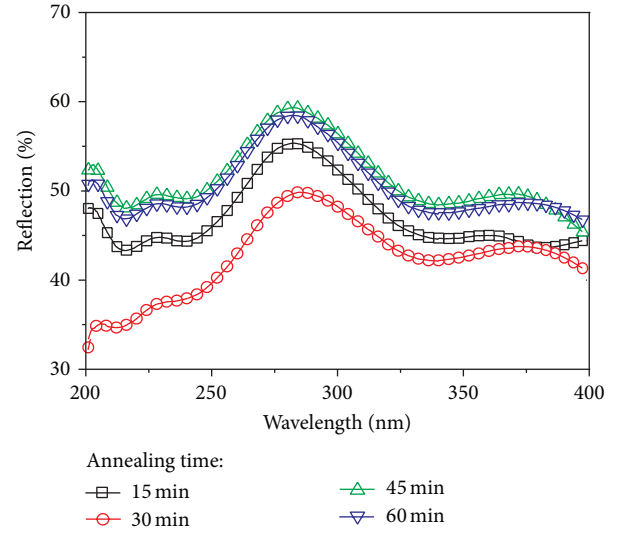


Figure 9: Reflection spectra of the poly-Si thin films using AIC with the capping layer for annealing time of (a) 15, (b) 30, (c) 45, and (d) 60 min.

could be clearly obtained. Moreover, a reduction of ultraviolet reflection usually indicates the appearance of a surface oxide, surface roughness, and/or structurally damaged material [19]. It is found in Figure 5 that the large grain sizes between 17 to 21 μm are obtained so as to reduce the structurally damaged boundaries. However, if structural disorder exists in the surface layer, it will cause a broadening and large reduction predominantly at these maximum peaks. As shown in Figure 2, the well crystallization can be obtained in the long annealing time. Therefore, as shown in Figure 9, it is observed that the measured reflection ratio is within 35~60% and two prominent peaks at the wavelength of 280 nm and 370 nm exist which is similar with that of an intrinsic polished monocrystalline silicon. Namely, the crystal quality of the prepared poly-Si using AIC with the capping layer is acceptable, comparable to a polished Si wafer.

4. Conclusions

In this paper, the microstructure, electrical, and optical properties of poly-Si prepared by aluminum induced crystallization with the capping layer of SiN_x were investigated. The structure comprising Al (30 nm)/SiN_x (20 nm)/a-Si layer (100 nm)/ITO coated glass was annealed at 350°C for the different annealing time of 15, 30, 45, and 60 min. We have verified that the capping layer of the SiN_x can effectively reduce the diffusion rate of Al atoms from Al layer through the Al/a-Si interface and thus improve the grain size and electrical properties such as resistivity, residual carrier concentration of the induced poly-Si film. The results of the crystal plane of the Si (110) from the XRD results and the Raman shift around the 510 cm^{-1} from the Raman spectra confirm that the a-Si thin film has been induced and transferred to be the polysilicon. The high-quality and large grain size poly-Si thin film can be obtained at such low temperature of 350°C. The OM image shows the large grain sizes of the prepared films are around 17 to 21 μm. The values of mobility are 82, 105, 112, and 92 cm^2/V-s, the values of the dark conductivity are within 0.29~0.31 Ω-cm^{-1}, and the values of the sheet resistance are all around 20 Ω/sq for the different annealing time of 15, 30, 45, and 60 min. The carrier concentration (n) can be calculated in an order of $10^{16}/cm^3$. The measured reflection ratio is within 35~60% and two prominent peaks at 280 nm and 370 nm wavelength exist which is similar with that of an intrinsic polished monocrystalline silicon.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to thank the financial support from the Ministry of Science and Technology, Southern Taiwan Science Park Administration (STSPA), and Industrial Development Bureau, Ministry of Economic Affairs, Taiwan under Contracts NSC101-2628-E-020-002-MY3, 102CE04, and 102E2057. The authors would also like to thank the National Nano Device Laboratories and the Precision Instrument Center of the National Pingtung University of Science and Technology for supporting the experimental equipment.

References

[1] S. D. Brotherton, "Polycrystalline silicon thin film transistors," *Semiconductor Science and Technology*, vol. 10, no. 6, pp. 721–738, 1995.

[2] R. Martins, L. Raniero, L. Pereira et al., "Nanostructured silicon and its application to solar cells, position sensors and thin film transistors," *Philosophical Magazine*, vol. 89, no. 28–30, pp. 2699–2721, 2009.

[3] M. S. Haque, H. A. Naseem, and W. D. Brown, "Aluminum-induced degradation and failure mechanisms of a-Si:H solar cells," *Solar Energy Materials and Solar Cells*, vol. 41-42, pp. 543–555, 1996.

[4] L. Mariucci, R. Carluccio, A. Pecora et al., "Lateral growth control in excimer laser crystallized polysilicon," *Thin Solid Films*, vol. 337, no. 1-2, pp. 137–142, 1999.

[5] S.-W. Lee, Y.-C. Jeon, and S.-K. Joo, "Pd induced lateral crystallization of amorphous Si thin films," *Applied Physics Letters*, vol. 66, pp. 1671–1673, 1995.

[6] D. Y. Kim, M. Gowtham, M. S. Shim, and J. Yi, "Polycrystalline silicon thin film made by metal-induced crystallization," *Materials Science in Semiconductor Processing*, vol. 7, no. 4–6, pp. 433–437, 2004.

[7] O. Nast, S. Brehme, D. H. Neuhaus, and S. R. Wenham, "Polycrystalline silicon thin films on glass by aluminum-induced crystallization," *IEEE Transactions on Electron Devices*, vol. 46, no. 10, pp. 2062–2068, 1999.

[8] O. Nast and S. R. Wenham, "Elucidation of the layer exchange mechanism in the formation of polycrystalline silicon by aluminum-induced crystallization," *Journal of Applied Physics*, vol. 88, no. 1, pp. 124–132, 2000.

[9] O. Nast, S. Brehme, S. Pritchard, A. G. Aberle, and S. R. Wenham, "Aluminium-induced crystallisation of silicon on glass for thin-film solar cells," *Solar Energy Materials and Solar Cells*, vol. 65, no. 1, pp. 385–392, 2001.

[10] M. S. Haque, H. A. Naseem, and W. D. Brown, "Interaction of aluminum with hydrogenated amorphous silicon at low temperatures," *Journal of Applied Physics*, vol. 75, no. 8, pp. 3928–3935, 1994.

[11] L. Cai, H. Wang, W. Brown, and M. Zou, "Large grain polycrystalline silicon film produced by nano-aluminum-enhanced crystallization of amorphous silicon," *Electrochemical and Solid-State Letters*, vol. 8, no. 7, pp. G179–G181, 2005.

[12] M. Zou, L. Cai, and W. Brown, "Nano-aluminum-induced low-temperature crystallization of PECVD amorphous silicon," *Electrochemical and Solid-State Letters*, vol. 8, no. 5, pp. G103–G105, 2005.

[13] M. Zou, L. Cai, H. Wang, and W. Brown, "Nano-aluminum-induced crystallization of amorphous silicon," *Materials Letters*, vol. 60, no. 11, pp. 1379–1382, 2006.

[14] J. H. Choi, D. Y. Kim, B. K. Choo, W. S. Sohn, and J. Jang, "Metal induced lateral crystallization of amorphous silicon through a silicon nitride cap layer," *Electrochemical and Solid-State Letters*, vol. 6, no. 1, pp. G16–G18, 2003.

[15] W. S. Sohn, J. H. Choi, K. H. Kim, J. H. Oh, S. S. Kim, and J. Jang, "Crystalline orientation of polycrystalline silicon with

disklike grains produced by silicide-mediated crystallization of amorphous silicon," *Journal of Applied Physics*, vol. 94, no. 7, pp. 4326–4331, 2003.

[16] H.-Y. Chu, M.-H. Weng, R.-Y. Yang, C.-W. Huang, and C.-H. Li, "Effect of Al thickness on the Al induced low temperature poly-Si film crystallization process," in *Proceedings of the 4th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS '09)*, pp. 641–644, Shenzhen, China, January 2009.

[17] M. I. Mendelson, "Average grain size in polycrystalline ceramics," *Journal of the American Ceramic Society*, vol. 52, no. 8, pp. 443–446, 1969.

[18] C. Ornaghi, G. Beaucarne, J. Poortmans, J. Nijs, and R. Mertens, "Aluminum-induced crystallization of amorphous silicon: influence of materials characteristics on the reaction," *Thin Solid Films*, vol. 451-452, pp. 476–480, 2004.

[19] P. I. Widenborg, A. B. Sproul, and A. G. Aberle, "Impurity and defect passivation in poly-Si films fabricated by aluminium-induced crystallisation," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion*, pp. 1233–1236, Osaka, Japan, May 2003.

[20] L. Pereira, H. Águas, R. M. S. Martins, P. Vilarinho, E. Fortunato, and R. Martins, "Polycrystalline silicon obtained by metal induced crystallization using different metals," *Thin Solid Films*, vol. 451-452, pp. 334–339, 2004.

[21] O. Shamiryan, I. Maidanchuk, N. Ahn, I. Choi, and H. K. Chung, "Electrical characterization of thin silicon films produced by metal-induced crystallization on insulating substrates by conductive AFM," *Journal of Surface Analysis*, vol. 17, pp. 260–263, 2011.

[22] Y. G. Wang, S. P. Lau, H. W. Lee et al., "Comprehensive study of ZnO films prepared by filtered cathodic vacuum arc at room temperature," *Journal of Applied Physics*, vol. 94, no. 3, pp. 1597–1604, 2003.