Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2014, Article ID 787132, 6 pages
http://dx.doi.org/10.1155/2014/787132

*Research Article*

# Investigation of Low-Frequency Noise Characterization of 28-nm High-k pMOSFET with Embedded SiGe Source/Drain

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Received 10 December 2013; Revised 19 February 2014; Accepted 20 February 2014; Published 30 March 2014

Academic Editor: Sheng-Po Chang



We have studied the low-frequency noise characterizations in 28-nm high-k (HK) pMOSFET with embedded SiGe source/drain (S/D) through $1/f$ noise and random telegraph noise measurements simultaneously. It is found that uniaxial compressive strain really existed in HK pMOSFET with embedded SiGe S/D. The compressive strain induced the decrease in the tunneling attenuation length reflecting in the oxide trap depth from $Si/SiO_2$ interface to the HK layer, so that the oxide traps at a distance from insulator/semiconductor interface cannot capture carrier in the channel. Consequently, lower $1/f$ noise level in HK pMOSFET with embedded SiGe S/D is observed, thanks to the less carrier fluctuations from trapping/detrapping behaviors. This result represents an intrinsic benefit of HK pMOSFET using embedded SiGe S/D in low-frequency noise characteristics.

## 1. Introduction

Low-frequency noise is an important issue for analog, digital, mixed signal, and RF application. Nowadays, complementary metal-oxide-semiconductor (CMOS) technology has intruded into RF and/or analog circuits, and hence the excessive low-frequency noise will lead to a limitation of the functionality for related circuits [1, 2]. Low-frequency noise, including flicker ($1/f$) noise and random telegraph noise (RTN), is increasingly attracting much interest in the CMOS device and technology community. In metal-oxide-semiconductor field-effect transistor (MOSFET) devices, the origin of $1/f$ noise and RTN is considered stemming from the carrier behaviors related to the oxide traps. $1/f$ noise is most often due to fluctuations in carrier number and/or carrier scattering [3, 4]. RTN is another special kind of noise, which also appears in a low-frequency spectrum and originates from the trapping/detrapping behavior of a single or few traps [5, 6].

On the other hand, the continued shrinking of conventional CMOS to enhance device performance has revealed limitations. The mobility enhancement has emerged as a key technology for improving drive current [7]. Ways of optimizing channel mobility had been proposed to overcome the limitations on the scaling down of devices and to further improve the speed of CMOS circuits. The introduction of channel strain engineering in the state-of-the-art CMOS technology is recognized as an indispensable performance booster in producing next generation CMOS devices [8, 9]. For p-type MOSFET (pMOSFET), using embedded SiGe in the recessed source/drain (S/D) region can efficiently provide uniaxial compressive strain in the channel and

improve hole mobility, bringing the enhancement of device performance [10–12]. In addition, high-k (HK) materials are also adopted into advanced CMOS process for solving the increased gate leakage current. This is because HK dielectrics are the promising candidate for gate insulator to achieve low equivalent oxide thickness as required for the advanced CMOS technology nodes [13]. However, a fabricated pMOSFET with SiGe S/D is possibly accompanied by the extra amount of process-induced defects, and a gate insulator that is replaced from conventional $SiO_2$ to HK materials usually causes the changes of trap properties in MOSFET, resulting in the influence on low-frequency noise characterizations. Though low-frequency noise characterizations in pMOSFET with SiGe S/D had been reported [12, 14], low-frequency noise in HK pMOSFET with SiGe S/D is still unclear and needs to be addressed to improve the understanding. In this study, the low-frequency noise characterizations of HK pMOSFET with embedded SiGe S/D are investigated through $1/f$ noise and RTN measurements simultaneously.

## 2. Experimental

Apart from the S/D engineering, a 28-nm HK first/meta gate last technology was used to prepare the pMOSFET samples for this work. The thickness of the $SiO_2$ interfacial layer was approximately 1.0~1.1 nm. A total of 20 atomic layer deposition cycles for $HfO_2$ were deposited on the top of the $SiO_2$ interfacial layer, and the thickness of all gate stacks was approximately 1.6~1.7 nm. A thin TiN layer was deposited on $HfO_2$ layer as a capping layer for selective removal of the dummy poly-Si gate [15]. After the S/D activation is annealed, the dummy poly-Si gate was removed and then other metals were deposited to tune the work function and achieve the idea value (5.0~5.2) [16]. The strained-Si HK pMOSFET structure features improvement by optimizing S/D recess shape following an epitaxially grown B-doped SiGe film embedded in the S/D regions with about 30% Ge concentration. Finally, the devices were completed with standard backend processes. The HK device without embedded SiGe was also fabricated and called as control device for comparison. The values of oxide capacitance derived from the equivalent oxide thickness of the CVC program [17] are $2.801 \times 10^{-6}$ and $2.746 \times 10^{-6}$ F/cm$^2$ for the control and the SiGe S/D devices, respectively. All the pMOSFETs with the gate dimension of $0.25\,\mu m \times 0.04\,\mu m$ (width × length) were used in this work. Prior to low-frequency noise measurements, the dc characteristics were measured using an Agilent B1500 semiconductor parameter analyzer. The $1/f$ noise measurements were carried out using SR570 low-noise current preamplifiers and an Agilent 35670A dynamic signal analyzer. The pMOSFETs were biased in linear operation ($V_D = -50$ mV) while varying the gate overdrive voltage ($V_G - V_T$) from the subthreshold regime (0.2 V) to the inversion regime (−0.3 V). The RTN measurements were made by waveform generator/fast measurement unit modules based on Agilent B1500 semiconductor parameter analyzer.

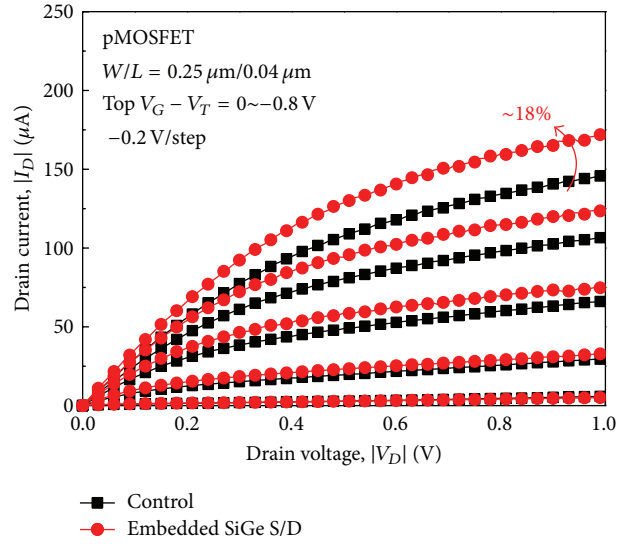


FIGURE 1: The $I_D - V_D$ characteristics for HK pMOSFET with and without embedded SiGe S/D.

## 3. Results and Discussion

Figure 1 shows the drain current ($I_D$) as a function of the drain voltage ($V_D$) for both pMOSFETs. Around 18% $I_D$ enhancement for SiGe S/D device is observed as compared to the control device at the same, $V_G - V_T = -0.8$ V and $V_D = -1.0$ V, which clearly indicates that the embedded SiGe S/D process can efficiently induce compressive strain in the channel. Figure 2 presents the drain current noise spectral density ($S_{ID}$) versus the frequency for both pMOSFETs taken from the average of six devices biased at different $V_G - V_T$. Both devices show typical $1/f_\gamma$ noise types with the frequency exponent ($\gamma$) close to unity. It means that the fluctuations of $1/f$ noise can be attributed to the carrier-number, mobility, or source-drain series-resistance fluctuations. In our devices, the $S_{ID}$ was found to be independent of the $V_D$, indicating that the $1/f$ noise source is not due to the contact or source-drain series resistance. The normalized drain current noise spectral density ($LS_{ID}/I^2_D$) and the transconductance to the drain current squared ($(g_m/I_D)^2$) as functions of the $I_D$ are plotted in Figure 3. The $LS_{ID}/I^2_D$ curves of both devices show fairly good proportionality with $(g_m/I_D)^2$ at the low $I_D$ level, indicating that the carrier number fluctuation dominates the $1/f$ noise, which caused by trapping and releasing of the carrier in the gate stacks [4, 5]. However, the $LS_{ID}/I^2_D$ curves cannot follow this trend at the high $I_D$ level, which implies a correlated mobility fluctuation was involved [6, 18]. In order to further evaluate the dominant mechanism and parameters of the $1/f$ noise model for both devices, the normalized input-referred voltage noise spectral density ($LS_{VG}$) as a function of ($V_G - V_T$) is shown in Figure 4. Both devices show two distinct regions in the associated $LS_{VG}$. In region I ($V_G - V_T \leq -0.1$ V), $LS_{VG}$ is independent of ($V_G - V_T$), which indicates a signature of umber fluctuations. In region II ($V_G - V_T > -0.1$ V), a parabolic dependence of $LS_{VG}$ on ($V_G - V_T$) is observed, further confirming that correlated mobility

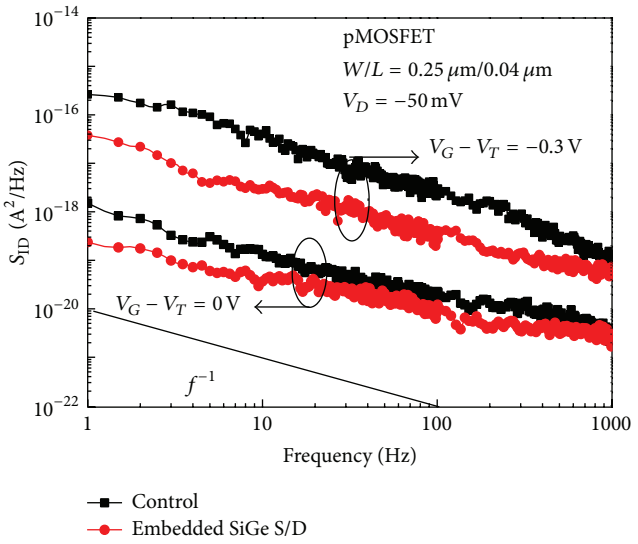


FIGURE 2: Drain current noise spectral density ($S_{ID}$) versus frequency for HK pMOSFET with and without embedded SiGe S/D.

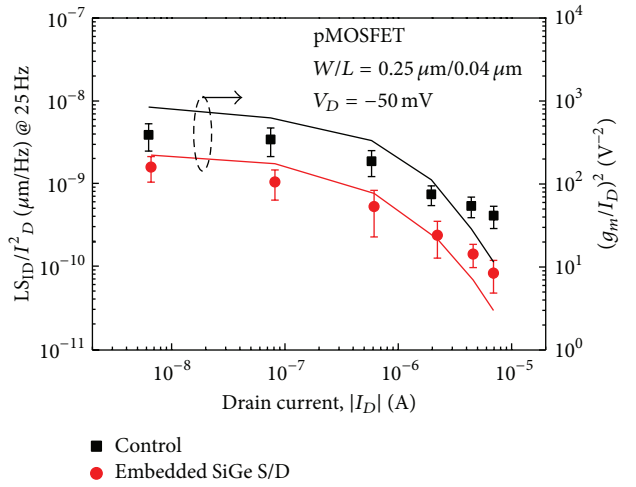


FIGURE 3: Normalized drain current noise spectral density ($LS_{ID}/I^2_D$) and the transconductance to the drain current squared ($(g_m/I_D)^2$) as functions of drain current for HK pMOSFET with and without embedded SiGe S/D.

fluctuations was involved. These results mean that the main source of $1/f$ noise for both devices can be ascribed to the unified model, which incorporates both the carrier number and the correlated mobility fluctuations. Furthermore, the $LS_{VG}$ can be expressed as [19]

$$LS_{VG} = \frac{q^2 KT}{WC_{ox}^2 f^r} \lambda N_t \left[1 + \alpha\mu_0 C_{ox} (V_G - V_T)\right]^2, \quad (1)$$

where $\lambda$ is the tunneling attenuation length for channel carriers penetrating into the gate dielectric, $N_t$ is the oxide trap density, $\alpha$ is a scattering coefficient, and $\mu_0$ is the low field mobility. The first term in the parentheses in (1) determines the base $LS_{VG}$ level in our region I and can be described

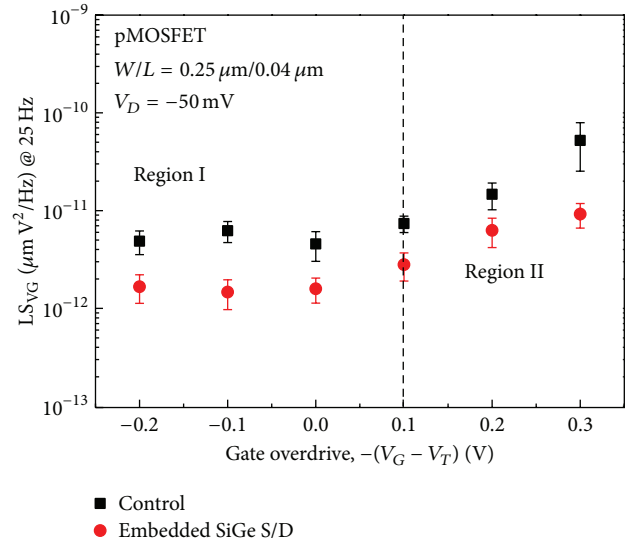


FIGURE 4: Normalized input-referred voltage noise spectral density ($LS_{VG}$) versus gate overdrive for HK pMOSFET with and without embedded SiGe S/D.

by number fluctuations, in which the $LS_{VG}$ is independent on $V_G - V_T$. The $\lambda N_t$ product is an important parameter related to the base $LS_{VG}$ level. The second term presents the curvature of $LS_{VG}$ versus $V_G - V_T$ in region II and can be described by correlated mobility fluctuations. The curvature of parabola is determined by the $\alpha\mu_0$ product. First, as compared with control device, the reduced $LS_{VG}$ level of the embedded SiGe S/D device implies the reduction of $\lambda$ or $N_t$. However, previous literature had reported that SiGe S/D process may lead higher $N_t$ [20, 21]. In other words, it can only be assumed that the reduced $\lambda$ mainly contributed to the decreased $LS_{VG}$ of SiGe S/D device. The possible mechanism of reduced $\lambda$ of SiGe S/D device is explained as follows. The uniaxial compressive stress-induced valence band offset and more holes tend to exist in top band. Therefore, the out-of-plane effective mass ($m_Z^*$) and tunneling barrier height for holes ($\varphi_B$) of SiGe S/D device are both larger than those of control one. As shown in Figure 5, an observed smaller gate current density ($J_g$) in SiGe S/D device confirmed the strain-induced increased $m_Z^*$ and $\varphi_B$ [22]. The $\lambda$ is also related to $m_Z^*$ and $\varphi_B$ by [19, 20]

$$\lambda = \sqrt{\frac{\hbar^2}{2m_Z^* \varphi_B}}, \quad (2)$$

where $\hbar$ is reduced Planck's constant. It suggests that strain-increased $m_Z^*$ and $\varphi_B$ bring a smaller $\lambda$ in SiGe S/D device. The relation between the trap depth ($X_T$) in insulator and $\lambda$ can be revealed according to an equation as $X_T = \lambda \ln(1/2\pi f\tau_0)$ [23]. The RTN measurement is a useful tool for probing the trap location in MOSFET [24–26]. It will be applied to confirm our observation and assumption of reduced $LS_{VG}$ in the $1/f$ noise measurement. The $I_D$ RTN characteristics of both devices as a function of the time show themselves in the form

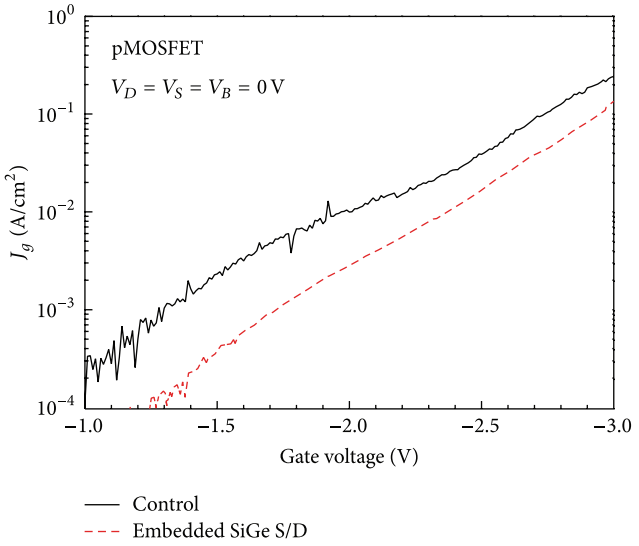


FIGURE 5: The gate current density ($J_g$) versus gate voltage for HK pMOSFET with and without embedded SiGe S/D.

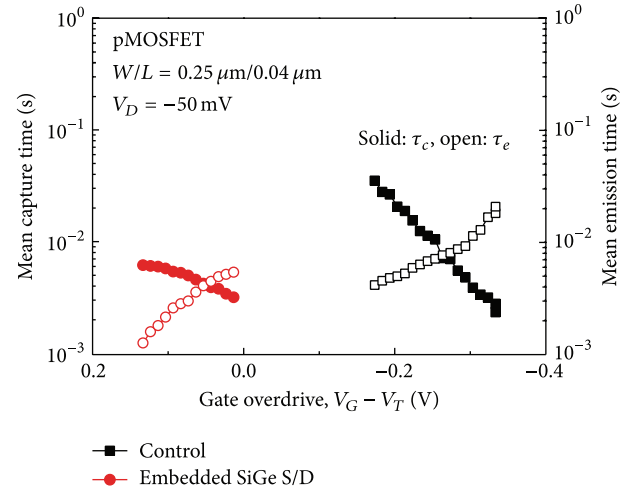


FIGURE 6: Comparison of the capture time (solid) and emission time (open) for HK pMOSFET with and without embedded SiGe S/D.

of switching events between two states (not shown here). These switching events are attributed to trapping/detrapping caused by an individual interface defect. The times in the high- and low-current states correspond to carrier capture and emission, respectively. The extracted mean capture time ($\tau_c$) and mean emission time constant ($\tau_e$) versus ($V_G - V_T$) are both presented in Figure 6. It can be found that the SiGe S/D device has the lower values of $\tau_c$ and $\tau_e$ and the weak dependence of $\tau_e$ on $V_G - V_T$, indicating that the trap position is closer to the insulator/semiconductor interface. Figure 7 shows the dependence of $\tau_c/\tau_e$ on ($V_G - V_T$) for both devices. From the data obtained for $\ln(\tau_c/\tau_e)$ dependence on gate voltage, the position of the trap into the oxide ($X_T$) is determined using (3) as follows [14, 25]:

$$\frac{\partial \ln(\tau_c/\tau_e)}{\partial V_{GS}} = \frac{q}{KT}\left(\frac{X_T}{t_{ox}}\right)\left[1 - \frac{KT}{q}\frac{G_m}{|I_{DS}|}\right], \quad (3)$$

where $t_{ox}$ is the oxide thickness, and $K$ is the Boltzmann constant. As expectation, the extracted $X_T$ is 1.68 nm and 1.14 nm for the control device and the SiGe S/D device, respectively. The reduced $X_T$ in SiGe S/D device is in well agreement on the analysis of $1/f$ noise (i.e., reduced $\lambda$) and can be ascribed to the strain-induced higher $\varphi_B$ for hole. Therefore, though the gate dielectric quality may be degraded by the SiGe S/D process, the traps far away from insulator/semiconductor interface cannot act for capturing carriers, thanks to the reduced $\lambda$, which stemmed from uniaxial compressive strain increasing $m_Z^*$ and $\varphi_B$. Consequently, the improvement of $LS_{VG}$ level was observed. On the other hand, in region II, the smaller curvature of $LS_{VG}$ of SiGe S/D device indicates the product of $\alpha\mu_0$ is smaller than that of control device, which can be attributed to the strain-induced lower carrier scattering and higher hole mobility at the same time [27, 28]. However, it should be noted that the $1/f$ performance of our HK pMOSFETs will be probably worse than counterparts with traditional $SiO_2$ insulator [14]. This is owing to the complexity of HK process that led to the higher volume trap densities in gate stacks [29].

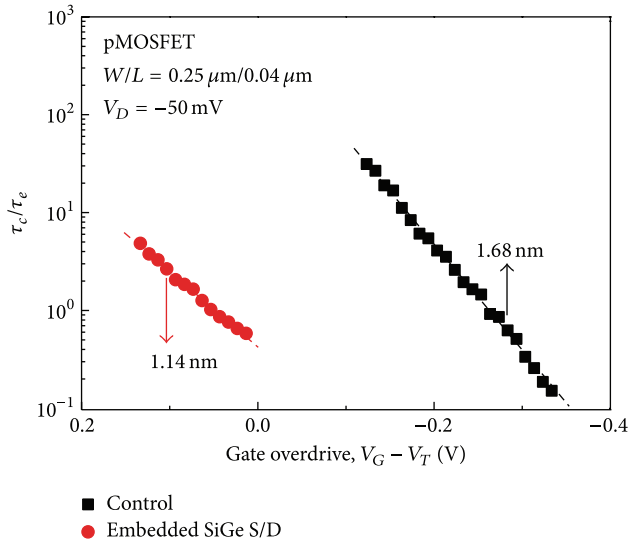


FIGURE 7: Plot of capture time ($\tau_c$) over emission time ($\tau_e$) versus gate overdrive for HK pMOSFET with and without embedded SiGe S/D.

## 4. Conclusions

In this paper, we have investigated the effect of compressive strain on low-frequency noise in HK pMOSFET. Through RTN measurement, we found that the HK pMOSFET with the embedded SiGe S/D has a shorter distance of the oxide trap position from the insulator/semiconductor interface. This is ascribed to the higher $\varphi_B$ and smaller $\lambda$ for hole stemmed from uniaxial compressive strain-induced bandgap offset. As a result, the improvement of $1/f$ noise is observed. It is clear that the better performance of low-frequency noise

in HK MOSFET device with strain technologies can be expected.

## Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

## Acknowledgments

The authors would like to thank the Advanced Optoelectronic Technology Center of NCKU for the financial support under Contract HUA103-3-15-051, the National Science Council of Taiwan for the financial support under Contract numbers NSC102-2221-E-006-259 and NSC102-2221-E-230-015, the Bureau of Energy, Ministry of Economic Affairs of Taiwan for the financial support under Contract number 102-E0603, and UMC staffs for their helpful support.

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