Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2014, Article ID 879813, 14 pages
http://dx.doi.org/10.1155/2014/879813

Research Article

Enhanced Device and Circuit-Level Performance Benchmarking of Graphene Nanoribbon Field-Effect Transistor against a Nano-MOSFET with Interconnects

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Received 10 December 2013; Revised 11 February 2014; Accepted 12 February 2014; Published 26 March 2014

Academic Editor: Tianxi Liu

Comparative benchmarking of a graphene nanoribbon field-effect transistor (GNRFET) and a nanoscale metal-oxide-semiconductor field-effect transistor (nano-MOSFET) for applications in ultralarge-scale integration (ULSI) is reported. GNRFET is found to be distinctly superior in the circuit-level architecture. The remarkable transport properties of GNR propel it into an alternative technology to circumvent the limitations imposed by the silicon-based electronics. Budding GNRFET, using the circuit-level modeling software SPICE, exhibits enriched performance for digital logic gates in 16 nm process technology. The assessment of these performance metrics includes energy-delay product (EDP) and power-delay product (PDP) of inverter and NOR and NAND gates, forming the building blocks for ULSI. The evaluation of EDP and PDP is carried out for an interconnect length that ranges up to 100 μm. An analysis, based on the drain and gate current-voltage (I_d-V_d and I_d-V_g), for subthreshold swing (SS), drain-induced barrier lowering (DIBL), and current on/off ratio for circuit implementation is given. GNRFET can overcome the short-channel effects that are prevalent in sub-100 nm Si MOSFET. GNRFET provides reduced EDP and PDP one order of magnitude that is lower than that of a MOSFET. Even though the GNRFET is energy efficient, the circuit performance of the device is limited by the interconnect capacitances.

1. Introduction

The number of transistors on a typical 1 × 1 cm chip has grown exponentially with twofold increase every 18 months keeping Moore's Law [1] on track. Serious hindrances are in sight as transistor scaling enters the nanometer domain. Short-channel effects are significant as devices are scaled below sub-100 nm, providing challenges and opportunities for device and process engineers. Researchers across the globe are exploring new nanomaterials with transformed architecture to circumvent the roadblocks of silicon-based nanotechnology for enhanced circuit performance. Interconnects also play a key role as channels reach nanometer scale and resistance surge takes on an increasing importance [2]. Carbon-based allotropes offer a distinct advantage in a variety of applications [3–8]. Graphene nanoribbons (GNRs) are one-dimensional (1D) nanostructures restricting carrier motion in only one direction, reducing scattering for enhanced mobility [6, 9]. The transistor current is quite high as electrons are injected from the source and transit to the drain terminal [6, 10–12]. A narrow width semiconducting GNR is utilized as a channel in a top-gated transistor [13–15]. This pushes the limits of complementary metal-oxide-semiconductor (CMOS) type of technology beyond its limits in a GNR. This paper focuses on modeling, simulation, and benchmarking of top-gated graphene nanoribbon field-effect transistors (GNRFETs) against MOSFET. In addition, the evaluation of logic performance is carried out for both devices. It is observed that there is a good agreement between GNRFET and MOSFET based on the drain current-voltage

Table 1: Design specifications C and S for various channel lengths.

Channel length (nm)	C (nm)	S (nm)	W (nm)
16	30	8	46
32	50	16	82
45	60	20	100
65	90	40	170
90	120	50	220
180	220	100	420

(I-V) characteristics. The energy-delay product (EDP) and power-delay product (PDP) are the performance metrics that represent the energy efficiencies of GNRFET and MOSFET logic gates. The simulations in this work are carried out for the 16 nm manufacturing processes. In the following, device model framework of our previous work [7, 16–19] is extended for the simulation and analysis of GNRFET and MOSFET at 16 nm node. Circuit-level models of GNRFET are benchmarked against MOSFET. Logic performances of carbon and silicon-based inverter and NAND and NOR gates are assessed. For a fair assessment, the same channel length, $L = 16$ nm, is adopted for GNRFET, PMOS, and NMOS. The device modeling is carried out in MATLAB and circuit development and simulation is performed using HSPICE and Cosmoscope.

2. Device Modeling

The simulated silicon MOSFET is based on Berkeley short-channel IGFET model (BSIM) which was the standard model for deep submicron CMOS circuit design in the early 2000s [20]. IC companies including Intel, IBM, AMD, National Semiconductor, and Samsung widely use the charge-based model as an electronic computer-aided design (ECAD) tool. BSIM4 version 4.7 MOSFET model is utilized in the simulation of NMOS and PMOS [21] in the present assessment. The top view of GNRFET with source and drain contacts is depicted in Figure 1. Various values of C and S (see Figure 2) are given in Table 1.

3. Proposed Layout and Design

The interpolated contact size C and spacer size S of 16 nm node process technology are illustrated in Figures 2(a) and 2(b), respectively.

The channel width, W, is a function of C and S as given by

$$W = C + 2S. \tag{1}$$

Table 1 gives design specifications for channel lengths from 16 to 180 nm range.

4. Analytical Modeling of GNRFET

In this section, the analytical model of GNRFET is derived. The channel surface potential V_{SC}, or self-consistent voltage as is commonly known, is solved numerically in MATLAB using Newton-Raphson algorithm to obtain the voltage potential at the top barrier along the channel [23]. The V_{SC} is given by

$$V_{SC} = V_L + V_p = \frac{-Q_t + \Delta Q}{C_\Sigma}, \tag{2}$$

where C_Σ is the total sum of capacitance at all the four terminals and Q_t is the total charge. ΔQ is the additional charge due to the increase of V_{SC}. V_L is the potential appearing across the channel region and V_P is existing across the parasitic regions. The other symbols in (2) are given as follows where N_s is the density of positive velocity states, N_d is the density of negative velocity states and N_0 is the electron density at equilibrium:

$$\begin{aligned} Q_t &= C_s V_s + C_g V_g + C_d V_d + C_{sub} V_{sub}, \\ C_\Sigma &= C_s + C_g + C_d + C_{sub}, \\ \Delta Q &= q\left(N_s + N_d + N_0\right). \end{aligned} \tag{3}$$

The carriers obey the Fermi-Dirac probability distribution as follows:

$$\begin{aligned} N_s &= \frac{1}{2}\int_{-\infty}^{+\infty} D(E)\, f\left(E - U_{SF}\right) dE, \\ N_d &= \frac{1}{2}\int_{-\infty}^{+\infty} D(E)\, f\left(E - U_{DF}\right) dE, \\ N_0 &= \int_{-\infty}^{+\infty} D(E)\, f\left(E - E_F\right) dE, \end{aligned} \tag{4}$$

where U_{SF} and U_{DF} are defined as

$$\begin{aligned} U_{SF} &= E_F - qV_{SC}, \\ U_{DF} &= E_F - qV_{SC} - qV_d. \end{aligned} \tag{5}$$

The one-dimensional (1D) density of state (DOS) function in (4) is defined as

$$D(E) = \frac{2g_v g_s}{3\pi a_{cc} t} \sum_i \frac{E}{\sqrt{E^2 - \left(E_G/2\right)^2}}, \tag{6}$$

where $a_{cc} = 0.142$ nm is the C–C bond length and $t = 3$ eV is the C–C bonding energy. In (6), E_G is the bandgap energy, g_s is the spin degeneracy, and g_v is the valley degeneracy. In an armchair GNR (aGNR), $g_v = 1$. A nonlinear regression model of V_{SC} is obtained through the use of the polynomial fit [24, 25]. The nonlinear approximation for V_{SC} dependence on V_d and V_g in the form of fifth-order polynomial is given to replace the Newton-Raphson algorithm in (2). The regression model is given as

$$\begin{aligned} V_{SC}\left(V_g, V_d\right) = {} & AV_d + BV_g{}^5 + CV_g{}^4 \\ & + DV_g{}^3 + EV_g{}^2 + FV_g + G, \end{aligned} \tag{7}$$

where A, B, C, D, E, F, and G are the coefficients extracted from MATLAB curve fitting tool.

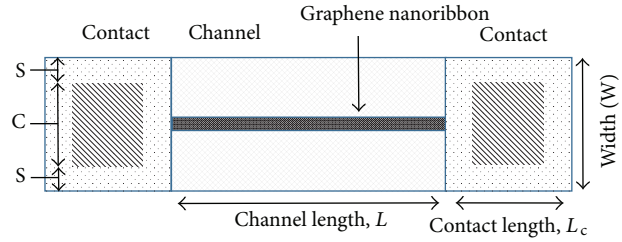

Figure 1: Top view of GNRFET device structure with contact and channel design layout architecture.

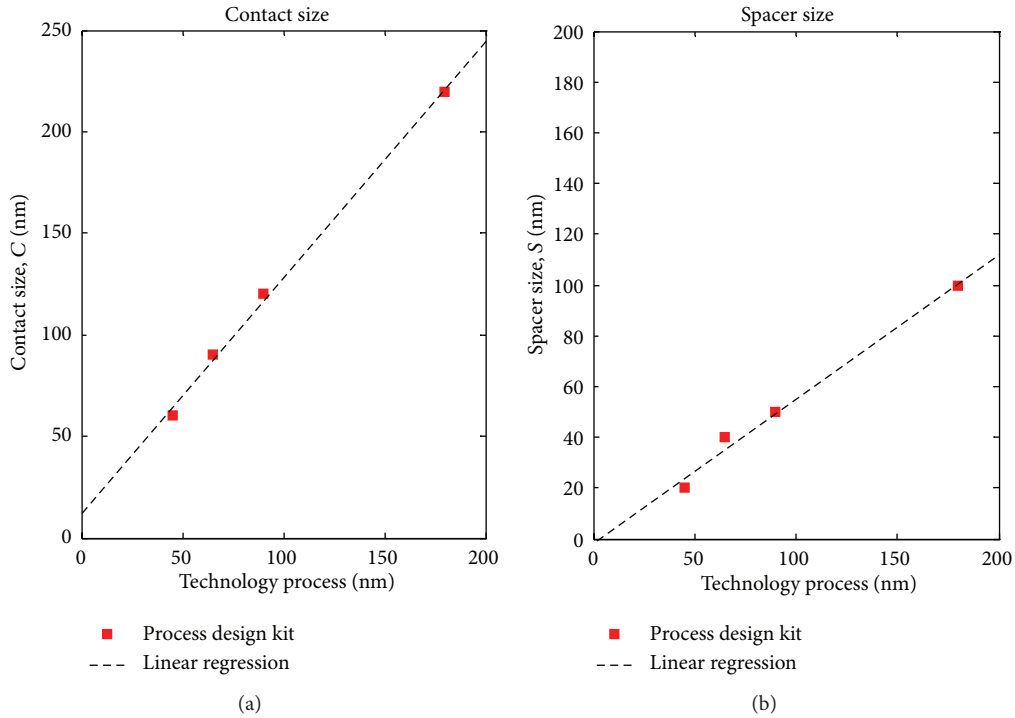

Figure 2: Interpolation of (a) contact and (b) spacer sizes.

Table 2: Values for the coefficients A to G.

Coefficient	Value
A	-3.5000×10^{-2}
B	1.0737×10^{-3}
C	-2.7542×10^{-3}
D	2.3754×10^{-3}
E	-6.3691×10^{-4}
F	-8.8009×10^{-1}
G	-3.5738×10^{-4}

The coefficients A to G in Table 2 are empirical parameters used for curve fitting (2).

HSPICE utilizes (8) to simulate the drain and gate I-V characteristic of GNRFET and MOSFET. The noniterative model allows cross-platform simulation, shorter execution time, and reduced computational cost [26]. In GNRFET, when gate and drain voltages are applied, V_{SC} is reduced by V_L. This would result in a flow of electron in the channel that increases V_{SC} by V_P due to introduction of the additional charges [27]. In the I_d-V_d simulation of GNRFET, the I_d-V_d equation can be written in V_d, V_s and V_g coefficients as given by

$$
\begin{aligned}
&I_d\left(V_g, V_d, V_s\right) \\
&= G_{\mathrm{ON}} \frac{k_B T}{q}\left[\log\left(1+\exp\left(\frac{q\left(E_F - V_{\mathrm{SC}}\left(V_g, V_d, V_s\right)\right)}{k_B T}\right)\right)\right] \cdots \\
&\quad - G_{\mathrm{ON}} \frac{k_B T}{q} \\
&\quad \times \left[\log\left(1+\exp\left(\frac{q\left(E_F - V_{\mathrm{SC}}\left(V_g, V_d, V_s\right) - V_d - V_s\right)}{k_B T}\right)\right)\right],
\end{aligned}
\tag{8}
$$

where G_{ON} is the on-conductance.

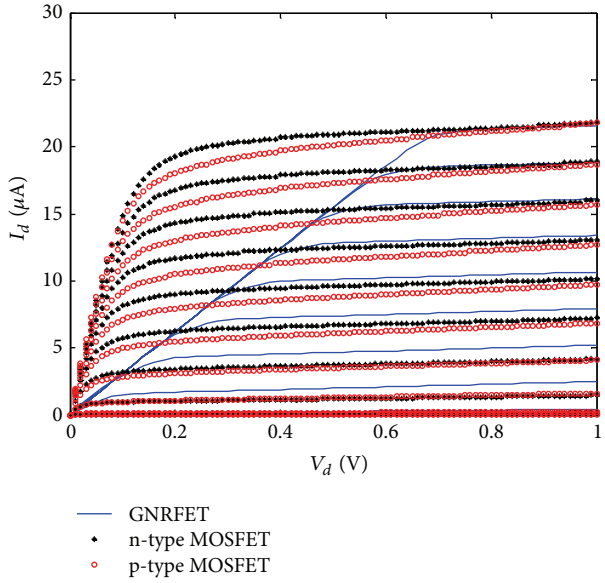

Figure 3: I_d-V_d characteristics n-type GNRFET, p-type, and n-type MOSFET for various gate voltages starting from V_g = 1 V at the top in 0.1 V decrement.

5. Device Simulation

The device performance of GNRFET and MOSFET are compared by evaluating their respective I_d-V_d characteristic as shown in Figure 3. The output response of p-type and n-type MOSFETs is superimposed for comparison purposes. Also, the I_d-V_d characteristics of p-type and n-type GNRFETs are symmetrical as in a CMOS and thus coincide with each other. Figure 4 illustrated the I_d-V_g transfer characteristic of n-type and p-type MOSFET and GNRFET. DIBL and SS are calculated from the I_d-V_g curve and are given as

$$\text{DIBL} = \frac{\partial V_T}{\partial V_d}, \qquad \text{SS} = \frac{\partial V_g}{\partial \left(\log_{10} I_d\right)}. \tag{9}$$

The range of the DIBL measurement is taken between $|V_d|$ = 0.1 V and $|V_d|$ = 1 V and the SS measurement is for the drain current curve at $|V_d|$ = 0.1 V. As deduced from Figure 3, GNRFET has a lower linear on-conductance compared to MOSFET. In addition, GNRFET achieves higher saturation current values than those of MOSFET for most gate voltages.

As listed in Table 3, the DIBL of MOSFET is better than GNRFET. The subthreshold swing (SS) of both devices is comparable. The I_{on}/I_{off} ratio of GNRFET is two-order magnitude lower than that of MOSFET. This is due to a lower linear on-conductance limit of a ballistic GNRFET. The on-conductance limit, G_{ON}, with zero contact resistance is given by

$$G_{ON} = \frac{2q^2}{h}, \tag{10}$$

Table 3: Device parameters and performance metrics of GNRFET, n-type, and p-type MOSFET.

Parameter	GNRFET	n-type MOSFET	p-type MOSFET
Electrical gate oxide thickness (nm)	2.0	1.0	1.6
Gate dielectric constant relative to vacuum	25	25	25
Subthreshold swing (mV/decade)	70.1704	61.7527	70.7253
Drain-induced barrier lowering (mV/V)	40.7448	35.2515	36.6697
On/off ratio, (I_{on}/I_{off})	3.42×10^4	1.25×10^6	6.9868×10^5

where q is the electronic charge and h is Planck's constant. The simulation is carried out using a high gate dielectric constant (high-k) with high thermal stability. In a practical microfabrication, zirconium dioxide which has high-k values between 20 and 25 is considered [28].

Note that different values of oxide thickness are being used to obtain almost symmetrical I-V characteristics for both p-type and n-type MOSFET, namely, in the linear region. It is found that when all the transistors adopt equal oxide thickness, the maximum current at V_d = 1 V and V_g = 1 V differs from one another. The output waveform will not have uniform square wave anymore. The propagation delay, rise time, and fall time will be significantly affected. Thus, they are no longer suitable for logic application due to the mismatch of the p-type and n-type I_d-V_d curves at the voltage transfer characteristics.

6. Circuit Design

In this Section, circuit simulation is considered. As part of the circuit design process, parasitic capacitance, namely, load capacitance C_L is determined for an accurate circuit representation. The top diagram in Figure 5 shows a typical arrangement of two inverters in series with C_L. The components of C_L are gate-drain capacitance C_{gd1}, C_{gd2}, drain-bulk capacitance C_{db1}, C_{db2}, and wire capacitance C_W as depicted in the bottom diagram of Figure 5. Note that the term wire capacitance is used interchangeably with interconnect capacitance. Table 4 lists the local, intermediate, and global copper and GNRFET interconnect capacitances for 32 nm, 22 nm, and 14 nm technology process. The finite element method (FEM) charts the pathways in obtaining capacitances as in [29]. The interconnects used in the simulation are considered to be in the intermediate layer [30] and vary from 1 μm to 100 μm in length [31]. It is found that for 0.18 μm technology, average interconnect lengths are considered to be 7 μm per fan-out [31]. These interconnect specifications from ITRS 2005 are shown in Table 4.

Table 5 shows the extrapolated interconnect capacitances for the 90 nm, 65 nm, 45 nm, and 16 nm process technologies. The capacitance values of copper and metallic GNR are extrapolated from Figure 6 using a linear function based on the intermediate capacitance in Table 4.

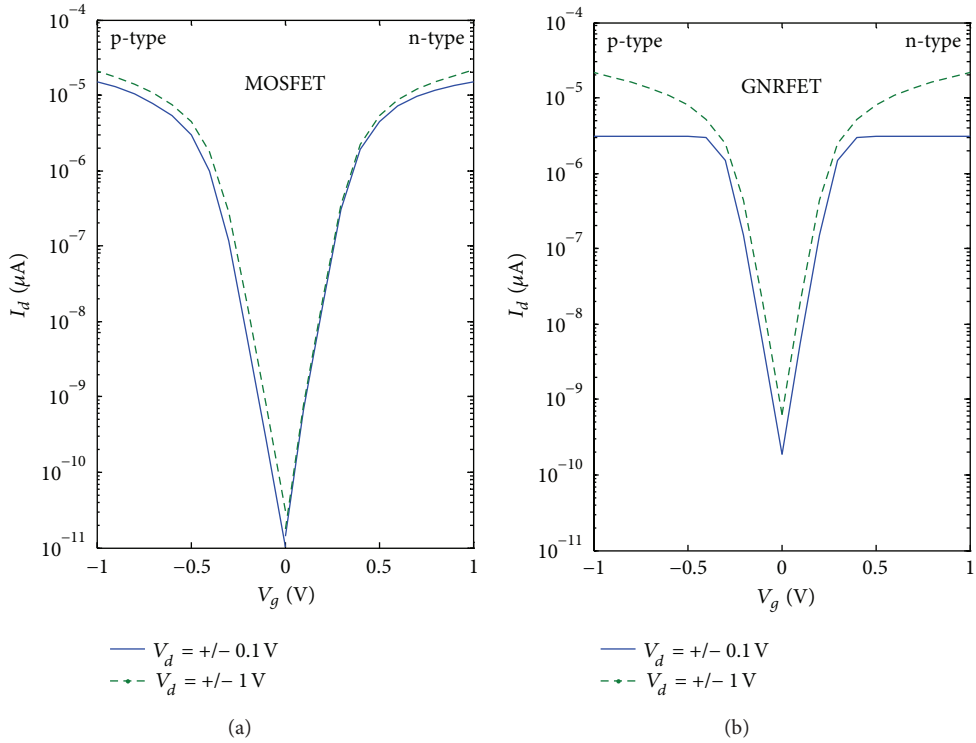

FIGURE 4: I_d-V_g transfer characteristic of n-type and p-type (a) MOSFET and symmetrical n-type and p-type (b) GNRFET FET for $|V_d|$ = 0.1 V and $|V_d|$ = 1 V.

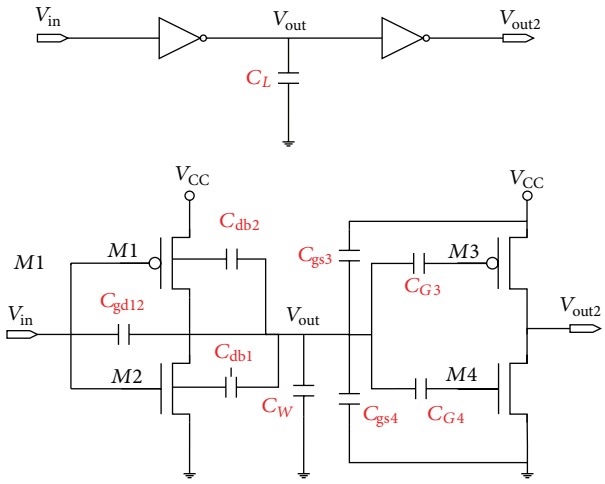

FIGURE 5: Two-cascaded inverter gate with parasitic capacitance.

Table 6 contains the relevant equations for the load and output capacitance for the logic gates.

7. Performance Analysis of Digital Circuit

HSPICE is used to simulate the logic operations of GNRFET and MOSFET. The schematic diagram and input-output waveforms of GNRFET and MOSFET NOT, two-input NAND (NAND2), two-input NOR (NOR2), three-input NAND (NAND3), and three-input NOR (NOR3) gates are delineated in Figures 7, 8, 9, 10, and 11, respectively. All the logic gates consist of 1 μm copper interconnects at the output terminals. In the simulation, the maximum fan-in for a gate is limited to 3. Correct logical operations are confirmed from the simulation results as shown in the input-output waveforms. Voltage spikes observed are found to be negligible in the output waveform of MOSFET in Figures 7(b)–11(b). The circuit inductance possibly causes spikes that are possible to be compensated by incorporating an on-chip decoupling capacitor at the output in parallel. Note that Figures 7–Figure 11 are important to calculate the propagation delay which is computed between 50% of the input rising to the 50% of the output rising. Together with the average power consumption, the metric performance of logic gates in term of EDP and PDP is obtained. PDP and EDP parameters are the figure of merit for logic devices. PDP and EDP are given by

$$\begin{aligned} \text{PDP} &= P_{\text{av}} \times t_p, \\ \text{EDP} &= \text{PDP} \times t_p, \end{aligned} \tag{11}$$

where P_{av} is the average power and t_p is the propagation delay. Table 7 lists the P_{av} and t_p for various logic gates as obtained from the simulation. The PDP and EDP for GNRFET are an order of lower magnitude compared to MOSFET due to smaller t_p and its ultralow P_{av} during logic operation as revealed in Table 7. GNRFET power consumption is by at least 1 order of magnitude lower than that of a MOSFET.

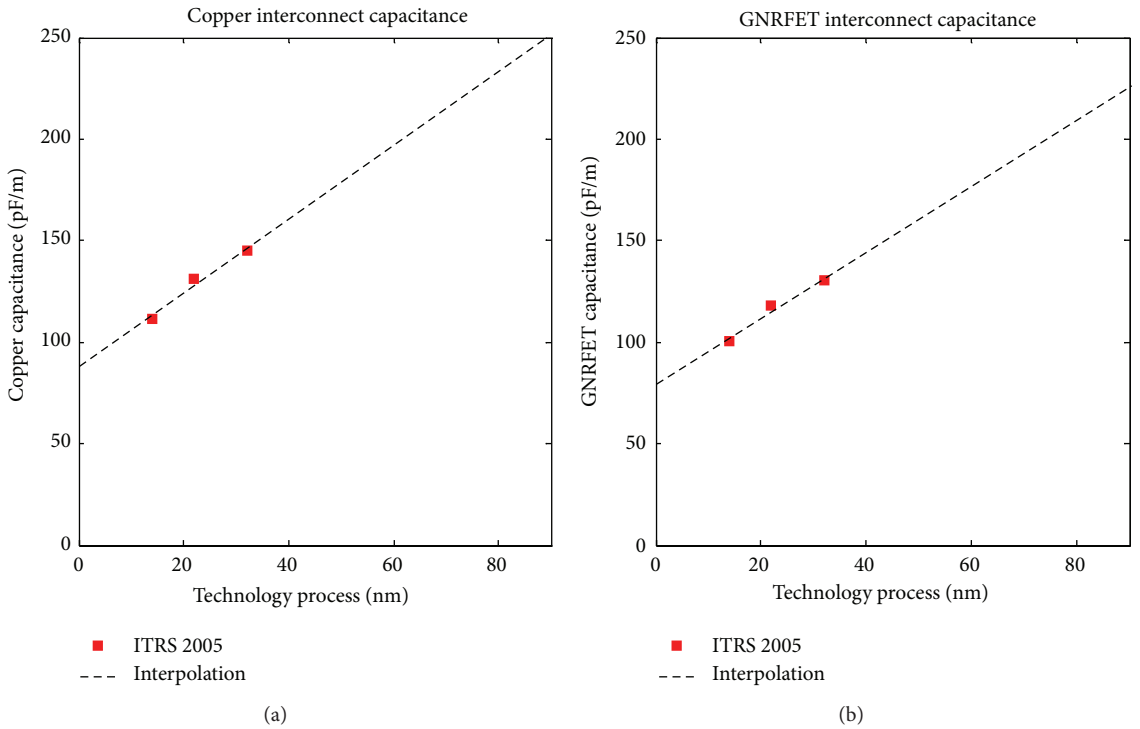

Figure 6: Extrapolation of interconnect capacitance for copper and GNR.

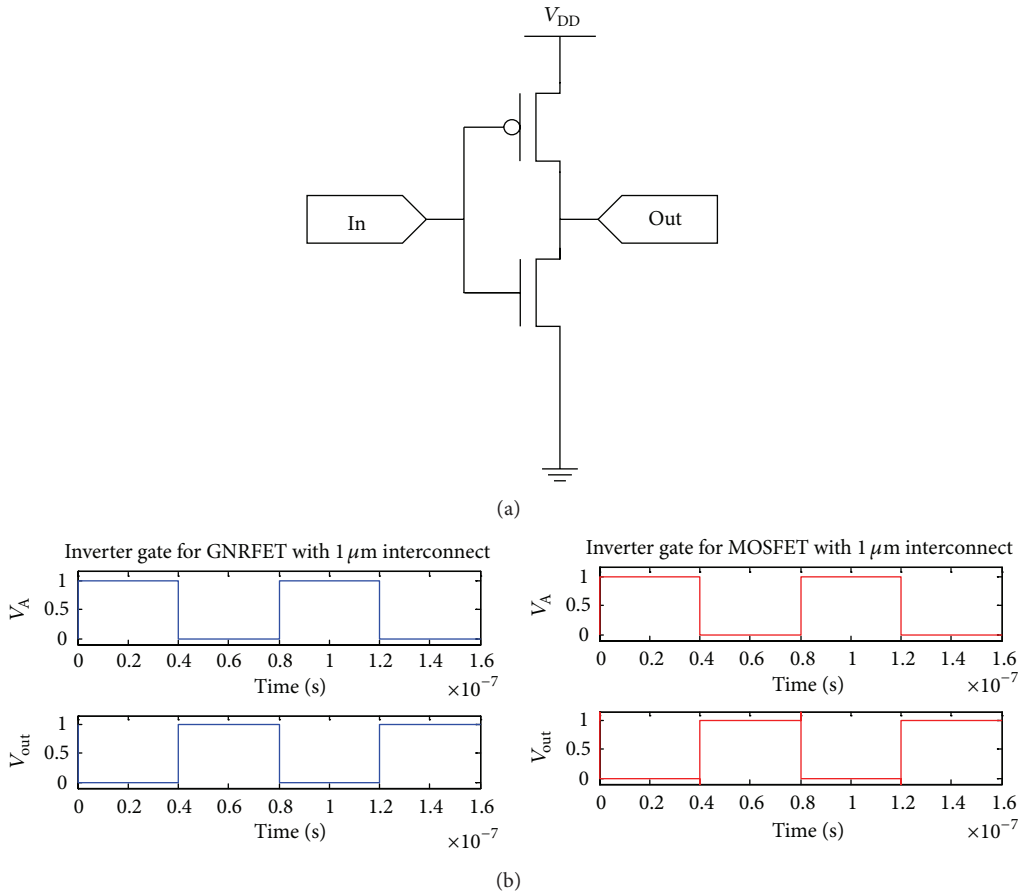

Figure 7: (a) Schematic of NOT gate. (b) Input and output waveforms for GNRFET and MOSFET with 1 μm interconnect.

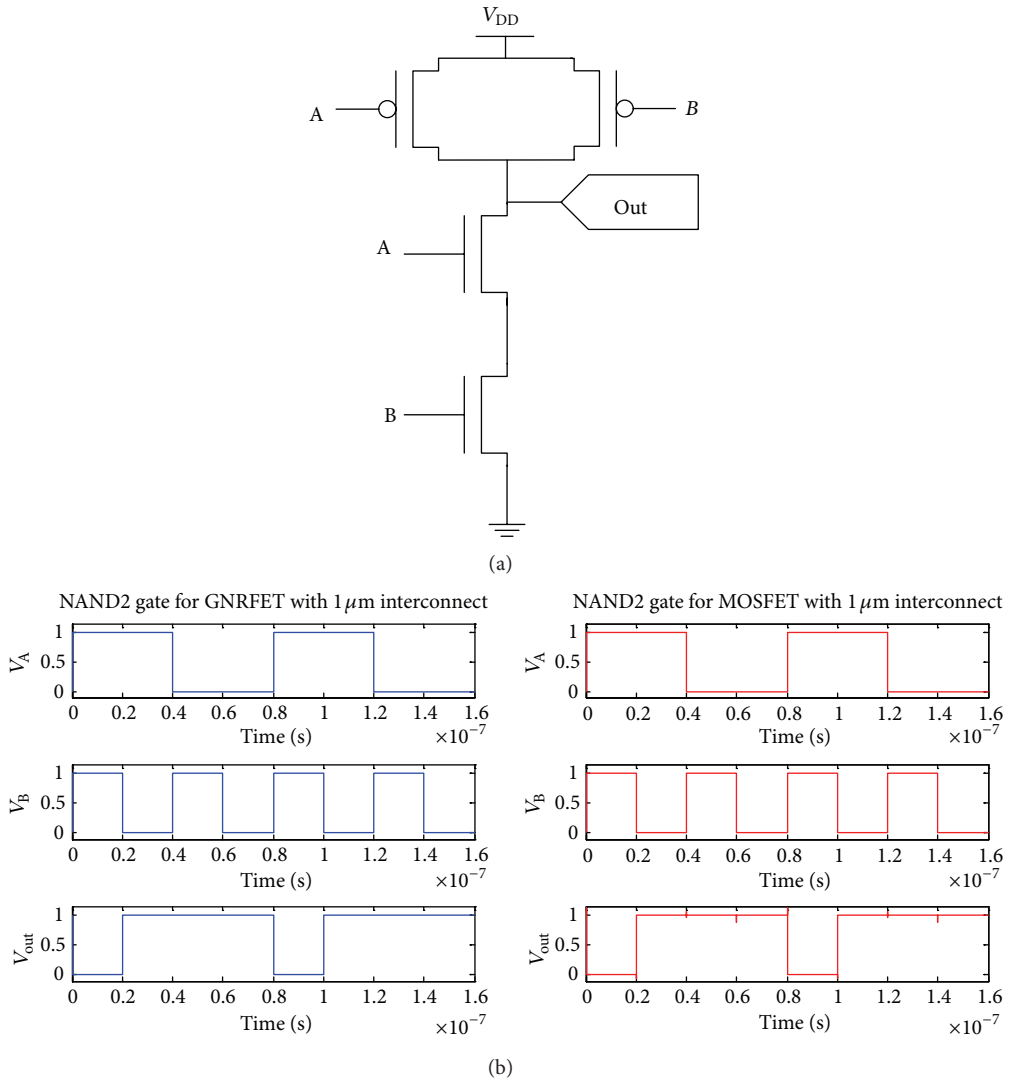

Figure 8: (a) Schematic of NAND2 gate. (b) Input and output waveforms for GNRFET and (b) MOSFET with 1 μm interconnect.

Table 4: ITRS 2005 based simulation parameters (adapted from [22]).

Technology process (nm)	32	22	14
Local and intermediate			
Width W (nm)	32	22	14
ILD thickness t_{ox} (nm)	54.40	39.60	25.20
C_{cu} (pF/m)	144.93	131.01	111.83
C_{gnrfet} (pF/m)	130.15	117.70	100.51
Global			
Width W (nm)	48	32	21
ILD thickness t_{ox} (nm)	110.40	76.80	52.50
C_{cu} (pF/m)	179.78	163.30	139.30
C_{gnrfet} (pF/m)	163.81	148.90	126.78

Table 5: Interconnect capacitances for 16, 45, 65, and 90 nm nodes.

Capacitance	Technology process (nm)			
	90	65	45	16
C_{cu} (pF/m)	252.32	206.60	170.03	116.99
C_{gnr} (pF/m)	226.87	185.70	152.76	105.01

Figure 12 depicts the layout for GNRFET NOR2 schematic shown in Figure 9(a). In the top-gated design, the GNR is placed under the metal gate and thus hidden from the view. The V_g is supplied to the device through terminals A and B. The vertical-interconnect-access (via) as labeled in Figure 12 allows a conductive connection between different layers. To realize the number of p-type and n-type transistors as given in Figure 9(a), three and four electrode contacts, respectively, are implemented in the layout. While the series configuration of the p-type transistors requires only three electrode contacts, and four electrode contacts are needed for the n-type transistors connected in parallel.

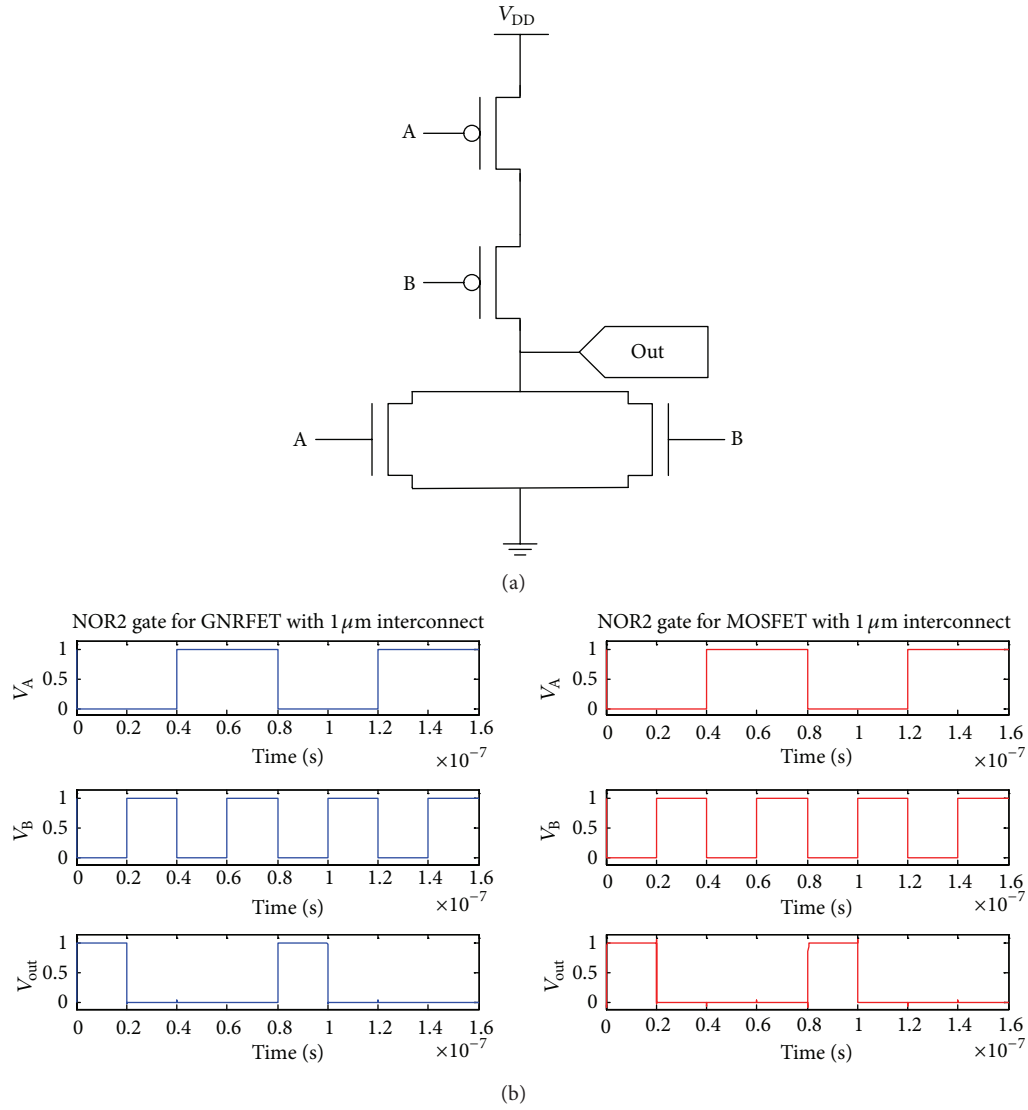

Figure 9: (a) Schematic of NOR2 gate. (b) Input and output waveforms for GNRFET and (b) MOSFET with 1 μm interconnect.

Table 6: Load and output capacitance for logic gates NOT, two-input NAND, two-input NOR, three-input NAND, and three-input NOR.

Gate logic	Capacitance
NOT	$C_L = C_{gd1} + C_{gd2} + C_{db1} + C_{db2} + C_W$
Two-input NAND	$C_1 = C_{db1} + C_{sb2} + C_{gd1} + C_{gs2}$
Two-input NOR	$C_L = C_{db2} + C_{db3} + C_{db4} + C_{gd2} + C_{gd3} + C_{gd4} + C_W$
Three-input NAND	$C_1 = C_{db1} + C_{sb2} + C_{gd1} + C_{gs2}$
Three-input NOR	$C_2 = C_{db2} + C_{sb3} + C_{gd2} + C_{gs3}$
	$C_L = C_{db3} + C_{db4} + C_{db5} + C_{db6} + C_{gd3} + C_{gd4} + C_{gd5} + C_{gd6} + C_W$

The Fermi velocity in a GNRFET is distinctly higher than that in a heavily doped MOSFET. Obviously, degenerate statistics is applicable in heavily doped channels. The intrinsic velocity for a nondegenerate low-doping level is limited to the thermal velocity which is lower than the Fermi velocity in heavily doped semiconductors. The device modeling of GNR adopts similar modeling framework in [17] where we have modified the density of states and quantum conductance limit of a ballistic SWCNT to GNR. The maximum drain current for a monolayer GNRFET is found to be at 19 μA. For CNTFET, the maximum drain current is at 46 μA. Nevertheless, both low dimensional carbon devices outperform silicon MOSFET in term of power-delay-product (PDP) and energy-delay-product (EDP) by at least one order of magnitude.

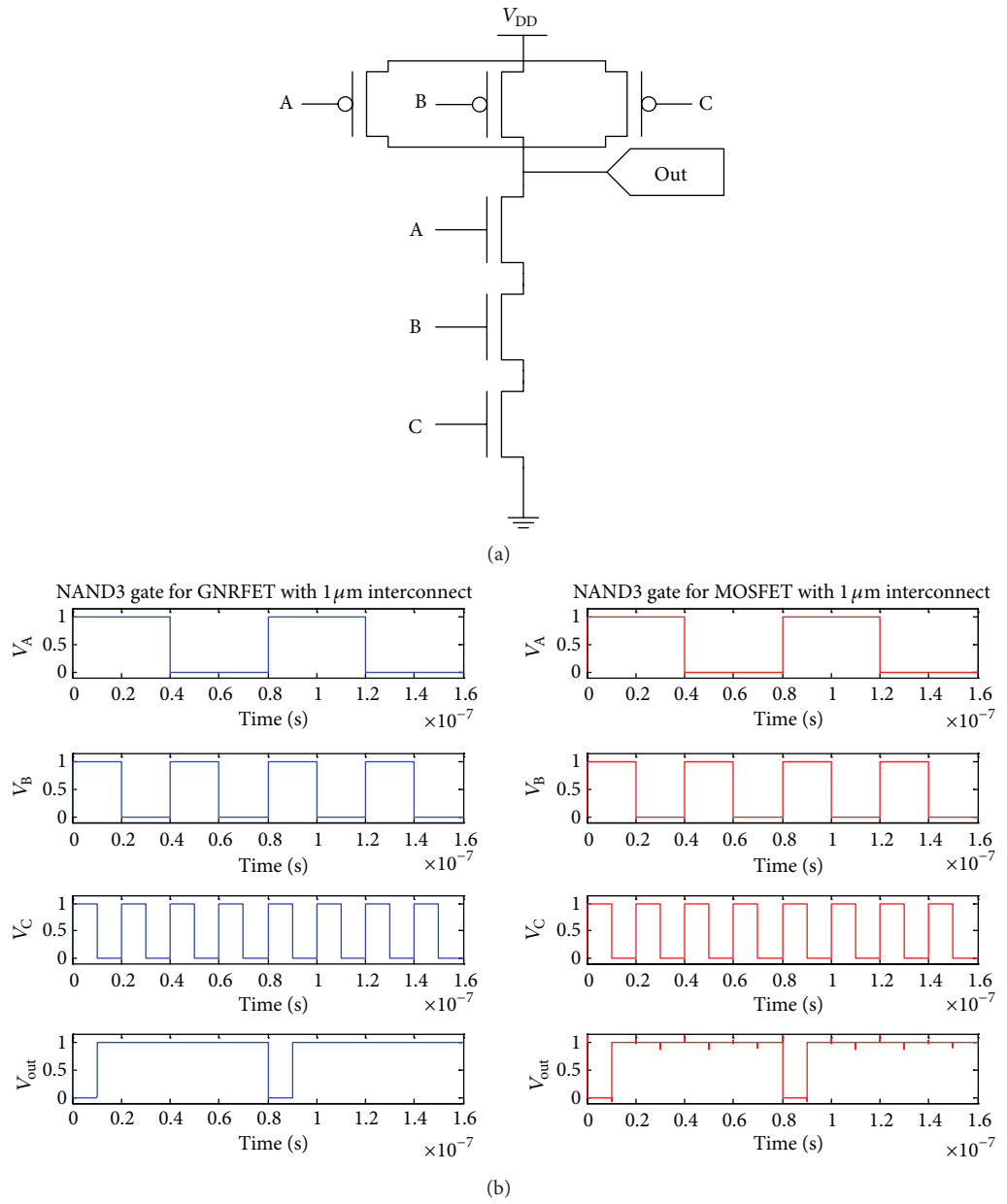

Figure 10: (a) Schematic of NAND3 gate. (b) Input and output waveforms for GNRFET and (b) MOSFET with 1 μm interconnect.

Table 7: Propagation delay and average power consumption of GNRFET and MOSFET with L = 16 nm and 1 μm interconnect for various logic gates.

Logic gates	Propagation delay, t_p (ps)		Average power, P_{av} (nJ/s)	
	GNRFET	MOSFET	GNRFET	MOSFET
Inverter	4.825	14.02	2.90	96.11
Two-input NAND	7.059	44.90	3.13	124.04
Three-input NAND	9.555	58.82	3.24	270.18
Two-input NOR	7.059	44.95	3.07	122.12
Three-input NOR	9.589	58.19	3.24	286.58

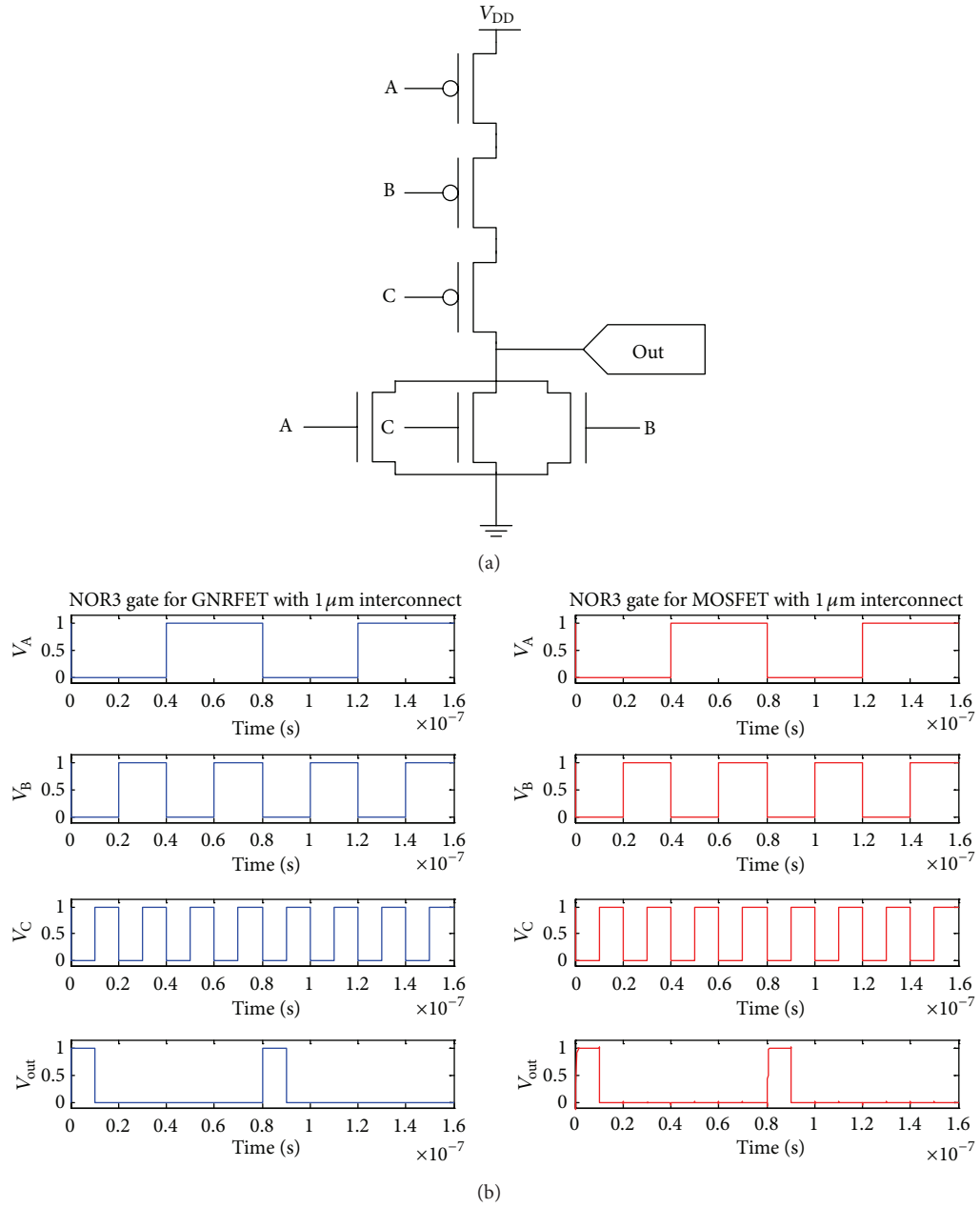

Figure 11: (a) Schematic of NOR3 gate. (b) Input and output waveforms for GNRFET and (b) MOSFET with 1 μm interconnect.

Figure 13 depicts the GNRFET PDP and EDP, respectively, for 0–100 μm copper interconnects in length for various logic gates. Figure 14 shows the MOSFET PDP and EDP, respectively, for 0–100 μm copper interconnect in length for various logic gates. The logic gates with high fan-in exhibit increased EDP and PDP as exhibited by these plots. The cutoff frequency at which the current gain is 1 is used to describe the high-frequency performance of a transistor. The current unity gain cutoff frequency of the intrinsic transistor [32, 33] with interconnect capacitance is given by

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_g + C_L + C_{\text{sub}}}, \tag{12}$$

where C_g is the gate capacitance, C_L is the load capacitance, and C_{sub} is the substrate capacitance. Devices with thicker substrate insulator (for instances, 500 nm) and smaller contact area have higher unity cutoff frequency. The unity current gain cutoff frequency for GNRFET circuit model is depicted in Figure 15. The model uses a copper interconnect of the 16 nm, 45 nm, 65 nm, 9 and 0 nm nodes technology. The simulation shows that a 16 nm GNRFET can deliver a unity cutoff frequency of 400 GHz. The interconnect length varies from 0.01 μm to 100 μm. It is found that cutoff frequency is inversely proportional to interconnect length. When the interconnects are longer than 10 μm, the frequency remains the same regardless of the technology nodes. Therefore, it

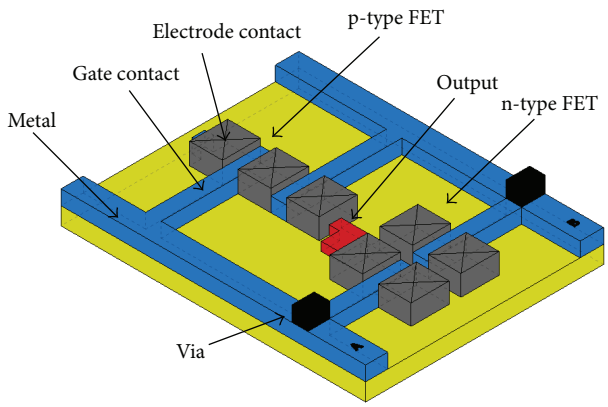

Figure 12: Proposed layout of GNRFET NOR2 gate with metal contacts and interconnects.

is essential to utilize interconnects as short as possible to tap the high-frequency capability of the CNTFETs [17] and GNRFETs. Our finding is consistent with the state-of-the-art graphene transistors that have been shown to reach operating frequencies up to 300 GHz experimentally [34].

8. Conclusions

Complementary CMOS based on *n*-type and *p*-type MOSFETs has been at the center stage in industrial environments because of low power consumption. A CMOS circuit draws power from the source only when an inverter is switching from low to high or vice versa. A CMOS inverter is a building block for other gates to build a complete ultralarge-scale-integrated (ULSI) ensemble. After the 2010 Nobel Prize awarded to graphene, graphene allotropes have overwhelmed the center stage to capture the advantage of *More than Moore's Era*. In fact, Arora and Bhattacharyya [35] show that CNT band structure can be drawn from that of graphene nanolayer with rollover in various chirality directions. GNR [36] offers similar endless opportunities. Considering these noteworthy developments, we believe that graphene allotropes offer distinct advantage over and above the CMOS architecture for a variety of applications in creating sensors, actuators, and transistors for implementation in the ULSI. As graphene allotropes bring to focus the advanced applications, we consider GNR as an example to demonstrate its superiority over the CMOS. Primary reason why graphene is superior to silicon is its intrinsic velocity. The drift in graphene is limited to the Fermi velocity $v_F \approx 10^6$ m/s that is 10 times than that of a silicon ($v_i \approx 10^5$ m/s). Saturation velocity limited to the intrinsic velocity v_i determines the high-frequency cutoff of a ULSI circuit. That is the reason that graphene-based electronics will offer unique advantage in high-frequency circuit design. As current saturates, the power in a ULSI circuit is governed by $P = VI_{sat}$ and hence becomes a linear function of voltage, in direct contrast to square law dictated by Ohm's law. The power consumption will be much lower in a graphene circuit affording the opportunity to lower the scale of the voltage source. Power-frequency product is a figure of merit in ULSI applications. The paper shows distinct advantages of graphene-based integration in ULSI circuits in designing various Boolean gates. The comparative study stretches the landscape of *More than Moore* era as traditional scaling reaches its limit. As demonstrated by Greenberg and del Alamo [37], interconnect degrades the device behavior. That is why it is important to include interconnects in the total package of these studies. The rise in the resistance in scaled-down channels also affects the voltage divider and current divider principles, normally based on Ohm's law. When interconnects are considered in series with the channel, the resistance surges for a smaller length resistor, creating the importance of comprehensive study [38]. Similarly, when parasitic channels are considered in parallel with the conducting channel, the resistance can be higher than what is predicted from Ohm's law. This rise in resistance can increase the RC time constants as demonstrated in [38, 39]. GNRFET with proper architecture can extend the domain of *More than Moore* era in meeting the requirements of the future. Short-channel effects that restrict the silicon technology to reach its full potential are controllable in GNRFET architecture. GNRFET has shown comparable device performance against 16 nm CMOS node. In terms of circuit performance in logic design, the PDP and EPD of GNRFET are distinctly better. The modern adage is "silicon comes from geology, but carbon comes from biology." This transformation from silicon to carbon-based graphene will usher new era for circuit design based on carbon electronics that is expected to be compatible with bioelements. ULSI designers will greatly benefit from this comparative study as they change their mode of thinking from CMOS to new graphene-based ULSI. We are also expecting that parasitic elements that inhibit the speed of ULSI circuits will pose less of a problem in future architectures based on our findings. The all-encompassing landscape covered in this paper will find broader applications benefitting not only the research labs in their characterization and performance evaluation, but also in giving new directions to the industry in product development that will benefit global community.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The authors would like to acknowledge the financial support from UTM GUP Research Grant (Vote nos.: Q.J130000.2523.04H32 and Q.J130000.2623.09J21) and Fundamental Research Grant Scheme (FRGS) (Vote nos.: R.J130000.7823.4F247, R.J130000.7823.4F273, and R.J130000.7823.4F314) of the Ministry of Higher Education (MOHE), Malaysia. Weng Soon Wong thanks Yayasan Sime Darby (YSD) for the scholarship given for his study at the Universiti Teknologi Malaysia (UTM). Vijay K. Arora appreciates the Distinguished Visiting Professorship of the UTM. UTM Research Management Centre (RMC) provided

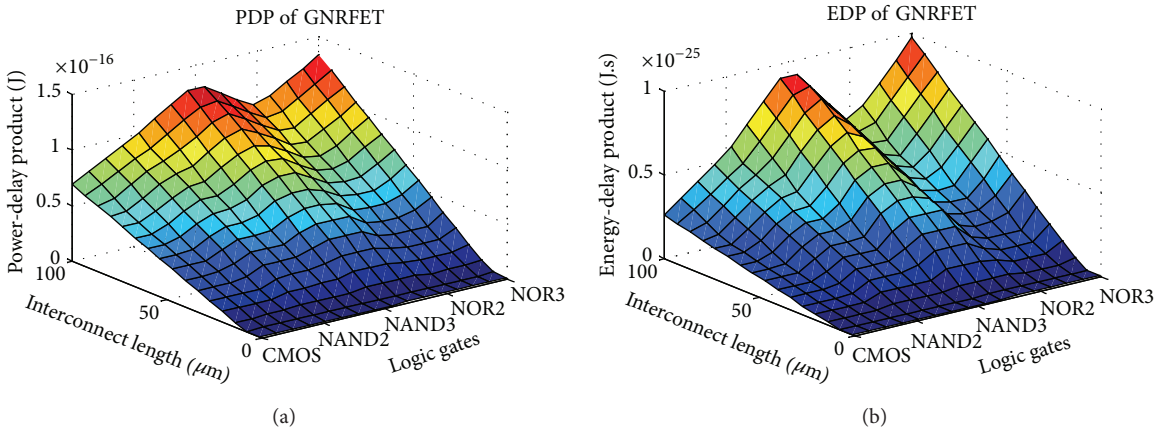

Figure 13: (a) PDP and (b) EDP of GNRFET logic gates for copper interconnect length from 0 to 100 μm.

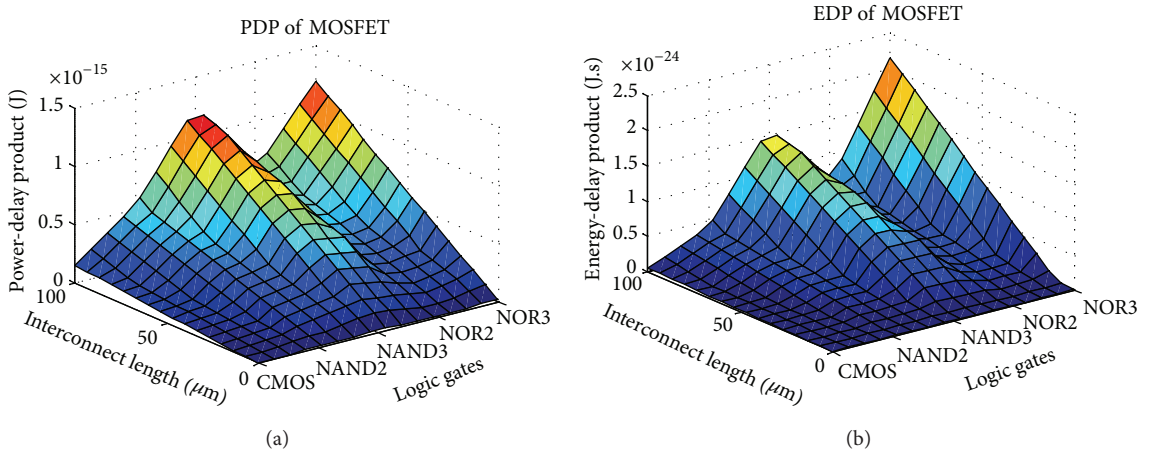

Figure 14: (a) PDP and (b) EDP of MOSFET logic gates for copper interconnect length from 0 to 100 μm.

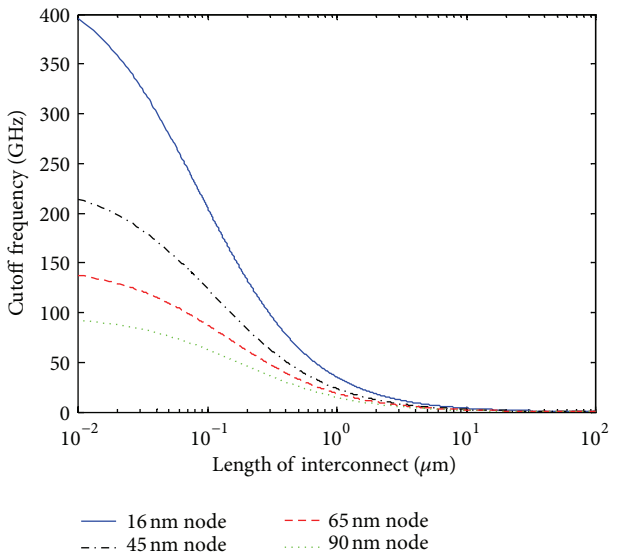

Figure 15: Unity cutoff frequency for GNRFET based on 16 nm, 45 nm, 65 nm, and 90 nm process technology.

excellent support conduciveness to the research environment needed to complete project of this magnitude with personnel of far-reaching background.

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